ISL36411

Quad Lane Extender

FN6965
Rev 2.00
Jun 21, 2016

The ISL36411 is a quad receive-side equalizer with extended functionality for advanced protocols operating with line rates up to 11.1Gbps. It integrates a driver/limiting amplifier with a programmable equalizer to compensate for the frequency dependent attenuation of PCB traces and twin-axial cables. The ISL36411 is capable of extending signal reach up to 10m on 28AWG cable. Supported protocols include 4k/8k video capable DisplayPort v1.3 (HBR1/2/3), USB 3.1 Gen 2 at 10Gbps. InfiniBand (QDR), 40G Ethernet (40GBASECR4/SR4), and 10G SFP+ specification (SFF-8431).

The small form factor, highly-integrated quad design is ideal for high-density data transmission applications including active copper cable assemblies. The four equalizing filters within the ISL36411 can each be set to provide optimal signal fidelity for a given media and length. The compensation level for the filters is set by two external control pins.

Operating on a single 1.2V power supply, the ISL36411 enables per channel throughputs of up to 11.1Gbps while passing USB3.x LFPS signals as low as 100kHz. High data rates are achieved by using Current Mode Logic (CML) inputs and outputs and is packaged in a 4mmx7mm 46 Ld QFN. Individual lane LOS support is included for module applications.

Related Literature

- AN1573, "ISL36411 Evaluation Board User Guide"

Features

- Supports four channels with data rates up to 11.1Gbps
- Low power (~110mW per channel)
- Low latency (<500ps)
- Four equalizers in 4mmx7mm QFN package for straight route-through architecture and simplified routing
- Equalizer boost is pin selectable
- Pin selectable equalizer boosts
- Supports 64b/66b encoded data - long run lengths
- Line silence preservation and individual lane LOS support
- 1.2V power supply
- LOS support

Applications

- DisplayPort v1.3 active copper cable modules
- QSFP active copper cable modules
- InfiniBand QDR
- 40G ethernet (40GBase-CR4/SR4)
- 100G ethernet (100GBase-CR10/SR10)
- High-speed Printed Circuit Board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach 3x
- Improved BER

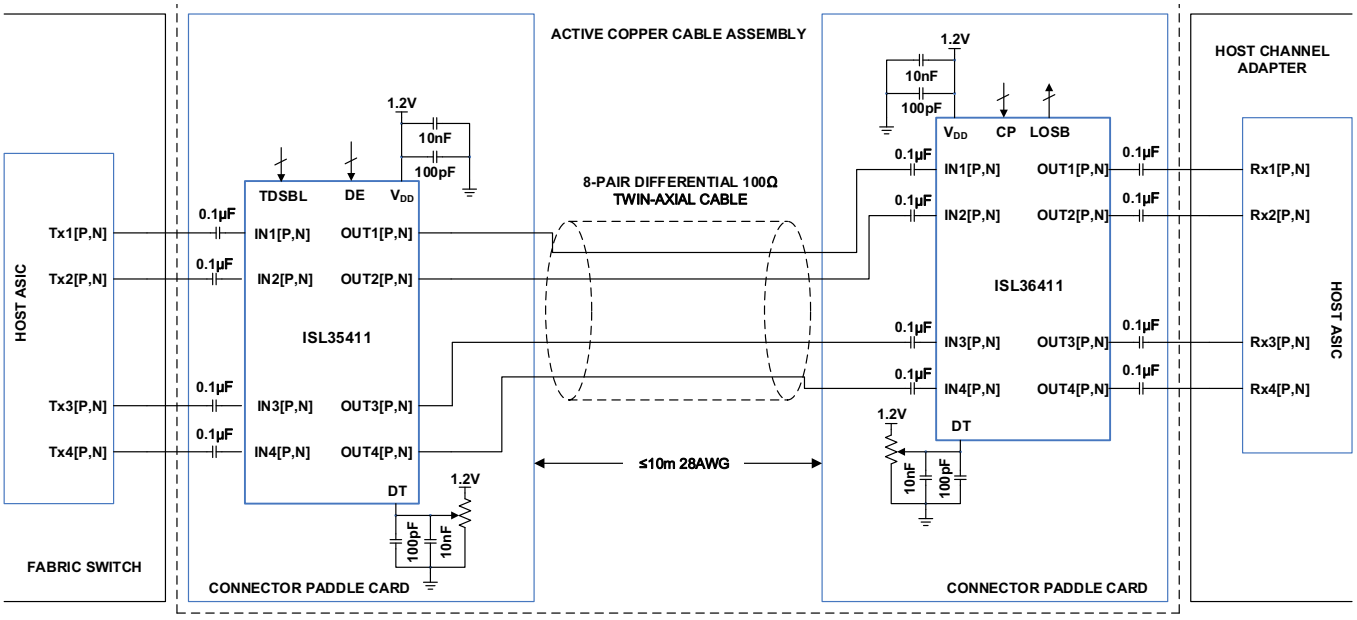


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL36411DRZ-TS	ISL36411DRZ	0 to +85	100 (Sample Reel)	46 Ld QFN	L46.4x7
ISL36411DRZ-T7	ISL36411DRZ	0 to +85	1k	46 Ld QFN	L46.4x7
ISL36411DRZ-EVALZ	Evaluation Board				

NOTES:

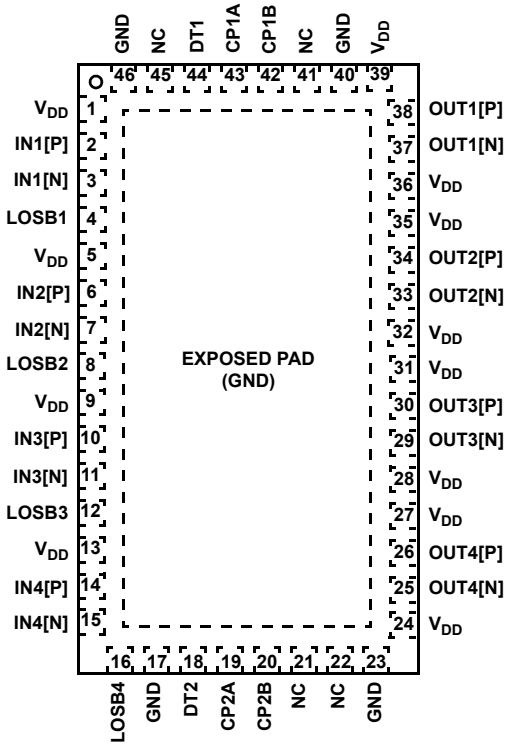
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL36411. For more information on MSL, please see tech brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	DATA RATE (Gb/s)	NUMBER OF Tx OR Rx	POWER CONSUMPTION (mW)	MAXIMUM CABLE LENGTH (24AWG) (m)	DIFFERENTIAL O/P SWING (mV_{P-P})	DE-EMPHASIS (dB)	EQUALIZATION (dB)	DIFFERENCES BETWEEN QLX PARTS	TARGET MARKET
ISL36411	11	4x Rx	440	20	650	N/A	30	N/A	DP1.3, 40GbE, QSFP+
ISL35411	11	4x Tx	340	20	600	4	N/A	N/A	DP1.3, 40GbE, QSFP+
QLX4600-SL30	6.25	4x Rx	312	30	600	N/A	30	4 pins for Loss of Signal (LOS)	DP1.2, SAS-6Gb, PCIe 2.0
QLX4600-S30	6.25	4x Rx	312	30	600	N/A	30	4 pins for Impedance Selection (= Power Down)	DP1.2, SAS-6Gb, PCIe 2.0

Pin Configuration

ISL36411
(46 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 5, 9, 13, 24, 27, 28, 31, 32, 35, 36, 39	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high frequency noise suppression.
IN1[P, N]	2, 3	Equalizer 1 differential input, CML. the use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB1	4	LOS BAR indicator 1. Low output when IN1 signal is below DT threshold.
IN2[P, N]	6, 7	Equalizer 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB2	8	LOS BAR indicator 2. Low output when IN2 signal is below DT threshold.
IN3[P, N]	10, 11	Equalizer 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB3	12	LOS BAR indicator 3. Low output when IN3 signal is below DT threshold.
IN4[P, N]	14, 15	Equalizer 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB4	16	LOS BAR indicator 4. Low output when IN4 signal is below DT threshold.
GND	17, 23, 40, 46	These pins should be grounded.
DT2	18	Detection Threshold for equalizers 3 and 4. Reference DC voltage threshold for input signal power detection. Data output OUT3 and OUT4 are muted when the power of IN3 and IN4, respectively, fall below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
CP2[A,B]	19, 20	Control pins for setting equalizers 3 and 4. CMOS logic inputs. Pins are read as a 2-digit number to set the boost level. A is the MSB and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
NC	21, 22, 41, 45	not connected: do not make any connections to these pins.
OUT4[N, P]	25, 26	Equalizer 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT3[N, P]	29, 30	Equalizer 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT2[N, P]	33, 34	Equalizer 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT1[N, P]	37, 38	Equalizer 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
CP1[B, A]	42, 43	Control pins for setting equalizers 1 and 2. CMOS logic inputs. Pins are read as a 2-digit number to set the boost level. A is the MSB and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
DT1	44	Detection Threshold for equalizers 1 and 2. Reference DC voltage threshold for input signal power detection. Data output OUT1 and OUT2 are muted when the power of IN1 and IN2, respectively, fall below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
Exposed Pad	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.5V
Voltage at All Input Pins. . . . . -0.3V to 1.5V
ESD Ratings
Human Body Model
High-Speed Pins 1.5kV
All Other Pins 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
46 Ld QFN Package (Notes 4, 5)	33	2.8

Operating Ambient Temperature Range . . . . . 0°C to +85°C
Storage Ambient Temperature Range. . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data applied to any channel	2.5		11.1	Gbps

Control Pin Characteristics V_{DD} = 1.2V, T_A = +25°C and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Output LOW Logic Level	V_{OL}	LOS[k]	0		250	mV
Output HIGH Logic Level	V_{OH}	LOS[k]	750		V_{DD}	mV
Input Current		Current draw on digital pin, i.e., CP[k][A,B]		100	200	µA

Electrical Specifications V_{DD} = 1.2V, T_A = +25°C and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETERS	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	NOTES
Supply Current	I_{DD}			368		mA	
Cable Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss; Up to 10m 28AWG standard twin-axial cable (approx. -27dB at 5GHz)	600		1600	mV_{P-P}	7
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N, with respect to V_{DD}	40	50	60	Ω	
Input Return Loss Limit (Differential)	$S_{DD}11$	100MHz to 4.1GHz		Note 8		dB	8
		4.1GHz to 11.1GHz		Note 9		dB	9
Input Return Loss Limit (Common-Mode)	$S_{CC}11$	100MHz to 2.5GHz		Note 10		dB	10
		2.5GHz to 11.1GHz		-3		dB	15
Input Return Loss Limit (Common-Mode to Differential Conversion)	$S_{DC}11$	100MHz to 11.1GHz		-10		dB	15

Electrical Specifications V_{DD} = 1.2V, T_A = +25°C and V_{IN} = 600mV_{P-P}, unless otherwise noted. (Continued)

PARAMETERS	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	NOTES
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins	450	600	850	mV_{P-P}	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss Limit (Differential)	$S_{DD}22$	100MHz to 4.1GHz		Note 8		dB	8
		4.1MHz to 11.1GHz		Note 9		dB	9
Output Return Loss Limit (Common-Mode)	$S_{CC}22$	100MHz to 2.5GHz		Note 10		dB	10
		2.5MHz to 11.1GHz		-3		dB	15
Output Return Loss Limit (Common-Mode to Differential Conversion)	$S_{DC}22$	100MHz to 11.1GHz		-10		dB	15
Output Residual Jitter		10Gbps; Up to 10m 28AWG std twin-axial cable (~ -27dB at 5GHz); 1200mV_{P-P} ≤ VIN ≤ 1600mV_{P-P}		0.35		UI	7, 11, 12
Output Transition Time	t_r, t_f	20% to 80%		32		ps	13
Lane-to-Lane Skew				50		ps	15
Propagation Delay		From IN[k] to OUT[k]		500		ps	15
LOS Assert Time		Time to assert loss-of-signal indicator when transitioning from active data mode to line silence mode		50		µs	14
LOS Deassert Time		Time to assert loss-of-signal indicator when transitioning from line silence mode to active data mode		50		µs	14
Data-to-Line Silence Response Time		K28.5 data pattern at 10Gbps		100		µs	14
Data-to-Line Silence Response Time		K28.5 data pattern at 10Gbps		100		µs	14

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. After channel loss, differential amplitudes at ISL36411 inputs must meet the input voltage range specified in "Absolute Maximum Ratings" on page 5.
8. Maximum Reflection Coefficient given by equation SDDXX(dB)= -12 + 2*√(f), with f in GHz. Established by characterization and not production tested.
9. Maximum Reflection Coefficient given by equation SDDXX(dB)= -6.3+13Log10(f/5.5), with f in GHz. Established by characterization and not production tested.
10. Reflection Coefficient given by equation SCCXX(dB) < -7 + 1.6*f, with f in GHz. Established by characterization and not production tested.
11. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (TJ) is DJ_{P-P} + 14.1 x RJ_{RMS}.
12. Measured using a PRBS 2^7-1 pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
13. Rise and fall times measured using a 1GHz clock with a 20ps edge rate.
14. For active data mode, cable input amplitude is 300mV_{P-P} (differential) or greater. For line silence mode, cable input amplitude is 20mV_{P-P} (differential) or less. Established by characterization and not production tested.
15. Limits established by characterization and are not production tested.

Typical Performance Characteristics

Performance is measured using the test setup illustrated in Figure 1. The signal from the pattern generator is launched into the twin-axial cable using an SMA adapter card. The chip evaluation board is connected to the output of the cable through another adapter card. The ISL36411 output signal is then visualized on a scope to determine signal integrity parameters such as jitter.

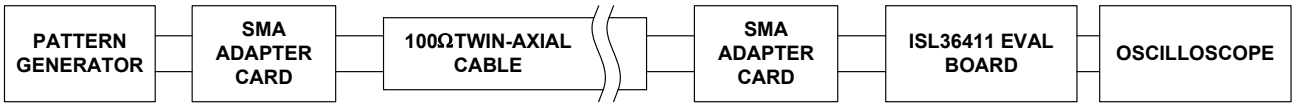


FIGURE 2. DEVICE CHARACTERIZATION SET UP

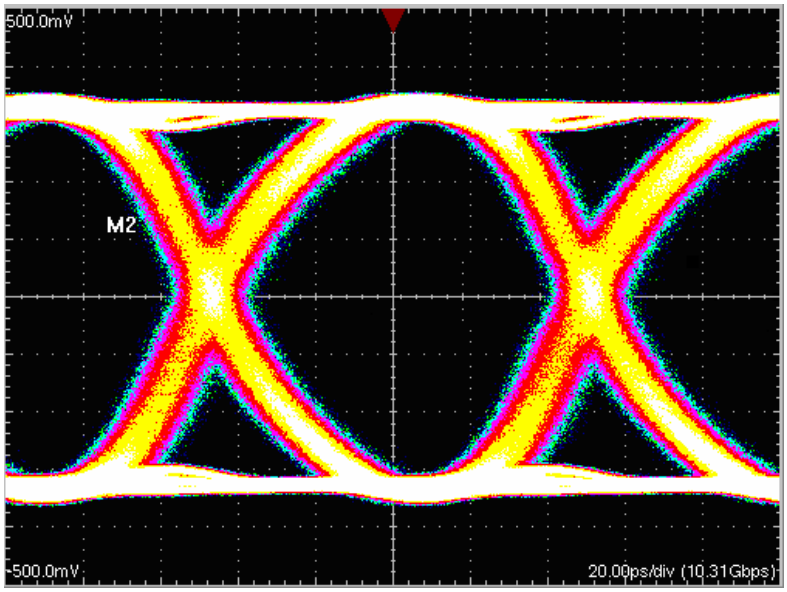


FIGURE 3. ISL36411 10.3125Gb/s OUTPUT FOR A 10M 28AWG CABLE

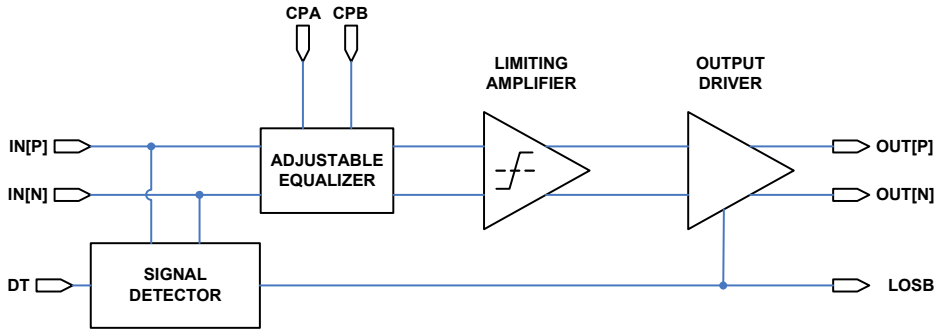


FIGURE 4. FUNCTIONAL DIAGRAM OF A SINGLE CHANNEL WITHIN THE ISL36411

Operation

The ISL36411 is an advanced quad lane-extender for high-speed interconnects. A functional diagram of one of the four channels in the ISL36411 is shown in Figure 4. In addition to a robust equalization filter to compensate for channel loss and restore signal fidelity, the ISL36411 contains unique integrated features to preserve special signaling protocols typically broken by other equalizers. The signal detect function is used to mute the channel output when the equalized signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence ("quiescent state" in InfiniBand contexts). Furthermore, the output of the signal detect/DT comparator is used as a Loss Of Signal (LOS) indicator to indicate the absence of a received signal.

As illustrated in Figure 4, the core of each high-speed signal path in the ISL36411 is a sophisticated equalizer followed by a limiting amplifier. The equalizer compensates for skin loss, dielectric loss and impedance discontinuities in the transmission channel. Each equalizer is followed by a limiting amplification stage that provides a clean output signal with full amplitude swing and fast rise-fall times for reliable signal decoding in a subsequent receiver.

Adjustable Equalization Boost

Each channel in the ISL36411 features a settable (in pairs) equalizer for custom signal restoration. The flexibility of this adjustable compensation architecture enables signal fidelity to be optimized on a channel-by-channel basis, providing support for a wide variety of channel characteristics and data rates ranging from 2.5Gbps to 11.1Gbps. Because the boost level is externally set rather than internally adapted, the ISL36411 provides reliable communication from the very first bit transmitted. There is no time needed for adaptation and control loop convergence. Furthermore, there are no pathological data patterns that will cause the ISL36411 to move to an incorrect boost level.

Control Pin Boost Setting

The connectivity of the CP pins is used to determine the boost level of each pair of channels. CP1 controls the boost of channels 1 and 2, CP2 controls the boosts of channels 3 and 4. Table 2 defines the mapping from the 2-bit CP word to the 8 possible boost levels.

TABLE 2. MAPPING BETWEEN BOOST LEVEL AND CP-PIN CONNECTIVITY

CPA	CPB	BOOST LEVEL
Float	Float	0
Float	GND	1
GND	V_{DD}	2
Float	V_{DD}	3
V_{DD}	Float	4
GND	Float	5
GND	GND	6
V_{DD}	GND	7
V_{DD}	V_{DD}	8

ISL36411 CML Input and Output Buffers

The input and output buffers for the high-speed data channels in the ISL36411 are implemented using CML (shown in Figures 5 and 6).

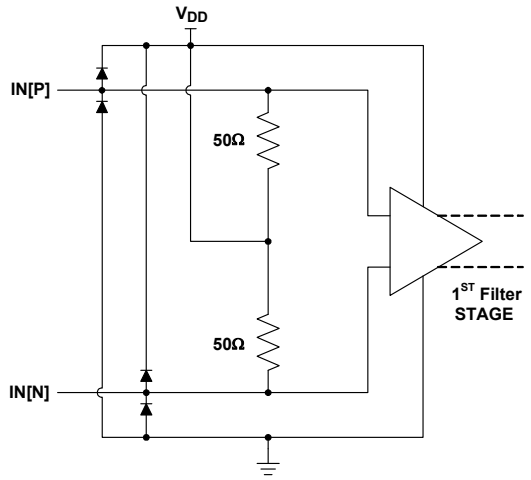


FIGURE 5. CML INPUT EQUIVALENT CIRCUIT

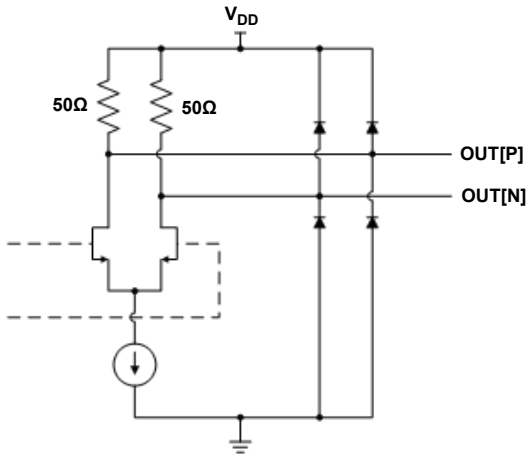


FIGURE 6. CML OUTPUT EQUIVALENT CIRCUIT

LINE SILENCE/QUIESCENT MODE

Line silence is commonly broken by the limiting amplification in other equalizers. This disruption can be detrimental in many systems that rely on line silence as part of the protocol. The ISL36411 contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the equalized signal and comparing that to a threshold set by the voltage at the DT pin. When the amplitude falls below the threshold, the output driver stages are muted and held at their nominal common-mode voltage.

NOTE: The output common-mode voltage remains constant during both active data transmission and output muting modes.

LOS Bar Indicator

Pins LOSB[k] are used to output the state of the muting circuitry to serve as a loss of signal indicator for channel k. This signal is directly derived from the muting signal off the DT-threshold signal detector output. The LOS signal goes LOW when the power signal is below the DT threshold and HIGH when the power goes above the DT threshold. This feature is meant to be used in optical systems (e.g. QSFP) where there are no quiescent or electrical-idle states. In these cases, the DT threshold is used to determine the sensitivity of the LOS indicator.

Detection Thereshold (DT) Pin Functionality

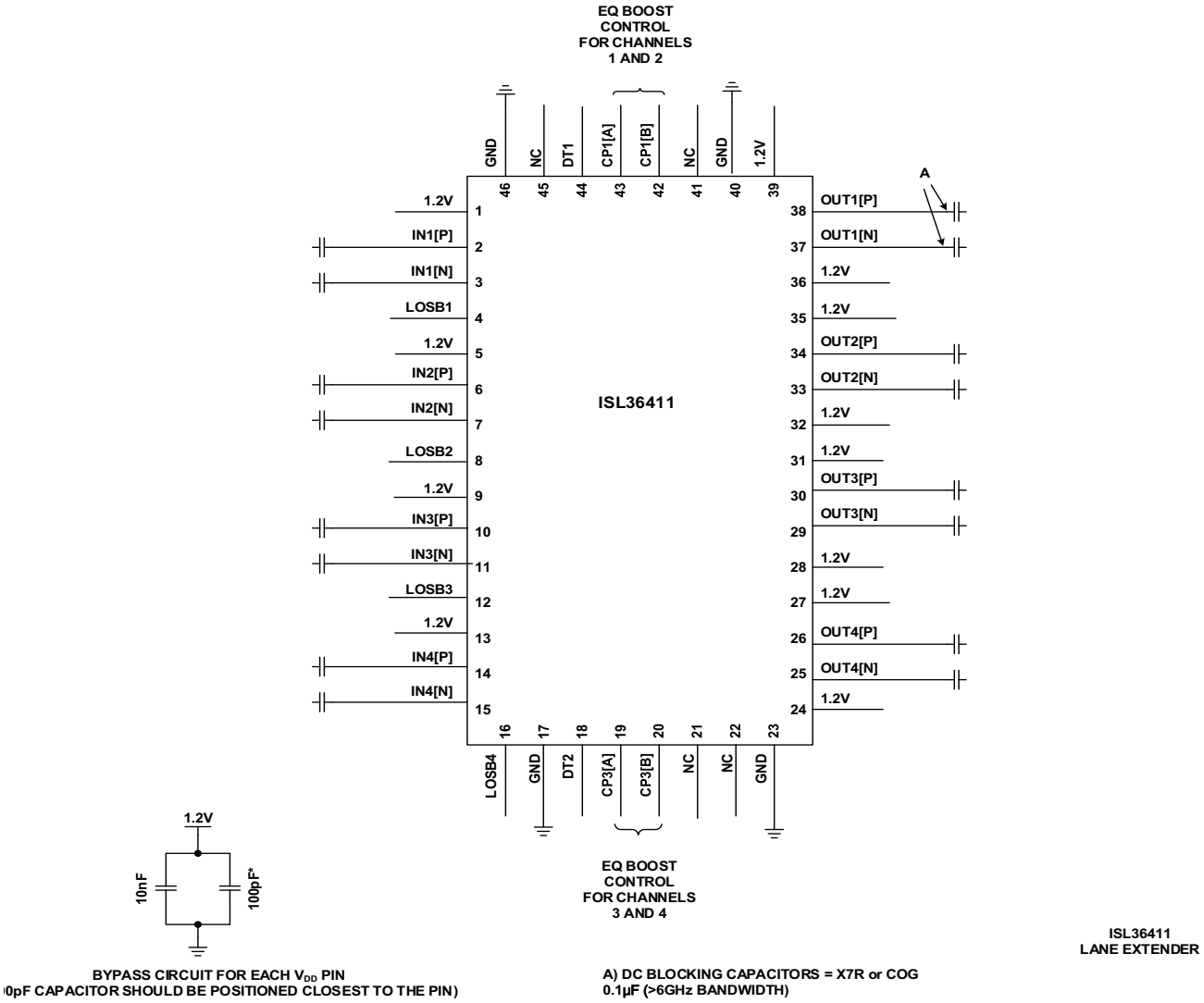
The ISL36411 is capable of maintaining periods of line silence by monitoring the channel for Loss Of Signal (LOS) conditions and subsequently muting the output driver when such a condition is detected. A reference voltage applied to the Detection Threshold (DT) pins is used to set the LOS threshold of the internal signal detection circuitry (one pin for a pair of channels). The DT voltage is set with an external pull-up resistor, RDT. For typical applications, a 15kΩ resistor is recommended for channels with loss greater than 12dB at 5GHz and a 0.9kΩ resistor is recommended for lower loss channels. Other values of the resistor may also be applicable; therefore DT settings should be verified on an application-specific basis.

PCB Layout Considerations

Because of the high speed of the ISL36411 signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All high speed differential pair traces should have a characteristic impedance of 50Ω with respect to ground plane and 100Ω with respect to each other.
- Avoid using vias for high speed traces as this will create discontinuity in the traces' characteristic impedance.
- Input and output traces need to have DC blocking capacitors (100nF). Capacitors should be placed as close to the chip as possible.
- For each differential pair, the positive trace and the negative trace need to be of the same length in order to avoid intra-pair skew. A Serpentine technique may be used to match trace lengths.
- Maintain a constant solid ground plane underneath the high-speed differential traces.
- Each V_{DD} pin should be connected to 1.2V and also bypassed to ground through a 10nF and a 100pF capacitor in parallel. Minimize the trace length and avoid vias between the V_{DD} pin and the bypass capacitors in order to maximize the power supply noise rejection.
- If 4 channels of the device are set to the same boost, then the quantity of CP resistors can be reduced by tying both CP pins together.

Application Information



NOTES:

16. See "Control Pin Boost Setting" on page 8 for information on how to connect the CP pins.
17. See "Detection Thereshold (DT) Pin Functionality" on page 9 for details on DT pin operation.

FIGURE 7. TYPICAL APPLICATION REFERENCE SCHEMATIC

About Q:ACTIVE Technology

Intersil has long realized that to enable the complex server clusters of next generation data centers, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE™ product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency and cable gauge size as well as increased airflow in tomorrow's data centers. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding data center.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow and improves power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
June 21, 2016	FN6965.2	Updated page 1 description of part. Added applications bullet "DisplayPort v1.3 active copper cable modules". Removed "High-speed active cable assemblies" application bullet. Added Related Literature section on page 1. Added Table 1 on page 2. Added Note 6 on page 6 and referenced in specification tables. Replaced Products section with the About Intersil section. Updated POD L46.4x7 to the latest revision changes are as follows: -3/15/13 Side view, changed pkg thickness from 0.70+/-0.05 to 0.75+/-0.05 Detail x, changed from 0.152 REF to 0.203 REF.
March 16, 2010	FN6965.1	page 5 Control pin characteristics: VOL: delete typical "0" Input current: max 200, typ 100 page 6 Output res jitter: 0.35 In Entries from Lane-to-Lane Skew all the way down, all the numbers should move to typ column Added High-Speed pins to ESD Ratings as follows to Abs Max Ratings: ESD Ratings Human Body Model High-Speed Pins 1.5kV All Other Pins 2kV Removed board footprint from page 10 due to information covered in outline drawing.
February 8, 2010	FN6965.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

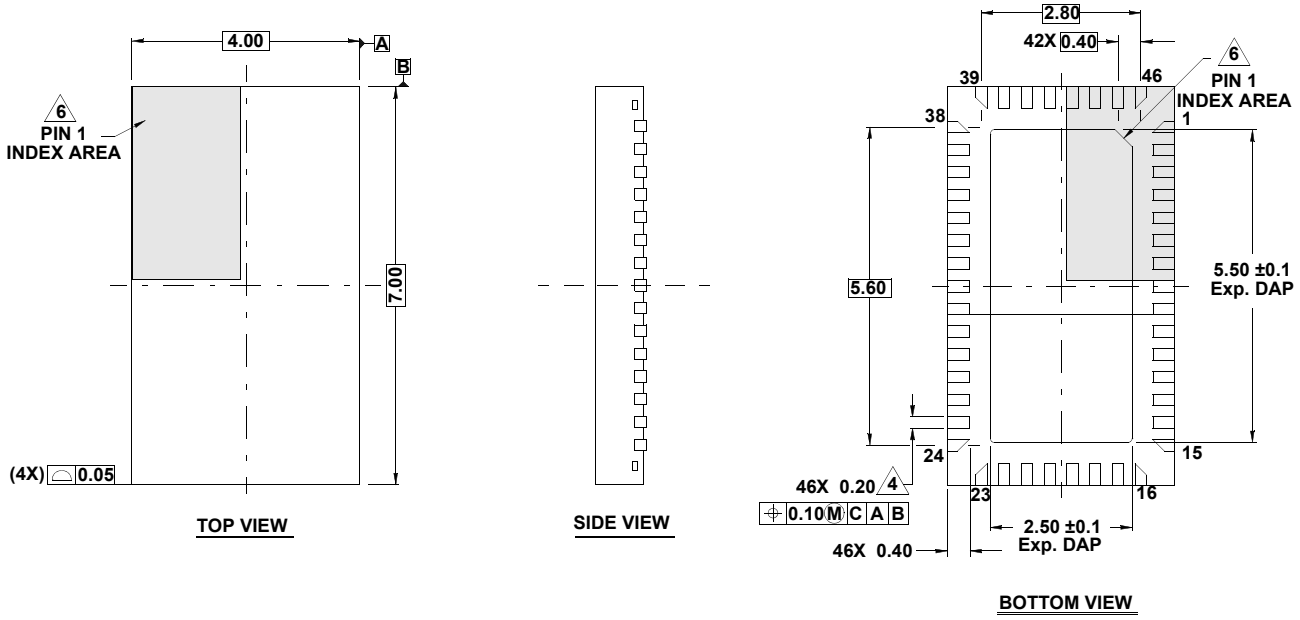
Reliability reports are also available from our website at www.intersil.com/support.

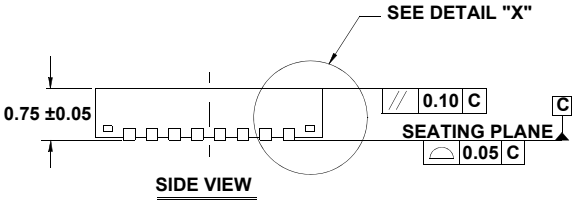
Package Outline Drawing

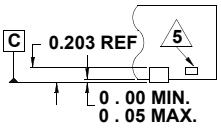
L46.4x7

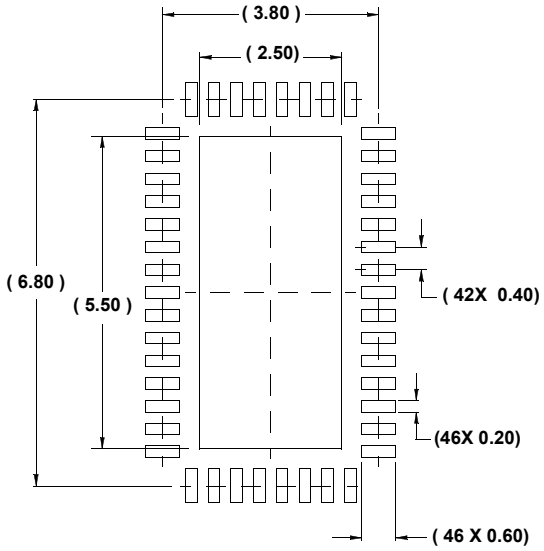
46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)

Rev 1, 3/13









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.