RoHS Compliant

NPN LOW POWER SILICON TRANSISTOR

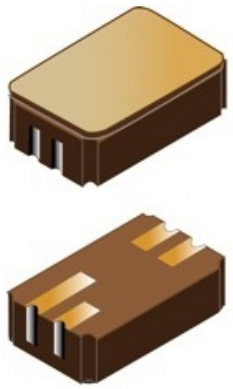
Qualified per MIL-PRF-19500/368

Qualified Levels:
JAN, JANTX, JANTXV and JANS

DESCRIPTION

This family of 2N3439UA through 2N3440UA high-frequency, epitaxial planar transistors feature low saturation voltage. The UA package is hermetically sealed and provides a low profile for minimizing board height. These devices are also available in U4, TO-5 and TO-39 packaging. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website http://www.microsemi.com.



UA Package

FEATURES

- JEDEC registered 2N3439UA through 2N3440UA series.
- JAN, JANTX, JANTXV, and JANS qualifications are available per MIL-PRF-19500/368.
- RoHS compliant by design.
- $V_{CE(sat)}$ = 0.5 V @ I_C = 50 mA.
- Turn-On time t_{on} = 1.0 µs max @ I_C = 20 mA, I_{B1} = 2.0 mA.
- Turn-Off time t_{off} = 10 µs max @ I_C = 20 mA, I_{B1} = -I_{B2} = 2.0 mA.

APPLICATIONS / BENEFITS

- General purpose transistors for medium power applications requiring high frequency switching and low package profile.
- Military and other high-reliability applications.

Also available in:

U4 package
(surface mount)
2N3439U4 – 2N3440U4

TO-5 package
(long leaded)
2N3439L – 2N3440L

TO-39 package
(leaded)
2N3439 – 2N3440

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Parameters / Test Conditions	Symbol	2N3439UA	2N3440UA	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	V
Collector-Base Voltage	V_{CBO}	450	300	V
Emitter-Base Voltage	V_{EBO}	7.0		V
Collector Current	I_C	1.0		A
Total Power Dissipation @ T_A = +25 °C (1) @ T_C = +25 °C (2) UA @ T_{SP} = +25 °C (3)	P_D	0.8 5.0 2.0		W
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

Notes: 1. Derate linearly @ 4.57 mW/°C for T_A > +25 °C.
2. Derate linearly @ 28.5 mW/°C for T_C > +25 °C.
3. Derate linearly @ 14 mW/°C for T_{SP} > +25 °C.

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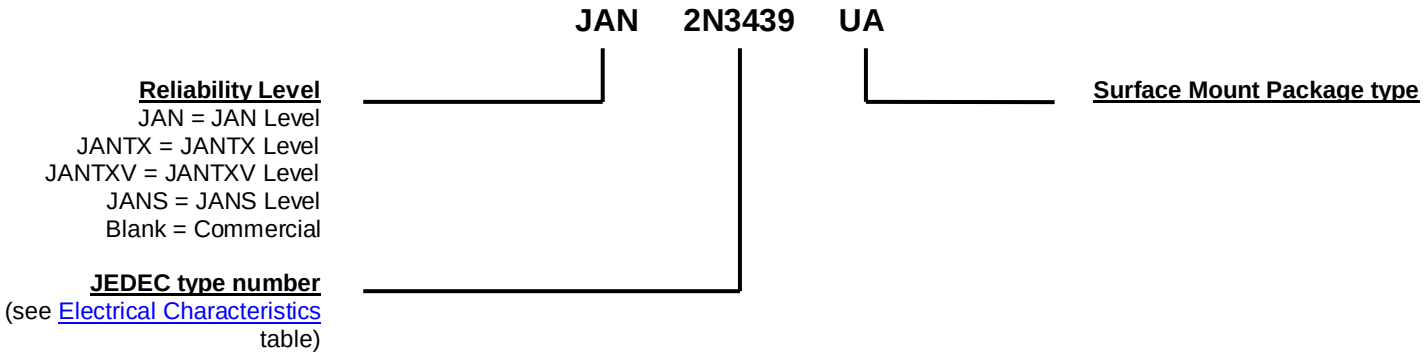
MECHANICAL and PACKAGING

- CASE: Hermetically sealed ceramic package.
- TERMINALS: Gold plate over nickel.
- MARKING: Manufacturer's ID, date code, part number.
- POLARITY: NPN (see package outline).
- TAPE & REEL option: Per EIA-481. Consult factory for quantities.
- WEIGHT: 0.12 grams.
- See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
C_{ibo}	Common-base open-circuit input capacitance.
C_{obo}	Common-base open-circuit output capacitance.
I_{CEO}	Collector cutoff current, base open.
I_{CEX}	Collector cutoff current, circuit between base and emitter.
I_{EBO}	Emitter cutoff current, collector open.
h_{FE}	Common-emitter static forward current transfer ratio.
V_{BE}	Base-emitter voltage, dc .
V_{CE}	Collector-emitter voltage, dc.
V_{CEO}	Collector-emitter voltage, base open.
V_{CBO}	Collector-emitter voltage, emitter open.
V_{EB}	Emitter-base voltage, dc .
V_{EBO}	Emitter-base voltage, collector open.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted)

OFF CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10 mA R_{BB1} = 470 Ω; V_{BB1} = 6 V L = 25 mH (min); f = 30 – 60 Hz	2N3439UA 2N3440UA	$V_{(BR)CEO}$	350 250		V
Collector-Emitter Cutoff Current V_{CE} = 300 V V_{CE} = 200 V	2N3439UA 2N3440UA	I_{CEO}		2.0 2.0	µA
Emitter-Base Cutoff Current V_{EB} = 7.0 V		I_{EBO}		10	µA
Collector-Emitter Cutoff Current V_{CE} = 450 V, V_{BE} = -1.5 V V_{CE} = 300 V, V_{BE} = -1.5 V	2N3439UA 2N3440UA	I_{CEX}		5.0 5.0	µA
Collector-Base Cutoff Current V_{CB} = 360 V V_{CB} = 250 V V_{CB} = 450 V V_{CB} = 300 V	2N3439UA 2N3440UA 2N3439UA 2N3440UA	I_{CBO}		2.0 2.0 5.0 5.0	µA

ON CHARACTERISTICS (1)

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Forward-Current Transfer Ratio I_C = 20 mA, V_{CE} = 10 V I_C = 2.0 mA, V_{CE} = 10 V I_C = 0.2 mA, V_{CE} = 10 V	h_{FE}	40 30 10	160	
Collector-Emitter Saturation Voltage I_C = 50 mA, I_B = 4.0 mA	$V_{CE(sat)}$		0.5	V
Base-Emitter Saturation Voltage I_C = 50 mA, I_B = 4.0 mA	$V_{BE(sat)}$		1.3	V

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 10 mA, V_{CE} = 10 V, f = 5.0 MHz	$\|h_{fe}\|$	3.0	15	
Forward Current Transfer Ratio I_C = 5.0 mA, V_{CE} = 10 V, f = 1.0 kHz	h_{fe}	25		
Output Capacitance V_{CB} = 10 V, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{obo}		10	pF
Input Capacitance V_{CB} = 5.0 V, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{ibo}		75	pF

(1) Pulse Test: Pulse Width = 300 µs, duty cycle ≤ 2.0%.

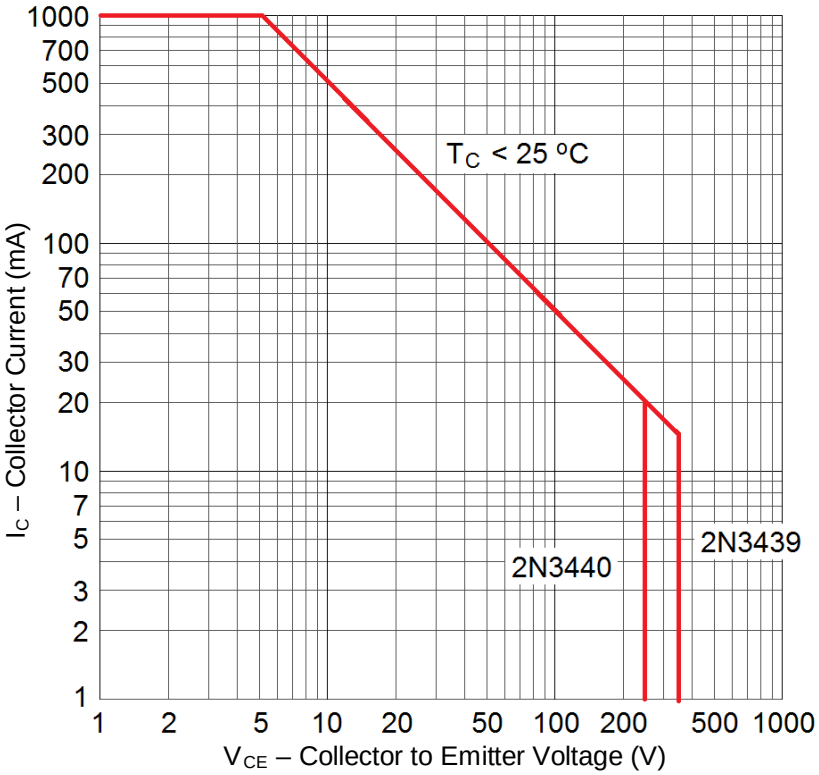
ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted) continued

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time V_{CC} = 200 V; I_C = 20 mA, I_{B1} = 2.0 mA	t_{on}		1.0	µs
Turn-Off Time V_{CC} = 200 V; I_C = 20 mA, I_{B1} = -I_{B2} = 2.0 mA	t_{off}		10	µs

SAFE OPERATING AREA (See graph below and also reference test method 3053 of MIL-STD-750.)

DC Tests	
T_C = +25 °C, 1 Cycle, t = 1.0 s	
Test 1	
V_{CE} = 5.0 V, I_C = 1.0 A	Both Types
Test 2	
V_{CE} = 350 V, I_C = 14 mA	2N3439UA
Test 3	
V_{CE} = 250 V, I_C = 20 mA	2N3440UA



Maximum Safe Operating graph (continuous dc)

GRAPHS

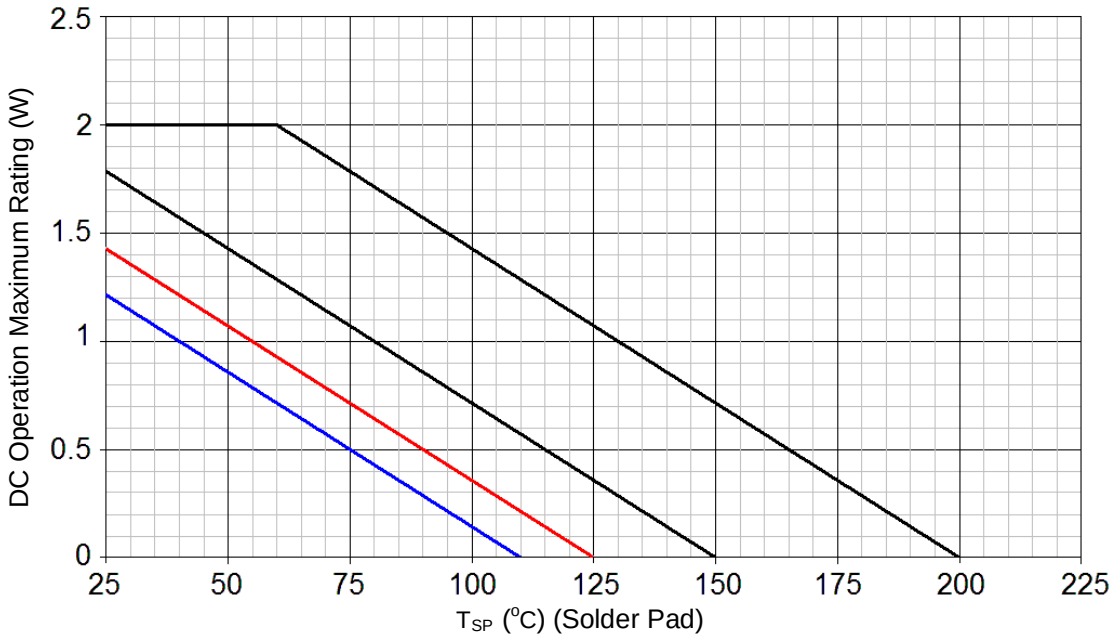


FIGURE 1
Temperature-Power Derating Curve
NOTES: Thermal Resistance Junction to Solder Pad = 70.0 °C/W
Max Finish-Alloy Temp = 175.0 °C

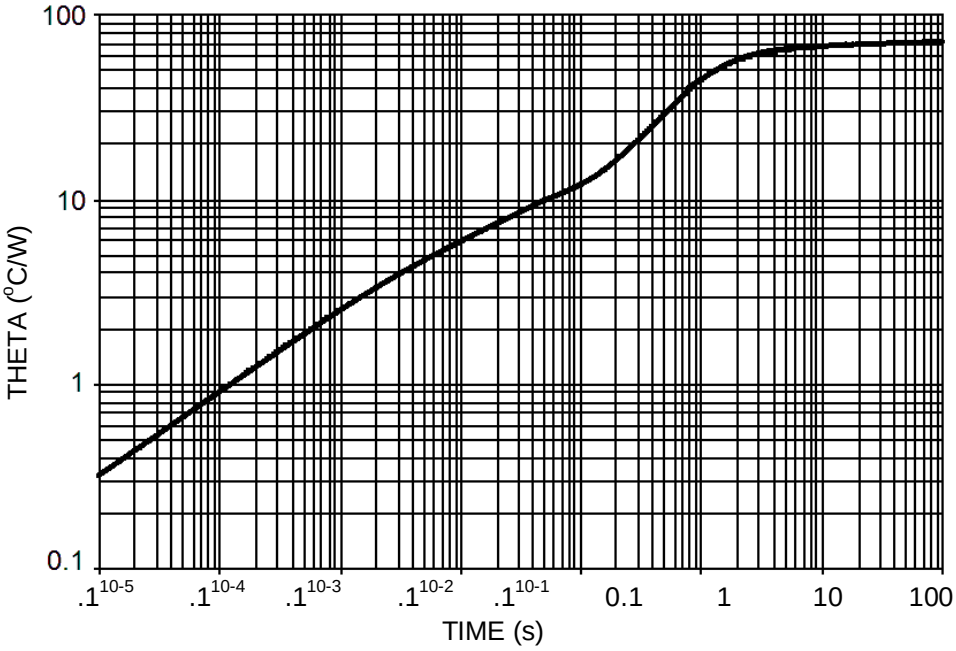
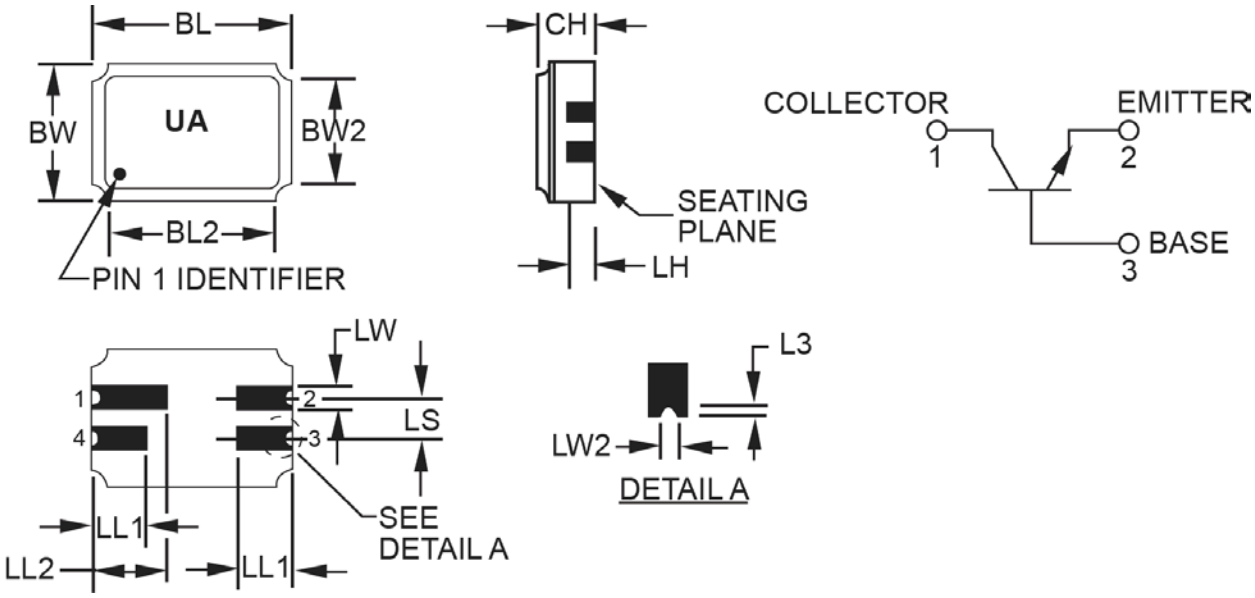


FIGURE 2
Maximum Thermal Impedance
NOTE: T_C = +25 °C, Thermal Resistance $R_{\theta JSP}$ = 70.0 °C/W, Pdiss = 2 W.

PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions " LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension " LW2" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	0.215	0.225	5.46	5.71	
BL2		0.225		5.71	
BW	0.145	0.155	3.68	3.93	
BW2		0.155		3.93	
CH	0.061	0.075	1.55	1.90	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	
LL1	0.032	0.048	0.81	1.22	
LL2	0.072	0.088	1.83	2.23	
LS	0.045	0.055	1.14	1.39	
LW	0.022	0.028	0.56	0.71	
LW2	0.006	0.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

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2N3439UA/TR