SLG59M1649V

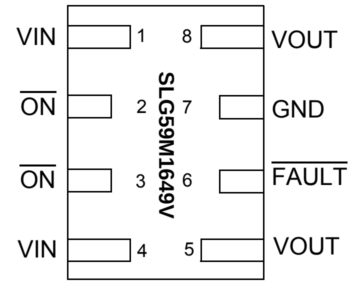
An Ultra-small, Low-power 23 mΩ/4 A P-Channel Integrated Power Switch with Reverse-Current Blocking

General Description

The SLG59M1649V is a self-powered, high-performance, 23 mΩ pFET integrated power switch designed for 1.5 to 5 V power rail applications up to 4 A. When enabled, internal reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a VOUT+50mV > VIN condition opens the switch). Upon the detection of a reverse condition, an open-drain $\overline{\text{FAULT}}$ output is asserted. In the event the VIN voltage is too low, the power switch also contains an internal UVLO threshold monitor to keep or to turn the switch OFF.

Designed to operate over a -40°C to 85°C range, the SLG59M1649V is available in a RoHS-compliant, ultra-small 1.0 x 1.6 mm STDFN package.

Pin Configuration



8-pin STDFN
(Top View)

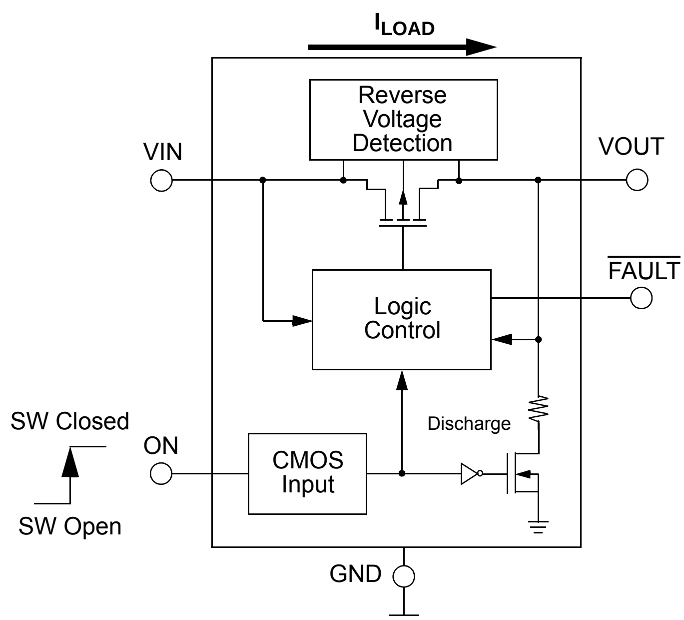
Features

- Steady-state Operating Current: Up to 4 A
- Low Typical RDS_{ON}:
  - 23 mΩ at VIN = 5 V
  - 31 mΩ at VIN = 2.5 V
  - 42 mΩ at VIN = 1.5 V
- Operating Voltage: 1.5 V to 5.5 V
- Reverse-voltage Detection ON or OFF
- Internal Gate Drive and VOUT Discharge
- Open-drain $\overline{\text{FAULT}}$ Signaling
- Operating temperature range: -40°C to 85°C
- Low θJA, 8-pin 1.0 mm x 1.6 mm STDFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant packaging

Applications

- Power-Rail Switching:
  - Notebook/Laptop/Tablet PCs
  - Smartphones/Wireless Handsets
  - High-definition Digital Cameras
  - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1, 4	VIN	Power/Input	With an internal 1.2V UVLO threshold, VIN supplies the power for the operation of the power switch, the internal control circuitry, and the source terminal of pFET. Bypass the VIN pin to GND with a 2.2 µF (or larger), low-ESR capacitor.
2, 3	ON	Input	A low-to-high transition on this pin initiates the operation of the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with VIL < 0.3 V and VIH > 1 V. As the ON input circuitry does not have an internal pull-down resistor, connect the ON pin directly to a GPIO controller – do not allow this pin to be open circuited.
5, 8	VOUT	Output	Output and drain terminal of MOSFET.
6	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within $T_{FAULT_{LOW}}$ when a (VOUT+VREVERSE > VIN) condition is detected. The $\overline{\text{FAULT}}$ output is deasserted within $T_{FAULT_{HIGH}}$ when the fault condition is removed. Connect an external 10-kΩ resistor from the $\overline{\text{FAULT}}$ pin to the system's local logic supply.
7	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1649V	STDFN	Industrial, -40 °C to 85 °C
SLG59M1649VTR	STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level			1		
Θ_{JA}	Thermal Resistance	1.0 x 1.6 mm 8L STDFN	--	82	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT	Each channel, T_J< 150°C	--	--	2	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	2.5	A
Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.						

Electrical Characteristics

1.5 V ≤ V_{IN} ≤ 5.5 V; C_{IN} = 2.2 µF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

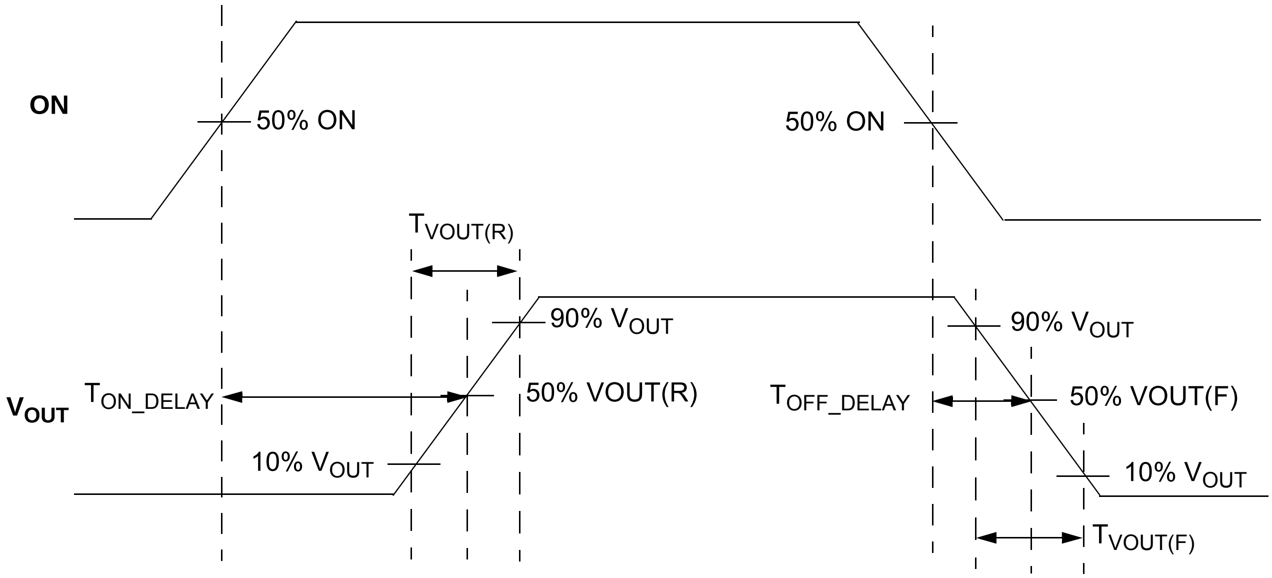
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Switch Input Voltage		1.5	--	5.5	V
$V_{IN(UVLO)}$	VIN Undervoltage Lockout Threshold	V_{IN} ↑, V_{ON} = 0V, I_{OUT} = -100mA	--	--	1.2	V
		V_{IN} ↓, V_{ON} = 0V, R_{LOAD} = 10Ω	0.5	--	--	V
I_{IN}	Quiescent Supply Current, Both Channels	V_{IN} = 5.25V, V_{ON} = HIGH, I_{OUT} = 0 mA	--	6.6	11	µA
		V_{IN} = 1.5 V, V_{ON} = HIGH, I_{OUT} = 0 mA	--	5	8	µA
$I_{IN(OFF)}$	OFF Mode Supply Current, Both Channels	V_{IN} = 5.25 V, V_{ON} = LOW, R_{LOAD} = 1 MΩ	--	2	3	µA
		V_{IN} = 1.5 V, V_{ON} = LOW, R_{LOAD} = 1 MΩ	--	0.8	2	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A = 25°C, V_{IN} = 5.0 V, I_{LOAD} = -200 mA	--	23	28	mΩ
		T_A = 25°C, V_{IN} = 2.5 V, I_{LOAD} = -200 mA	--	31	38	mΩ
		T_A = 25°C, V_{IN} = 1.5 V, I_{LOAD} = -200 mA	--	42	50	mΩ
$V_{REVERSE}$	Reverse-current Voltage Threshold		--	50	--	mV
$I_{REVERSE}$	Reverse-current Leakage Current after Reverse Current Event	$V_{OUT} – V_{IN} > V_{REVERSE}$; T_A = 25°C; ON = GND	--	1	--	µA
V_{ON}	ON Pin Voltage Range		0		V_{IN}	V
$I_{ON(Leakage)}$	ON Pin Leakage Current	1.4 V ≤ V_{ON} ≤ V_{IN}or V_{ON} = GND	--	--	1	µA
ON_V_{IH}	ON Pin Input High Voltage		1	--	V_{DD}	V
ON_V_{IL}	ON Pin Input Low Voltage		-0.3	0	0.3	V
ON_{HYS}	ON Hysteresis		--	60	--	mV

Electrical Characteristics (continued)

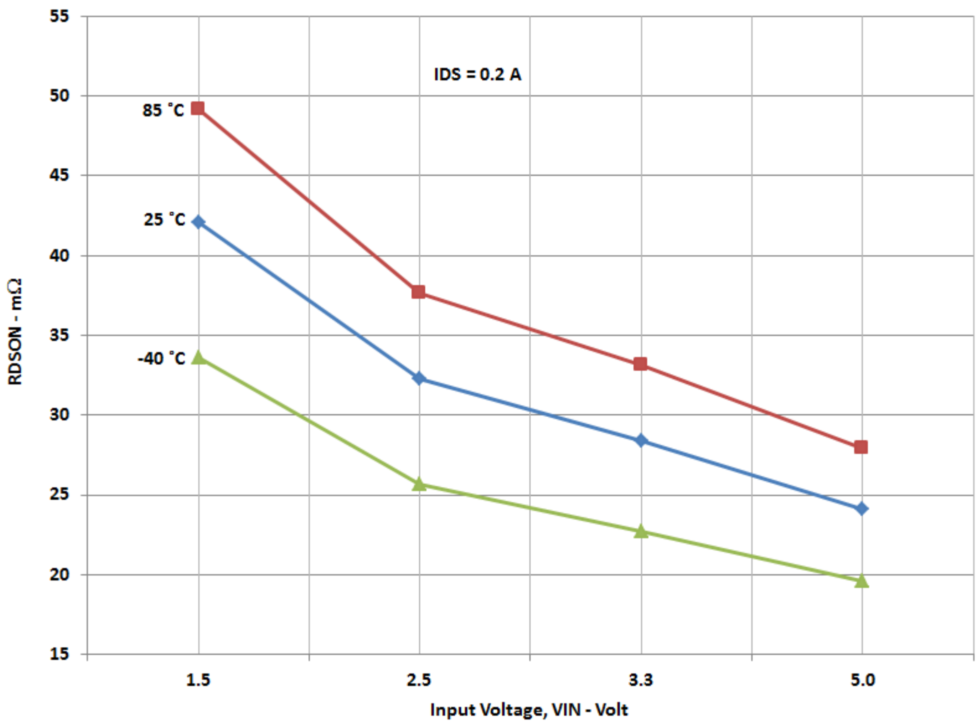
1.5 V ≤ V_{IN} ≤ 5.5 V; C_{IN} = 2.2 µF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
R_{DSCHRG}	Output Discharge Resistance	V_{IN} = 5 V; V_{OUT} < 0.4 V	50	80	120	Ω
T_{REV}	Reverse-current Detect Response Delay	V_{IN} = 5 V	--	10	--	µs
T_{REARM}	Reverse Detect Rearm Time		--	1.5	--	ms
T_{ON_Delay}	ON Delay Time	50% ON to 50% V_{OUT} ↑; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	180	235	µs
		50% ON to 50% V_{OUT} ↑; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	110	145	µs
$T_{VOUT(R)}$	VOUT Rise Time	10% to 90% V_{OUT} ↑; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	130	170	µs
		10% to 90% V_{OUT} ↑; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	66	86	µs
$T_{VOUT(F)}$	VOUT Fall Time	90% to 10% V_{OUT} ↓; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	2.2	3.6	µs
		90% to 10% V_{OUT} ↓; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	2.2	3.6	µs
T_{OFF_Delay}	OFF Delay Time	50% ON to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	3.5	5	µs
		50% ON to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	5	7	µs
$T\overline{FAULT}_{LOW}$	$\overline{\text{FAULT}}$ Assertion Time	Reverse-voltage Detection to $\overline{\text{FAULT}}$↓; 1.5 V ≤ $_{IN}$ ≤ 5 V; ON = Low	--	2	--	µs
		1.5 V ≤ V_{IN} ≤ 5 V; ON = High	--	0.5	--	µs
$T\overline{FAULT}_{HIGH}$	$\overline{\text{FAULT}}$ De-assertion Time	Delay to $\overline{\text{FAULT}}$↑ after fault condition is removed; 1.5 V ≤ V_{IN} ≤ 5 V; ON = Low	--	7	--	ms
		1.5 V ≤ V_{IN} ≤ 5 V; ON = High	--	2	--	ms
$\overline{FAULT}_{VOL}$	$\overline{\text{FAULT}}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1 mA	--	--	0.2	V

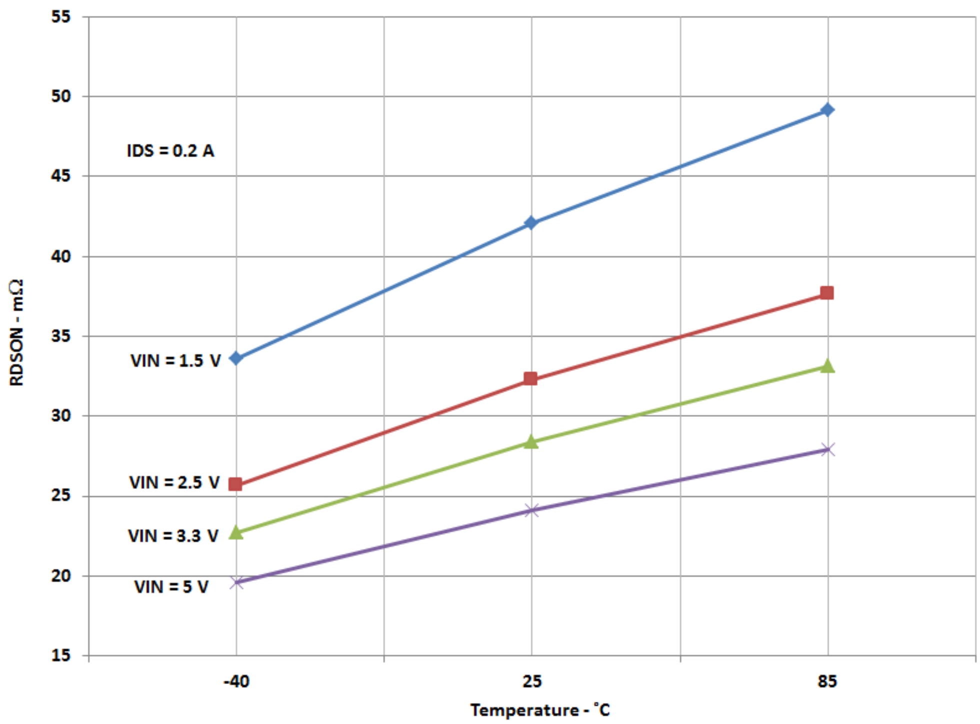
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



RDS$_{ON}$ vs. V$_{IN}$ and Temperature



RDS$_{ON}$ vs.Temperature and V$_{IN}$



VIN Inrush Current Details

When the SLG59M1649V is enabled with ON ↑, the power switch closes to charge the VOUT output capacitor to VIN. The charging current drawn from VIN is commonly referred to as "VIN inrush current" and can cause the input power source to collapse if the VIN inrush current is too high.

Since the VOUT rise time of the SLG59M1649V is fixed, VIN inrush current is then a function of the output capacitance at VOUT. The expression relating VIN inrush current, the SLG59M1649V VOUT rise time, and COUT is:

$$\text{VIN Inrush Current} = \text{COUT x } \frac{\Delta\text{VOUT}}{\text{VOUT Rise Time}}$$

where in this expression ΔVOUT is equivalent to VIN if the initial SLG59M1649V's output voltages are zero.

In the table below are examples of VIN inrush currents assuming zero initial charge on COUT as a function of VIN.

VIN	VOUT Rise Time	COUT	Inrush Current
1.5 V	66 µs	0.1 µF	2.3 mA
5 V	130 µs	0.1 µF	3.8 mA

Since the relationship is linear and if COUT were increased to 1 µF, then the VIN inrush currents would be 10x higher in either example. If a large COUT capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the CIN-to-COUT ratio to minimize VIN droop during turn-on.

For other VOUT rise time options, please contact Silego for additional information.

Power Dissipation

The junction temperature of the SLG59M1649V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1649V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{OUT}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{OUT} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \Theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

In nominal operating mode, the SLG59M1649V's power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{IN}-V_{OUT}) and the magnitude of that channel's output current (I_{OUT}):

$$PD_{TOTAL} = (V_{IN}-V_{OUT}) \times I_{OUT} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} - (R_{LOAD} \times I_{OUT})) \times I_{OUT}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

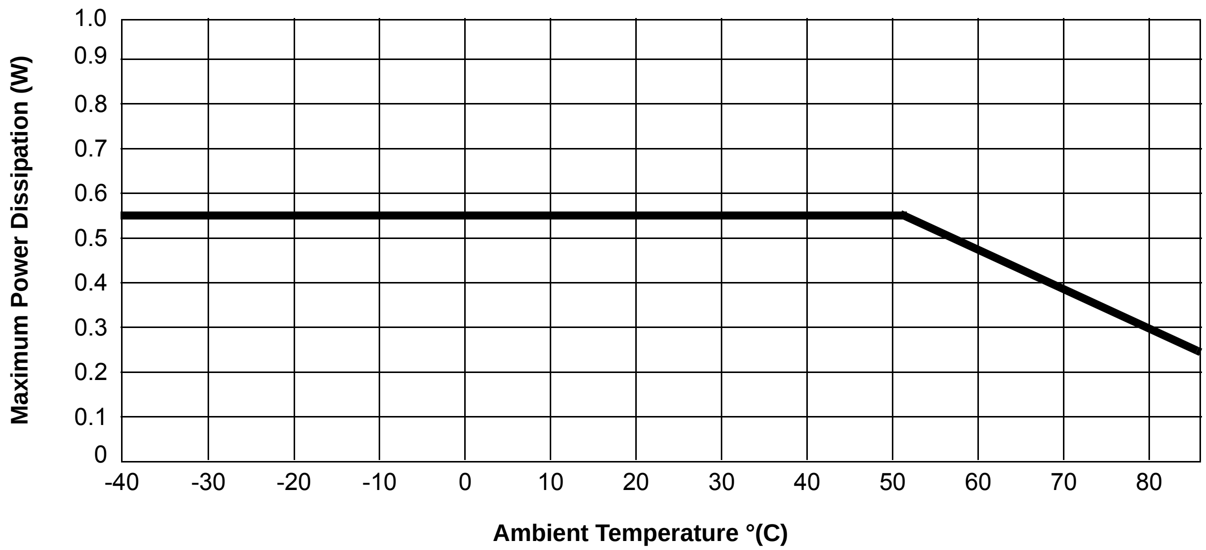
V_{IN} = Input Voltage, in Volts (V)

$R_{LOAD]}$ = Output Load Resistance, in Ohms (Ω)

I_{OUT} = Output current, in Amps (A)

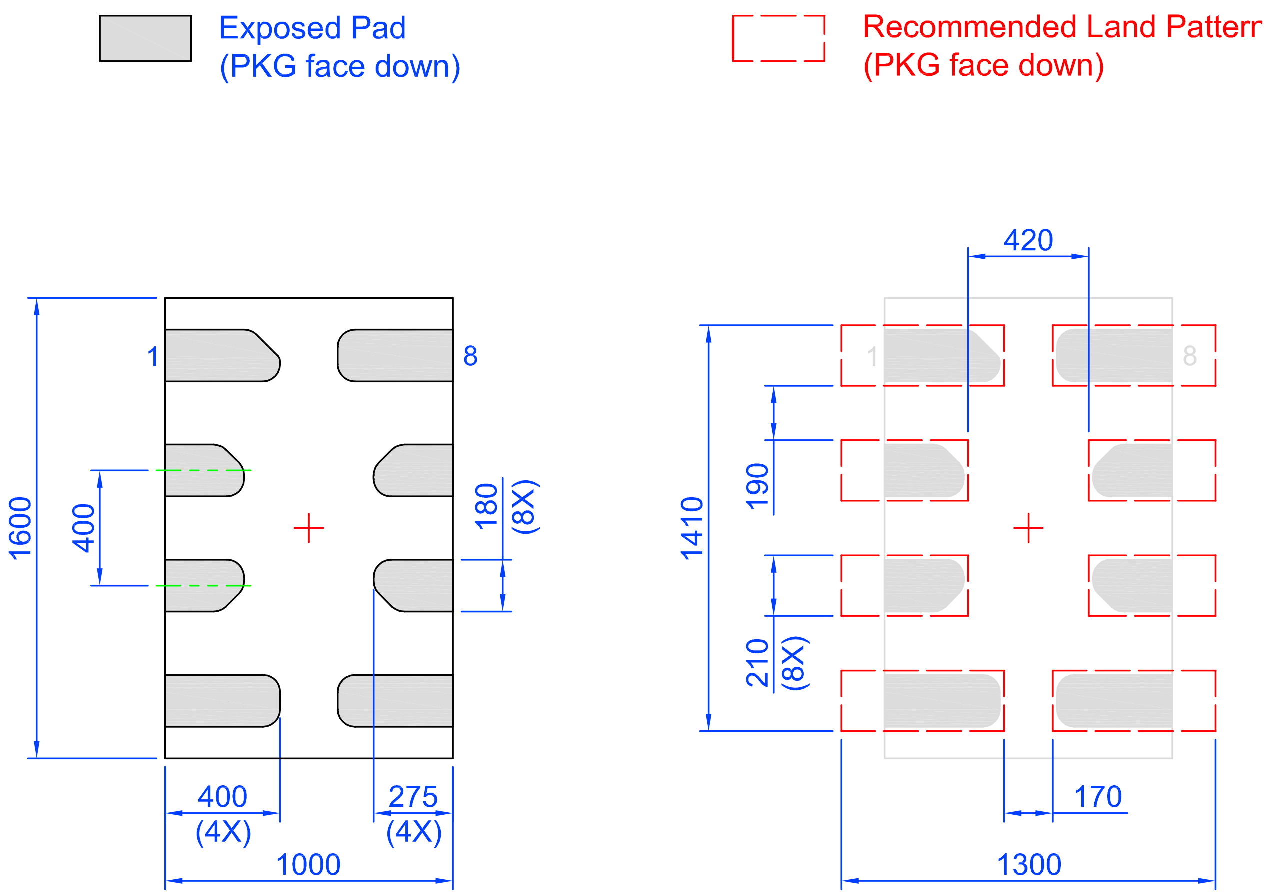
V_{OUT}= Output voltage, or $R_{LOAD} \times I_{OUT}$

Power Dissipation Derating Curve



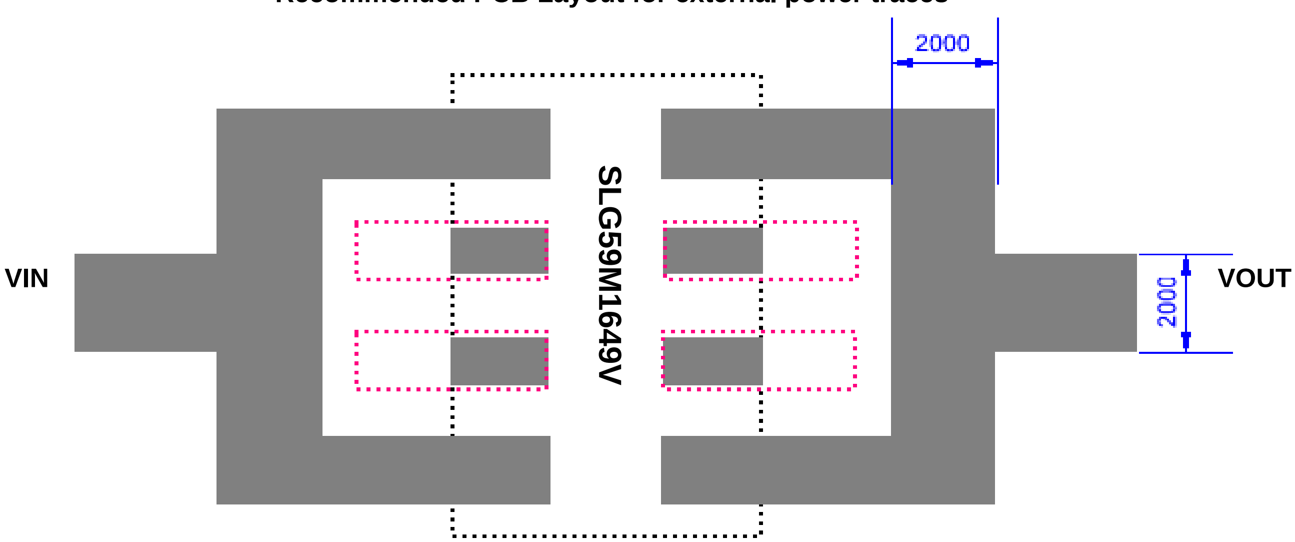
Note: Each V_{IN}, V_{OUT} = 1 in^2 1.2 oz. copper on FR4

SLG59M1649V Layout Suggestion



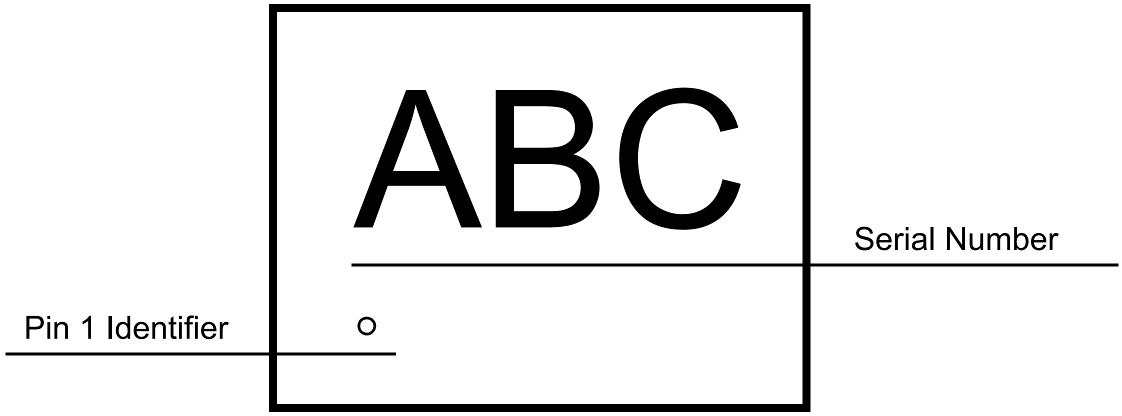
Note: All dimensions shown in micrometers (µm)

Recommended PCB Layout for external power traces



Note: All dimensions shown in µm (micrometers)

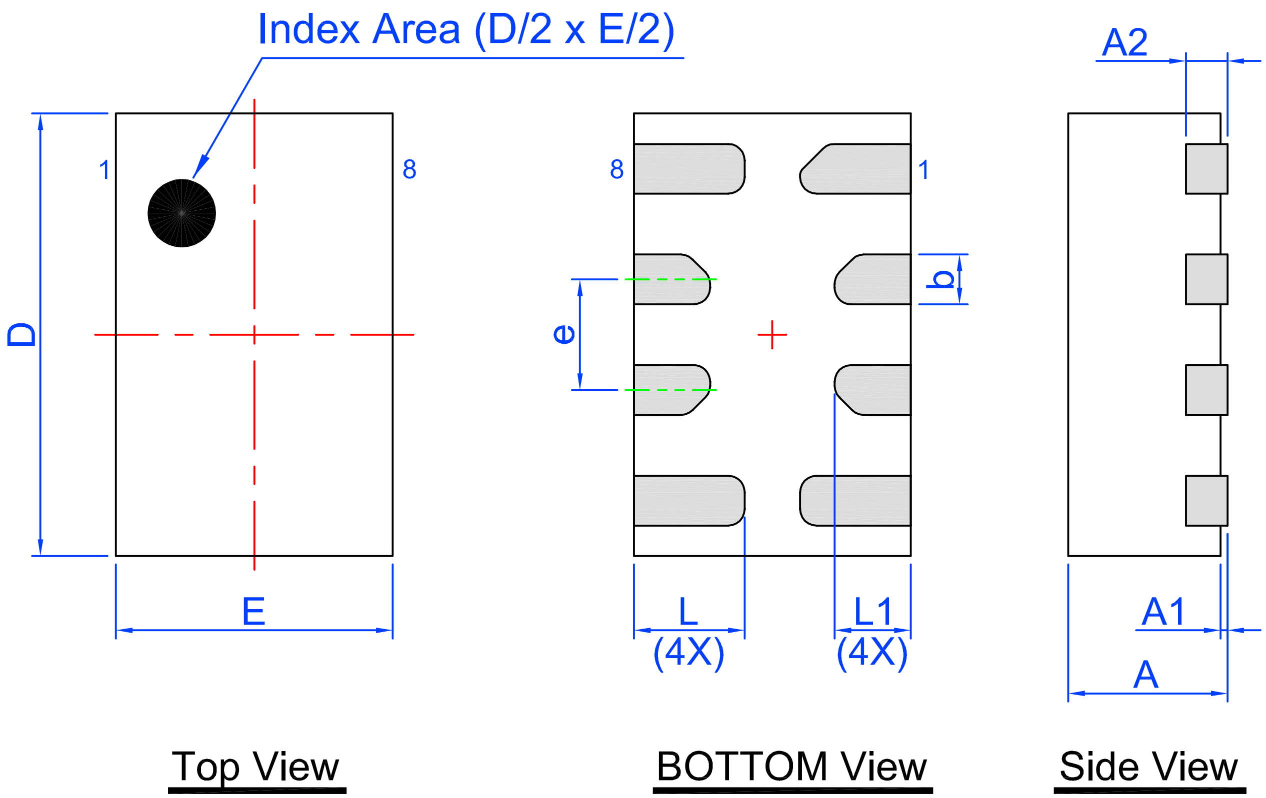
Package Top Marking System Definition



ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

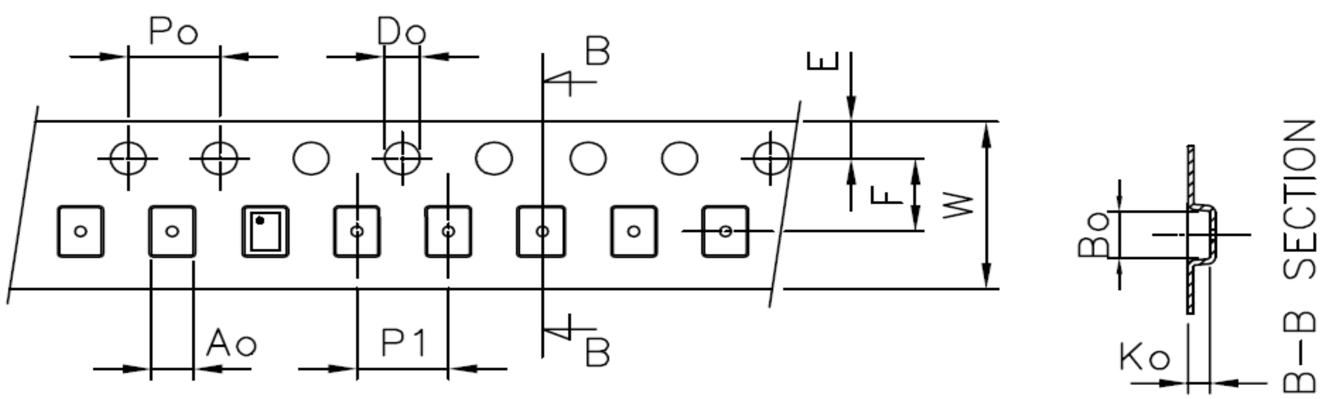
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.225	0.275	0.325
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FCD Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FCD Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/22/2016	0.52	Updated Electrical Characteristics Added Charts
2/17/2016	0.51	Updated POD and Landing Pattern
02/9/2016	0.50	Preliminary Release