

FEATURES

- Window monitoring with minimum processor I/O
- Individually monitoring N rails with only N + 1 processor I/O
- 400 mV, $\pm 0.275\%$ threshold at $V_{DD} = 3.3\text{ V}$, 25°C
- Supply range: 1.7 V to 5.5 V
- Low quiescent current: 17 μA maximum at 125°C
- Input range includes ground
- Internal hysteresis: 9.2 mV typical
- Low input bias current: 2.5 nA maximum
- Open-drain outputs
- Power good indication output
- Designated over voltage indication output
- Low profile (1 mm), 6-lead TSOT package

APPLICATIONS

- Supply voltage monitoring
- Li-Ion monitoring
- Portable applications
- Handheld instruments

GENERAL DESCRIPTION

The ADCMP671 voltage monitor consists of two low power, high accuracy comparators and reference circuits. It operates on a supply voltage from 1.7 V to 5.5 V and draws 17 μA maximum, making it suitable for low power system monitoring and portable applications. The part is designed to monitor and report supply undervoltage and overvoltage fault. The low input bias current and voltage reference allows resistor adjustable UV and OV threshold down to 400 mV. The ADCMP671 has two open-drain outputs: the PWRGD output indicates that the supply is within the UV and OV window, and the $\overline{\text{OV}}$ output indicates that the supply is overvoltage. This output combination allows users to window monitor N supplies with an N + 1 processor input/output (I/O). Each output is guaranteed to sink greater than 5 mA over temperature.

The ADCMP671 is available in 6-lead TSOT package. The device operates over the -40°C to $+125^\circ\text{C}$ temperature range.

FUNCTIONAL BLOCK DIAGRAM

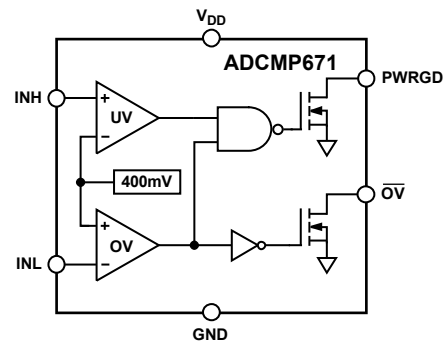


Figure 1.

10166-001

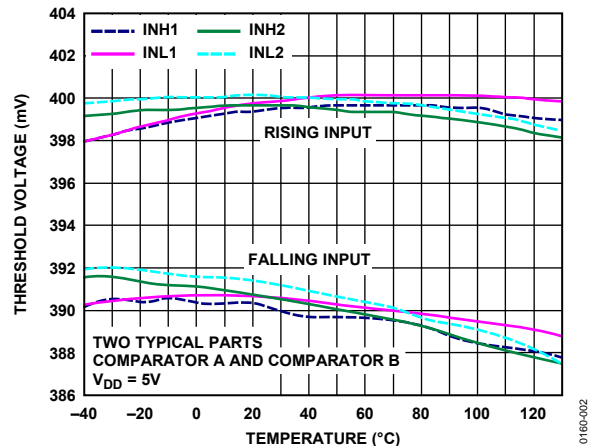


Figure 2. Comparator Thresholds vs. Temperature

10166-002

Rev. 0

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REVISION HISTORY

11/11—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 1.7\text{ V to }5.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage ($V_{TH(R)}$)	396.6	400.4	404.3	mV	$V_{DD} = 1.7\text{ V}$
	399.3	400.4	401.5	mV	$V_{DD} = 3.3\text{ V}$
	398.5	400.4	402.2	mV	$V_{DD} = 5.5\text{ V}$
Falling Input Threshold Voltage ($V_{TH(F)}$)	387	391	395.4	mV	$V_{DD} = 1.7\text{ V}$
	389.2	391	392.9	mV	$V_{DD} = 3.3\text{ V}$
	388.5	391	393.2	mV	$V_{DD} = 5.5\text{ V}$
Rising Input Threshold Voltage Accuracy			± 0.275	%	$V_{DD} = 3.3\text{ V}$
Falling Input Threshold Voltage Accuracy			± 0.475	%	$V_{DD} = 3.3\text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	7.8	9.2	11.1	mV	
INPUT CHARACTERISTICS					
Input Bias Current		0.01	1	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = V_{DD}$
		0.01	1	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = 0.1\text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²		140	200	mV	$V_{DD} = 1.7\text{ V}$, $I_{OUT} = 3\text{ mA}$
		130	200	mV	$V_{DD} = 5.5\text{ V}$, $I_{OUT} = 5\text{ mA}$
Output Leakage Current ³		0.01	0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = V_{DD}$
		0.01	0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = 5.5\text{ V}$
DYNAMIC PERFORMANCE^{2, 4}					
High-to-Low Propagation Delay		10		μs	$V_{DD} = 5.5\text{ V}$, $V_{OL} = 400\text{ mV}$
Low-to-High Propagation Delay		8		μs	$V_{DD} = 5.5\text{ V}$, $V_{OH} = 0.9 \times V_{DD}$
Output Rise Time		0.5		μs	$V_{DD} = 5.5\text{ V}$, $V_{OUT} = (0.1\text{ to }0.9) \times V_{DD}$
Output Fall Time		0.07		μs	$V_{DD} = 5.5\text{ V}$, $V_{OUT} = (0.1\text{ to }0.9) \times V_{DD}$
POWER SUPPLY					
Supply Current ⁵		5.7	10	μA	$V_{DD} = 1.7\text{ V}$
		6.5	11	μA	$V_{DD} = 5.5\text{ V}$

¹ $R_L = 100\text{ k}\Omega$, $V_{OUT} = 2\text{ V}$ swing.

² $V_{IN} = 10\text{ mV}$ input overdrive.

³ $V_{IN} = 40\text{ mV}$ overdrive.

⁴ $R_L = 10\text{ k}\Omega$.

⁵ No load current.

$V_{DD} = 1.7\text{ V to }5.5\text{ V}$, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage ($V_{TH(R)}$)	395.3		405.3	mV	$V_{DD} = 1.7\text{ V}$
	397.3		403.3	mV	$V_{DD} = 3.3\text{ V}$
	396.8		403.8	mV	$V_{DD} = 5.5\text{ V}$
Falling Input Threshold Voltage ($V_{TH(F)}$)	385.8		397.3	mV	$V_{DD} = 1.7\text{ V}$
	386.2		394.8	mV	$V_{DD} = 3.3\text{ V}$
	385.8		395.2	mV	$V_{DD} = 5.5\text{ V}$
Rising Input Threshold Voltage Accuracy			± 0.75	%	$V_{DD} = 3.3\text{ V}$
Falling Input Threshold Voltage Accuracy			± 1.1	%	$V_{DD} = 3.3\text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	6.8		12.2	mV	
INPUT CHARACTERISTICS					
Input Bias Current			1	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = V_{DD}$
			1	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = 0.1\text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7\text{ V}$, $I_{OUT} = 3\text{ mA}$
			250	mV	$V_{DD} = 5.5\text{ V}$, $I_{OUT} = 5\text{ mA}$
Output Leakage Current ³			0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = V_{DD}$
			0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = 5.5\text{ V}$
POWER SUPPLY					
Supply Current ⁴			13	μA	$V_{DD} = 1.7\text{ V}$
			14	μA	$V_{DD} = 5.5\text{ V}$

¹ $R_L = 100\text{ k}\Omega$, $V_{OUT} = 2\text{ V}$ swing.

² $V_{IN} = 10\text{ mV}$ input overdrive.

³ $V_{IN} = 40\text{ mV}$ overdrive.

⁴ No load.

$V_{DD} = 1.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage ($V_{TH(R)}$)	391.2		407.8	mV	$V_{DD} = 1.7\text{ V}$
	393.1		405.9	mV	$V_{DD} = 3.3\text{ V}$
	393.5		405.4	mV	$V_{DD} = 5.5\text{ V}$
Falling Input Threshold Voltage ($V_{TH(F)}$)	383.3		400.9	mV	$V_{DD} = 1.7\text{ V}$
	384.7		398.4	mV	$V_{DD} = 3.3\text{ V}$
	384.4		398.2	mV	$V_{DD} = 5.5\text{ V}$
Rising Input Threshold Voltage Accuracy			± 1.6	%	$V_{DD} = 3.3\text{ V}$
Falling Input Threshold Voltage Accuracy			± 1.75	%	$V_{DD} = 3.3\text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	5.4		12.6	mV	
INPUT CHARACTERISTICS					
Input Bias Current			1	nA	$V_{DD} = 1.7\text{ V}, V_{IN} = V_{DD}$
			1	nA	$V_{DD} = 1.7\text{ V}, V_{IN} = 0.1\text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7\text{ V}, I_{OUT} = 3\text{ mA}$
			250	mV	$V_{DD} = 5.5\text{ V}, I_{OUT} = 5\text{ mA}$
Output Leakage Current ³			0.1	μA	$V_{DD} = 1.7\text{ V}, V_{OUT} = V_{DD}$
			0.1	μA	$V_{DD} = 1.7\text{ V}, V_{OUT} = 5.5\text{ V}$
POWER SUPPLY					
Supply Current ⁴			14	μA	$V_{DD} = 1.7\text{ V}$
			15	μA	$V_{DD} = 5.5\text{ V}$

¹ $R_L = 100\text{ k}\Omega$, $V_{OUT} = 2\text{ V}$ swing.

² $V_{IN} = 10\text{ mV}$ input overdrive.

³ $V_{IN} = 40\text{ mV}$ overdrive.

⁴ No load.

$V_{DD} = 1.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage ($V_{TH(R)}$)	391.2		407.8	mV	$V_{DD} = 1.7\text{ V}$
	393.1		405.9	mV	$V_{DD} = 3.3\text{ V}$
	393.1		405.8	mV	$V_{DD} = 5.5\text{ V}$
Falling Input Threshold Voltage ($V_{TH(F)}$)	381.1		400.9	mV	$V_{DD} = 1.7\text{ V}$
	381.2		398.4	mV	$V_{DD} = 3.3\text{ V}$
	381		398.2	mV	$V_{DD} = 5.5\text{ V}$
Rising Input Threshold Voltage Accuracy			±1.6	%	$V_{DD} = 3.3\text{ V}$
Falling Input Threshold Voltage Accuracy			±2.2	%	$V_{DD} = 3.3\text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	5.4		13.5	mV	
INPUT CHARACTERISTICS					
Input Bias Current			2.5	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = V_{DD}$
			2.5	nA	$V_{DD} = 1.7\text{ V}$, $V_{IN} = 0.1\text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7\text{ V}$, $I_{OUT} = 3\text{ mA}$
			250	mV	$V_{DD} = 5.5\text{ V}$, $I_{OUT} = 5\text{ mA}$
Output Leakage Current ³			0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = V_{DD}$
			0.1	μA	$V_{DD} = 1.7\text{ V}$, $V_{OUT} = 5.5\text{ V}$
POWER SUPPLY					
Supply Current ⁴			16	μA	$V_{DD} = 1.7\text{ V}$
			17	μA	$V_{DD} = 5.5\text{ V}$

¹ $R_L = 100\text{ k}\Omega$, $V_{OUT} = 2\text{ V}$ swing.

² $V_{IN} = 10\text{ mV}$ input overdrive.

³ $V_{IN} = 40\text{ mV}$ overdrive.

⁴ No load.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V _{DD}	−0.3 V to +6 V
INH, INL	−0.3 V to +6 V
$\overline{\text{OV}}$, PWRGD	−0.3 V to +6 V
Output Short-Circuit Duration ¹	Indefinite
Input Current	−10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

¹ When the output is shorted indefinitely, the use of a heat sink may be required to keep the junction temperature within the absolute maximum ratings.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead TSOT	200	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

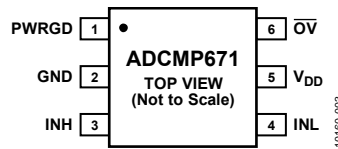


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PWRGD	Open-Drain Active High Power Good Output. It asserts when the input falls within the UV and OV window, for example, INH high and INL low.
2	GND	Ground.
3	INH	Monitors for Supply Undervoltage Fault Through an External Resistor Divider Network. It is internally connected to the noninverting input of a comparator. The other input of the comparator is connected to a 400 mV reference.
4	INL	Monitors for Supply Overvoltage Fault Through an External Resistor Divider Network. It is internally connected to the inverting input of a comparator. The other input of the comparator is connected to a 400 mV reference.
5	V _{DD}	Power Supply Pin.
6	OV	Open-Drain Output Active Low Overvoltage Fault Indication Output. It asserts when there is an overvoltage fault, for example, INL high.

TYPICAL PERFORMANCE CHARACTERISTICS

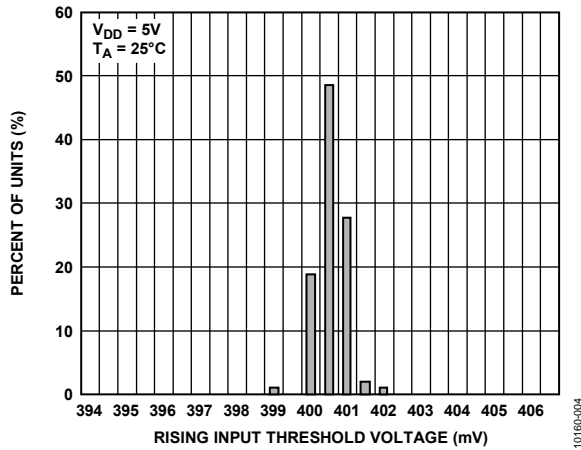


Figure 4. Distribution of Rising Input Threshold Voltage

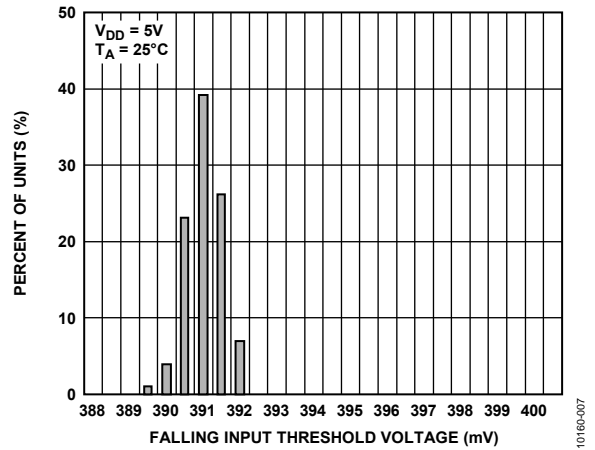


Figure 7. Distribution of Falling Input Threshold Voltage

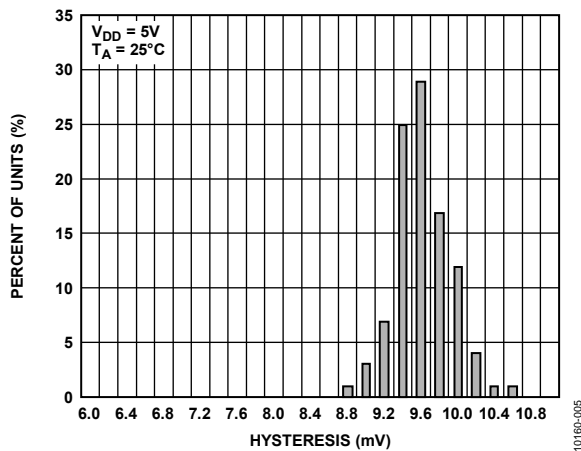


Figure 5. Distribution of Hysteresis

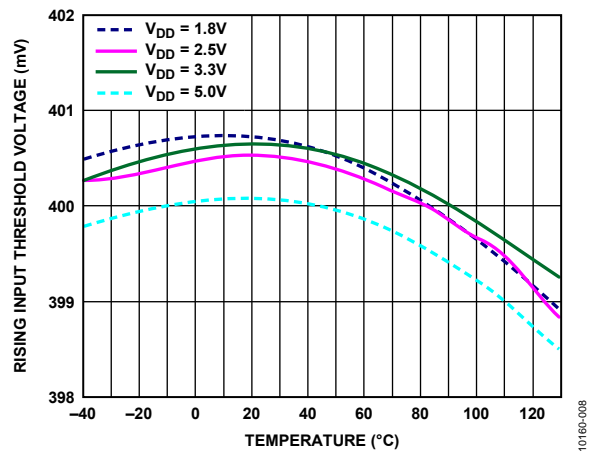


Figure 8. Rising Input Threshold Voltage vs. Temperature for Various V_{DD} Voltages

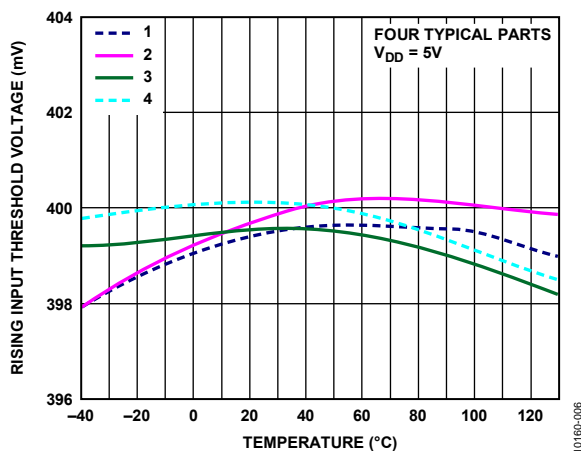


Figure 6. Rising Input Threshold Voltage vs. Temperature for Four Typical Parts

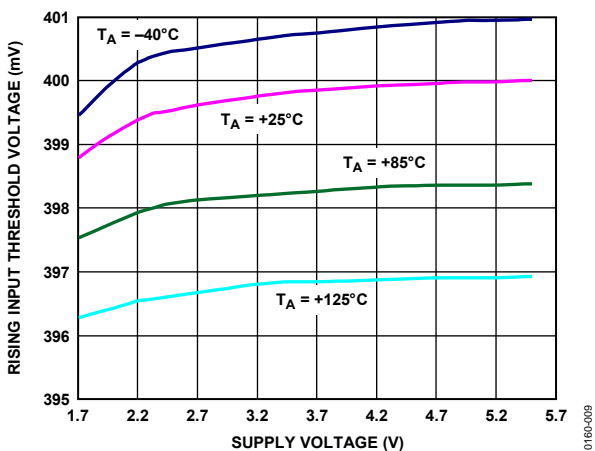


Figure 9. Rising Input Threshold Voltage vs. Supply Voltage

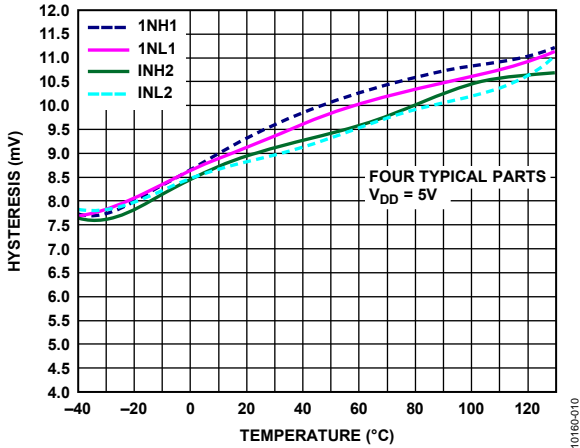


Figure 10. Hysteresis vs. Temperature for Four Typical Parts

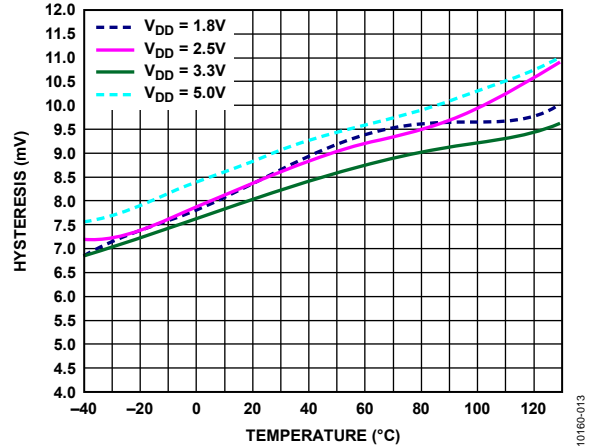


Figure 13. Hysteresis vs. Temperature for Various V_{DD} Voltages

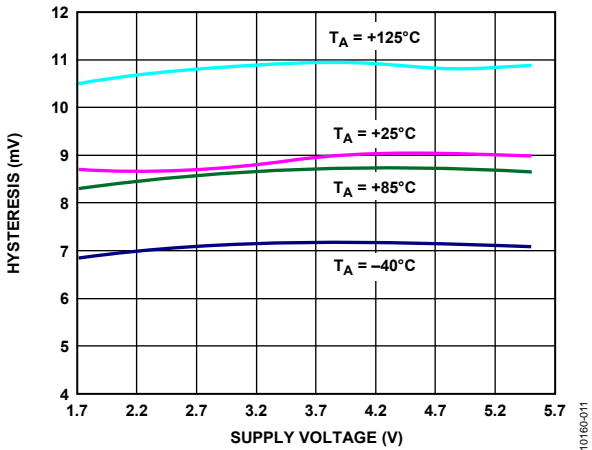


Figure 11. Hysteresis vs. Supply Voltage

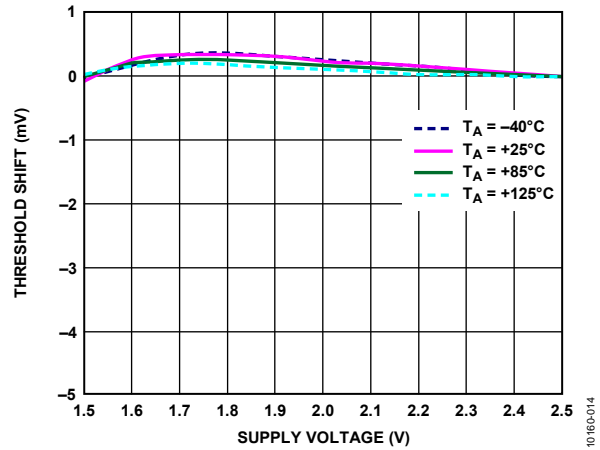


Figure 14. Minimum Supply Voltage

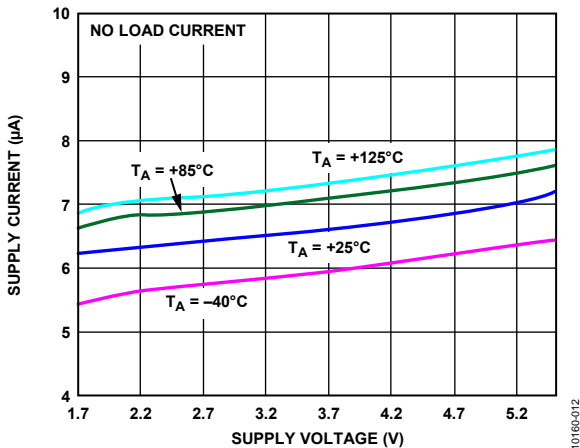


Figure 12. Quiescent Supply Current vs. Supply Voltage

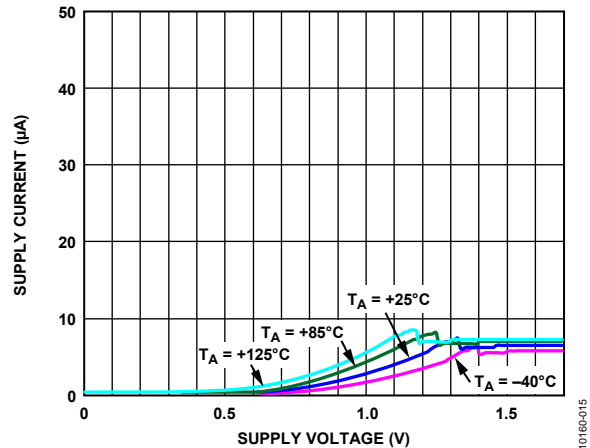


Figure 15. Start-Up Supply Current

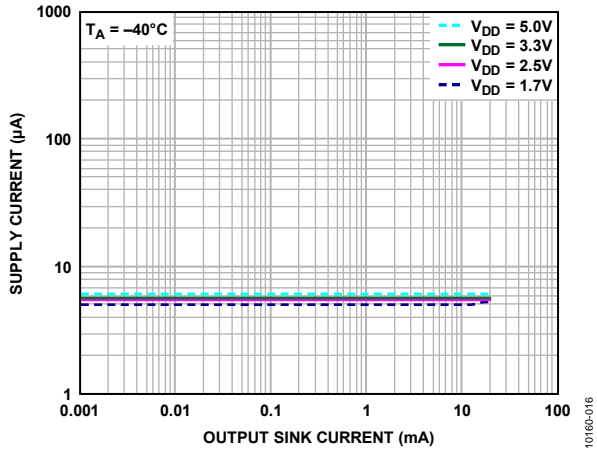


Figure 16. Supply Current vs. Output Sink Current for $T_A = -40^\circ\text{C}$

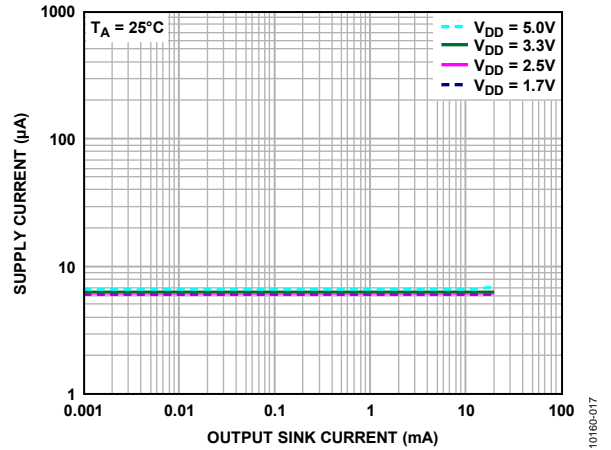


Figure 19. Supply Current vs. Output Sink Current for $T_A = 25^\circ\text{C}$

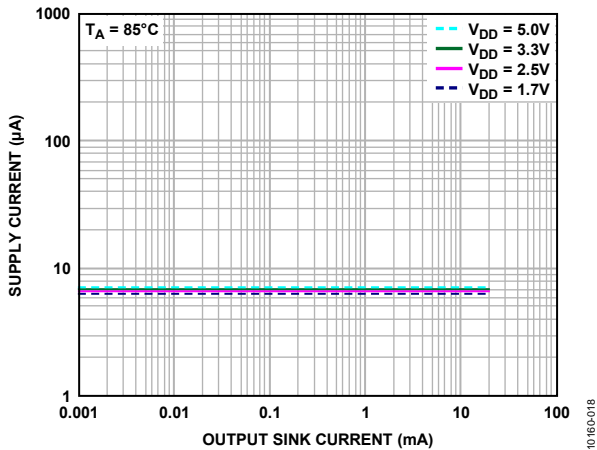


Figure 17. Supply Current vs. Output Sink Current for $T_A = 85^\circ\text{C}$

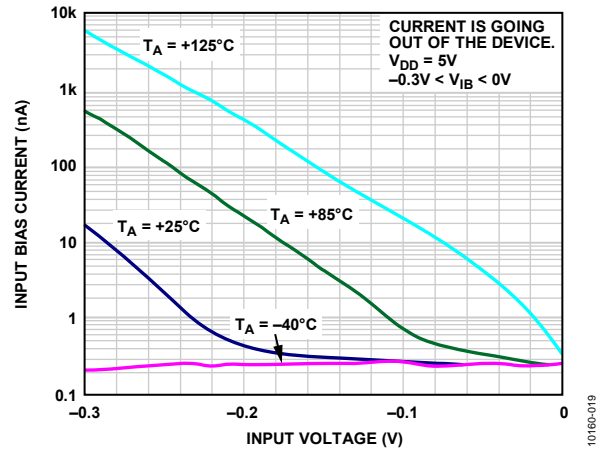


Figure 20. Below Ground Input Bias Current vs. Input Voltage

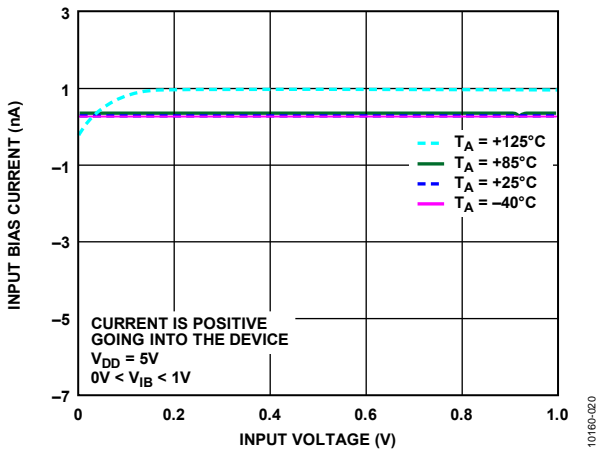


Figure 18. Low Level Input Bias Current vs. Input Voltage

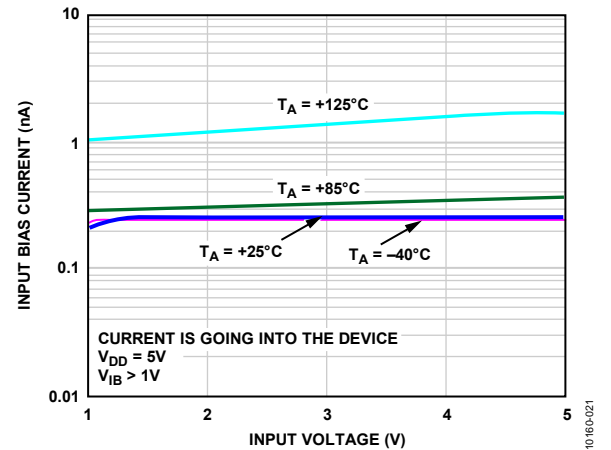


Figure 21. High Level Input Bias Current vs. Input Voltage

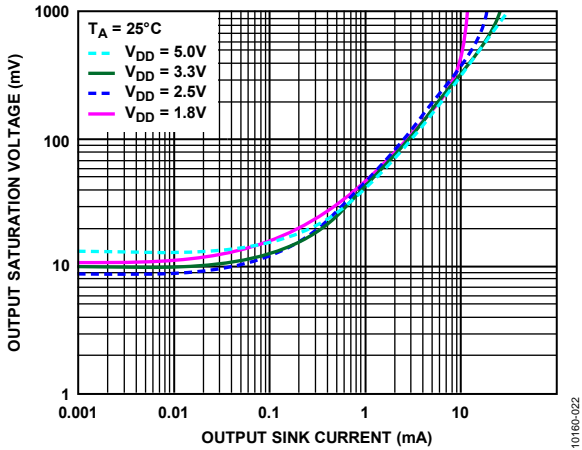


Figure 22. Output Saturation Voltage vs. Output Sink Current for $T_A = 25^\circ\text{C}$

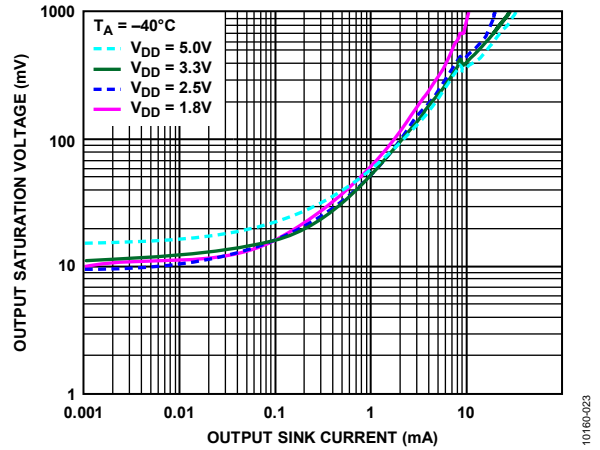


Figure 25. Output Saturation Voltage vs. Output Sink Current for $T_A = -40^\circ\text{C}$

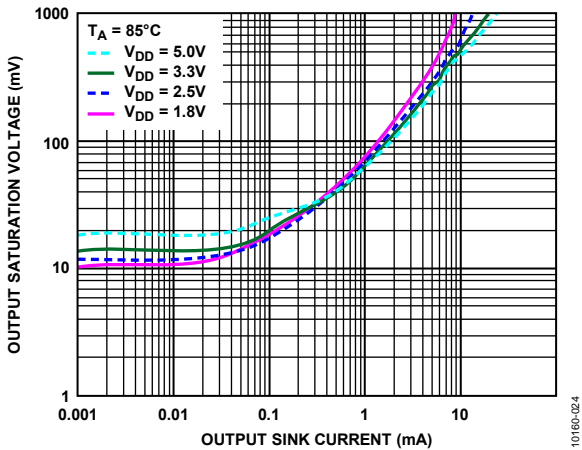


Figure 23. Output Saturation Voltage vs. Output Sink Current for $T_A = 85^\circ\text{C}$

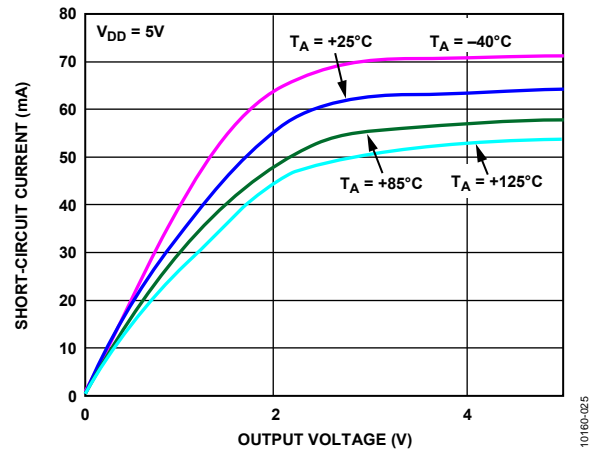


Figure 26. Output Short-Circuit Current vs. Output Voltage

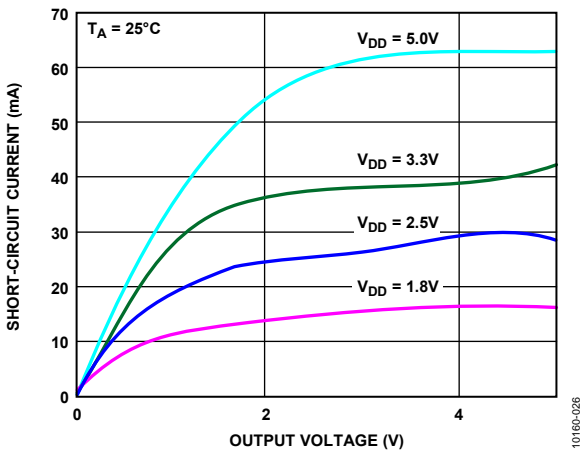


Figure 24. Output Short-Circuit Current vs. Output Voltage

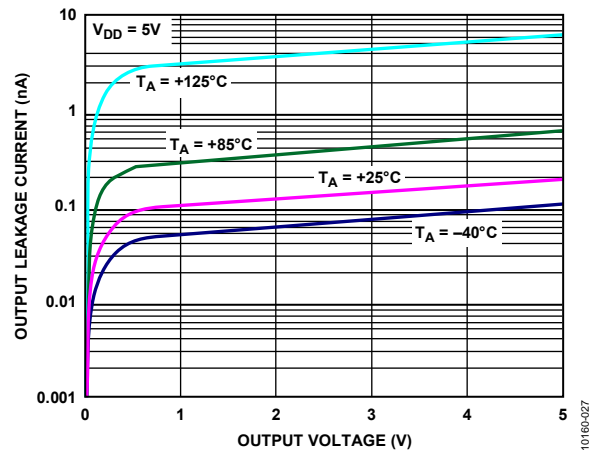


Figure 27. Output Leakage Current vs. Output Voltage

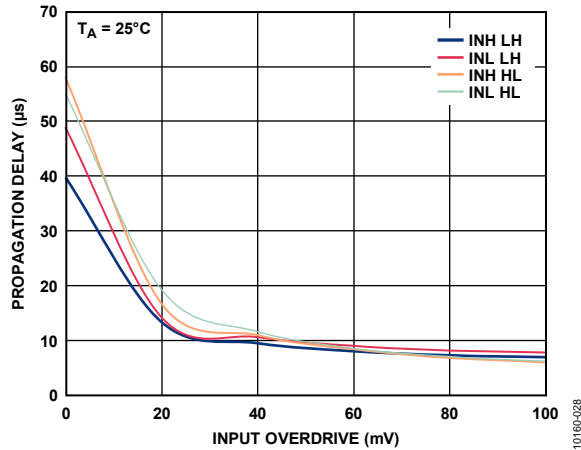


Figure 28. Propagation Delay vs. Input Overdrive

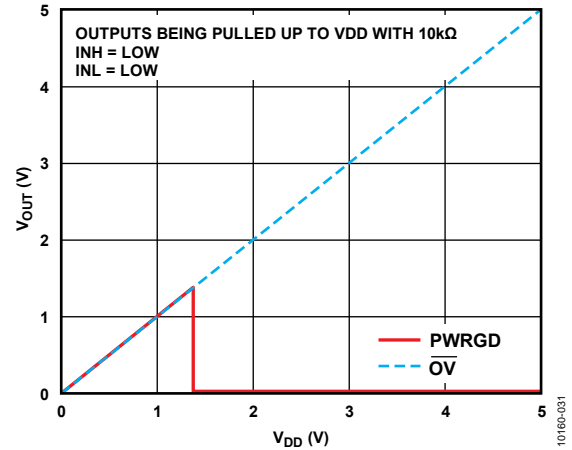


Figure 31. Output Voltage vs. Supply Voltage with Both INH and INL Low

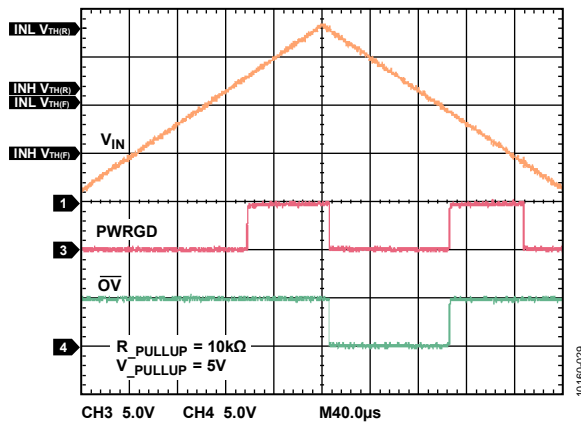


Figure 29. Propagation Delay

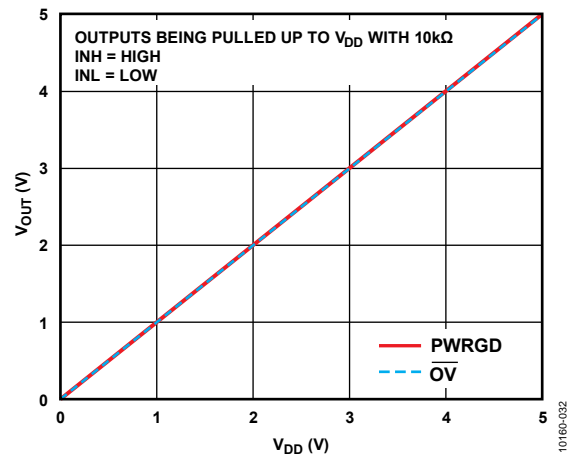


Figure 32. Output Voltage vs. Supply Voltage with INH High and INL Low

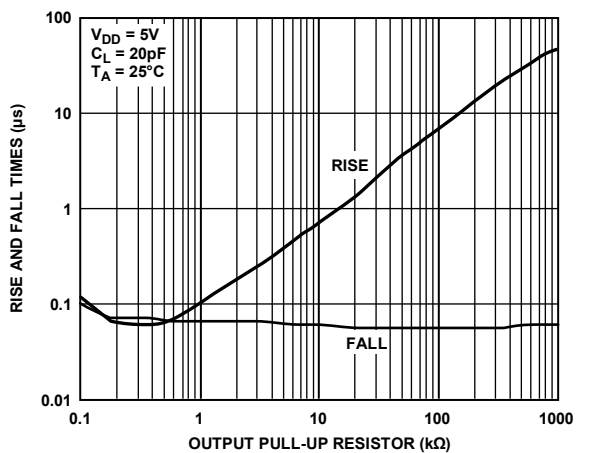


Figure 30. Rise and Fall Times vs. Output Pull-Up Resistor

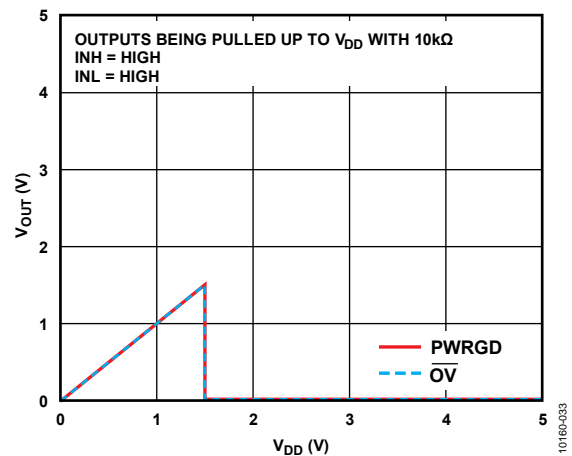


Figure 33. Output Voltage vs. Supply Voltage with Both INH and INL High

APPLICATIONS INFORMATION

The [ADCMP671](#) is a UV and OV monitor with a built-in 400 mV reference that operates from 1.7 V to 5.5 V. The comparator is 0.275% accurate with a built-in hysteresis of 9.2 mV. The outputs are open-drain, capable of sinking 40 mA.

COMPARATORS AND INTERNAL REFERENCE

There are two comparators inside the [ADCMP671](#). The comparator with its noninverting input connected to the INH pin (and its inverting input connected internally to the 400 mV reference) is for undervoltage detection, and the comparator with its inverting input available through the INL pin (and its noninverting input connected internally to the 400 mV reference) is for overvoltage detection. The rising input threshold voltage of the comparators is designed to be equal to that of the reference.

POWER SUPPLY

The [ADCMP671](#) is designed to operate from 1.7 V to 5.5 V. A 0.1 μ F decoupling capacitor is recommended between V_{DD} and GND.

INPUTS

The comparator inputs are limited to the maximum V_{DD} voltage range. The voltage on these inputs can be more than V_{DD} but never more than the maximum allowed V_{DD} voltage. When adding a resistor string to the input, choose resistor values carefully because the input bias current is in parallel with the bottom resistor of the string. Therefore, choose the bottom resistor first to control the error introduced by the bias current.

To minimize the number of external components use three resistor dividers to program the UV and OV thresholds.

HYSTERESIS

To prevent oscillations at the output caused by noise or slowly moving signals passing the switching threshold, each comparator has a built-in hysteresis of approximately 8.9 mV.

VOLTAGE MONITORING SCHEME

When monitoring a supply rail, the desired nominal operating voltage for monitoring is denoted by V_M , I_M is the nominal current through the resistor divider, V_{OV} is the overvoltage trip point, and V_{UV} is the undervoltage trip point.

Figure 34 illustrates the voltage monitoring input connection. Three external resistors, R_X , R_Y , and R_Z , divide the positive voltage for monitoring (V_M) into the high-side voltage (V_H) and low-side voltage (V_L). The high-side voltage is connected to the INH pin, and the low-side voltage is connected to the INL pin.

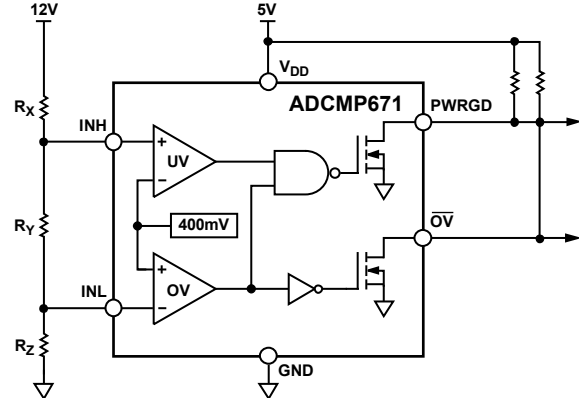


Figure 34. Undervoltage/Overvoltage Monitoring Configuration

To trigger an overvoltage condition, the low-side voltage (in this case, V_L) must exceed the 0.4 V threshold on the INL pin. The low-side voltage, V_L , is given by the following equation:

$$V_L = V_{OV} \left(\frac{R_Z}{R_X + R_Y + R_Z} \right) = 0.4 \text{ V}$$

Also,

$$R_X + R_Y + R_Z = \frac{V_M}{I_M}$$

Therefore, R_Z , which sets the desired trip point for the overvoltage monitor, is calculated using the following equation:

$$R_Z = \frac{(0.4)(V_M)}{(V_{OV})(I_M)}$$

To trigger the undervoltage condition, the high-side voltage, V_H , must fall below the 0.4 V threshold on the INH pin. The high-side voltage, V_H , is given by the following equation:

$$V_H = V_{UV} \left(\frac{R_Y + R_Z}{R_X + R_Y + R_Z} \right) = 0.4 \text{ V}$$

Because R_Z is already known, R_Y can be expressed as follows:

$$R_Y = \frac{(0.4)(V_M)}{(V_{UV})(I_M)} - R_Z$$

When R_Y and R_Z are known, R_X is calculated using the following equation:

$$R_X = \frac{(V_M)}{(I_M)} - R_Z - R_Y$$

If V_M , I_M , V_{OV} , or V_{UV} changes each step must be recalculated.

OUTPUTS

The PWRGD output is used to indicate supply power good for the rail being monitored. It asserts if the monitored voltage falls within the UV and OV threshold window. The \overline{OV} output acts as a dedicated overvoltage indication output, allows the board manager to take decisive action to protect the system from overvoltage faults. Both outputs are open-drain and can be pulled up to voltages above V_{DD} . These outputs are capable of sinking current up to 40 mA.

In the multisupply monitoring application, multiple ADCMP671 can be used with their \overline{OV} pin tied together to generate a single overvoltage fault alert signal, as shown in Figure 35. During power up and power down, the power management processor of the board can manage supply sequencing based on PWRGD signals. In the event of supply overvoltage fault, the processor can react quickly to the provide necessary circuit protection because of its dedicated \overline{OV} alert. The processor is also able to identify the faulty supply from combining the information on the PWRGD pins. This allows the processor to use the $N + 1$ input pins to individually monitor N channels of supplies.

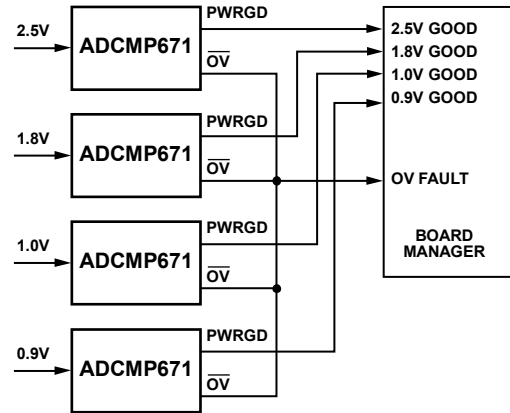
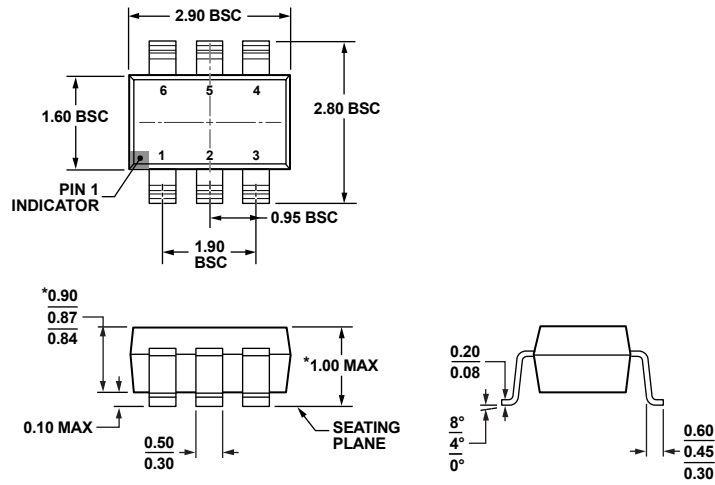


Figure 35. N Rails Monitoring with N + 1 Processor I/O

1016P-035

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-AA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 36. 6-Lead Thin Small Outline Transistor Package [TSOT] (UJ-6)

Dimensions shown in millimeters

102808-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADCMP671-1YUJZ-RL7	-40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	LLS

¹ Z = RoHS Compliant Part.