

**SERIES:** AMT20 | **DESCRIPTION:** MODULAR ENCODER

**FEATURES**

- 12 bit (4,096 positions)
- SPI communication
- small size 37mm
- incremental line count up to 1,024
- single pulse index
- capacitive ASIC technology
- modular locking hub design for ease of installation
- SPI adjustable settings
- 'One Touch' zero position


**ELECTRICAL**

parameter	conditions/description	min	typ	max	units
power supply		4.5	5	5.5	V
current consumption	with unloaded outputs		8	10	mA
quadrature resolution	96, 192, 200, 250, 400, 500, 512, 1024				PPR
incremental output signals	quadrature A, B signals and index Z				
incremental output waveform	TTL voltage square wave				
output current	sink/source			2	mA
SPI output	natural binary				
SPI bus	PIC 16F690 (see datasheet)				
SPI resolution				12	bit
position accuracy				0.2	deg

1. All resolutions stated are before quadrature decoding. (example: 1000 ppr x 4 = 4000 counts)

**MECHANICAL**

parameter	conditions/description	min	typ	max	units
max. rotational speed				8,000	RPM
mounting options	A) 2 each M1.6 on 16 mm (0.63") bolt circle B) 2 each #4 on 19.05 mm (0.75") bolt circle C) 2 each M1.6 or M2 on 20 mm (0.787") bolt circle D) 3 each M1.6 or M2 on 20.9 mm (0.823") bolt circle with washers in option B holes E) 3 each M1.6 or M2 on 22 mm (0.866") bolt circle F) 4 each M1.6 or M2 on 25.4 mm (1") bolt circle				

**ENVIRONMENTAL**

parameter	conditions/description	min	typ	max	units
operating temperature		-40		125	°C
humidity	non-condensing			85	%
vibration	10 ~ 500 Hz, 5 min sweep, 2 hour each XYZ			5	G
shock	3 pulses, 6 ms, 3 each XYZ			200	G










## PART NUMBER KEY

The AMT203 is designed for 12 bit binary (4,096) operation. For customers who may use the optional quadrature output, one of the resolutions below may be selected as the default quadrature output.



## AMT203-V KIT

In order to provide maximum flexibility for our customers, the AMT203 series is provided in kit form standard. This allows the user to implement the encoder into a range of applications using one sku#, reducing engineering and inventory costs.

SLEEVES								
								
8mm	1/4 inch (6.35mm)	6mm	5mm	3/16 inch (4.76mm)	4mm	1/8 inch (3.175mm)	3mm	2mm
Blue	Snow	Red1	Green1	Yellow1	Gray60	Purple1	Orange	Light Sky Blue



## ENCODER INTERFACE

### Standard Connector Option

### Locking Connector Option

PINOUT CONNECTOR 1	
#	FUNCTION
14	T_Bit
13	N/A
12	X
11	N/A
10	A
9	N/A
8	B
7	MOSI
6	5 V+
5	SCK
4	GND
3	MISO
2	CSB
1	N/A



Mating Connector:  
Samtec ISDF-07-D

DETAIL B  
SCALE 4 : 1

Mating Connector:  
Samtec ISDF-07-D-L

DETAIL B  
SCALE 4 : 1

### Encoder Side

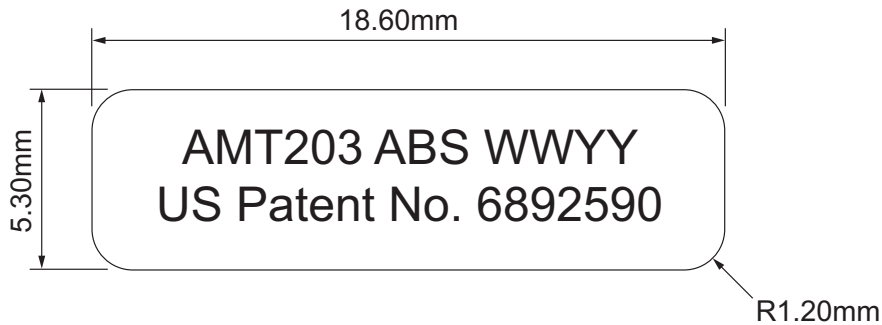
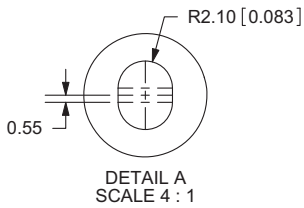
### Demo Board Side



**MECHANICAL DRAWING**



TOLERANCE:  
±0.05mm UNLESS OTHERWISE  
SPECIFIED



SCALE 5:1

## APPLICATION NOTES

### Encoder operational mode

- Initialization mode: At power up the encoder goes through an initiation and stabilization procedure. This includes microprocessor stabilization and the program for combining Coarse and Fine channel of the encoder for getting the absolute start position. This takes less than 0.1 seconds.
- Tracking mode: Only the Fine channel is active and the MCU internal position register is updated with data from Fine:
  - MCU 12 bit position register is updated from Fine every 48  $\mu$ s.
  - For accurate position update without above time delay, outputs for incremental A quad B or Count and Up/Dwn from the Fine channel are provided. These outputs are operational up to 8000 RPM and there is no speed error. There is an acceleration error dependent on an internal filter constant of about 100  $\mu$ s.
  - When using the incremental output there also is an Index output available, with one index pulse per turn.

## Serial Peripheral Interface Commands

The SPI or Serial Peripheral Interface Bus is a standard interface promoted by Motorola and Microchip among others. It consists of 4 signals:

- MOSI: Master Out Slave In
- MISO: Master In Slave Out
- SCK: Serial Clock
- CSB: Chip Select (active low)

## SPI BUS

The SPI bus runs full duplex and transfers multiples of 8 bits in a frame. The SPI type is the most common (CPOL=0, CPHA=0), also known as Microwire. Data is captured on the rising edge of SCK and the output data is changed after the falling edge of SCK.



### Terminology

MSB = most significant byte  
 LSB = least significant byte  
 msb = most significant bit  
 lsb = least significant bit

Serial Peripheral Interface Bus (SPI) on AMT203

Figure 7: SPI BUS Timing Diagram

The msb data out on MISO is valid soon after CSB goes low. The MOSI data is valid soon after the falling edge of SCK. The Encoder drives data out on MISO as long as CSB is low.

Normally, CSB goes low, then after 8 clocks the command is interpreted. CSB high resets the clock counter, and terminates any command sequence.

## SPI Commands:

The commands are all 8 bits long, the msb is shifted in first, and is the leftmost bit shown in Figure 7.

### Encoder Protocol Considerations:

The Encoder is designed to operate with a high speed SPI link, in full duplex mode. This implies the host can issue commands and read data as quickly as necessary but there has to be an acknowledgement from the slave just before the data is transferred.

Essentially the host issues a command, receives zero or more wait sequences (0xA5 or 1010,0101) then the echo of the command followed by an optional payload.

So, for example to read the position, the host issues rd\_pos (0x10 or 0001,0000), receiving a series of wait sequences (0xA5) then a reflected rd\_pos (0x10), then the MSB data followed by the LSB data.

It is recommended that the host leave a 20 us gap between reads to avoid extending the read time by forcing wait sequences.

### Command 0x00: nop\_a5

This command is ignored by the Encoder and simply causes the next data to be read. The encoder responds with 0xA5 if there is nothing else to send.

### Command 0x10: rd\_pos

This command causes a read of the current position.

The sequence is as follows:

- 1) issue read command, receive idle character
- 2) issue NOP, receive idle character 0xA5 or 0x10
- 3) repeat step 2 if it is 0xA5
- 4) issue NOP and receive MSB position (4 bits valid data)
- 5) issue NOP and receive LSB position (8 bits valid data)

Note that it is possible to overlap commands, so instead of NOP is several steps above the user could start another operation. The read and write FIFOs for the PCI streams are 16 bytes long and it is up to the user to avoid overflow.

### Command 0x70: set\_zero\_point

This command sets the current position to zero and saves this setting in the EEPROM. The host should send nop\_a5 repeatedly after sending this command, the response will be 0xa5 while update is proceeding and 0x80 is the response when update is finished.

## REVISION HISTORY

rev.	description	date
1.0	initial release	05/01/2010
1.01	updated pin-out	10/01/2010
1.02	updated application note	01/01/2011
1.03	updated SPI commands	09/16/2011
1.04	addition of shock and incremental output current data, correction of vibration data, updated part number key	09/30/2011
1.05	updated Part Number Key	03/09/2012
1.06	updated tools	07/13/2012
1.07	added locking connector drawing	02/12/2013
1.08	updated spec	12/09/2013

The revision history provided is for informational purposes only and is believed to be accurate.



**CUI INC**<sup>®</sup>

**Headquarters**  
20050 SW 112th Ave.  
Tualatin, OR 97062  
**800.275.4899**

Fax 503.612.2383  
**cui.com**  
techsupport@cui.com

CUI offers a one (1) year limited warranty. Complete warranty information is listed on our website.

CUI reserves the right to make changes to the product at any time without notice. Information provided by CUI is believed to be accurate and reliable. However, no responsibility is assumed by CUI for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

CUI products are not authorized or warranted for use as critical components in equipment that requires an extremely high level of reliability. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.