

N-channel 1050 V, 1 Ω typ., 6 A MDmesh™ K5

Power MOSFETs in TO-220, TO-220FP and TO-247 packages

Datasheet - production data

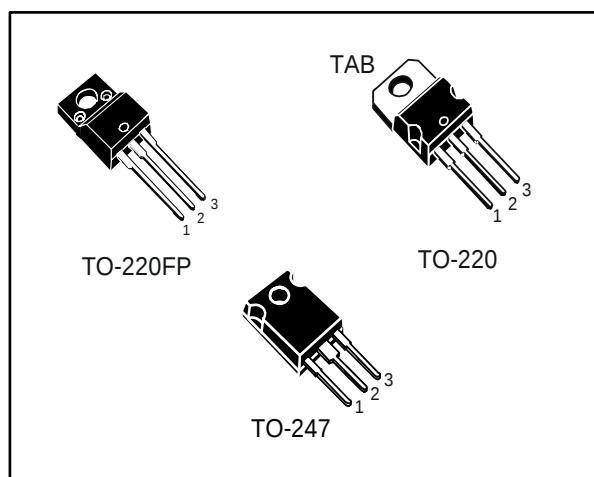
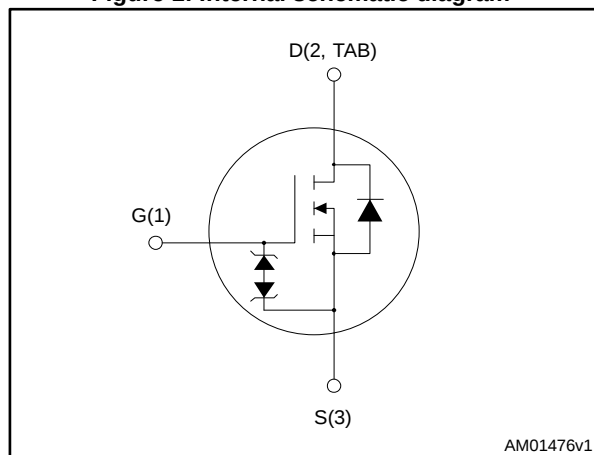


Figure 1: Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF10N105K5	1050 V	1.3 Ω	6 A	30 W
STP10N105K5				130 W
STW10N105K5				130 W

- Industry's lowest $R_{DS(on)}$
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STF10N105K5	10N105K5	TO-220FP	Tube
STP10N105K5	10N105K5	TO-220	Tube
STW10N105K5	10N105K5	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
V_{GS}	Gate- source voltage	30			V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	6			A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3.78			A
$I_{DM}^{(1)}$	Drain current (pulsed)	24			A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	130		30	W
I_{AR}	Max. current during repetitive or single pulse avalanche	2			A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	140			mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5			V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	2500			V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			$^{\circ}\text{C}$

Notes:⁽¹⁾ Pulse width limited by safe operating area.⁽²⁾ $I_{SD} \leq 6\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{peak} \leq V_{(BR)DSS}$.⁽³⁾ $V_{SD} \leq 840$.

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max.	0.96			$^{\circ}\text{C}/\text{W}$
	Thermal resistance junction-case max.			4.2	
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.50			$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	1050			V
I _{DSS}	Zero gate voltage, drain current (V _{GS} = 0)	V _{DS} = 1050 V			1	μA
		V _{DS} = 1050 V, T _C = 125 °C			50	μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 20 V; V _{DS} = 0			10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 3 A		1	1.3	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	545	-	pF
C _{oss}	Output capacitance			30		pF
C _{rss}	Reverse transfer capacitance			1.3		pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 840 V		65		pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related			22		pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain		7		Ω
Q _g	Total gate charge	V _{DD} = 840 V, I _D = 6 A V _{GS} = 10 V		21.5		nC
Q _{gs}	Gate-source charge			3.3		nC
Q _{gd}	Gate-drain charge			15.5		nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 525 V, I _D = 3 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	19	-	ns
t _r	Rise time			8		ns
t _{d(off)}	Turn-off-delay time			50		ns
t _f	Fall time			21.5		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		6	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				24	A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 6 A, V _{GS} = 0			1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 6 A, di/dt = 100 A/μs V _{DD} = 60 V		345		ns
Q _{rr}	Reverse recovery charge			3.53		μC
I _{RRM}	Reverse recovery current			20.5		A
t _{rr}	Reverse recovery time	I _{SD} = 6 A, di/dt = 100 A/μs V _{DD} = 60 V T _J = 150 °C		540		ns
Q _{rr}	Reverse recovery charge			5.05		μC
I _{RRM}	Reverse recovery current			18.5		A

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽²⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for TO-220

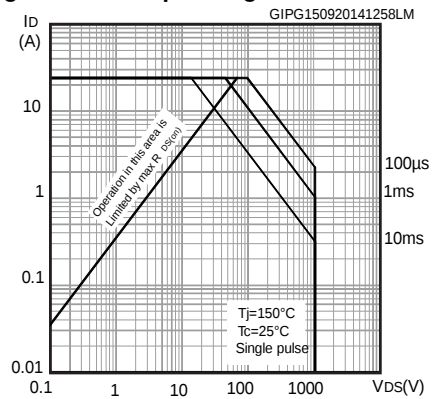


Figure 3: Thermal impedance TO-220

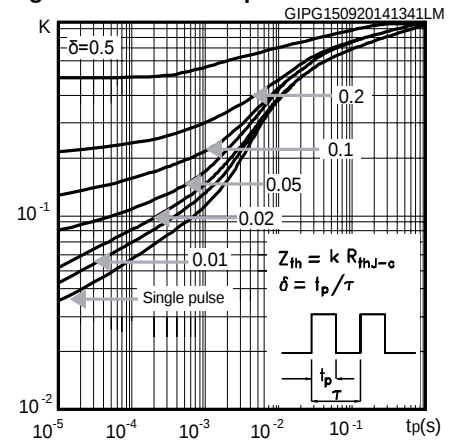


Figure 4: Safe operating area for TO-220FP

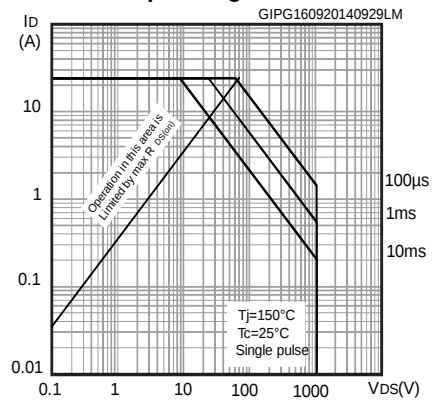


Figure 5: Thermal impedance TO-220FP

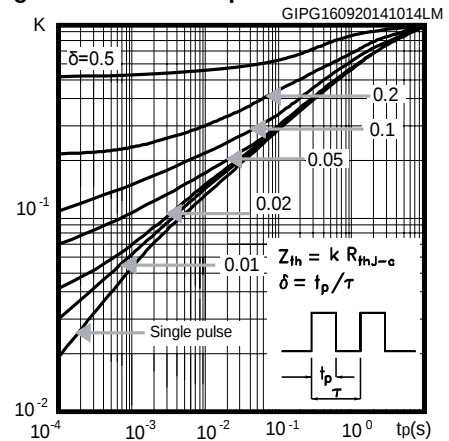


Figure 6: Safe operating area for TO-247

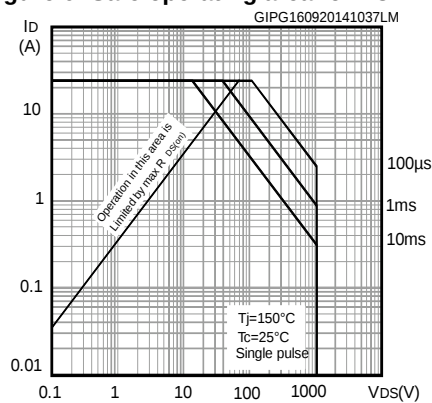


Figure 7: Thermal impedance TO-247

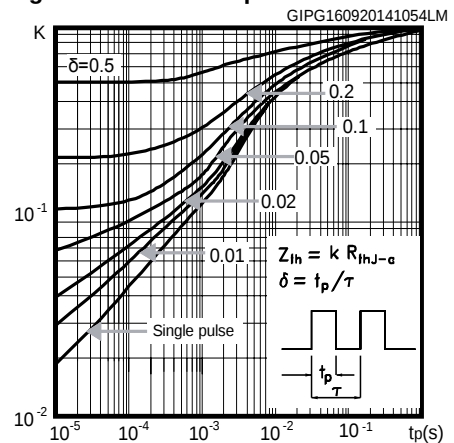


Figure 8: Output characteristics

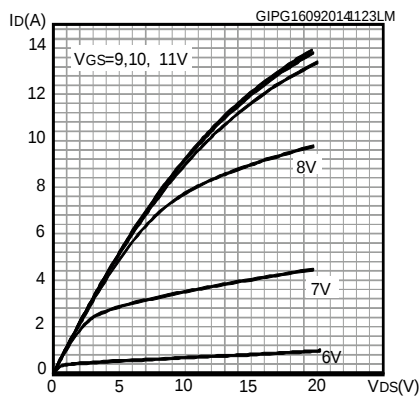


Figure 9: Transfer characteristics

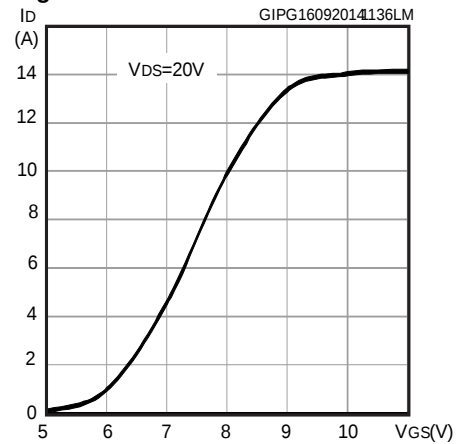


Figure 10: Gate charge vs gate-source voltage

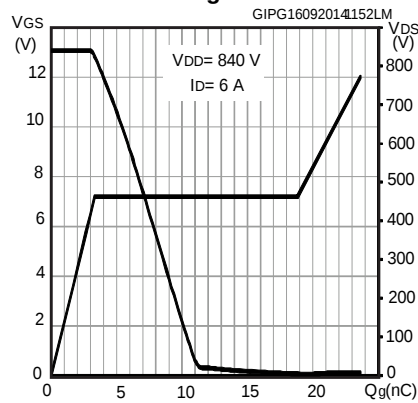


Figure 11: Static drain-source on-resistance

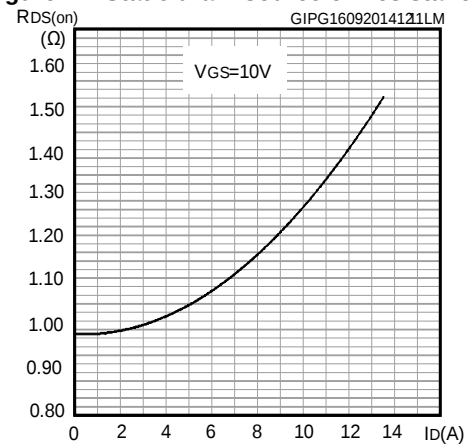


Figure 12: Capacitance variation

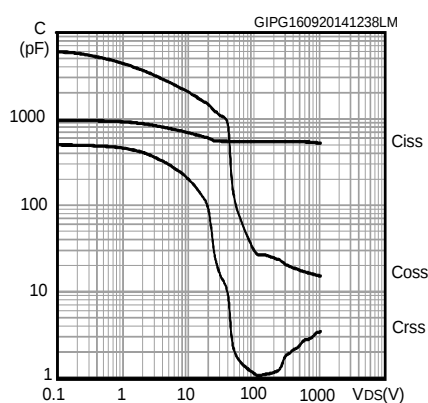


Figure 13: Normalized gate threshold voltage vs temperature

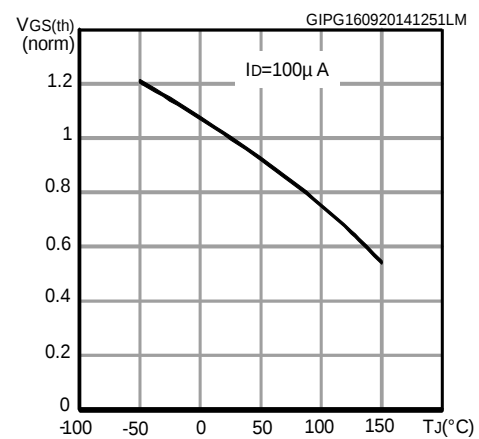
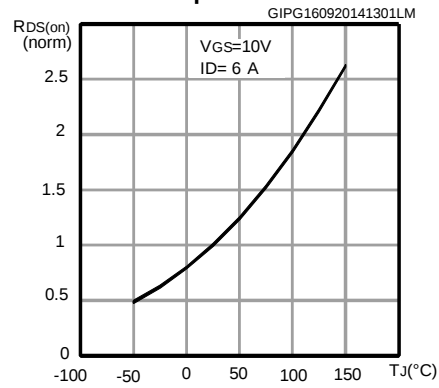
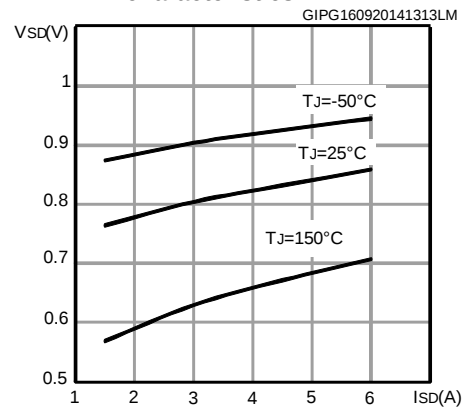
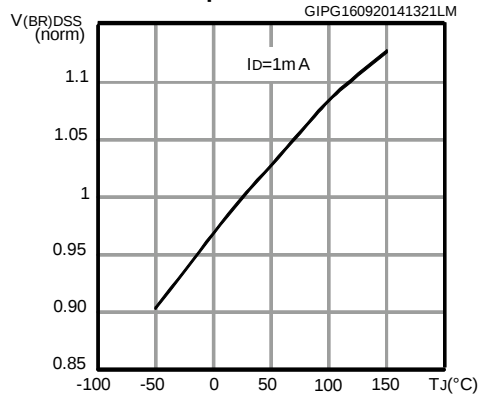
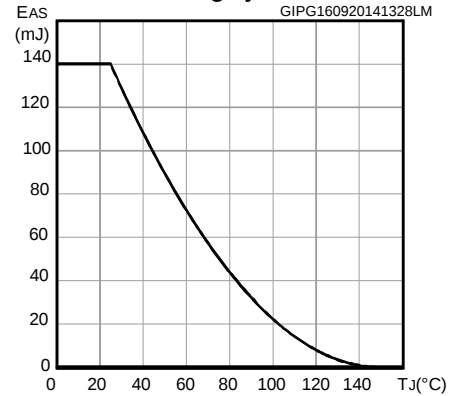


Figure 14: Normalized on-resistance vs temperature**Figure 15: Source-drain diode forward characteristics****Figure 16: Normalized VBR(DSS) vs temperature****Figure 17: Maximum avalanche energy vs starting T_J** 

3 Test circuits

Figure 18: Switching times test circuit for resistive load

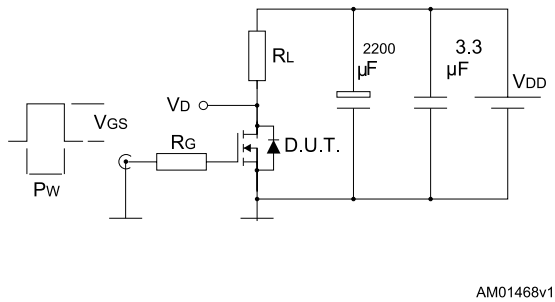


Figure 19: Gate charge test circuit

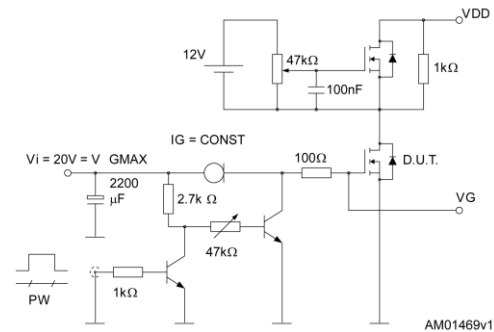


Figure 20: Test circuit for inductive load switching and diode recovery times

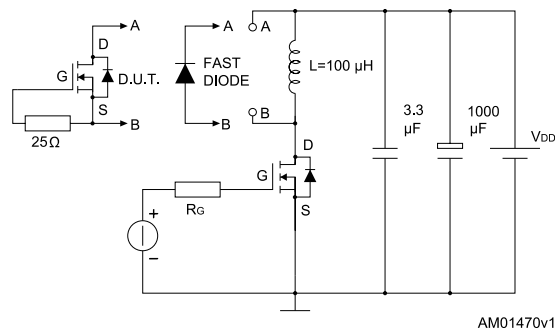


Figure 21: Unclamped inductive load test circuit

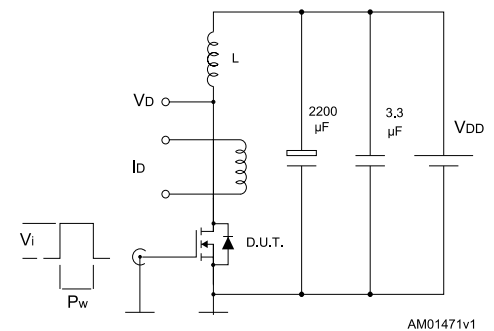


Figure 22: Unclamped inductive waveform

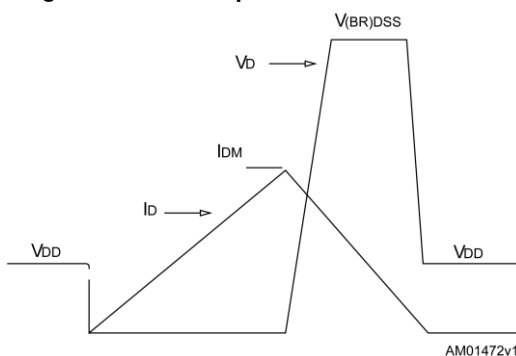
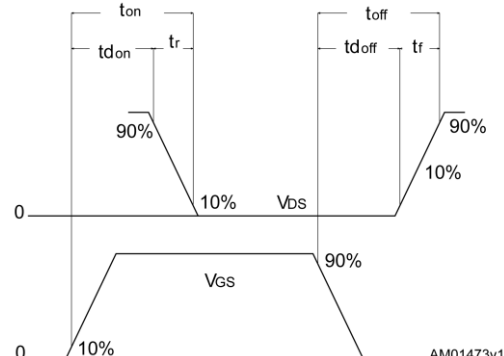


Figure 23: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 TO-220 package mechanical data

Figure 24: TO-220 type A drawings

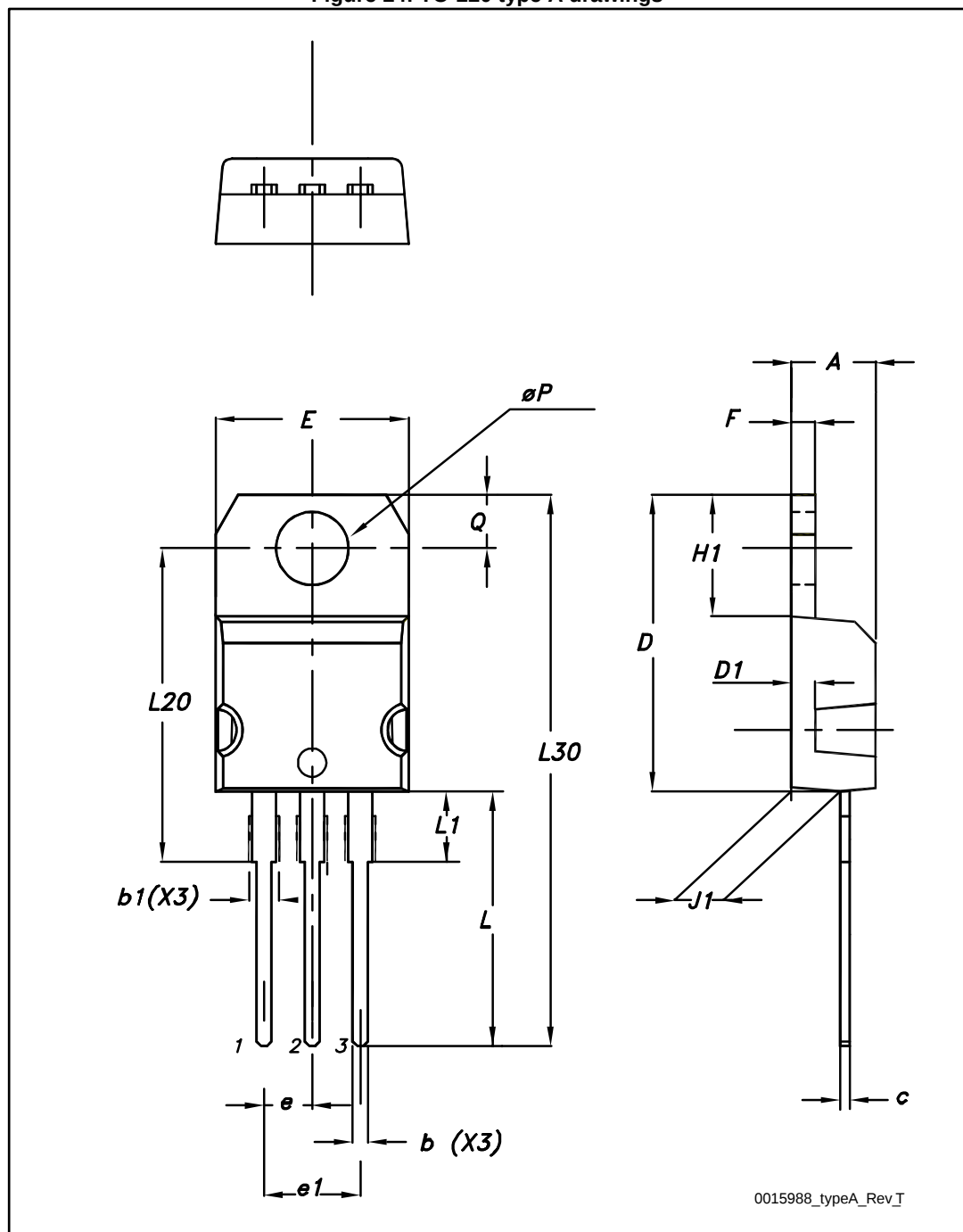


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 TO-247 package mechanical data

Figure 25: TO-247 drawings

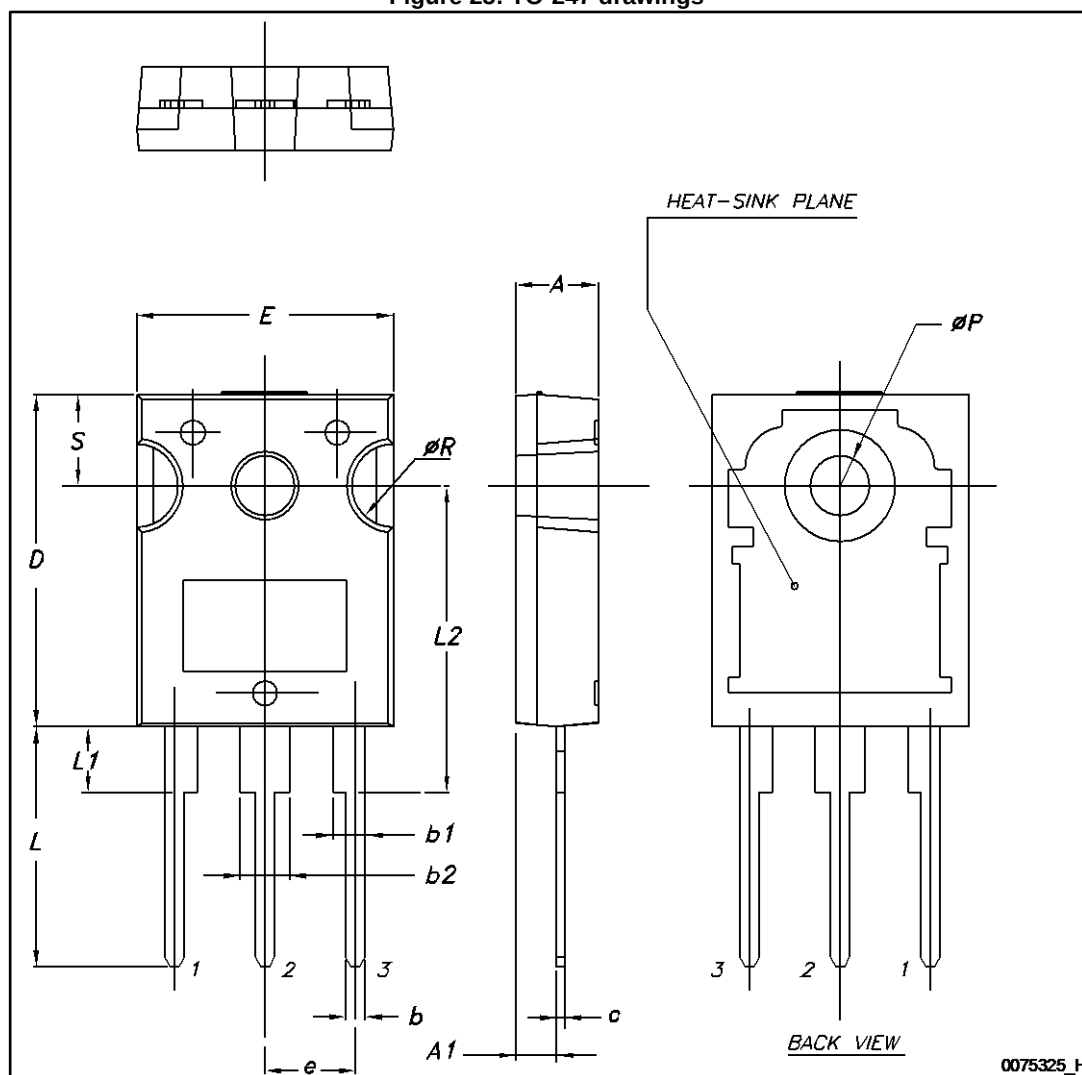


Table 10: TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S	5.30	5.50	5.70

4.3 TO-220FP package mechanical data

Figure 26: TO-220FP drawings

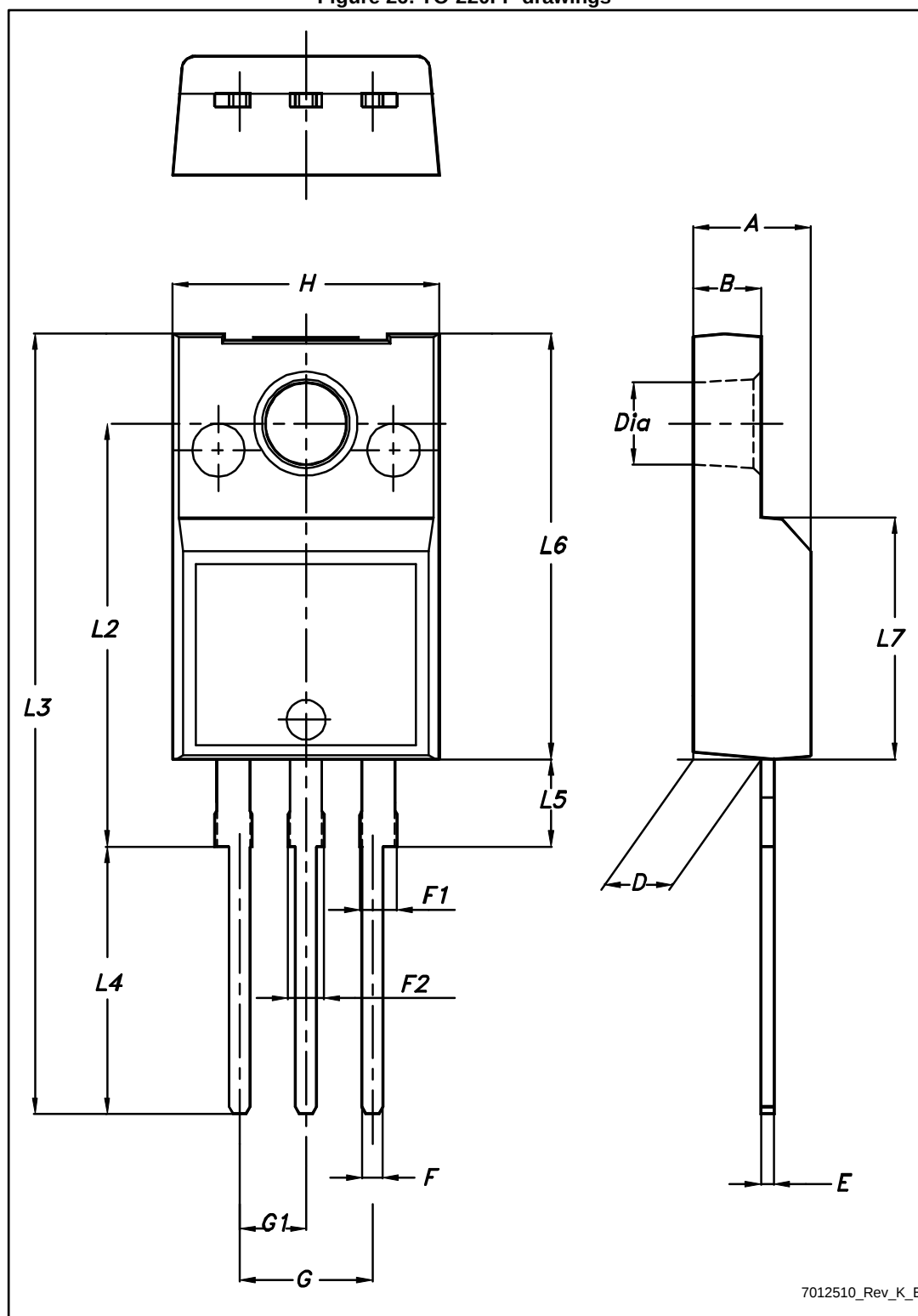


Table 11: TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
07-Oct-2014	1	First release.
14-Oct-2014	2	Document status promoted from preliminary to production data.

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