Low Cost, Triple Differential Drivers for Wideband Video

Data Sheet

AD8141/AD8142

FEATURES

Triple, high speed differential drivers
- **255 MHz, −3 dB large signal bandwidth**
- **65 MHz, 0.1 dB flatness**
- **1150 V/µs slew rate**
- **12 ns settling time**

Single 5 V or split supply operation
Fixed gain of 2
Internal common-mode feedback network
- **Output balance error −50 dB at 50 MHz**

AD8142 has integrated sync-on-common-mode circuitry
High-Z output when disabled
Differential-to-differential or single-ended-to-differential operation
High isolation between amplifiers: −100 dB at 10 MHz
Low power: 44 mA at 5 V
Available in space-saving packaging: 4 mm × 4 mm LFCSP

APPLICATIONS

Keyboard-video-mouse (KVM) networking
Video distribution
Digital signage
Security cameras

FUNCTIONAL BLOCK DIAGRAMS

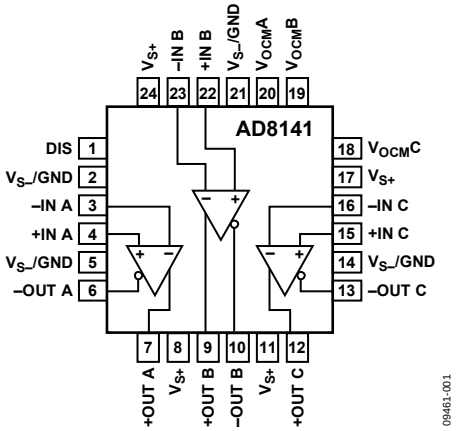

Figure 1.

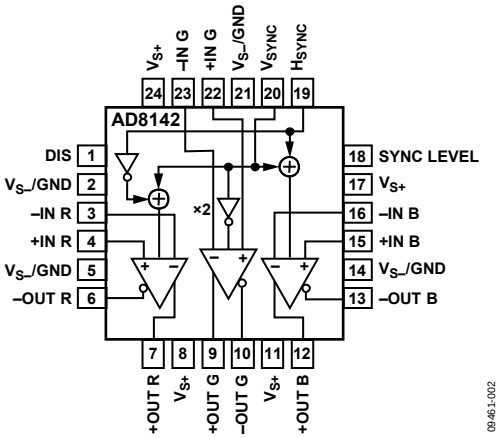

Figure 2.

GENERAL DESCRIPTION

The AD8141 and AD8142 are triple, low cost, differential or single-ended-input-to-differential-output drivers. Each amplifier has a fixed gain of 2 to compensate for the attenuation of the line termination resistors. The AD8141 and AD8142 are specifically designed for RGB signals but can be used for any type of signals. The amplifiers have very fast slew rate and settling time while being manufactured on a cost effective CMOS process. They are optimized for high resolution video performance with a 0.1 dB flatness of 65 MHz, which allows driving high resolution video over any type of UTP cable.

The drivers have an internal common-mode feedback loop that provides output amplitude and phase matching, achieving −50 dB balance error at 50 MHz and thereby suppressing even-order harmonics and minimizing radiated electromagnetic interference (EMI).

The AD8142 includes a unique sync-on-common-mode feature that allows the user to transmit balanced horizontal and vertical video sync signals over the three common-mode channels. Additionally, the AD8141 and AD8142 both have a disable feature that, when asserted, produces high-Z outputs, allowing line isolation and easy multiplexing.

The AD8141 and AD8142 are available in a 24-lead 4 mm × 4 mm LFCSP and operate over a temperature range of −40°C to +85°C. They can be used with the AD8145 triple differential-to-single-ended receiver, AD8123 triple equalizer, AD8120 triple delay line, and the AD8117 or AD8175 crosspoint switches to produce a high resolution video distribution system.

Rev. B **Document Feedback**

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REVISION HISTORY

3/2017—Rev. A to Rev. B
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

4/2013—Rev. 0 to Rev. A
Changed Gain to Green Common-Mode Output Maximum Parameter from 1.2 V/V to 2.20 V/V; Table 1 ... 3

7/2011—Revision 0: Initial Version

SPECIFICATIONS

V_{S+} = 5 V, V_{S-} = 0 V, $R_{L,dm}$ = 200 Ω, T_A = 25°C, V_{OCM} = 1.5 V (AD8141), H_{SYNC}, V_{SYNC}, and SYNC LEVEL = 0 V (AD8142), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
Dynamic Performance					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p, AD8141/AD8142		275/285		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p, AD8141/AD8142		255/265		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		65		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75% (rise/fall)		1150/1250		V/µs
Settling Time to 0.1%	V_O = 2 V step		12		ns
Isolation Between Amplifiers	f = 10 MHz, between Amplifier R and Amplifier G		−100		dB
Differential Input Characteristics					
Input Common-Mode Voltage Range	$V_{OCM} = V_{s+}/2$	V_{S-} + 0.2		V_{S+} − 1	V
Input Resistance	Differential		2		kΩ
	Single-ended input		1.5		kΩ
Input Capacitance	Differential		2		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−60		dB
Differential Output Characteristics					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$, $\Delta V_{IN, dm}$ = ±1 V	1.95	2	2.04	V/V
Output Voltage Swing	Each single-ended output	V_{S-} + 0.18		V_{S+} − 0.4	V
Output Offset Voltage		−70	1.5	+70	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±30		µV/°C
Output Balance Error	f = 50 MHz		−50		dB
	DC		−66	−43	dB
Output Voltage Noise (RTO)	f = 20 MHz		41		nV/√Hz
Maximum Number of Parallel Loads	1.4 V p-p into 200 Ω per load		4		Loads
COMMON-MODE INPUT PERFORMANCE (AD8141)					
V_{OCM} Dynamic Performance					
−3 dB Bandwidth	ΔV_{OCM} = 100 mV p-p		114		MHz
Slew Rate	V_{OCM} = 0.5 V to 2.5 V, 25% to 75% (rise/fall)		130/155		V/µs
DC Gain	ΔV_{OCM} = ±1 V	0.98	1.00	1.02	V/V
V_{OCM} Input Characteristics					
Input Voltage Range		V_{S-} + 0.2		V_{S+} − 0.2	V
Input Resistance	Thevenin to midsupply		2.8		kΩ
Input Offset Voltage		−87	−30	+26	mV
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−60		dB
COMMON-MODE SYNC PERFORMANCE (AD8142)					
Slew Rate	$V_{OUT, cm}$ = 0.5 V to +2.5 V; 25% to 75% (rise/fall)		130/155		V/µs
Nominal Output Common-Mode Level			V_{S-} + 1.5		V
H_{SYNC} AND V_{SYNC} INPUTS (AD8142)					
Input Low Voltage	Referenced to GND		0 to 1.6		V
Input High Voltage	Referenced to GND		1.9 to 5		V
SYNC LEVEL INPUT (AD8142)					
Input Voltage Range	Referenced to V_{S-}	V_{S-}		V_{S-} + 1	V
Setting to Achieve 0.5 V Pulse Levels	Referenced to V_{S-}		V_{S-} + 0.5		V
Gain to Red Common-Mode Output	$\Delta V_{OUT, cm}/\Delta V_{SYNC\ LEVEL}$	0.85	1.00	1.15	V/V
Gain to Green Common-Mode Output	$\Delta V_{OUT, cm}/\Delta V_{SYNC\ LEVEL}$	1.80	2.00	2.20	V/V
Gain to Blue Common-Mode Output	$\Delta V_{OUT, cm}/\Delta V_{SYNC\ LEVEL}$	−1.15	−1.00	−0.85	V/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	Positive supply	4.5		5.5	V
Quiescent Current	AD8141/AD8142		44/47	56/57	mA
	Disabled		1.2	1.6	mA
PSRR			−77		dB
OUTPUT HIGH-Z PERFORMANCE					
DIS Input Low Voltage			0 to 1.6		V
DIS Input High Voltage			1.9 to V_{S+}		V
DIS Assert Time			5		ns
DIS Deassert Time			50		ns
Differential Output Impedance Magnitude With DIS Asserted	1 MHz, each output, DIS input at V_{S+}		11		kΩ
	10 MHz, each output, DIS input at V_{S+}		1.9		kΩ
ISOLATION					
Input-to-Output	1 MHz, each output, DIS input at V_{S+}		−78		dB
	10 MHz, each output, DIS input at V_{S+}		−58		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	5.5 V
H_{SYNC}, V_{SYNC}, SYNC LEVEL	V_{S-}/V_{S+}
Power Dissipation	See Figure 3
Input Common-Mode Voltage	V_{S-}/V_{S+}
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 3. Thermal Resistance with the Underside Pad Thermally Connected to a Copper Plane

Package Type/PCB Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP/4-Layer	38	4.7	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8141/AD8142 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8141/AD8142. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of differential and common-mode currents flowing to the loads, as well as currents flowing through the internal differential and common-mode feedback loops. The internal resistor tap used in the common-mode feedback loop places a 12.5 kΩ differential load on the output. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}. The exposed pad on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a PCB plane to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 24-lead LFCSP (38°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

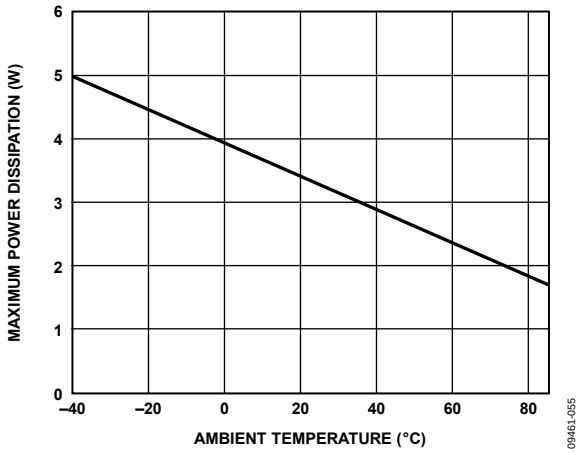


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

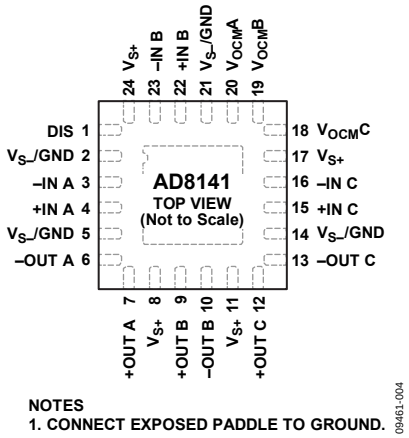


Figure 4. AD8141 Pin Configuration

Table 4. AD8141 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DIS	Disable. This pin places outputs in high-Z condition and lowers supply current.
2, 5, 14, 21	V_{S-}/GND	Negative Power Supply Voltage.
3	–IN A	Inverting Input, Amplifier A.
4	+IN A	Noninverting Input, Amplifier A.
6	–OUT A	Negative Output, Amplifier A.
7	+OUT A	Positive Output, Amplifier A.
8, 11, 17, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT B	Positive Output, Amplifier B.
10	–OUT B	Negative Output, Amplifier B.
12	+OUT C	Positive Output, Amplifier C.
13	–OUT C	Negative Output, Amplifier C.
15	+IN C	Noninverting Input, Amplifier C.
16	–IN C	Inverting Input, Amplifier C.
18	V_{OCM}C	The voltage applied to this pin controls the output common-mode voltage for Amplifier C.
19	V_{OCM}B	The voltage applied to this pin controls the output common-mode voltage for Amplifier B.
20	V_{OCM}A	The voltage applied to this pin controls the output common-mode voltage for Amplifier A.
22	+IN B	Noninverting Input, Amplifier B.
23	–IN B	Inverting Input, Amplifier B.
	EPAD	Connect Exposed Paddle to Ground.

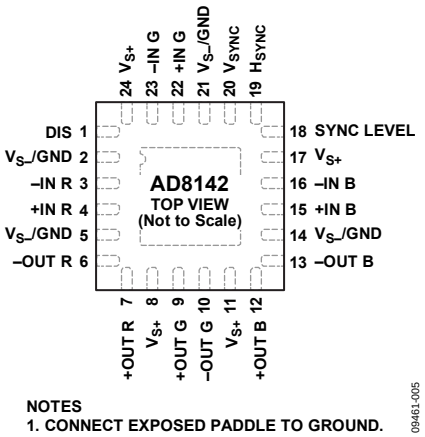


Figure 5. AD8142 Pin Configuration

Table 5. AD8142 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DIS	Disable. This pin places outputs in high-Z condition and lowers supply current.
2, 5, 14, 21	V_{S-}/GND	Negative Power Supply Voltage. GND is for single 5 V applications.
3	–IN R	Inverting Input, Red Amplifier.
4	+IN R	Noninverting Input, Red Amplifier.
6	–OUT R	Negative Output, Red Amplifier.
7	+OUT R	Positive Output, Red Amplifier.
8, 11, 17, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT G	Positive Output, Green Amplifier.
10	–OUT G	Negative Output, Green Amplifier.
12	+OUT B	Positive Output, Blue Amplifier.
13	–OUT B	Negative Output, Blue Amplifier.
15	+IN B	Noninverting Input, Blue Amplifier.
16	–IN B	Inverting Input, Blue Amplifier.
18	SYNC LEVEL	The voltage applied to this pin with respect to V_{S-}/GND controls the amplitude of the sync pulses that are applied to the common-mode voltages.
19	H_{SYNC}	Horizontal Sync Pulse Input with Respect to Ground.
20	V_{SYNC}	Vertical Sync Pulse Input with Respect to Ground.
22	+IN G	Noninverting Input, Green Amplifier.
23	–IN G	Inverting Input, Green Amplifier.
	EPAD	Connect Exposed Paddle to Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{S+} = 5 V, V_{S-} = 0 V, $R_{L,dm}$ = 200 Ω, T_A = 25°C, V_{OCM} = 1.5 V (AD8141), H_{SYNC}, V_{SYNC}, and SYNC LEVEL = 0 V (AD8142), unless otherwise noted.

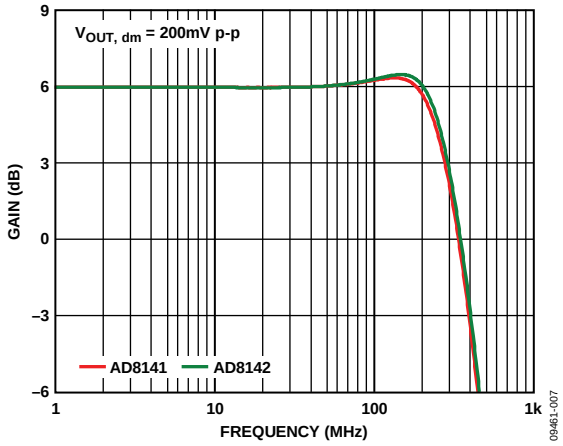


Figure 6. Small Signal Frequency Response

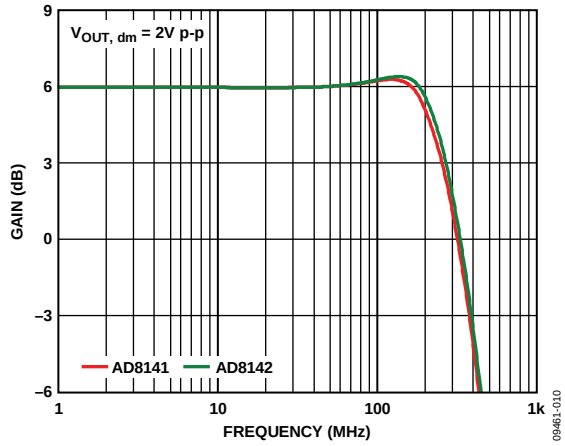


Figure 9. Large Signal Frequency Response

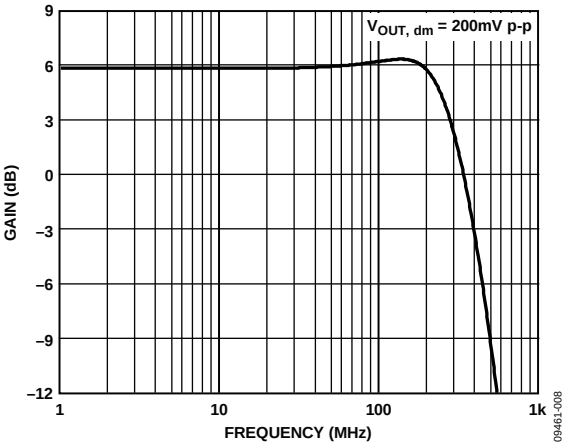


Figure 7. Small Signal Frequency Response at V_{OCM} = 2.5 V (AD8141)

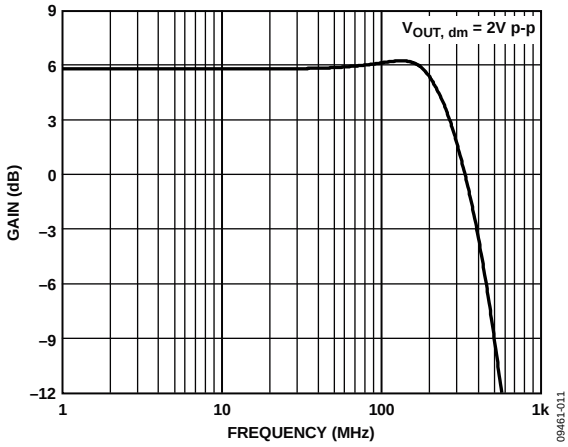


Figure 10. Large Signal Frequency Response at V_{OCM} = 2.5 V (AD8141)

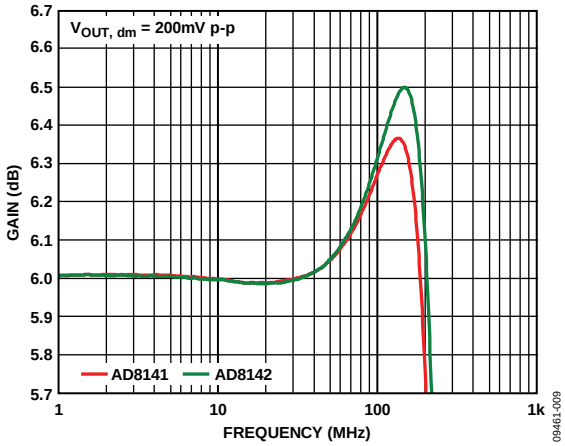


Figure 8. Small Signal 0.1 dB Flatness

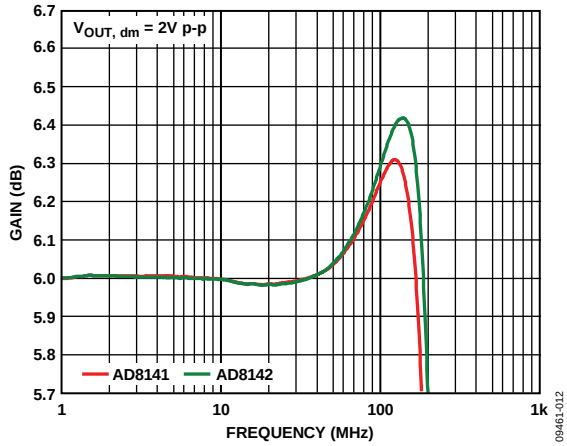


Figure 11. Large Signal 0.1 dB Flatness

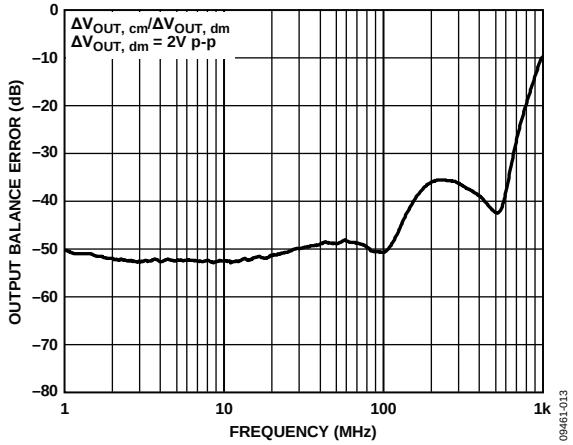


Figure 12. Output Balance Error vs. Frequency

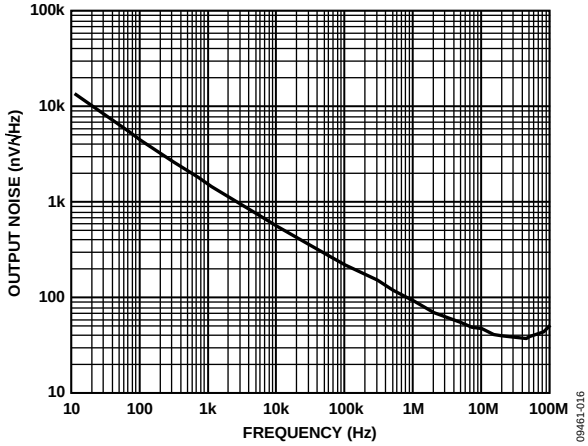


Figure 15. Output Voltage Noise Density vs. Frequency

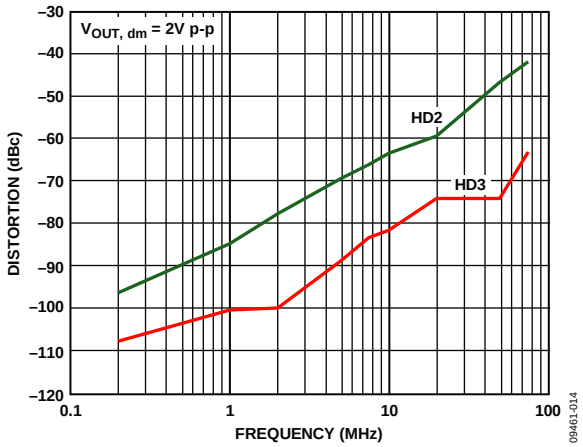


Figure 13. AD8141 Harmonic Distortion vs. Frequency

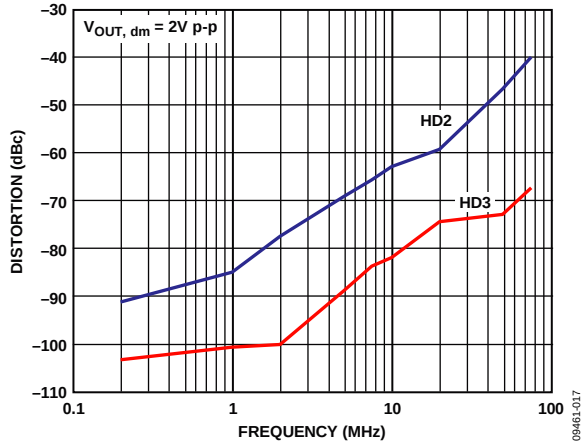


Figure 16. AD8142 Harmonic Distortion vs. Frequency

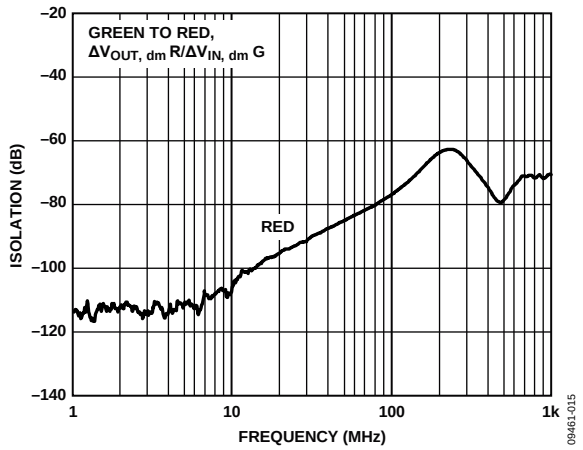


Figure 14. Channel-to-Channel Isolation vs. Frequency

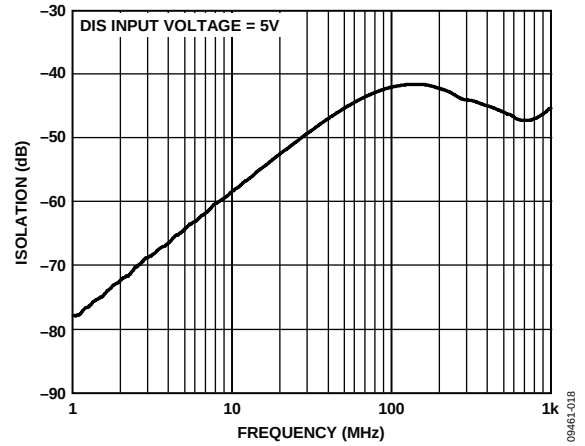


Figure 17. Disabled Input-to-Output Isolation vs. Frequency

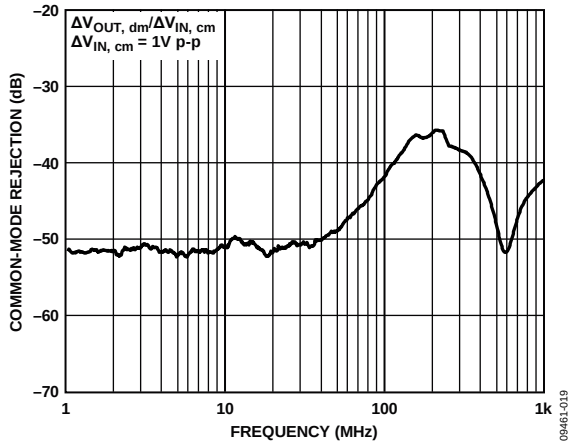


Figure 18. Common-Mode Rejection vs. Frequency

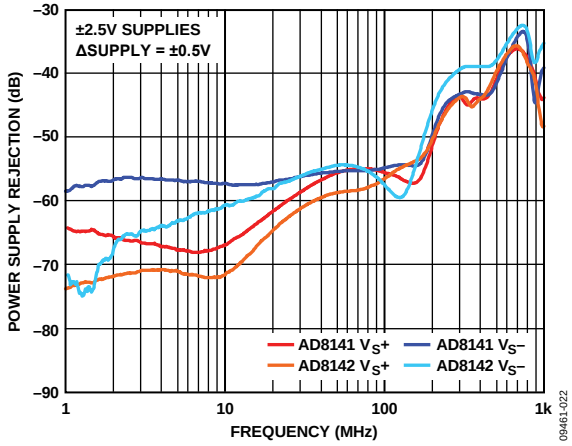


Figure 21. Power Supply Rejection vs. Frequency

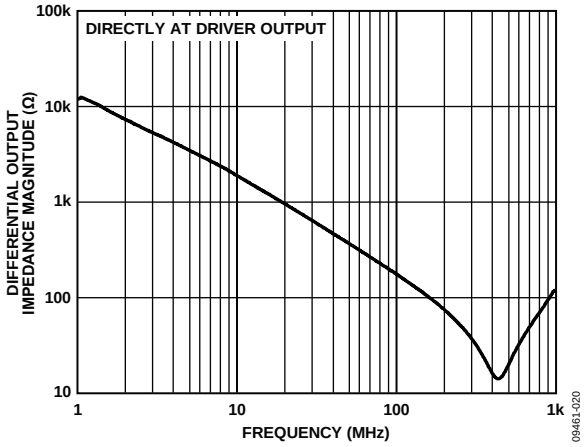


Figure 19. Disabled Output Impedance Magnitude vs. Frequency

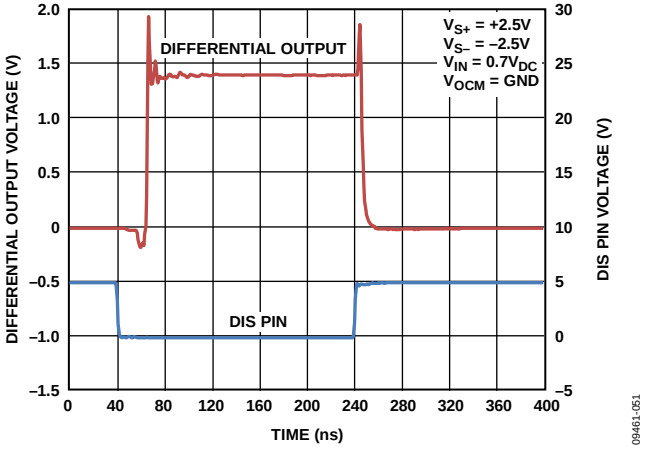


Figure 22. Disable Response Time

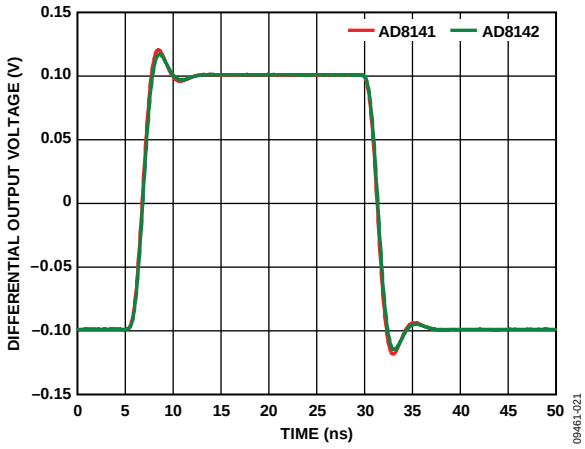


Figure 20. Small Signal Transient Response

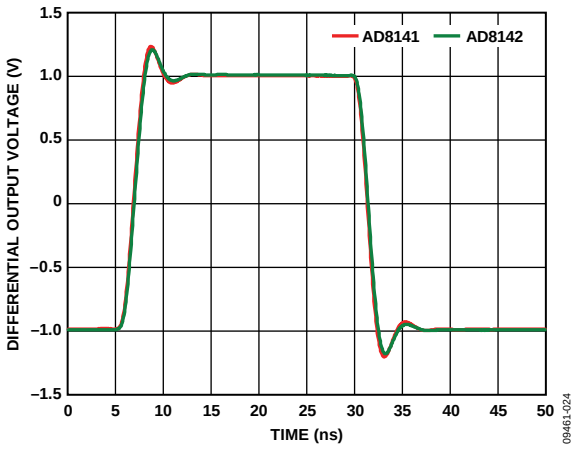


Figure 23. Large Signal Transient Response

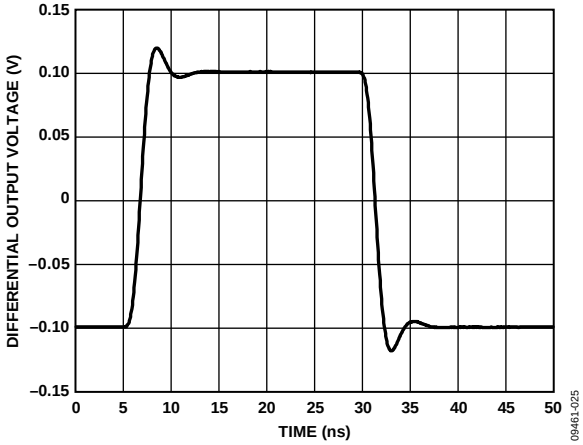


Figure 24. Small Signal Transient Response, V_{OCM} = 2.5 V (AD8141)

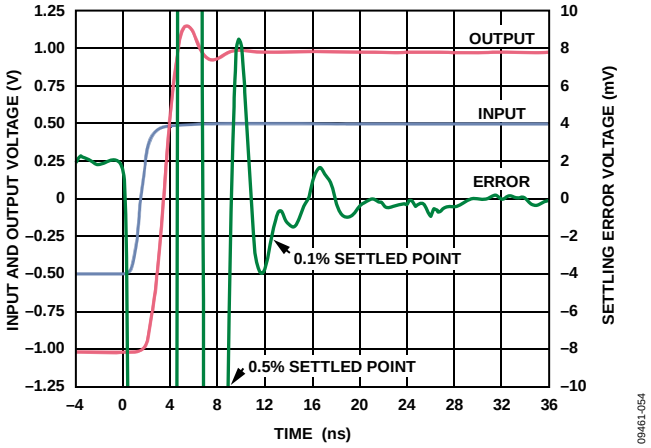


Figure 25. Differential Settling Time

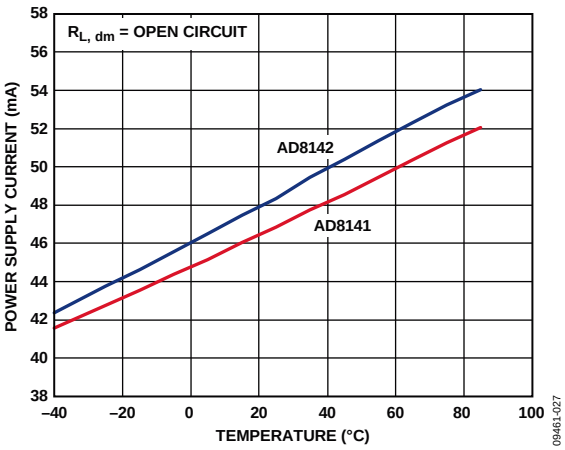


Figure 26. Positive Power Supply Current vs. Temperature

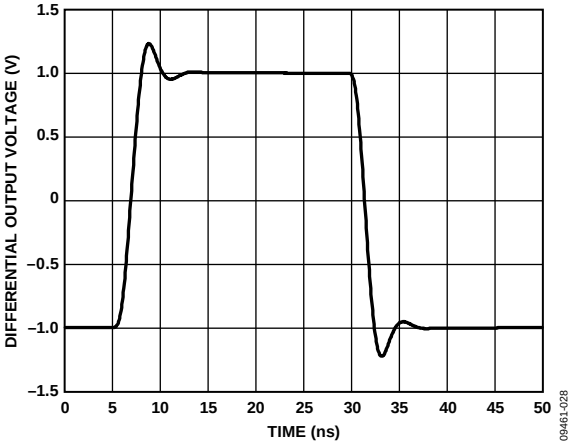


Figure 27. Large Signal Transient Response, V_{OCM} = 2.5 V (AD8141)

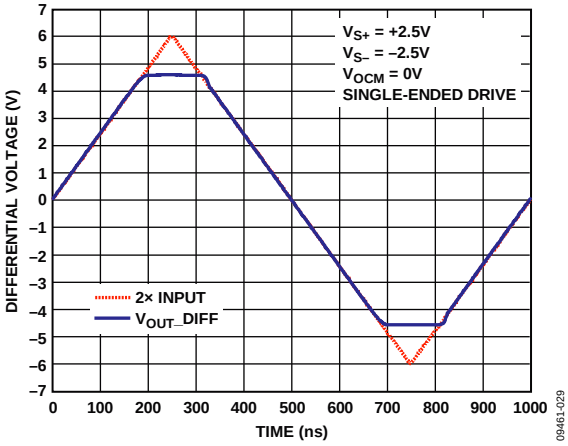


Figure 28. AD8141 Differential Overdrive Recovery

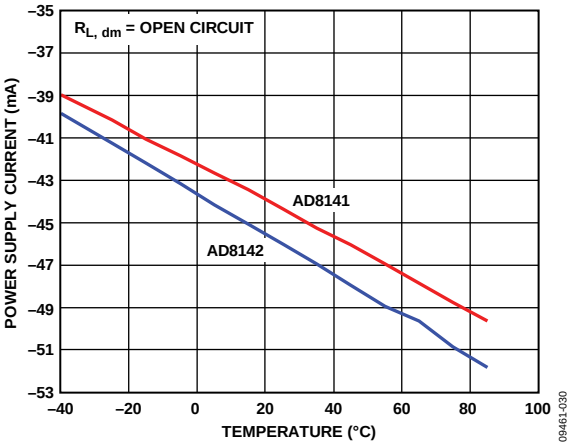


Figure 29. Negative Power Supply Current vs. Temperature

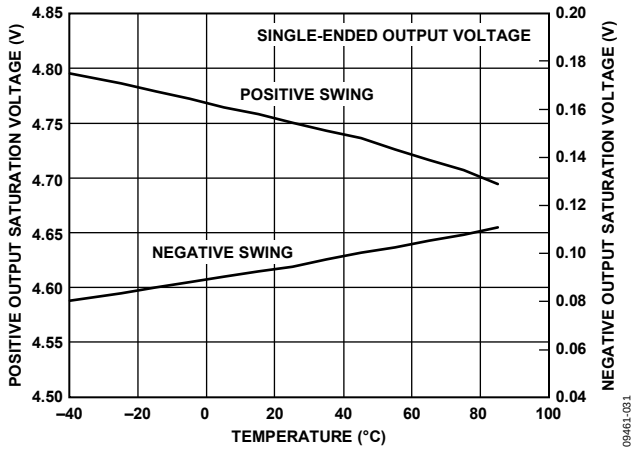


Figure 30. Output Saturation vs. Temperature

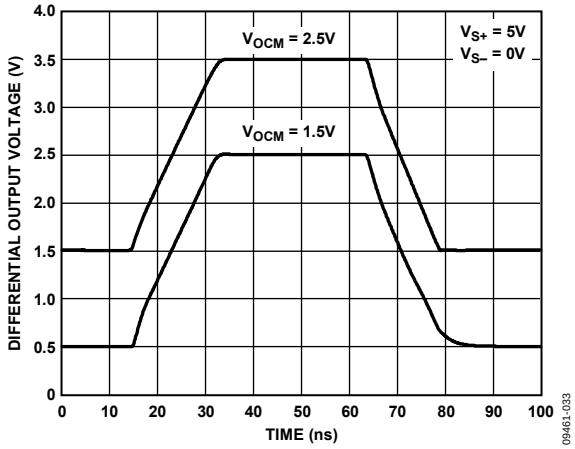


Figure 32. V_{OCM} Large Signal Transient Response (AD8141)

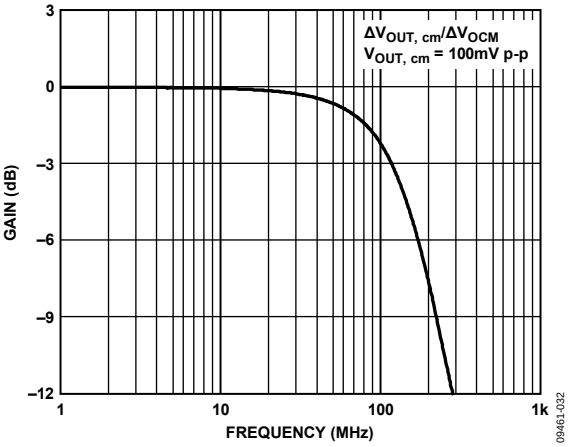


Figure 31. V_{OCM} Frequency Response (AD8141)

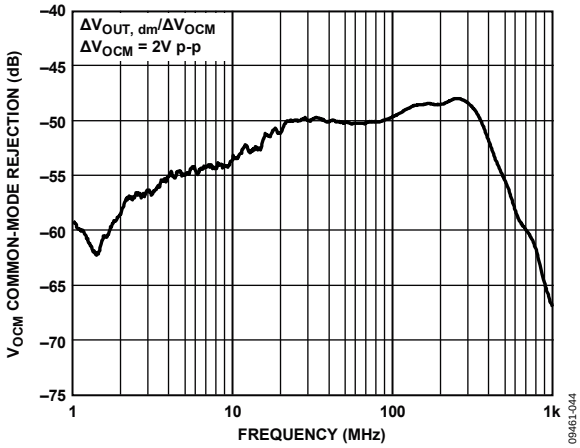


Figure 33. V_{OCM} Common-Mode Rejection vs. Frequency

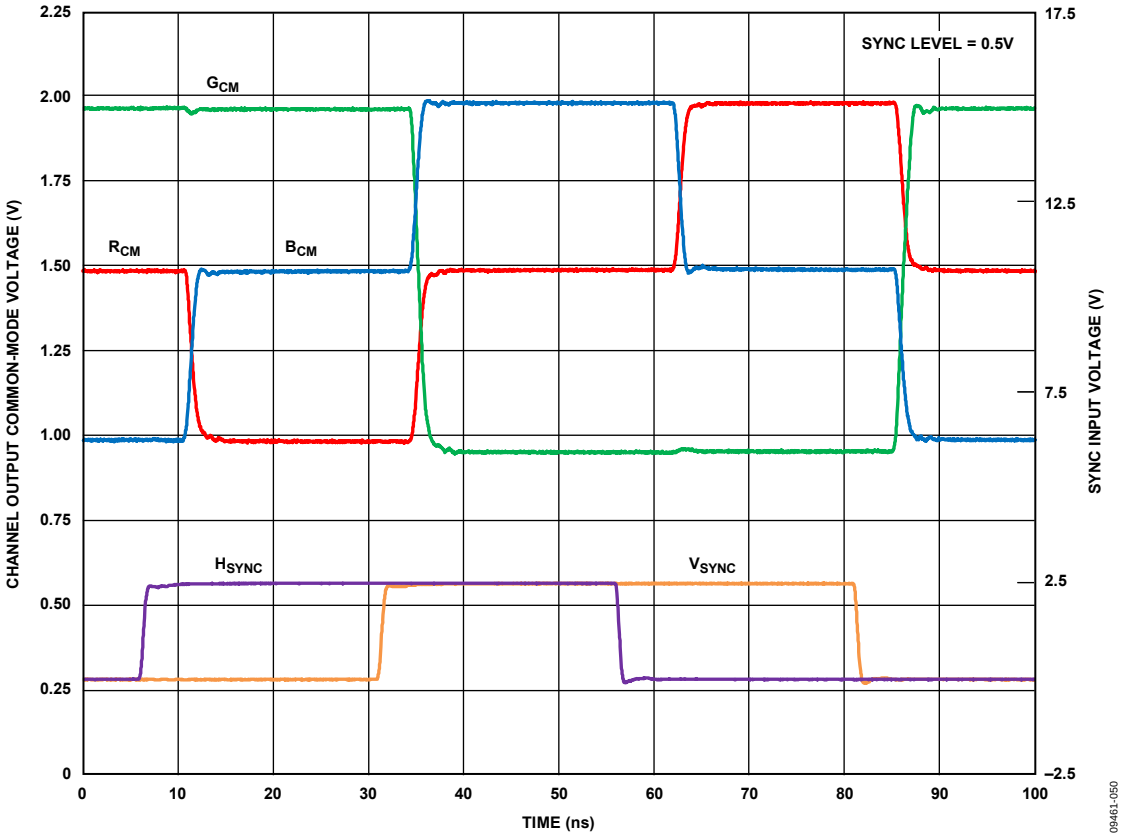


Figure 34. AD8142 Output Common-Mode Signals for Various Sync Pulse Inputs

BASIC TEST CIRCUIT

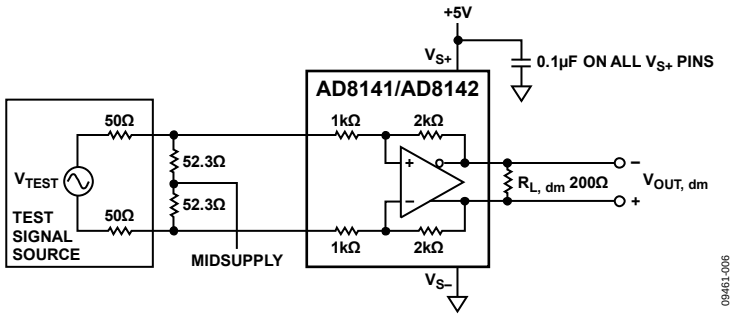


Figure 35. Basic Test Circuit

TERMINOLOGY

Differential Voltage

Differential voltage refers to the difference between two node voltages that are balanced with respect to each other. For example, in Figure 36, the output differential voltage (or output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{OP} - V_{ON})$$

Common-mode voltage refers to the average of two node voltages with respect to a common reference (usually the local ground). The output common-mode voltage is defined as

$$V_{OUT,cm} = \frac{(V_{OP} + V_{ON})}{2}$$

Output Balance

Output balance is a measure of how well the differential output signals are matched in amplitude and how close they are to exactly 180° apart in phase. Balance can be easily determined by placing a well-matched resistor divider between the differential output voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance error is the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential-mode voltage in response to a differential input signal.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,cm}}{\Delta V_{OUT,dm}} \right|$$

THEORY OF OPERATION

The differential drivers contained in the AD8141 and AD8142 differ from conventional op amps in that they have two outputs whose voltages move in opposite directions. Like op amps, they rely on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8141 and AD8142 drivers make it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has generally required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes, the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

Each AD8141/AD8142 driver uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by the internal resistors, controls the differential output voltage only. The internal common-mode feedback loop controls the common-mode output voltage only. This architecture makes it easy to arbitrarily set the output common-mode level by simply applying a voltage to the V_{OCM} input. The output common-mode voltage is forced, by internal common-mode feedback, to equal the voltage applied to the V_{OCM} input, while simultaneously balancing the differential output voltage. The AD8141 V_{OCM} inputs are available to the user, whereas the AD8142 V_{OCM} inputs are internally connected to sync-on-common-mode circuitry that automatically imbeds the H_{SYNC} and V_{SYNC} signals on the three output common-mode voltages.

The overall driver architecture produces outputs that are highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude that are 180° apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The drivers use two negative feedback loops, each with high open-loop gain, to force their differential and common-mode output voltages in such a way as to minimize the differential and common-mode input error voltages. The differential input error voltage is defined as the voltage between the differential inputs labeled V_{AP} and V_{AN} in Figure 36. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 36 can be described by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G} = 2$$

where R_F = 2.0 kΩ and R_G = 1.0 kΩ nominally.

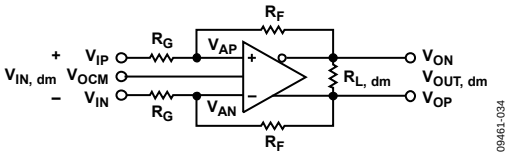


Figure 36. Circuit Definitions

CALCULATING AN APPLICATION CIRCUIT'S INPUT IMPEDANCE

The effective input impedance of a circuit such as that in Figure 36 at V_{IP} and V_{IN} depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the differential input impedance, $R_{IN,dm}$ between the inputs V_{IP} and V_{IN} is simply

$$R_{IN,dm} = 2 \times R_G = 2.0\ \text{k}\Omega$$

In the case of a single-ended input signal (for example, if V_{IN} is grounded and the input signal is applied to V_{IP}), the input impedance becomes

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}}\right) = 1.5\ \text{k}\Omega$$

The input impedance of the circuit is higher than for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The driver inputs are designed to facilitate level-shifting of ground referenced input signals on a single power supply. For a single-ended input, this implies, for example, that the voltage at V_{IN} in Figure 36 is 0 V when the amplifier's negative power supply voltage is also set to 0 V.

It is important to ensure that the common-mode voltage at the amplifier inputs, V_{AP} and V_{AN}, stays within its specified range. Because the V_{AP} and V_{AN} voltages are driven to be essentially equal by negative feedback, the amplifier's input common-mode voltage can be expressed as a single term, V_{ACM}. V_{ACM} can be calculated as

$$V_{ACM} = \frac{V_{OCM} + 2V_{ICM}}{3}$$

where V_{ICM} is the common-mode voltage of the input signal, that is,

$$V_{ICM} = \frac{V_{IP} + V_{IN}}{2}$$

TERMINATING A SINGLE-ENDED INPUT

Each driver has a nominal fixed gain of 2, with R_F = 2.0 kΩ and R_G = 1.0 kΩ. A typical single-ended video signal source applied to the AD8141/AD8142 input has a maximum terminated output voltage of 0.7 V p-p and source resistance of 75 Ω. Because the terminated output voltage of the source is 0.7 V p-p, the open-circuit output voltage of the source is 1.4 V p-p. The source shown in Figure 37 indicates this open-circuit voltage. The following three steps illustrate how to terminate a signal from a typical single-ended 75 Ω video source.

1. The single-ended input impedance is calculated as R_{IN} = 1.5 kΩ.

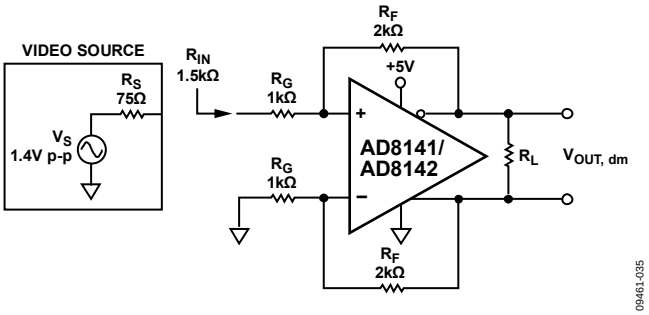


Figure 37. Calculating Single-Ended Input Impedance, R_{IN}

2. To match the 75 Ω source resistance, the termination resistor, R_T, is calculated using $R_T||1.125$ kΩ = 75 Ω. The closest standard 1% value for R_T is 80.6 Ω.

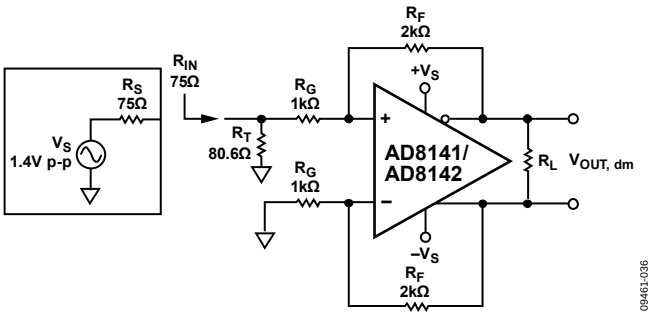


Figure 38. Adding Termination Resistor R_T

3. It can be seen from Figure 38 that the effective R_G in the upper feedback loop is now greater than the R_G in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, a correction resistor (R_{TS}) is added in series with R_G in the lower loop. R_{TS} is the closest 1% resistor to the Thevenin equivalent of the source resistance R_S and the termination resistance R_T, equal to $R_S||R_T$.

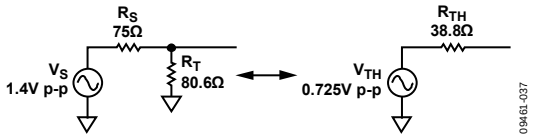


Figure 39. Calculating the Thevenin Equivalent

1. $R_{TH} = R_S||R_T$ = 38.8 Ω, and R_{TS} = 38.3 Ω. Note that V_{TH} is greater than 0.7 V p-p, which was obtained with R_T = 75 Ω alone. The modified circuit with the Thevenin equivalent of the terminated source and R_{TS} in the lower feedback loop is shown in Figure 40.

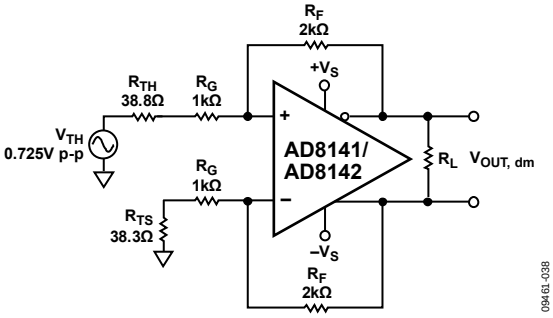


Figure 40. Thevenin Equivalent and Matched Gain Resistors

Figure 40 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of R_G is increased in both loops, lowering the overall closed-loop gain. The second is that V_{TH} is a little larger than 0.7 V p-p, as it is if R_T = 75 Ω alone. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops, the effects essentially cancel each other out. For smaller R_F and R_G, however, the diminished closed-loop gain is not canceled completely by the increased V_{TH}.

The desired differential output in this example is 1.4 V p-p because the terminated input signal is 0.7 V p-p and the closed-loop gain = 2. The actual differential output voltage is equal to (0.725 V p-p)(2 kΩ/1038.3 Ω) = 1.4 V p-p. This illustrates how the two aforementioned effects cancel for large R_F and R_G.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the output impedance of the drivers to reduce phase margin, resulting in high frequency ringing in the pulse response. The best way to minimize this effect is to place the source termination resistors immediately at the amplifier outputs to minimize parasitic capacitances formed by unnecessarily long traces.

DISABLE

The AD8141 and AD8142 have disable pins that, when pulled high, significantly reduce the power consumed while simultaneously placing the outputs in high-Z states. The disable feature can be used to multiplex two drivers. See Figure 17, Figure 19, and Figure 22 for the disabled input-to-output isolation, output impedance, and response performance. The threshold levels for the disable pin are listed in Table 1.

An output glitch occurs whenever the disable feature is asserted or deasserted. See the Applications Information section for details.

AD8142 SYNC-ON-COMMON-MODE

The AD8142 includes on-chip, sync-on-common-mode circuitry that encodes externally applied H_{SYNC} and V_{SYNC} signals onto the common-mode output voltages of each of the R, G, and B drivers. The circuit encodes the horizontal and vertical sync pulses in a way that results in low radiated energy. A simplified circuit that illustrates how the pulses are encoded is shown in Figure 41. For a more detailed description of the sync scheme, see the Applications Information section.

The sync-on-common-mode circuit generates a current based on the voltage applied to the SYNC LEVEL input pin (Pin 18) with respect to the negative supply. With SYNC LEVEL input tied to V_{S-}, the common-mode output of all drivers is set at 1.5 V above the negative supply. Using a resistor divider, a voltage can be applied between V_{S-} and SYNC LEVEL that determines the maximum deviation of the common-mode outputs from their midsupply level. If, for instance, SYNC LEVEL − V_{S-} = 0.5 V and the supply voltage is 5 V, then the common-mode outputs fall within an envelope of 1.5 V ± 0.5 V. The state of each $V_{OUT, cm}$ output based on the H_{SYNC} and V_{SYNC} inputs is determined by the equations defined in the Applications Information section.

For the positive supplies between 2.5 V and 5 V, the sync-on-common-mode circuit can be used by directly applying standard H_{SYNC} and V_{SYNC} signals to the respective AD8142 inputs. These inputs adhere to standard logic thresholds (see Table 1 for the exact levels). The H_{SYNC} and V_{SYNC} inputs, therefore, can be driven directly off the output of a computer video card without concern of being overdriven. The input path from the H_{SYNC} and V_{SYNC} inputs to the switches in the current mode level-shifting circuit are well matched to eliminate false switching transients. This maximizes common-mode balance and minimizes radiated energy.

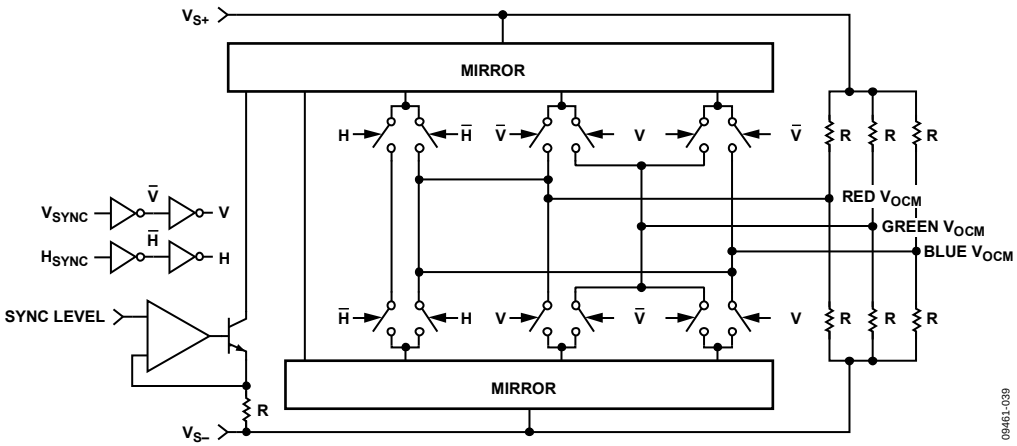


Figure 41. Sync-On-Common-Mode Simplified Circuit

APPLICATIONS INFORMATION

DRIVING RGB VIDEO OVER CAT-5 CABLE

The AD8141 and AD8142 are devices whose foremost application is driving RGB and component video signals over unshielded twisted pair (UTP) cable in video distribution networks. Single-ended video signals are easily converted to differential signals for transmission over the cable, and the internally fixed gain of 2 automatically compensates for the losses incurred by the source and load terminations. Figure 42 shows the AD8141/AD8142 in a triple, single-ended-to-differential application when driven from a 75 Ω video source.

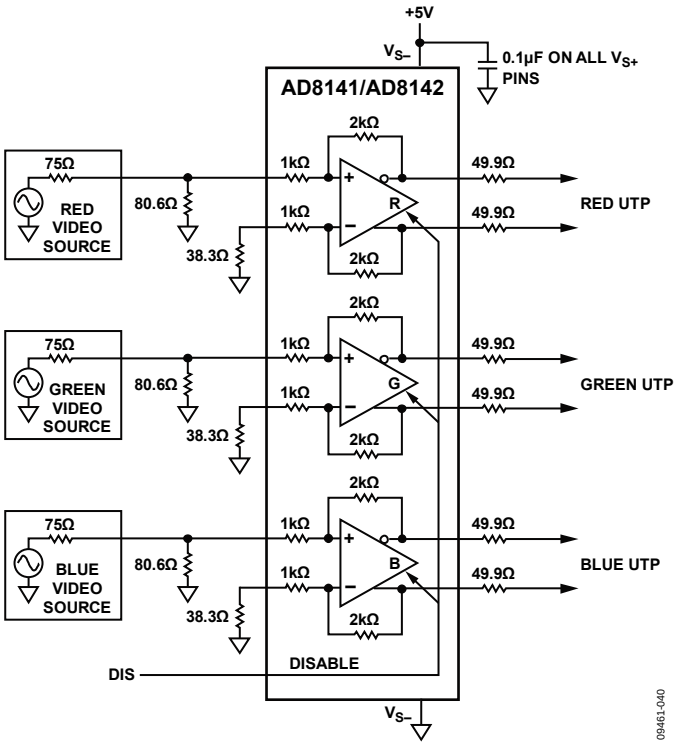


Figure 42. AD8141/AD8142 in Single-Ended-to-Differential Application on Single 5 V Supply (Sync Pulse Encoding Not Shown)

SINGLE 5 V SUPPLY APPLICATION INFORMATION

The AD8141 and AD8142 require a nominal voltage of 5 V across their V_{S+} and V_{S-} power supply pins, and that their EPADs be connected to system ground; the voltage between V_{S+} and the local system ground must be greater than or equal to 2.5 V and less than or equal to 5 V. These requirements can be met by a single +5 V supply, or split supplies such as ±2.5 V, +3 V/−2 V, and so on. Operating the AD8141 and AD8142 with ±2.5 V supplies provides considerable power savings compared with other drivers operating at ±5 V supplies, without any disadvantages with regard to input and output ranges in most cases.

The receivers used with the AD8141 and AD8142, such as the AD8145, AD8143, AD8123, and AD8128, generally operate with split supplies, ranging from ±5 V to ±12 V. The split supply arrangement results in a receiver input common-mode range that is centered at 0 V relative to the local ground reference and ranges to within a volt or two from each rail. Ground potential differences normally exist between the driver end and the receiver end, and these differences cause the relative common-mode voltages between the driver and receiver to shift. See Figure 43 for an example.

In Figure 43, $V_{R,CM} = V_{O,CM} + V_{SHIFT}$. If $V_{O,CM} = 0$ V and $V_{SHIFT} = 2$ V, $V_{R,CM}$ is 2 V. This is because the receiver ground is shifted down by 2 V relative to the driver ground, and the common-mode level on the cable stays constant. It can be seen from this example that the most margin to absorb ground shifts exists when the center of the receiver input common-mode voltage range relative to its ground is the same as the output common-mode voltage of the driver with respect to its ground.

Most receivers operate with their input common-mode ranges centered at 0 V; therefore, the best case for the driver is to set its output common-mode voltage to 0 V. This is not possible for the AD8141 or AD8142 on a single 5 V supply, but it can be accomplished using split supplies. If a single 5 V supply is required, the rail-to-rail output allows the AD8141 output common-mode voltage to be set to less than 1 V to be as close as possible to the ideal setting of 0 V. Whereas the AD8141 has uncommitted V_{OCM} inputs, the AD8142 has internal sync-encoding circuitry that fixes the nominal output common-mode voltage at 1.5 V above the negative rail. Each part has a resistive divider on the V_{OCM} input that sets the nominal output common-mode voltage to 1.5 V above the negative rail when no external voltage is applied. The divider consists of a 8.75 kΩ resistor to V_{S+} and a 3.75 kΩ resistor to V_{S-}, forming a Thevenin equivalent load of 2.6 kΩ to 30% of the voltage across the supplies. In the single 5 V supply case, the Thevenin load voltage is 30% of 5 V above 0 V, or 1.5 V.

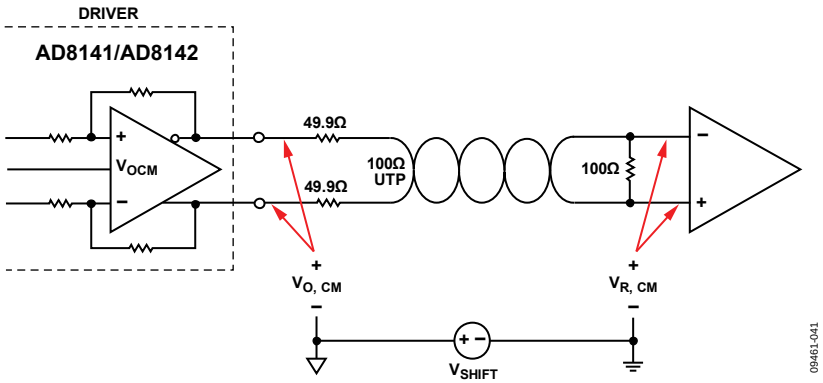


Figure 43. End-to-End Common-Mode Shifts due to Ground Shifts

AD8142 SIGNAL LEVELS ON VARIOUS SUPPLIES

Figure 44 and Figure 45 illustrate the key video signal levels seen in typical applications operating on a single +5 V supply and ±2.5 V supplies; common-mode sync pulses are omitted from the circuit drawing for clarity but are shown in a separate waveform drawing of the signals directly at the AD8142 outputs, shown just below the associated circuit drawing. The sync pulses are common-mode, that is, they move in the same direction on each output polarity. In Figure 44 and Figure 45, this means that the H_{SYNC} pulses are either both green or both blue for the red and black video signals.

DISABLE FEATURE

When asserted, the disable feature minimizes quiescent current consumption and provides a high-Z output. It offers a convenient means to connect two driver outputs together in parallel to form a tristate multiplexed application. The disable feature can also be used to minimize quiescent current drawn when a particular device is not being used.

The disable pin is a binary input that controls the state of the AD8141/AD8142 outputs. Its binary input levels are compatible with most TTL and CMOS families (see Table 1 for the logic levels). The AD8141/AD8142 output is disabled when the disable input is driven to its high state, and the AD8141/AD8142 operates in its normal fashion when the disable input is driven to its low state.

An unavoidable common-mode glitch occurs at the outputs when switching between disabled and enabled states and vice versa. The glitch lasts for a few tens of nanoseconds and is on the order of 2 V or 3 V. If the disable feature is used, it is recommended that common-mode protection be used on the receiver (see the AD8143 data sheet for a detailed description of common-mode protection)

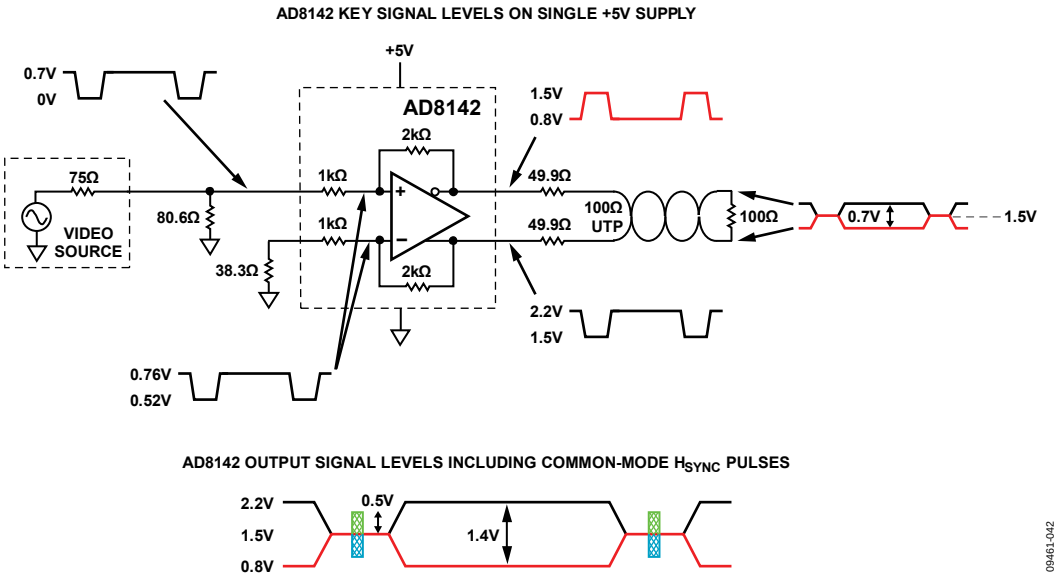


Figure 44. AD8142 Key Signal Levels on Single 5 V Supply; Upper Drawing Shows Schematic, and Lower Drawing Shows Output Signals with H_{SYNC} Pulses

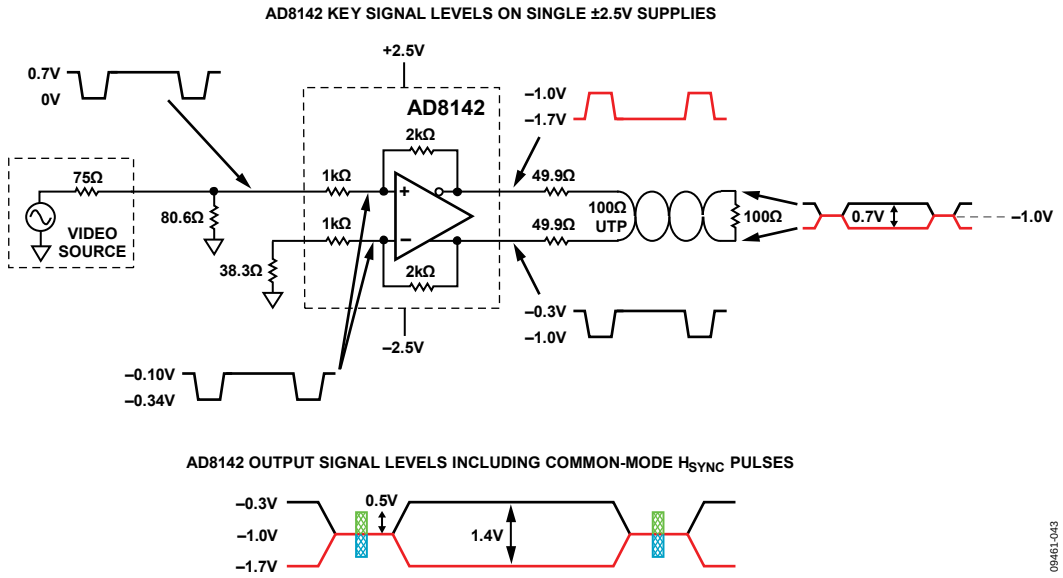


Figure 45. AD8142 Key Signal Levels on ±2.5 V Supplies; Upper Drawing Shows Schematic, and Lower Drawing Shows Output Signals with H_{SYNC} Pulses

DRIVING MULTIPLE OUTPUTS

The AD8141/AD8142 can drive four parallel UTP cables (50 Ω differential load) with only 1.5% reduction in output swing (see Figure 46). As is expected, driving fewer parallel cables results in less output swing reduction.

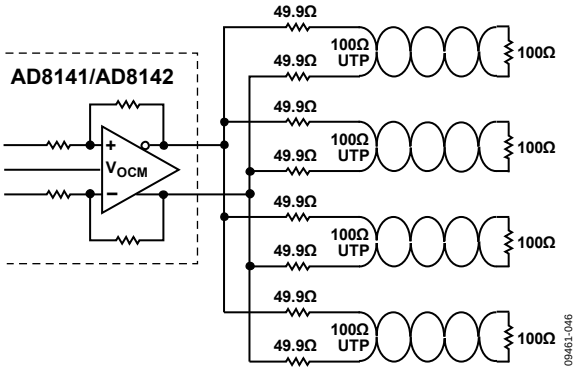
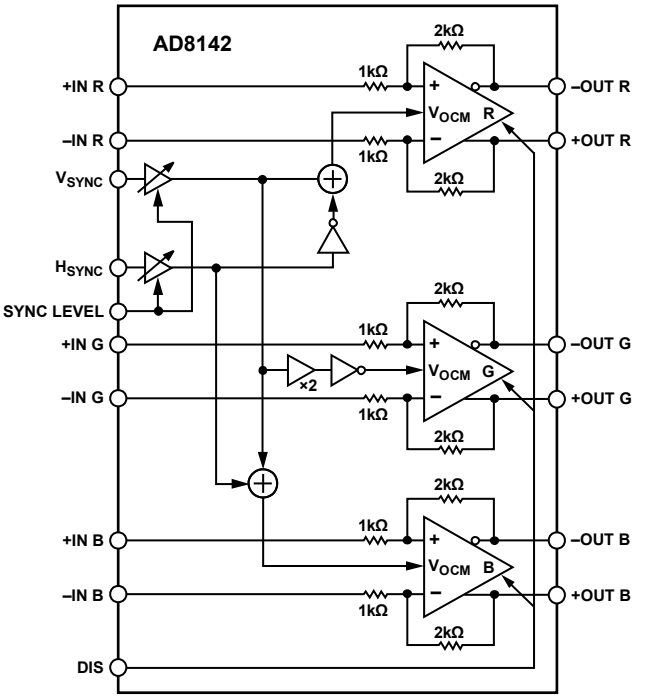


Figure 46. Driving Four UTP Cables in Parallel

VIDEO SYNC-ON-COMMON-MODE (AD8142)

In computer video applications, the horizontal and vertical sync signals are most often separate from the video information signals. For example, in typical computer monitor applications, the red, green, and blue (RGB) color signals are transmitted over separate cables, as are the vertical and horizontal sync signals. When transmitting these types of video signals over long distances on UTP cable, it is desirable to reduce the required number of physical channels. One way to do this is to encode the vertical and horizontal sync signals as weighted sums and differences of the output common-mode signals. The RGB color signals are each transmitted differentially over separate physical channels. The fact that the differential and common-mode signals are orthogonal allows the RGB color and sync signals to be separated at the channel's receiver.

Cat-5 type cable contains four balanced twisted-pair physical channels that can support both differential and common-mode signals. Transmitting typical computer monitor video over this cable can be accomplished by using three of the twisted pairs for the RGB and sync signals. Each color is transmitted differentially, one on each of the three pairs. The encoded sync signals are transmitted among the common-mode signals of each of the three pairs. To minimize EMI from the sync signals, the common-mode signals on each of the three pairs produced by the sync encoding scheme induce electric and magnetic fields that, for the most part, cancel each other. A conceptual block diagram of the sync encoding scheme is presented in Figure 47. Because the AD8142 has the sync encoding scheme implemented internally, the user simply applies the horizontal and vertical sync signals directly to the appropriate inputs. As described in the Theory of Operation section, the AD8142 accepts ground-referenced logic-level sync pulses (see Table 1 for the exact levels). In many cases, the sync pulses can be applied directly from video card VGA connector outputs.



V_{OCM} WEIGHTING EQUATIONS ON +5V SUPPLY:

RED $V_{OCM} = \frac{K}{2}(V_{SYNC} - H_{SYNC}) + 1.5V$

GREEN $V_{OCM} = \frac{K}{2}(-2V_{SYNC}) + 1.5V$

BLUE $V_{OCM} = \frac{K}{2}(V_{SYNC} + H_{SYNC}) + 1.5V$

Figure 47. AD8142 Conceptual Sync-On-Common-Mode Encoding Scheme

The transmitted common-mode sync signal magnitudes are scaled by applying a dc voltage to the SYNC LEVEL input, referenced to the negative supply. The difference between the voltage applied to the SYNC LEVEL input and the negative supply sets the peak deviation of the encoded sync signals about the midsupply common-mode voltage. For example, with the SYNC LEVEL input set at V_{S-} + 500 mV, the deviation of the encoded sync pulses about the nominal midsupply common-mode voltage is nominally ±500 mV. The equations in Figure 47 describe how the V_{SYNC} and H_{SYNC} signals are encoded on each color's midsupply common-mode signal. In these equations, the weights of the V_{SYNC} and H_{SYNC} signals are ±1 (that is, +1 for high, −1 for low), and the constant, K, is equal to the peak deviation of the encoded sync signals.

Figure 48 shows how the sync signals appear on each common-mode voltage in a single 5 V supply application when the voltage applied to the SYNC LEVEL input is set to V_{S-} + 500 mV. Although the typical setting for the SYNC LEVEL voltage is 500 mV above the negative supply, it can be increased, if necessary, in extremely noisy environments. Increasing the SYNC LEVEL voltage too much has the potential to produce excessive EMI.

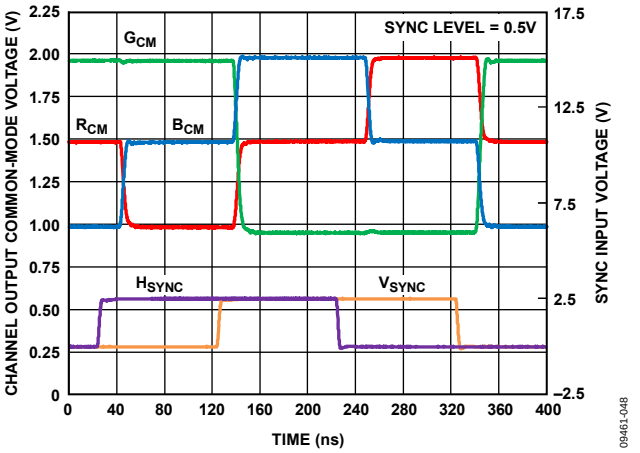


Figure 48. AD8142 Sync-On-Common-Mode Signals in Single 5 V Application

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

When designing with the AD8141 and AD8142, adhere to standard high speed printed circuit board (PCB) layout practices. A solid ground plane is recommended and good wideband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

AMPLIFIER-TO-AMPLIFIER ISOLATION

The least amount of isolation between the three AD8142 amplifiers exists between the green and red channels (Amplifier A and Amplifier B for the AD8141). This is, therefore, viewed as the worst-case isolation, which is reflected in Table 1 and the Theory of Operation section.

EXPOSED PADDLE (EPAD)

The 24-lead LFCSP package has an exposed paddle on the underside of its body. To achieve the specified thermal resistance, it must have a good thermal connection to one of the PCB planes. The exposed paddle must be soldered to a pad on top of the board that is connected with several thermal vias to a ground plane.

TYPICAL AD8142 5 V APPLICATION CIRCUIT

Figure 49 illustrates a typical AD8142 application circuit on a single 5 V supply.

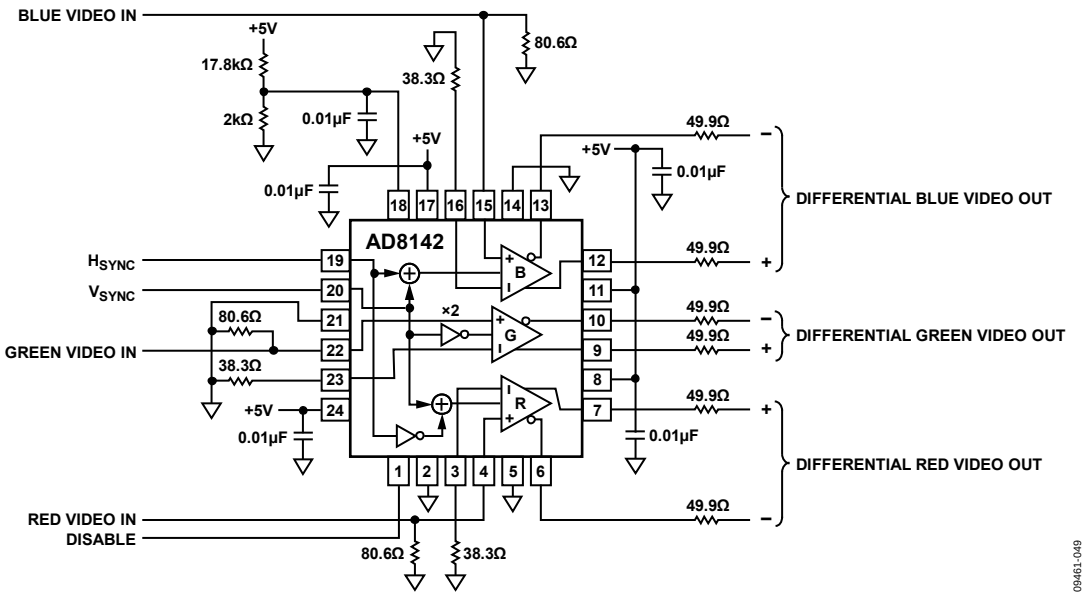
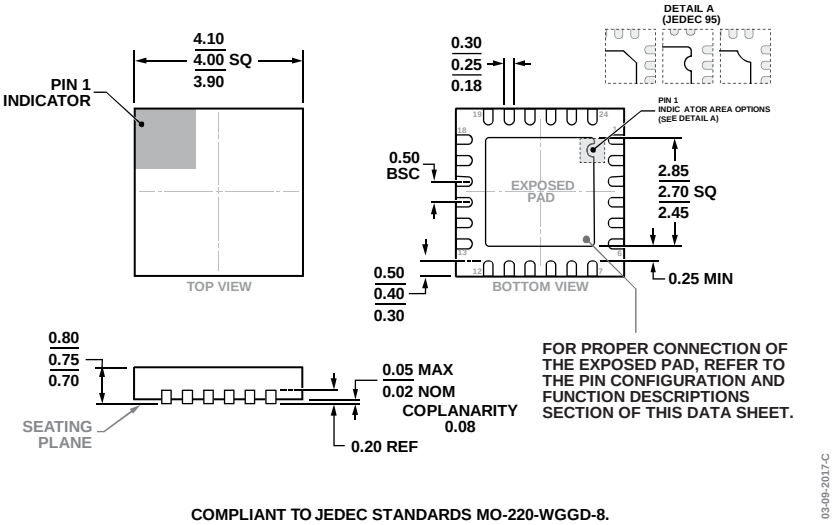


Figure 49. Typical AD8142 Application Circuit on a Single 5 V Supply

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 50. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Option
AD8141ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
AD8141ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
AD8141ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
AD8142ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
AD8142ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8
AD8142ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-8

[1] Z = RoHS Compliant Part.

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