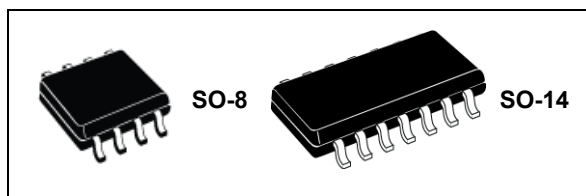


## High voltage high and low-side 2 A gate driver

Datasheet - production data



### Features

- Transient withstand voltage 600 V
- $dV/dt$  immunity  $\pm 50$  V/ns in full temperature range
- Driver current capability:
  - 2 A source typ. at 25 °C
  - 2.5 A sink typ. at 25 °C
- Short propagation delay: 85 ns
- Switching times 25 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Interlocking function
- UVLO on both high-side and low-side sections
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

### Applications

- Motor driver for home appliances, factory automation, industrial drives and fans
- HID ballasts
- Power supply units
- DC-DC converters
- Induction heating
- Wireless chargers
- Industrial inverters
- UPS
- Welding

### Description

The L6498 is a high voltage device manufactured with the BCD6 “OFF-LINE” technology. It is a single chip half-bridge gate driver for the N-channel power MOSFET or IGBT.

The high-side (floating) section is designed to stand a DC voltage rail up to 500 V, with 600 V transient withstand voltage. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing control units such as microcontrollers or DSP.

Both device outputs can sink 2.5 A and source 2 A, making the L6498 particularly suited for medium and high capacity power MOSFETs\IGBTs.

The outputs cannot be simultaneously driven high thanks to an integrated interlocking function.

The independent UVLO protection circuits present on both the lower and upper driving sections prevent the power switches from being operated in low efficiency or dangerous conditions.

The integrated bootstrap diode as well as all of the integrated features of this driver make the application PCB design simpler and more compact, and help to reduce the overall bill of material.

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# 1 Block diagrams

Figure 1. Block diagram SO-8

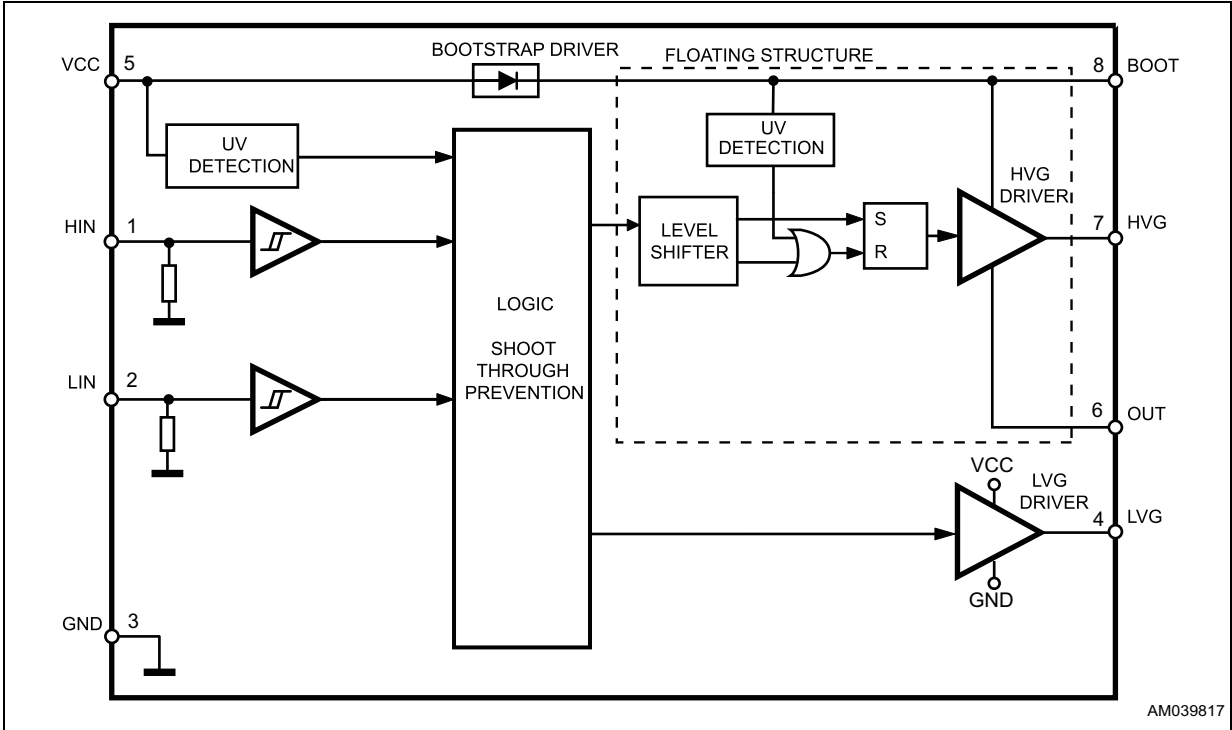
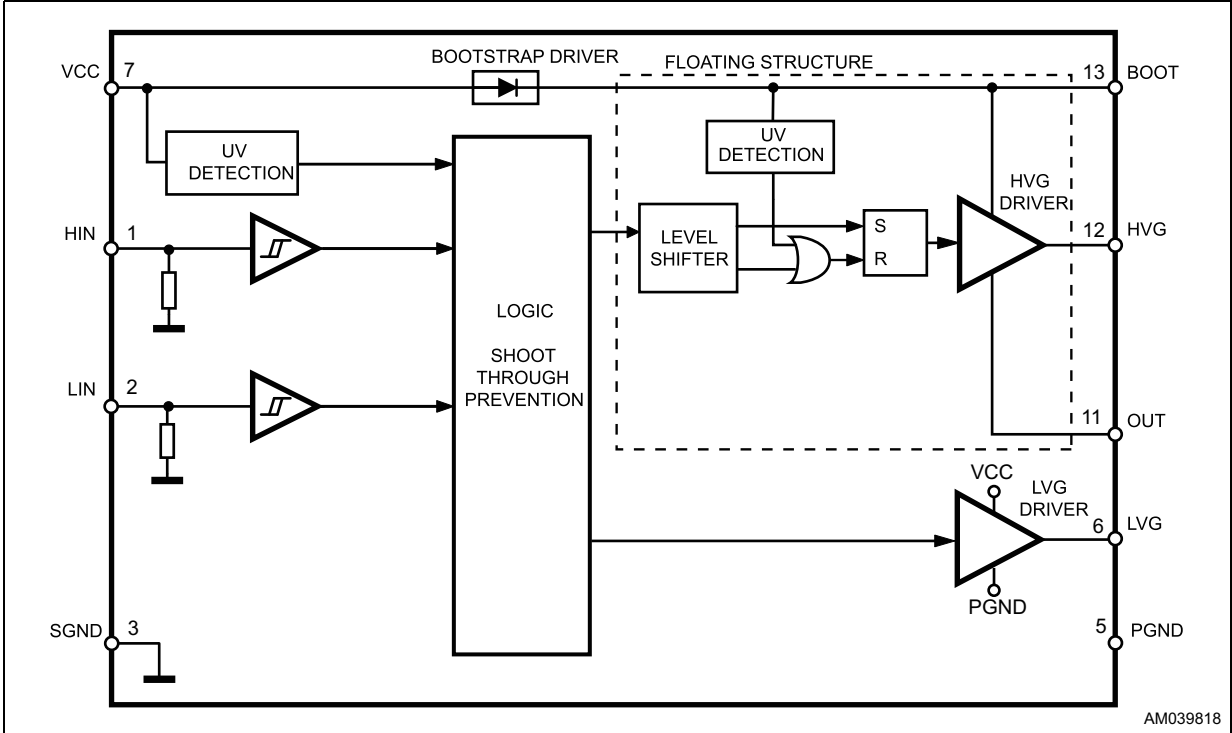


Figure 2. Block diagram SO-14



## 2 Pin description and connection diagram

Figure 3. Pin connection SO-8 (top view)

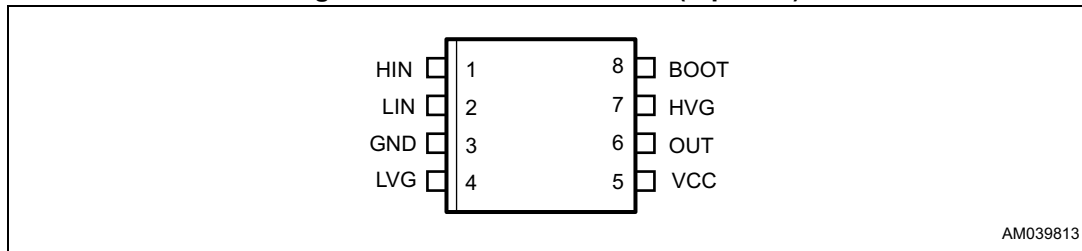


Figure 4. Pin connection SO-14 (top view)

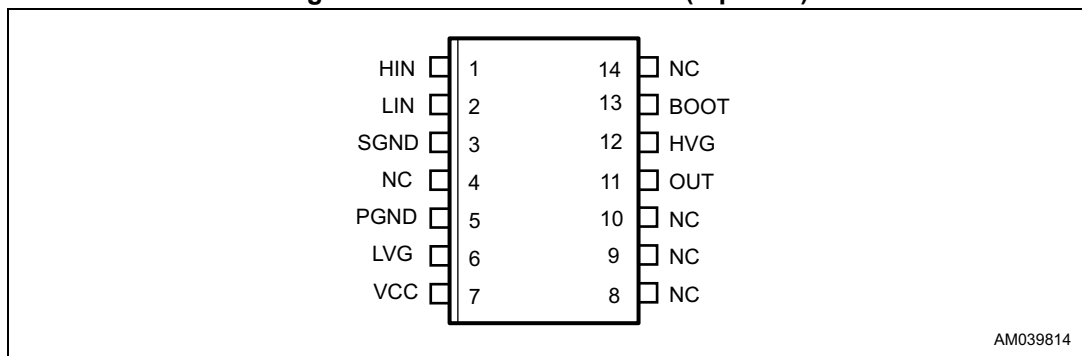


Table 1. Pin description

| Pin no. |                 | Pin name           | Type | Function                                   |
|---------|-----------------|--------------------|------|--------------------------------------------|
| SO-8    | SO-14           |                    |      |                                            |
| 1       | 1               | HIN                | I    | High-side driver logic input (active high) |
| 2       | 2               | LIN                | I    | Low-side driver logic input (active high)  |
| 3       | -               | GND                | P    | Device ground                              |
| 4       | 6               | LVG <sup>(1)</sup> | O    | Low-side driver output                     |
| 5       | 7               | VCC                | P    | Lower section supply voltage               |
| 6       | 11              | OUT                | P    | High-side (floating) common voltage        |
| 7       | 12              | HVG <sup>(1)</sup> | O    | High-side driver output                    |
| 8       | 13              | BOOT               | P    | Bootstrapped supply voltage                |
| -       | 3               | SGND               | P    | Signal ground                              |
| -       | 5               | PGND               | P    | Power ground                               |
| -       | 4, 8, 9, 10, 14 | NC                 | -    | Not connected                              |

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at  $I_{\text{sink}} = 10 \text{ mA}$ ), with  $V_{\text{CC}} > 3 \text{ V}$ . This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

### 3 Electrical data

#### 3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings<sup>(1)</sup>

| Symbol        | Parameter                                                      | Value           |                  | Unit |
|---------------|----------------------------------------------------------------|-----------------|------------------|------|
|               |                                                                | Min.            | Max.             |      |
| $V_{CC}$      | Supply voltage                                                 | -0.3            | 21               | V    |
| $V_{PGND}$    | Low-side driver ground                                         | $V_{CC} - 21$   | $V_{CC} + 0.3$   | V    |
| $V_{OUT}$     | Output voltage                                                 | $V_{BOOT} - 21$ | $V_{BOOT} + 0.3$ | V    |
| $V_{BOOT}$    | Boot DC voltage                                                | -0.3            | 500              | V    |
|               | Boot transient withstand voltage ( $T_{pulse} < 1\text{ ms}$ ) | -               | 620              | V    |
| $V_{hvg}$     | High-side gate output voltage                                  | $V_{OUT} - 0.3$ | $V_{BOOT} + 0.3$ | V    |
| $V_{lvg}$     | Low-side gate output voltage                                   | (P)GND - 0.3    | $V_{CC} + 0.3$   | V    |
| $V_i$         | Logic input pins voltage                                       | -0.3            | 15               | V    |
| $dV_{OUT}/dt$ | Allowed output slew rate                                       | -               | 50               | V/ns |
| $P_{TOT}$     | Total power dissipation ( $T_A = 25\text{ °C}$ ) SO-14         | -               | 1                | W    |
| $T_J$         | Junction temperature                                           | -               | 150              | °C   |
| $T_{stg}$     | Storage temperature                                            | -50             | 150              | °C   |
| ESD           | Human body model                                               | 2               |                  | kV   |

1. Each voltage referred to GND\SGND unless otherwise specified.

#### 3.2 Thermal data

Table 3. Thermal data

| Symbol       | Parameter                              | Package | Value | Unit |
|--------------|----------------------------------------|---------|-------|------|
| $R_{th(JA)}$ | Thermal resistance junction to ambient | SO-8    | 185   | °C/W |
|              |                                        | SO-14   | 120   |      |

### 3.3 Recommended operating conditions

Table 4. Recommended operating conditions

| Symbol         | Pin         | Parameter                          | Test condition                    | Min.              | Max. | Unit |
|----------------|-------------|------------------------------------|-----------------------------------|-------------------|------|------|
| $V_{CC}$       | VCC         | Supply voltage                     | -                                 | 10                | 20   | V    |
| $V_{PS}^{(1)}$ | SGND - PGND | Low-side driver ground             | -                                 | -5                | +5   | V    |
| $V_{BO}^{(2)}$ | BOOT - OUT  | Floating supply voltage            | -                                 | 9.3               | 20   | V    |
| $V_{OUT}$      | OUT         | DC output voltage                  | -                                 | -9 <sup>(3)</sup> | 480  | V    |
|                |             | OUT transient withstand voltage    | $T_{pulse} < 1\text{ ms}$         | -                 | 600  | V    |
| $f_{SW}$       | -           | Maximum switching frequency        | HVG, LVG load $C_L = 1\text{ nF}$ | -                 | 800  | kHz  |
| $T_J$          | -           | Junction temperature               | -                                 | -40               | 125  | °C   |
| $T_A$          | -           | Ambient temperature <sup>(4)</sup> | -                                 | -40               | 125  | °C   |

1.  $V_{PS} = V_{PGND} - SGND$ .

2.  $V_{BO} = V_{BOOT} - V_{OUT}$ .

3. LVG off.  $V_{CC} = 12.5\text{ V}$ . Logic is operational if  $V_{BOOT} > 5\text{ V}$ .

4. Maximum ambient temperature is actually limited by  $T_J$ .

## 4 Electrical characteristics

Table 5. Electrical characteristics ( $V_{CC} = 15\text{ V}$ ;  $T_J = +25\text{ °C}$ ;  $PGND = SGND$ )

| Symbol                                           | Pin                    | Parameter                                      | Test condition                                                  | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|------------------------|------------------------------------------------|-----------------------------------------------------------------|------|------|------|------|
| Low-side section supply                          |                        |                                                |                                                                 |      |      |      |      |
| V <sub>CC_hys</sub>                              | VCC vs.<br>(S)GND      | V <sub>CC</sub> UV hysteresis                  | -                                                               | 0.5  | 0.6  | 0.72 | V    |
| V <sub>CC_thON</sub>                             |                        | V <sub>CC</sub> UV turn ON threshold           | -                                                               | 8.7  | 9.3  | 9.8  | V    |
| V <sub>CC_thOFF</sub>                            |                        | V <sub>CC</sub> UV turn OFF threshold          | -                                                               | 8.2  | 8.7  | 9.2  | V    |
| I <sub>QCCU</sub>                                |                        | Undervoltage quiescent supply current          | V <sub>CC</sub> = 7 V<br>LIN = GND; HIN = GND                   | -    | 160  | 210  | μA   |
| I <sub>QCC</sub>                                 |                        | Quiescent current                              | V <sub>CC</sub> = 15 V<br>LIN = 5 V; HIN = GND                  | -    | 340  | 480  | μA   |
| High-side floating section supply <sup>(1)</sup> |                        |                                                |                                                                 |      |      |      |      |
| V <sub>BO_hys</sub>                              | BOOT vs.<br>OUT        | V <sub>BO</sub> UV hysteresis                  | -                                                               | 0.48 | 0.6  | 0.7  | V    |
| V <sub>BO_thON</sub>                             |                        | V <sub>BO</sub> UV turn ON threshold           | -                                                               | 8.0  | 8.6  | 9.1  | V    |
| V <sub>BO_thOFF</sub>                            |                        | V <sub>BO</sub> UV turn OFF threshold          | -                                                               | 7.5  | 8.0  | 8.5  | V    |
| I <sub>QBOU</sub>                                |                        | Undervoltage V <sub>BO</sub> quiescent current | V <sub>BO</sub> = 7 V<br>LIN = GND; HIN = 5 V                   | -    | 20   | 30   | μA   |
| I <sub>QBO</sub>                                 |                        | V <sub>BO</sub> quiescent current              | V <sub>BO</sub> = 15 V<br>LIN = GND; HIN = 5 V                  | -    | 90   | 120  | μA   |
| I <sub>LK</sub>                                  | -                      | High voltage leakage current                   | V <sub>hvg</sub> = V <sub>OUT</sub> = V <sub>BOOT</sub> = 600 V | -    | -    | 8    | μA   |
| R <sub>DS(on)</sub>                              | -                      | Bootstrap diode on resistance <sup>(2)</sup>   | -                                                               | -    | 175  | -    | Ω    |
| Output driving buffers                           |                        |                                                |                                                                 |      |      |      |      |
| I <sub>so</sub>                                  | LVG, HVG               | High/low-side source short-circuit current     | LVG/HVG ON<br>T <sub>J</sub> = 25 °C                            | 1.7  | 2    | -    | A    |
|                                                  |                        |                                                | Full temperature range                                          | 1.4  | -    | -    | A    |
| I <sub>si</sub>                                  |                        | High/low-side sink short-circuit current       | LVG/HVG ON<br>T <sub>J</sub> = 25 °C                            | 2    | 2.5  | -    | A    |
|                                                  |                        |                                                | Full temperature range                                          | 1.55 | -    | -    | A    |
| Logic inputs                                     |                        |                                                |                                                                 |      |      |      |      |
| V <sub>il</sub>                                  | LIN, HIN<br>vs. (S)GND | Low level logic threshold voltage              | -                                                               | 0.95 | -    | 1.45 | V    |
| V <sub>ih</sub>                                  |                        | High level logic threshold voltage             | -                                                               | 2    | -    | 2.5  | V    |
| I <sub>HINh</sub>                                | HIN vs.<br>(S)GND      | HIN logic “1” input bias current               | HIN = 15 V                                                      | 120  | 200  | 260  | μA   |
| I <sub>HINI</sub>                                |                        | HIN logic “0” input bias current               | HIN = 0 V                                                       | -    | -    | 1    | μA   |
| I <sub>LINI</sub>                                | LIN vs.<br>(S)GND      | LIN logic “1” input bias current               | LIN = 15 V                                                      | 120  | 200  | 260  | μA   |
| I <sub>LINh</sub>                                |                        | LIN logic “0” input bias current               | LIN = 0 V                                                       | -    | -    | 1    | μA   |

Table 5. Electrical characteristics ( $V_{CC} = 15\text{ V}$ ;  $T_J = +25\text{ }^{\circ}\text{C}$ ; PGND = SGND (continued))

| Symbol                                        | Pin                    | Parameter                                               | Test condition                                                                                                 | Min. | Typ. | Max. | Unit      |
|-----------------------------------------------|------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------|------|------|-----------|
| $R_{PD}$                                      | LIN, HIN<br>vs. (S)GND | Logic inputs pull-down resistor                         | -                                                                                                              | 58   | 75   | 125  | $k\Omega$ |
| <b>Dynamic characteristics (see Figure 5)</b> |                        |                                                         |                                                                                                                |      |      |      |           |
| $t_{on}$                                      | HIN vs.<br>HVG;        | High/low-side driver turn-on<br>propagation delay       | $V_{OUT} = 0\text{ V}$ ;<br>$V_{BOOT} = V_{CC}$ ;<br>$C_L = 1\text{ nF}$ ;<br>$V_i = 0\text{ to }3.3\text{ V}$ | -    | 85   | 120  | ns        |
| $t_{off}$                                     | LIN vs.<br>LVG         | High/low-side driver turn-off<br>propagation delay      |                                                                                                                | -    | 85   | 120  | ns        |
| MT                                            | -                      | Delay matching, HS and LS<br>turn-on/off <sup>(3)</sup> | -                                                                                                              | -    | -    | 30   | ns        |
| $t_r$                                         | LVG, HVG               | Rise time                                               | $C_L = 1\text{ nF}$                                                                                            | -    | 25   | -    | ns        |
| $t_f$                                         |                        | Fall time                                               | $C_L = 1\text{ nF}$                                                                                            | -    | 25   | -    | ns        |

1.  $V_{BO} = V_{BOOT} - V_{OUT}$ .

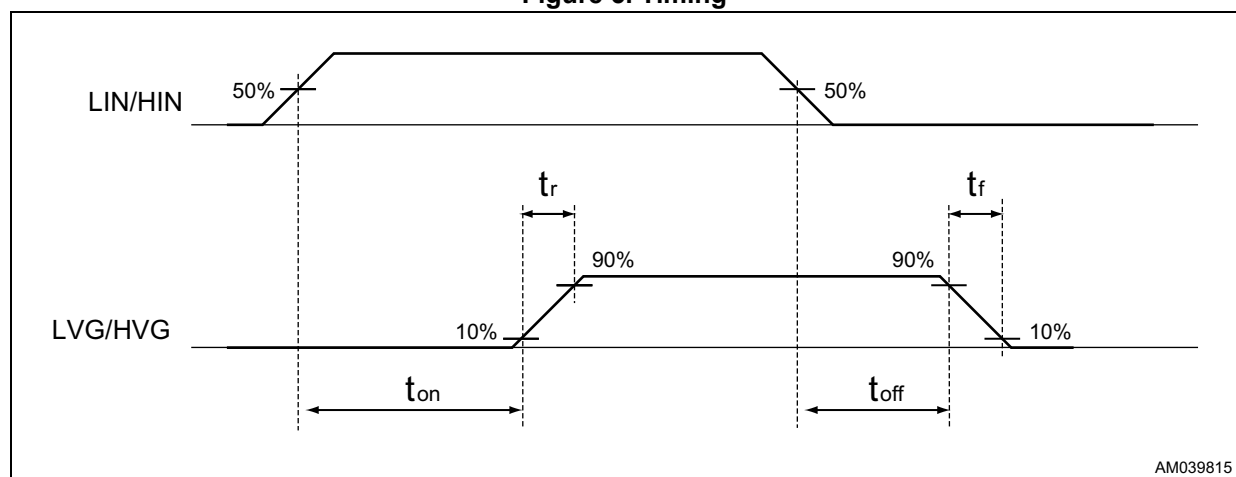
2.  $R_{DSON}$  is tested in the following way:

$$R_{DSON} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})]$$

where  $I_1$  is BOOT pin current when  $V_{BOOT} = V_{BOOT1}$ ,  $I_2$  when  $V_{BOOT} = V_{BOOT2}$ .

3.  $MT = \max. (|t_{on}(LVG) - t_{off}(LVG)|, |t_{on}(HVG) - t_{off}(HVG)|, |t_{off}(LVG) - t_{on}(HVG)|, |t_{off}(HVG) - t_{on}(LVG)|)$ .

Figure 5. Timing





## 5 Truth table

Table 6. Truth table

| Input |     | Output           |                  |
|-------|-----|------------------|------------------|
| LIN   | HIN | LVG              | HVG              |
| L     | L   | L                | L                |
| L     | H   | L                | H                |
| H     | L   | H                | L                |
| H     | H   | L <sup>(1)</sup> | L <sup>(1)</sup> |

1. Interlocking function.

# 6 Typical application diagram

Figure 6. Typical application diagram

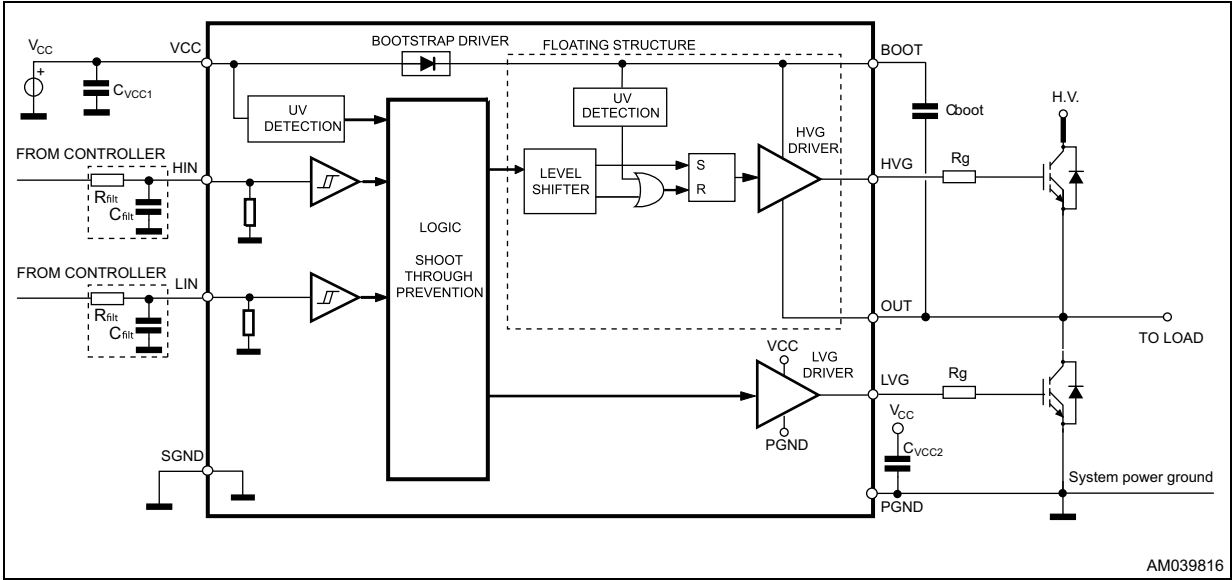


Figure 7. Suggested PCB layout (SO-8)

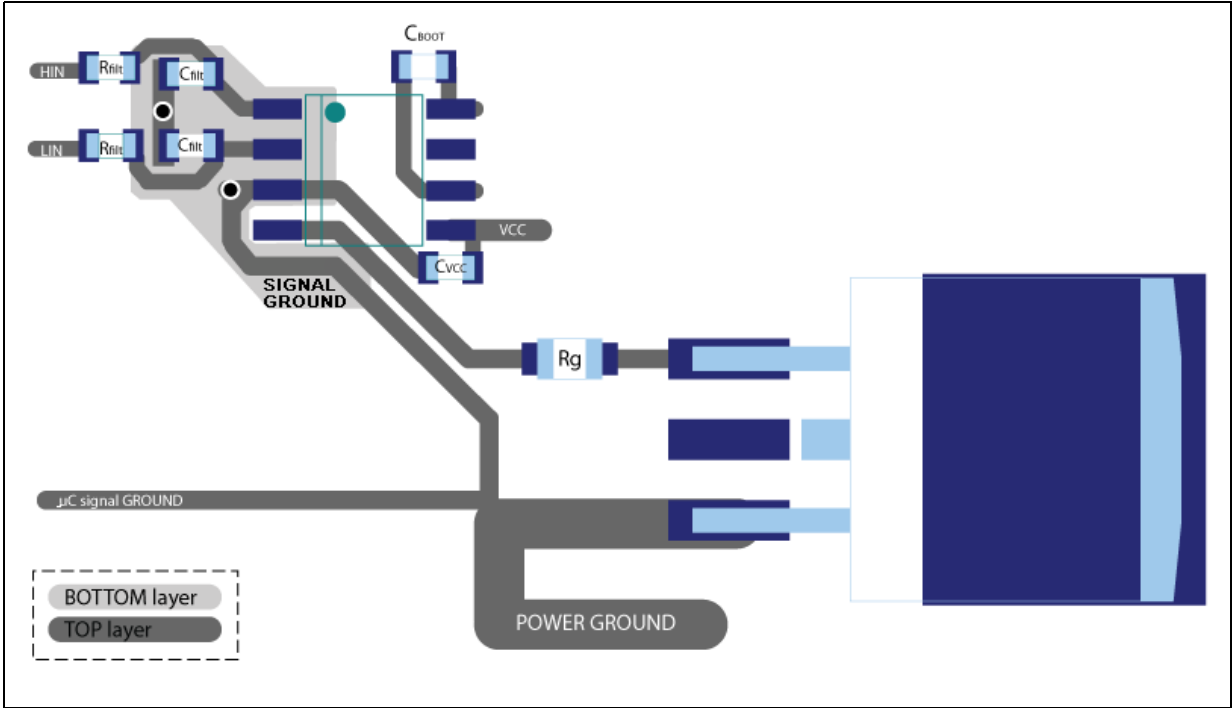
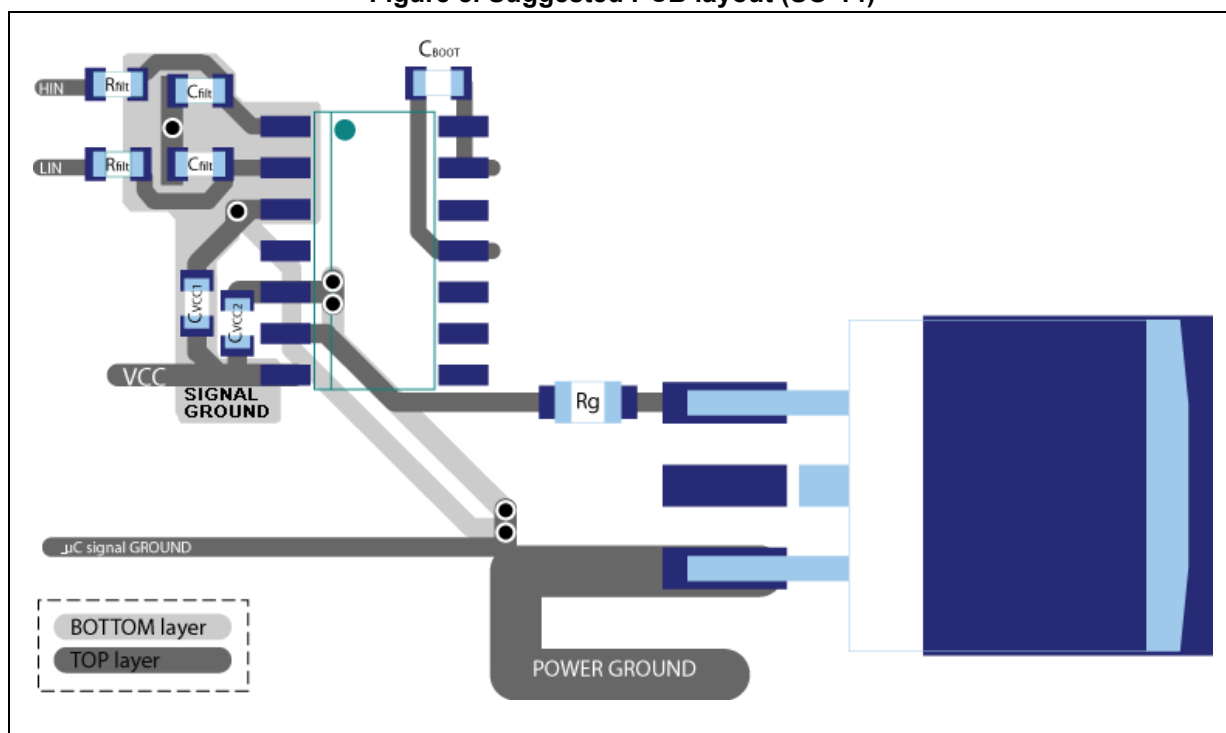


Figure 8. Suggested PCB layout (SO-14)



## 7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode ([Figure 9](#)). In the L6498 an integrated structure replaces the external diode.

### C<sub>BOOT</sub> selection and charging

To choose the proper C<sub>BOOT</sub> value the external MOS can be seen as an equivalent capacitor. This capacitor C<sub>EXT</sub> is related to the MOS total gate charge:

#### Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C<sub>EXT</sub> and C<sub>BOOT</sub> is proportional to the cyclical voltage loss. It has to be:

#### Equation 2

$$C_{BOOT} \gg C_{EXT}$$

if Q<sub>gate</sub> is 30 nC and V<sub>gate</sub> is 10 V, C<sub>EXT</sub> is 3 nF. With C<sub>BOOT</sub> = 100 nF the drop is 300 mV.

If HVG has to be supplied for a long time, the C<sub>BOOT</sub> selection has also to take into account the leakage and quiescent losses.

HVG steady-state consumption is lower than 120 μA, so if HVG T<sub>ON</sub> is 5 ms, C<sub>BOOT</sub> has to supply 0.6 μC. This charge on a 1 μF capacitor means a voltage drop of 0.6 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V<sub>OUT</sub> is close to SGND (or lower) and in the meanwhile the LVG is on. The charging time (T<sub>charge</sub>) of the C<sub>BOOT</sub> is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R<sub>DS(on)</sub> (typical value: 175 Ω). At low frequency this drop can be neglected. Anyway, the rise of frequency has to take into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

#### Equation 3

$$V_{drop} = I_{charge} R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

where Q<sub>gate</sub> is the gate charge of the external power MOS, R<sub>DS(on)</sub> is the on resistance of the bootstrap DMOS and T<sub>charge</sub> is the charging time of the bootstrap capacitor.

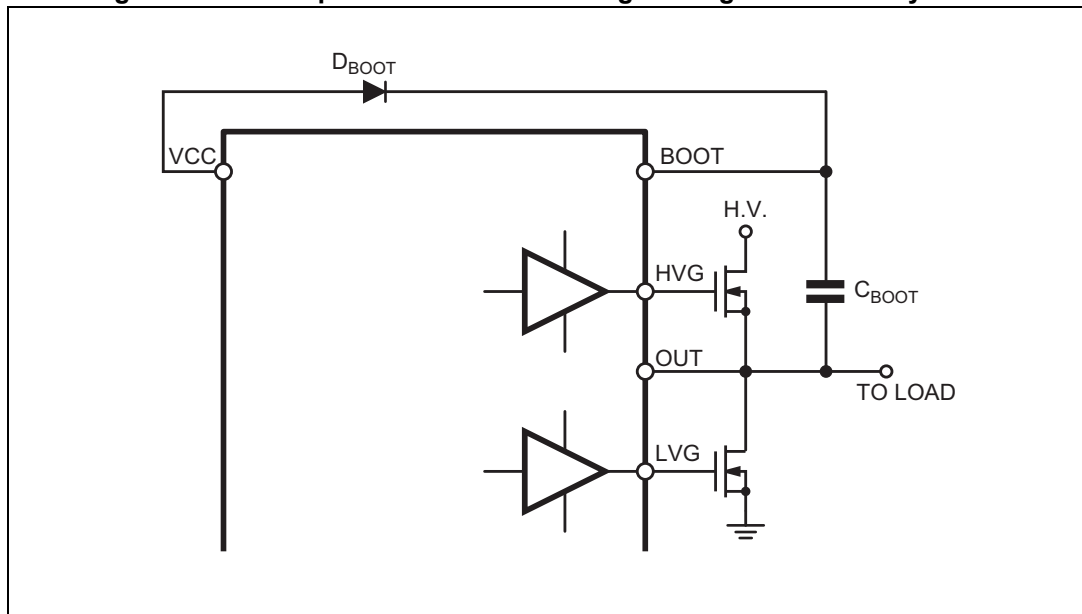
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the  $T_{\text{charge}}$  is 5  $\mu\text{s}$ . In fact:

**Equation 4**

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 175\Omega \sim 1\text{V}$$

$V_{\text{drop}}$  has to be taken into account when the voltage drop on  $C_{\text{BOOT}}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

**Figure 9. Bootstrap driver with external high voltage fast recovery diode**



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 8.1 SO-8 package information

Figure 10. SO-8 package outline

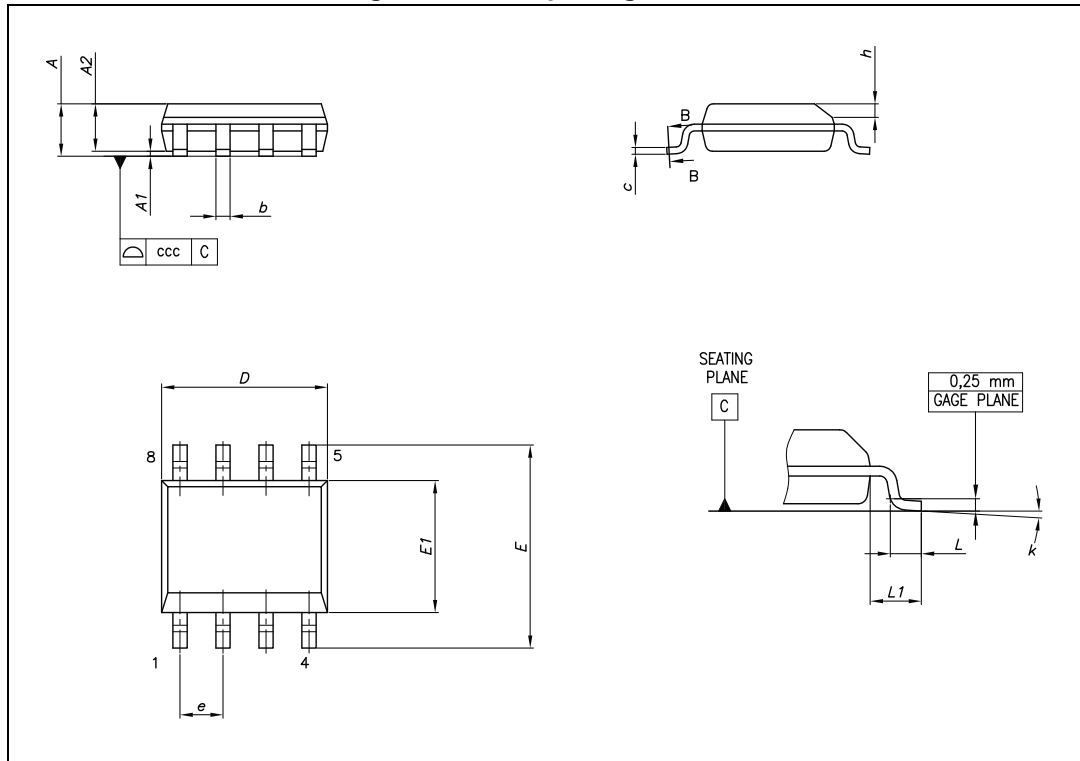
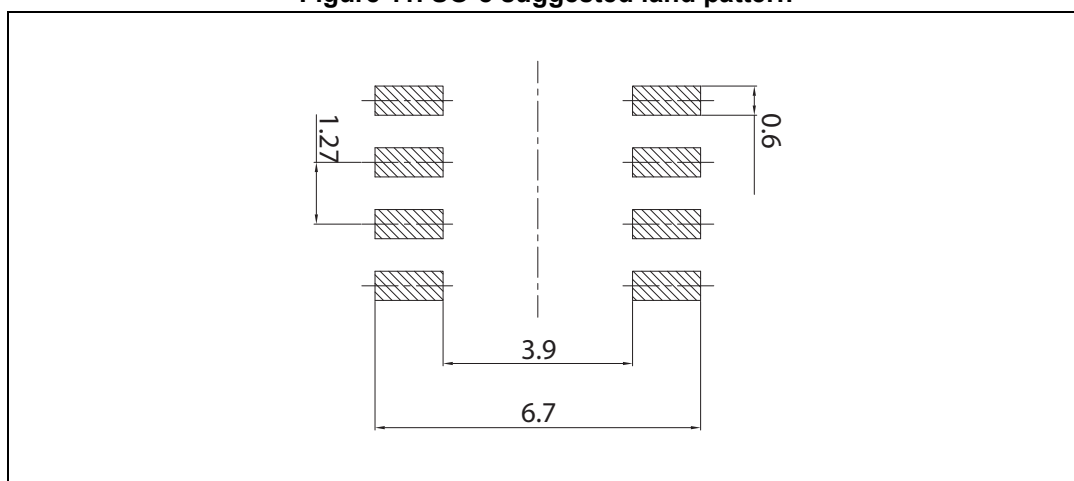


Table 7. SO-8 package mechanical data

| Symbol | Dimensions (mm) |      |      | Notes   |
|--------|-----------------|------|------|---------|
|        | Min.            | Typ. | Max. |         |
| A      | -               | -    | 1.75 | -       |
| A1     | 0.10            | -    | 0.25 | -       |
| A2     | 1.25            | -    | -    | -       |
| b      | 0.28            | -    | 0.48 | -       |
| c      | 0.17            | -    | 0.23 | -       |
| D      | 4.80            | 4.90 | 5.00 | -       |
| E      | 5.80            | 6.00 | 6.20 | -       |
| E1     | 3.80            | 3.90 | 4.00 | -       |
| e      | -               | 1.27 | -    | -       |
| h      | 0.25            | -    | 0.50 | -       |
| L      | 0.40            | -    | 1.27 | -       |
| L1     | -               | 1.04 | -    | -       |
| k      | 0               | -    | 8    | Degrees |
| ccc    | -               | -    | 0.10 | -       |

Figure 11. SO-8 suggested land pattern





## 8.2 SO-14 package information

Figure 12. SO-14 package outline

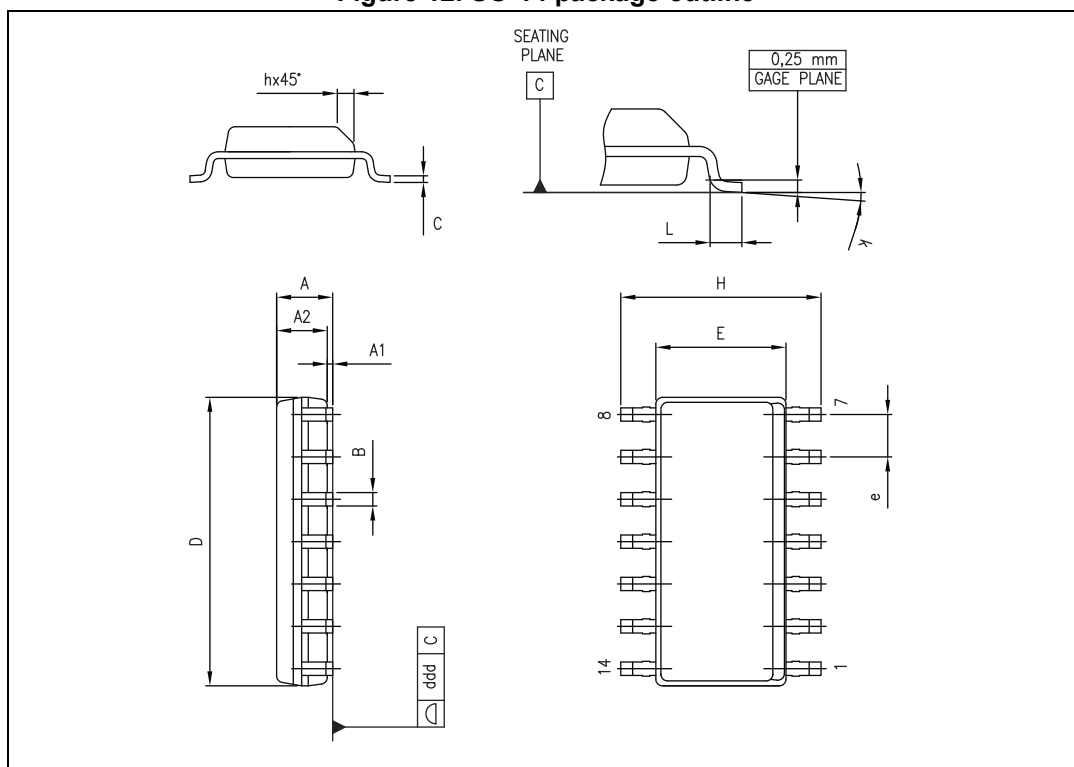
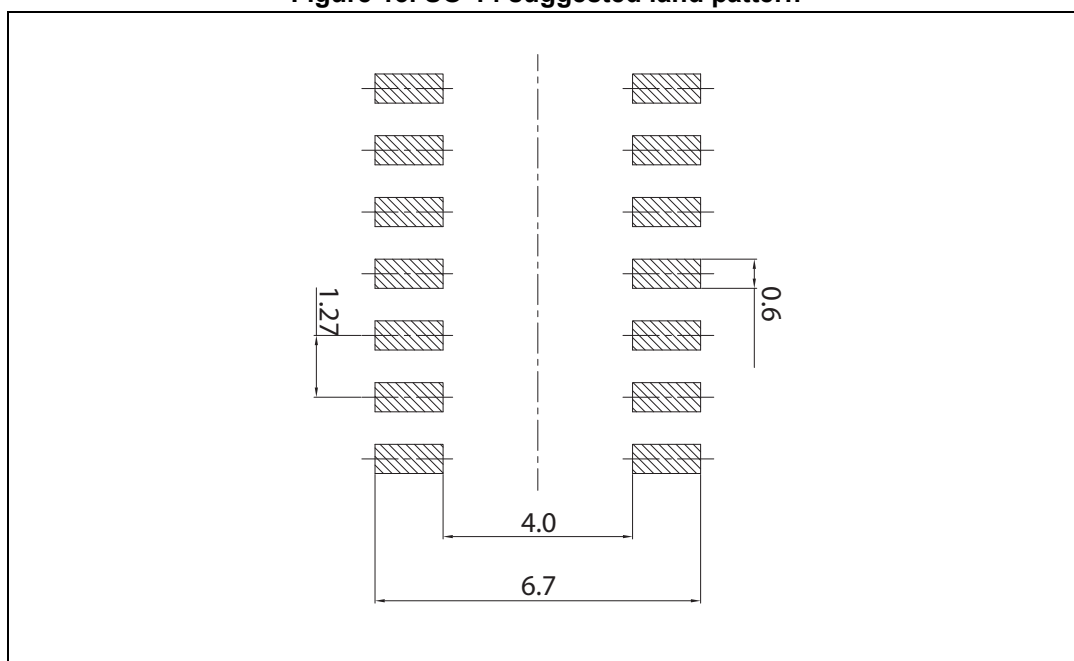


Table 8. SO-14 package mechanical data

| Symbol | Dimensions (mm) |      |      |
|--------|-----------------|------|------|
|        | Min.            | Typ. | Max. |
| A      | 1.35            | -    | 1.75 |
| A1     | 0.10            | -    | 0.25 |
| A2     | 1.10            | -    | 1.65 |
| B      | 0.33            | -    | 0.51 |
| C      | 0.19            | -    | 0.25 |
| D      | 8.55            | -    | 8.75 |
| E      | 3.80            | -    | 4.00 |
| e      | -               | 1.27 | -    |
| H      | 5.80            | -    | 6.20 |
| h      | 0               | -    | -    |
| 25     | -               | 0.50 | -    |
| L      | 0.40            | -    | 1.27 |
| k      | 0               | -    | 8    |
| ddd    | -               | -    | 0.10 |

Figure 13. SO-14 suggested land pattern



## 9 Ordering information

**Table 9. Device summary**

| Order code | Package | Packaging     |
|------------|---------|---------------|
| L6498D     | SO-8    | Tube          |
| L6498DTR   | SO-8    | Tape and reel |
| L6498LD    | SO-14   | Tube          |
| L6498LDTR  | SO-14   | Tape and reel |

## 10 Revision history

**Table 10. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                 |
|-------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 08-Feb-2017 | 1        | Initial release.                                                                                                                                                                                                                        |
| 26-Apr-2017 | 2        | Updated <i>Table 5 on page 7</i> (replaced “I <sub>NR_PD</sub> ” by “R <sub>PD</sub> ”, added Test condition to “t <sub>off</sub> ”).<br>Updated order codes in <i>Table 9 on page 19</i> .<br>Minor modifications throughout document. |
| 13-Sep-2017 | 3        | Updated <i>Table 4 on page 6</i> (added T <sub>A</sub> symbol and note <i>4.</i> ).                                                                                                                                                     |

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