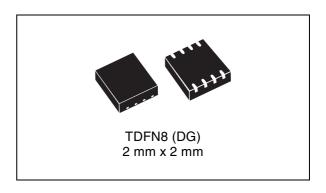


STM6520

Dual push-button Smart Reset[™] with push-button controlled output delay

Features

- Dual Smart ResetTM push-button inputs, with user-selectable extended reset setup delay (by two-state input logic): t_{SRC} = 6, 10 s (min.)
- Push-button controlled reset pulse duration (no fixed nor minimum pulse width guaranteed)
- No power-on reset
- Dual reset outputs
 - RST1 active-low, open-drain
 - RST2 active-high, push-pull
- Fixed Smart Reset[™] input logic voltage levels
- Broad operating voltage range 1.65 V to 5.5 V, inactive reset output levels valid down to 1.0 V
- Low supply current 1.5 µA
- Operating temperature: -30 °C to +85 °C
- TDFN8 package: 2 mm x 2 mm x 0.75 mm
- RoHS compliant



Applications

- Mobile phones, smartphones
- e-books
- MP3 players
- Games
- Portable navigation devices
- Any application that requires delayed reset push-button(s) response for improved system stability

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STM6520 Description

1 Description

The Smart ResetTM devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart ResetTM input delay time (t_{SRC}) and combined push-button inputs, which together ensures a safe reset and eliminates the need for a specific dedicated reset button.

This reset configuration provides versatility and allows the application to discriminate between a software generated interrupt and a hard system reset. When the input push-buttons are connected to microcontroller interrupt inputs, and are closed for a short time, the processor can only be interrupted. If the system still does not respond properly, continuing to keep the push-buttons closed for the extended setup time t_{SRC} causes a hard reset of the processor through the reset outputs.

The STM6520 has two combined delayed Smart ResetTM inputs ($\overline{SR0}$, $\overline{SR1}$) with two user-selectable delayed Smart ResetTM setup time (t_{SRC}) options of 7.5 s and 12.5 s typ., selected by a dual-state Smart ResetTM DSR input pin. When DSR is connected to ground, $t_{SRC} = 7.5$ s, when connected to V_{CC} , $t_{SRC} = 12.5$ s (typ.). There are two reset outputs, both going active simultaneously after both of the Smart ResetTM inputs were held active for the selected t_{SRC} delay time. The outputs remain asserted until either or both inputs go to inactive logic level (for this device the output reset pulse duration is fully push-button controlled, meaning neither fixed nor minimum reset pulse width, nor power-on reset pulse is implemented). The first reset output, $\overline{RST1}$, is active-low, open-drain; the second reset output, RST2, is active-high, push-pull. The device fully operates over a broad V_{CC} range 1.65 to 5.5 V. Below 1.575 V typ. the inputs are ignored and outputs are deasserted; the deasserted reset output levels are then valid down to 1.0 V.

Figure 1. Logic diagram

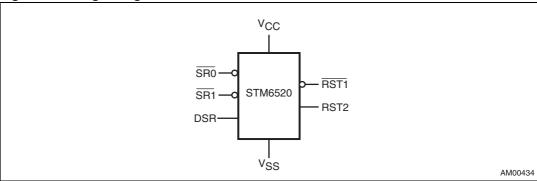
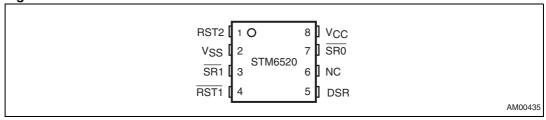


Figure 2. Pin connections



Device overview STM6520

2 Device overview

Table 1. Signal names

Symbol	Input/output	Description
RST1	Output	First reset output, active-low, open-drain.
RST2	Output	Second reset output, active-high, push-pull.
SR0	Input	Primary push-button Smart Reset™ input. Active-low.
SR1	Input	Secondary push-button Smart Reset™ input. Active-low.
DSR	Input	A dual-state Smart Reset TM input delay selection pin. When connected to ground, $t_{SRC} = 7.5 \text{ s}$; when connected to V_{CC} , $t_{SRC} = 12.5 \text{ s}$ (typ.). DSR is a DC-type input, intended to be either permanently grounded or permanently connected to V_{CC} .
V _{CC}	Supply voltage	Positive supply voltage for the device. A 0.1 μF decoupling ceramic capacitor is recommended to be connected between V_{CC} and V_{SS} pins.
V _{SS}	Supply ground	Ground
NC		No connect (not bonded; should be connected to V _{SS}).

STM6520 Pin descriptions

3 Pin descriptions

3.1 Power supply (V_{CC})

This pin is used to provide power to the Smart ResetTM device. A 0.1 μ F ceramic decoupling capacitor is recommended to be connected between the V_{CC} and V_{SS} pins, as close to the STM6520 device as possible.

3.2 Ground (V_{SS})

This is the ground pin for the device.

3.3 Smart Reset™ inputs (SR0, SR1)

Push-button Smart ResetTM inputs, active-low. Both inputs need to be asserted simultaneously for at least t_{SRC} to activate the reset outputs.

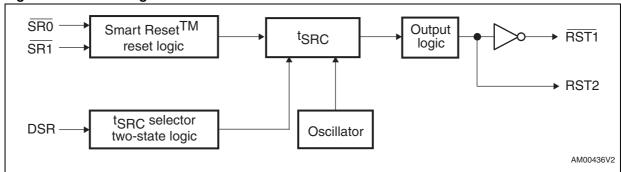
3.4 User-selectable Smart Reset™ delay (DSR)

An input that allows the user to program the setup time (t_{SRC}) for which both the push-buttons need to be pressed to activate the reset outputs. Controlled by different voltage levels on the DSR pin: when connected to ground, t_{SRC} = 7.5 s, when connected to V_{CC} , t_{SRC} = 12.5 s (typ.). DSR is a DC-type input, intended to be either permanently grounded or permanently connected to V_{CC} .

3.5 Reset outputs (RST1, RST2)

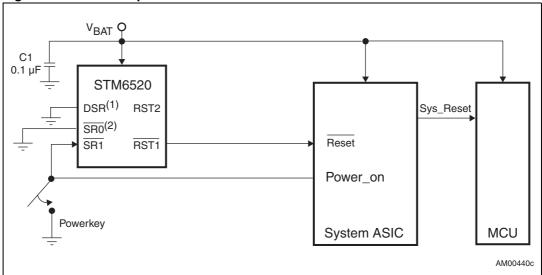
RST1 is active-low, open-drain, RST2 active-high, push-pull. Neither fixed nor minimum output reset pulse duration, nor power-on reset is implemented. Releasing any of the push-buttons while reset outputs are active, causes both outputs to deassert.

Figure 3. Block diagram



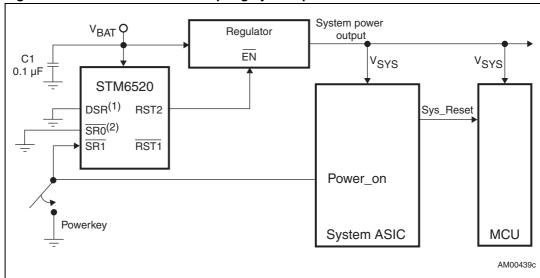
4 Typical application diagram

Figure 4. RST1 output used for microcontroller reset



- 1. DSR pin (pin 5) must be tied to V_{CC} or V_{SS} .
- 2. When only one Smart Reset $^{\text{TM}}$ input is used, connect the unused one permanently to V_{SS} .

Figure 5. RST2 used for interrupting system power



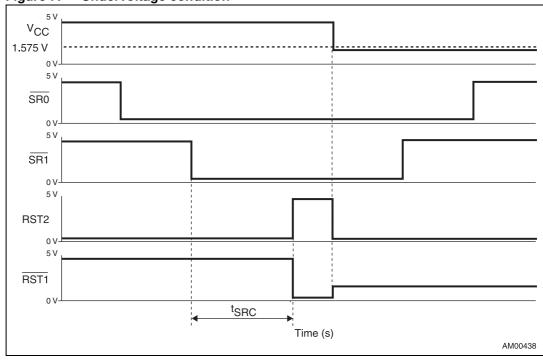
- 1. DSR pin (pin 5) must be tied to V_{CC} or V_{SS} .
- 2. When only one Smart Reset $^{\text{TM}}$ input is used, connect the unused one permanently to V_{SS} .

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1.65 V 1.65 V V_{BAT} 1.0 V 1.0 V Start End Push-button timer timer controlled output; N seconds SR0 Glitch t_{SRC} immunity SR1 RST1 RST2 AM00437

Figure 6. Timing waveforms





Note:

If undervoltage occurs (V_{CC} drops below 1.575 V typ.) while reset outputs are active, both outputs are released and go inactive.

5 Typical operating characteristics



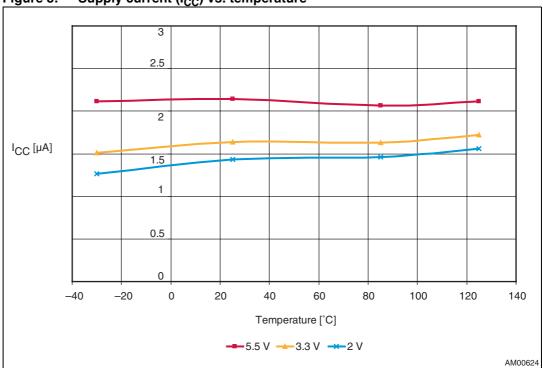
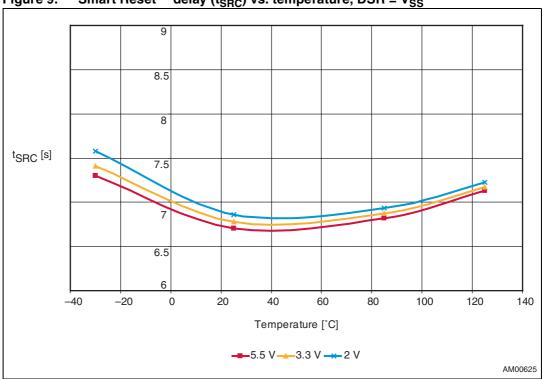


Figure 9. Smart ResetTM delay (t_{SRC}) vs. temperature, DSR = V_{SS}



STM6520 Maximum rating

6 Maximum rating

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit	
T _{STG}	Storage temperature (V _{CC} off)		-55 to +150	°C
T _{SLD} ⁽¹⁾	Lead solder temperature for 10 seconds	260	°C	
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
V _{IO}	Input or output voltage	-0.3 to 5.5 ⁽²⁾	V	
V _{CC}	Supply voltage	-0.3 to 7	٧	
ESD				
V _{HBM}	Electrostatic discharge protection, human body all pins (JESD22-A114-B level 2)	model,	2	kV
V _{RCDM}	Electrostatic discharge protection, charged dev all pins	1	kV	
V _{MM}	Electrostatic discharge protection, machine mo (JESD22-A115-A level A)	del, all pins	200	V
	Latch-up (V _{CC} pin, reset input pins)		EIA/JESD78	

^{1.} Reflow at peak temperature of 260 $^{\circ}$ C. The time above 255 $^{\circ}$ C must not exceed 30 seconds.

^{2.} For RST2 -0.3 to $V_{CC} + 0.3$ V only.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics table that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 3: Operating and measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and measurement conditions

Parameter	Value	Unit
V _{CC} supply voltage	1.65 to 5.5	V
Ambient operating temperature (T _A)	-30 to +85	°C
Input rise and fall times	≤5	ns
Input pulse voltages	0.2 to 0.8 V _{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V _{CC}	V

Figure 10. AC testing input/output waveforms



Table 4. DC and AC characteristics

Symbol	Parameter	Test conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V _{CC}	Supply voltage range	Operating voltage ⁽³⁾	1.65		5.5	V
		$V_{CC} = 3.0 \text{ V}, t_{SRC}$ counter is inactive		1.5	2.5	μΑ
1	Supply voltage	$V_{CC} = 5.0 \text{ V}, t_{SRC} \text{ counter is inactive}$		2.0	3.0	μΑ
I _{CC}	Supply vollage	V_{CC} = 3.0 V, t_{SRC} counter is active		3.5		μΑ
		$V_{CC} = 5.0 \text{ V}, t_{SRC} \text{ counter is active}$		4.7		μΑ
		$V_{CC} \ge 4.5 \text{ V, sinking } 3.2 \text{ mA}$			0.3	V
V_{OL}	Reset output voltage low	$V_{CC} \ge 3.3 \text{ V, sinking } 2.5 \text{ mA}$			0.3	V
		V _{CC} ≥ 1.65 V, sinking 1 mA			0.3	V
		$V_{CC} \ge 4.5 \text{ V}, I_{SOURCE} = 0.8 \text{ mA}$	0.8 V _{CC}			٧
V_{OH}	Reset output voltage high, RST2	$V_{CC} \ge 2.7 \text{ V, } I_{SOURCE} = 0.5 \text{ mA}$	0.8 V _{CC}			٧
		$V_{CC} \ge 1.65 \text{ V}, I_{SOURCE} = 0.25 \text{ mA}$	0.8 V _{CC}			٧
I_{LO}	Output leakage current, RST1	Open-drain, V _{RST1} = 5.5 V	-0.1		0.1	μΑ
Smart R	eset [™]					
+	Smart DagatTM dalay	DSR = V _{SS}	6	7.5	9	S
t _{SRC}	Smart Reset™ delay	DSR = V _{CC}	10	12.5	15	S
V _{IL}	SR0, SR1 input voltage low		V _{SS} - 0.3		0.3	V
V _{IH}	SR0, SR1 input voltage high		0.85		5.5	V
ILI	Input leakage current (SRO, SR1, DSR pins)		-1		1	μΑ
	Input glitch immunity ⁽⁴⁾	Corresponds to the actual t _{SRC}		t _{SRC}		S

^{1.} Valid for ambient operating temperature: $T_A = -30$ to +85 °C; $V_{CC} = 1.65$ to 5.5 V (except where noted).

^{2.} Typical value is at 25 $^{\circ}\text{C}$ and V_{CC} = 3.3 V unless otherwise noted.

^{3.} Reset outputs are deasserted below 1.575 V typ. and remain deasserted down to V_{CC} = 1 V.

^{4.} Input glitch immunity is equal to $t_{\mbox{\footnotesize SRC}}$ (when both SR inputs are low), otherwise infinite.

Package mechanical data 8

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

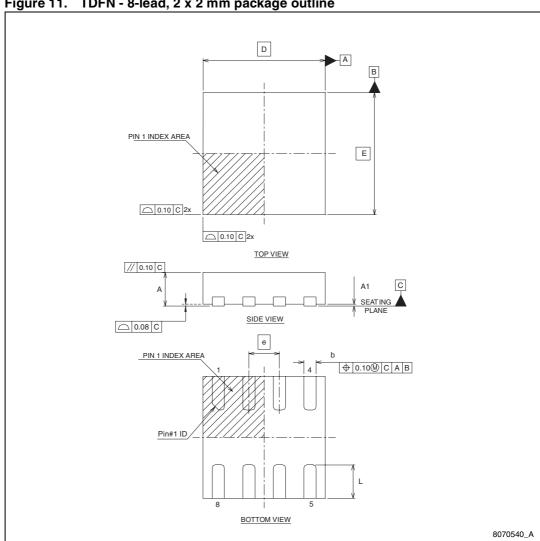


Figure 11. TDFN - 8-lead, 2 x 2 mm package outline

Table 5. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm package mechanical data

Cumbal	D	imension (mn	1)	Dimension (inches)			
Symbol	Min.	Nom.	Max.	Min.	Nom.	Max.	
А	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
b	0.15	0.20	0.25	0.006	0.008	0.010	
D BSC	1.9	2.00	2.1	0.075	0.079	0.083	
E BSC	1.9	2.00	2.1	0.075	0.079	0.083	
е		0.50			0.020		
L	0.45	0.55	0.65	0.018	0.022	0.026	

Package footprint STM6520

9 Package footprint

Figure 12. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

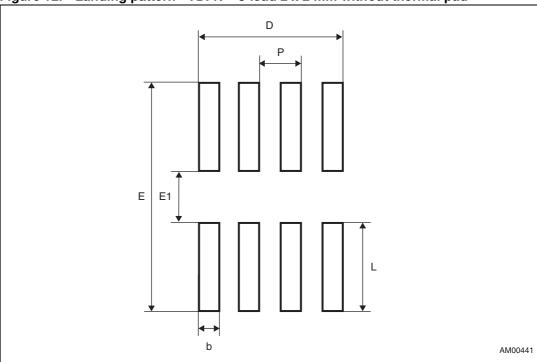


Table 6. Parameter for landing pattern - TDFN - 8-lead 2 x 2 mm package

Donomoton	Description	Dimension (mm)			
Parameter	Description	Min.	Nom.	Max.	
L	Contact length	1.05	_	1.15	
b	Contact width	0.25	_	0.30	
E	Max. land pattern Y-direction	_	2.85	_	
E1	Contact gap spacing	_	0.65	_	
D	Max. land pattern X-direction	_	1.75	_	
Р	Contact pitch	_	0.5	_	

10 Tape and reel information

Figure 13. Carrier tape

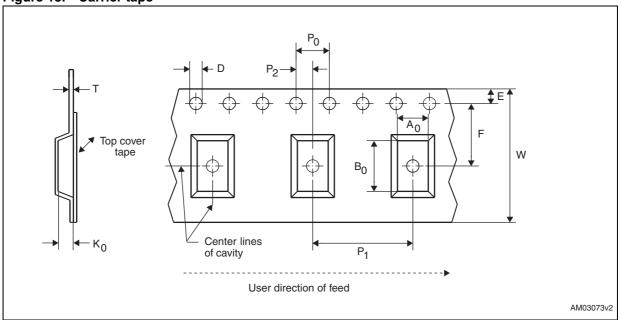


Table 7. Carrier tape dimensions

Package	W	D	E	P ₀	P ₂	F	A ₀	B ₀	K ₀	P ₁	Т	Unit	Bulk qty.
TDFN8	8.00 +0.30 -0.10	1.50 +0.10/ -0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

G measured at hub

AM00443

40 mm min. acces hole at slot location C _____ Α Full radius Tape slot in core for tape start 25 mm min width

Figure 14. Reel dimensions

Table 8. **Reel dimensions**

Tape sizes	A max.	B min.	С	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/- 0.20	20.20	60	8.4 +2/-0	14.40

Figure 15. Tape trailer/leader

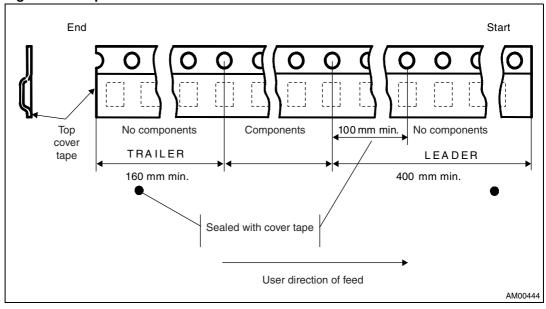
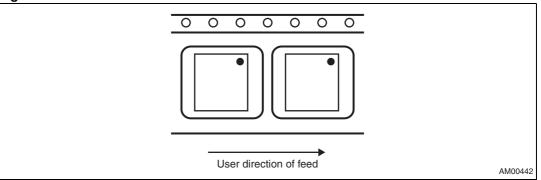


Figure 16. Pin 1 orientation



Note: 1 Drawings are not to scale.

2 All dimensions are in mm, unless otherwise noted.

Ordering information STM6520

11 Ordering information

Table 9. Ordering information scheme Example: STM6520 A Q R R DG 9 Device type STM6520 Reset (V_{CC} monitoring threshold) voltage V_{RST} $A = no V_{CC}$ monitoring feature Smart Reset™ setup delay (t_{SRC}) Q = 7.5 or 12.5 s typ., user-selected (two-state); input comparator on SRO, SR1, no input pull-ups **Outputs type** $R = \overline{RST1}$ active-low, open-drain, no pull-up; RST2 active-high, push-pull Reset pulse timeout period (t_{REC}) $R = push-button controlled (no defined t_{REC}, no power-on reset)$ **Package** DG = TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch Temperature range $9 = -30 \, ^{\circ}\text{C} \text{ to } +85 \, ^{\circ}\text{C}$ Shipping method

F = ECOPACK® package, tape and reel

For other options, voltage threshold values etc. or for more information on any aspect of this device, please contact the ST sales office nearest you.

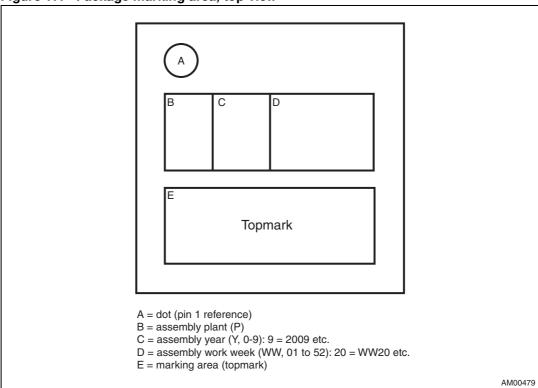
20/23 Doc ID 15953 Rev 6

12 Package marking information

Table 10. Package marking

Part number	Package	Topmark
STM6520AQRRDG9F	TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch	DRM
STM6520AQRRDG9F	TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch	ERM

Figure 17. Package marking area, top view



Revision history STM6520

13 Revision history

Table 11. Document revision history

Date	Revision	Changes
08-Jul-2009	1	Initial release.
20-Oct-2009	2	Document reformatted, updated Section 1: Description, Table 1, Figure 4, Figure 5, Table 4, renamed Section 2: Device overview, added Section 5: Typical operating characteristics, updated supply voltage range in Table 4.
20-Jan-2010	3	Updated Section 1: Description, Table 1.
06-May-2010	4	Updated title, Features, Applications, Table 5.
31-May-2010	5	Replaced "smart reset" by "Smart Reset™", updated Applications, Section 1, Section 3.1, Section 3.5, Figure 4, Figure 5, Table 2, Table 4, Table 6 and Table 10.
06-Jan-2011	6	Updated I _{CC} - supply voltage in <i>Table 4</i> .

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