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Kind regards,

Team Nexperia

PEMD14; PUMD14

NPN/PNP resistor-equipped transistors;
R1 = 47 k Ω , R2 = open

Rev. 02 — 2 September 2009

Product data sheet

1. Product profile

1.1 General description

NPN/PNP resistor-equipped transistors

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/PNP complement
	NXP	JEITA		
PEMD14	SOT666	-	PEMB14	PEMH14
PUMD14	SOT363	SC-88	PUMB14	PUMH14

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place cost

1.3 Applications

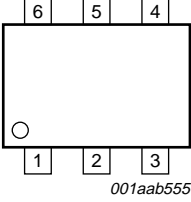
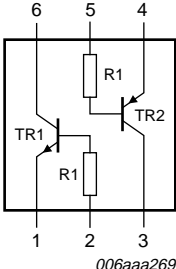
- Low current peripheral driver
- Control of IC inputs
- Replacement of general-purpose transistors in digital applications

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		33	47	61	k Ω

2. Pinning information

Table 3. Pinning			
Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
		001aab555	006aaa269

3. Ordering information

Table 4. Ordering information			
Type number	Package		
	Name	Description	Version
PEMD14	-	plastic surface mounted package; 6 leads	SOT666
PUMD14	SC-88	plastic surface mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes	
Type number	Marking code ^[1]
PEMD14	5B
PUMD14	T2*

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
I_O	output current (DC)		-	100	mA
I_{CM}	peak collector current		-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$			
	SOT363		[1]	200	mW
	SOT666		[1] [2]	200	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$			
	SOT363		[1]	300	mW
	SOT666		[1] [2]	300	mW

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ °C}$				
	SOT363		[1]	-	625	K/W
	SOT666		[1] [2]	-	625	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ °C}$				
	SOT363		[1]	-	416	K/W
	SOT666		[1] [2]	-	416	K/W

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

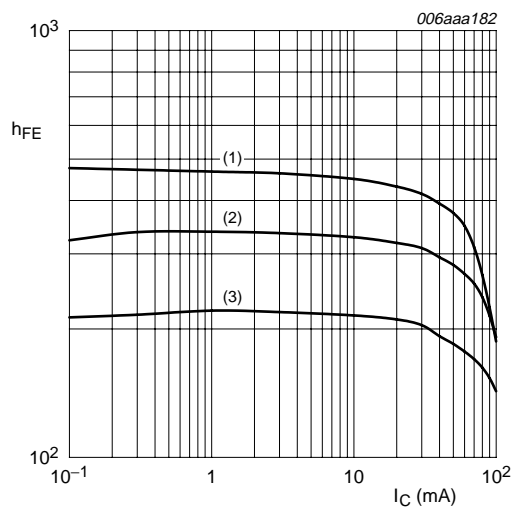
[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8. Characteristics

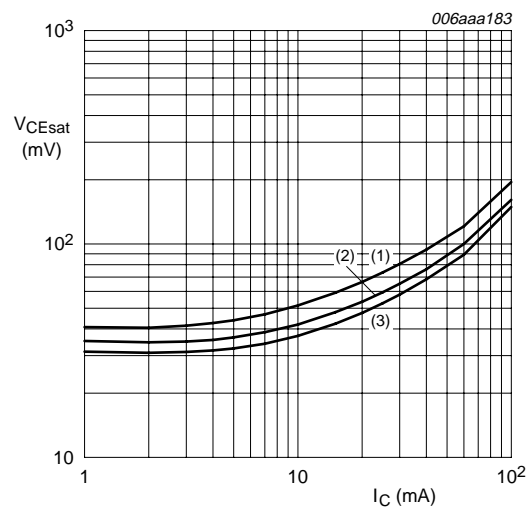
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
R1	bias resistor 1 (input)		33	47	61	k Ω
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF



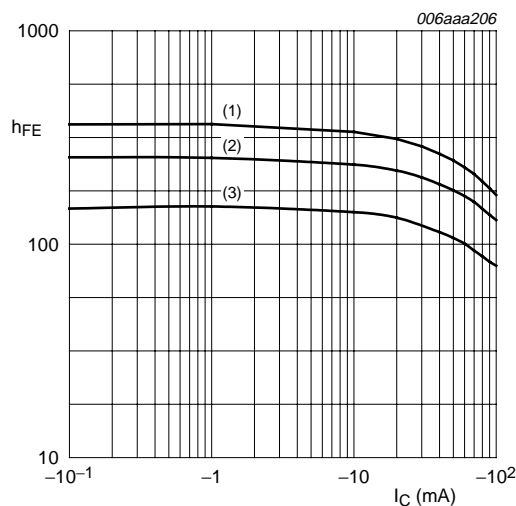
- $V_{CE} = 5\text{ V}$
- (1) $T_{amb} = 100^\circ\text{C}$
 - (2) $T_{amb} = 25^\circ\text{C}$
 - (3) $T_{amb} = -40^\circ\text{C}$

Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values



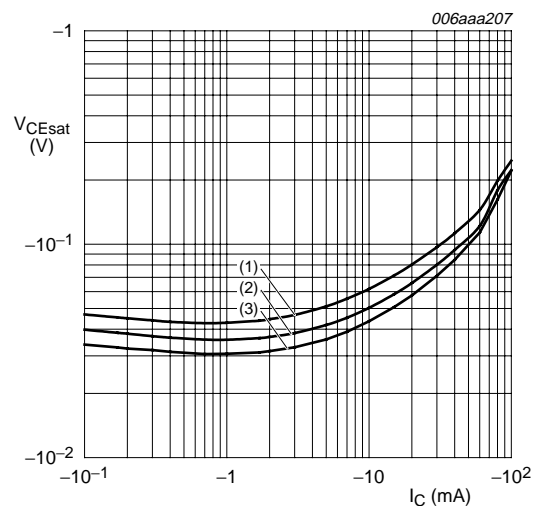
- $I_C/I_B = 20$
- (1) $T_{amb} = 100^\circ\text{C}$
 - (2) $T_{amb} = 25^\circ\text{C}$
 - (3) $T_{amb} = -40^\circ\text{C}$

Fig 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = 100^\circ\text{C}$
 - (2) $T_{amb} = 25^\circ\text{C}$
 - (3) $T_{amb} = -40^\circ\text{C}$

Fig 3. TR2 (PNP): DC current gain as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100^\circ\text{C}$
 - (2) $T_{amb} = 25^\circ\text{C}$
 - (3) $T_{amb} = -40^\circ\text{C}$

Fig 4. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package; 6 leads

SOT363

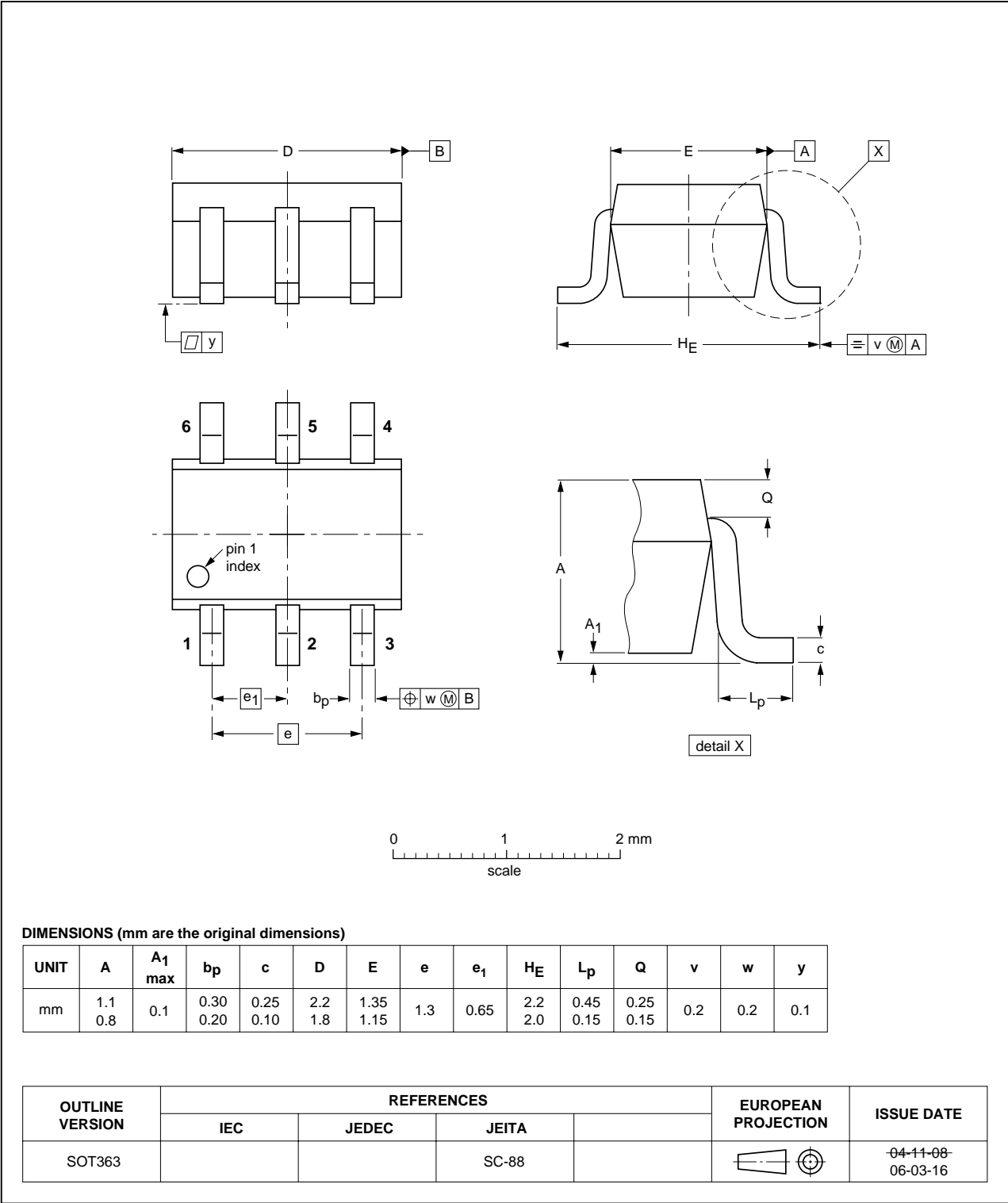


Fig 5. Package outline SOT363 (SC-88)

Plastic surface-mounted package; 6 leads

SOT666

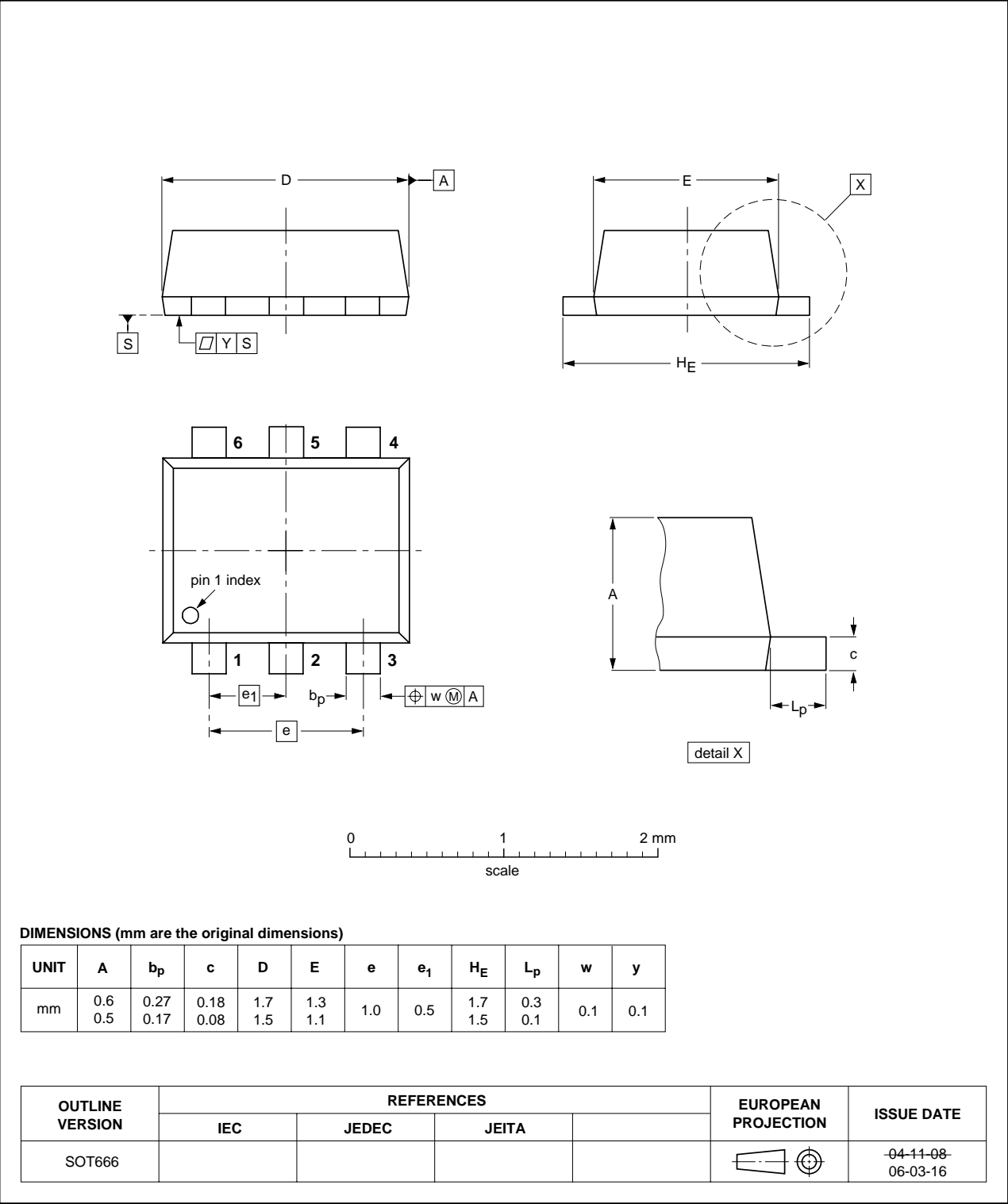


Fig 6. Package outline SOT666

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

Type number	Package	Description	Packing quantity		
			3000	4000	10000
PEMD14	SOT666	4 mm pitch, 8 mm tape and reel	-	-115	-
PUMD14	SOT363	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-135
PUMD14	SOT363	4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-165

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD14_PUMD14_2	20090902	Product data sheet	-	PEMD14_PUMD14_1
Modifications:	<ul style="list-style-type: none">• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.• Figure 5 "Package outline SOT363 (SC-88)": updated• Figure 6 "Package outline SOT666": updated			
PEMD14_PUMD14_1	20050114	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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