Introduction

The Xilinx® LogiCORE™ IP LTE Fast Fourier Transform (FFT) implements all transform lengths required by the 3GPP LTE specification, including the 1536-point transform for 15 MHz bandwidth support.

Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/lte_fft_eval/index.htm

Features

- Forward and inverse complex FFT, run-time configurable

- Supports transform point sizes 128, 256, 512, 1024, 1536, 2048

- Data sample precision b_x = 14 – 17

- Phase factor precision b_w = 14 – 17

- Optional run-time configurable point size

- Run-time configurable fixed scaling schedule, or unscaled datapath

- Bit/digit reversed or natural output order

- Optional cyclic prefix insertion

- Four architectures offer a trade-off between core size and transform time

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 All Programmable SoC 7 Series
Supported User Interfaces	Not Applicable
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Encrypted VHDL C Model
Supported S/W Driver	Not Applicable
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:
1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide

Send Feedback

Applications

The LTE FFT IP core can be used to implement the Fast Fourier Transform requirements of the 3GPP LTE standard. The core can be used to implement both inverse FFT for the downlink and direct FFT for the uplink. The core is a component of the Xilinx LTE Baseband Targeted Design Platform.

Overview

The LTE FFT core computes an N-point forward DFT or inverse DFT where N can be *128, 256, 512, 1024, 1536, 2048*.

The input data is a vector of N complex values represented as dual b_x-bit twos-complement numbers, that is, b_x bits for each of the real and imaginary components of the data sample, where b_x is in the range 14 to 17 bits inclusive. Similarly, the phase factors b_w can be 14 to 17 bits wide.

The N element output vector is represented using b_x bits for each of the real and imaginary components of the output data. Input data is presented in natural order and the output data can be in either natural or bit/digit reversed order.

Two arithmetic options are available for computing the FFT:

- Full-precision unscaled arithmetic

- Scaled fixed-point arithmetic, with a user-specified scaling schedule

The point size N, the choice of forward or inverse transform, the scaling schedule and the cyclic prefix length are run-time configurable. Transform type (forward or inverse), scaling schedule and cyclic prefix length can be changed on a frame-by-frame basis. Changing the point size immediately resets the core.

Four architecture options are available:

- Pipelined, Streaming I/O

- Radix-4, Burst I/O

- Radix-2, Burst I/O

- Radix-2 Lite, Burst I/O

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the LTE Fast Fourier Transform product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

When the core is used under an evaluation license, it times out after approximately four hours when using a 100 MHz system clock. After this period the core no longer accepts new START inputs. Any frames being processed when timeout occurs might be corrupted.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/05/2017	2.0	• Added Butterfly options to Vivado IDE • Remove 32-bit support for Linux and Windows C Model
11/18/2015	2.0	Added UltraScale+ device support.
06/04/2014	2.0	Initial Xilinx release. This document replaces XMP125.

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