Dual 36V Synchronous 1.6A Buck LED Driver with I²C

FEATURES

- **Wide Input Voltage Range: 4V to 36V**
- **Two Independent 1.6A/40V Synchronous Bucks**
- **I²C Interface for Internal True Color PWM™ Dimming (8192:1), Analog Dimming and Fault Reporting**
- **1000:1 External True Color PWM Dimming and 10:1 External Analog Dimming**
- **PMOS Switch Driver for PWM and Output Disconnect**
- ±3% Constant Current Regulation
- Adjustable Frequency: 200kHz to 2MHz
- Frequency Synchronization with Clock Output
- Programmable OPENLED Protection with Reporting
- Short-Circuit Protection with Reporting
- Programmable Undervoltage Lockout with Hysteresis
- Internal Compensation
- 9 Unique Device Addresses for I²C
- Available in 5mm × 6mm 36-Lead QFN Package

APPLICATIONS

- General Purpose, Industrial, Medical and Automotive Lighting
- Constant-Current, Constant-Voltage Source

DESCRIPTION

The LT®3964 is a dual synchronous step-down DC/DC converter with I²C interface designed to operate as a constant-current and constant-voltage source and is ideal for driving LEDs. The fixed frequency and peak current mode topology result in stable operation over a wide range of supply and output voltages. The ground referred voltage FB pin serves as the input for several LED protection features, and also allows the converter to operate as a constant-voltage source. The maximum output current is set by an external resistor, and the output current amplifier has a rail-to-rail common mode range. LT3964 uses an I²C interface to communicate with a microcontroller to read LED faults, write PWM and analog dimming registers and set fault masking. The I²C PWM input provides LED dimming ratios up to 8192:1. The I²C programmable CTRL register sets the gain of the external CTRL pin, and maximum current sense threshold, providing additional analog dimming capability.

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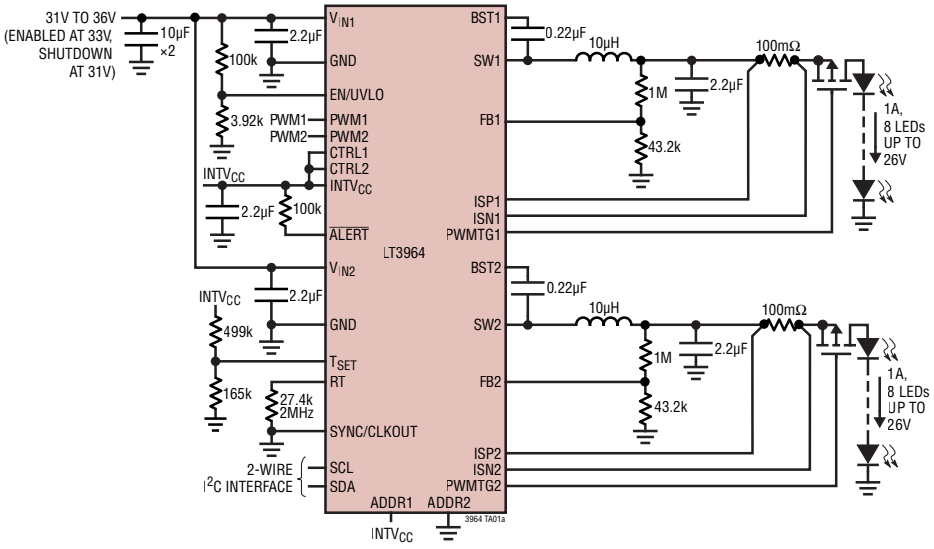
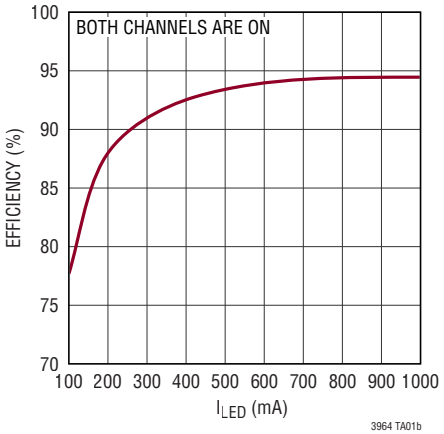
TYPICAL APPLICATION

50W Dual Buck 1A LED Driver



Efficiency, V_{IN} = 34V

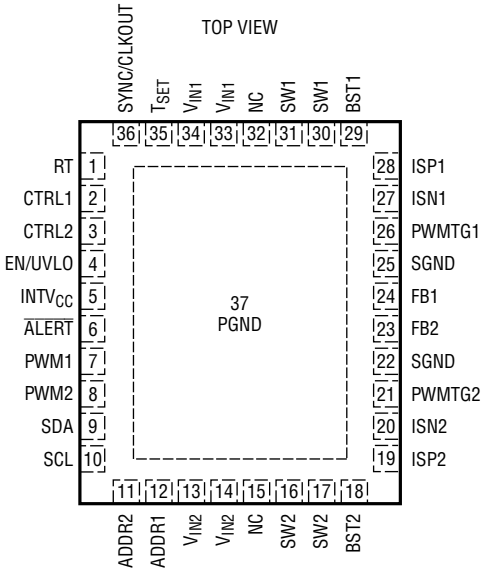


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, EN/UVLO 40V
ISP1, ISN1, ISP2, ISN2.....40V
PWMTG1, PWMTG2, RT .....Note 2
SW1, SW2.....40V
BST1, BST2.....44.5V
BST1 to SW1, BST2 to SW2 .....4.5V
FB1, FB2, CTRL1, CTRL2, ADDR1, ADDR2 .....5V
SYNC/CLKOUT, PWM1, PWM2, T_{SET}.....6V
SDA, SCL, $\overline{ALERT}$ 6V
$INTV_{CC}$.....Note 3
Operating Junction Temperature (Notes 4, 5)
LT3964E/LT3964I..... –40°C to 125°C
LT3964H..... –40°C to 150°C
Storage Temperature Range ..... –60°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 37) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT3964#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3964EUHE#PBF	LT3964EUHE#TRPBF	3964	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3964IUHE#PBF	LT3964IUHE#TRPBF	3964	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3964HUHE#PBF	LT3964HUHE#TRPBF	3964	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V, $V_{EN/UVLO}$ = 5V, CTRL1 = CTRL2 = 2V, PWM1 = PWM2 = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{IN2} Operating Supply Range		●	4		36	V
V_{IN1} Pin Quiescent Current	Not Switching			2.5		mA
V_{IN1} Pin Shutdown Current	EN/UVLO = 1.15V, PWM1,2 = 0V EN/UVLO = 0V				200 1	µA µA
V_{IN2} Pin Quiescent Current	Not Switching			1	10	µA
V_{IN2} Pin Shutdown Current	EN/UVLO = 1.15V, PWM1,2 = 0V EN/UVLO = 0V				1 1	µA µA
EN/UVLO Threshold Voltage Falling		●	1.158	1.18	1.202	V
EN/UVLO Rising Hysteresis				60		mV
EN/UVLO Input Low Voltage					0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V			4		µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.3V			2	100	nA
Linear Regulator						
$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = –30mA, Non Switching	●	3.9	4	4.1	V
$INTV_{CC}$ Line Regulation	6V ≤ V_{IN1} ≤ 40V			0.03		%/V
$INTV_{CC}$ Load Regulation	–30mA ≤ I_{INTVCC} ≤ 0mA			0.03		%/mA
$INTV_{CC}$ Undervoltage Lockout			3.1	3.2	3.3	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				50		mV
$INTV_{CC}$ Current Limit	V_{IN1} = 12V, V_{INTVCC} = 3V			110		mA
Dropout (V_{IN1} – V_{INTVCC})	V_{IN1} = 4V, I_{INTVCC} = –20mA, Not Switching			300		mV
Error Amplifier						
Full Scale LED Current Sense Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$)	ISP1,2 = 24V, CTRL1,2 = 1.5V, ADIM1,2[7:0] = 0xFF ISP1,2 = 0V, CTRL1,2 = 1.5V, ADIM1,2[7:0] = 0xFF	● ●	97 96	100 100	103 104	mV mV
1/2 Scale LED Current Sense Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$)	ISP1,2 = 24V, CTRL1,2 = 0.7V, ADIM1,2[7:0] = 0xFF ISP1,2 = 0V, CTRL1,2 = 0.7V, ADIM1,2[7:0] = 0xFF	● ●	47 46	50 50	53 54	mV mV
1/4th Scale LED Current Sense Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$) Modulated by I^2C Input ADIM1,2[7:0]	ISP1,2 = 24V, CTRL1,2 = 0.7V, ADIM1,2[7:0] = 0x7F ISP1,2 = 0V, CTRL1,2 = 0.7V, ADIM1,2[7:0] = 0x7F	● ●	22 21	25 25	28 29	mV mV
1/10th Scale LED Current Sense Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$)	ISP1,2 = 24V, CTRL1,2 = 0.3V, ADIM1,2[7:0] = 0xFF ISP1,2 = 0V, CTRL1,2 = 0.3V, ADIM1,2[7:0] = 0xFF	● ●	7 6	10 10	13 14	mV mV
ISP1,2/ISN1,2 Overcurrent Protection Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$)	ISP1,2 = 24V			930		mV
C/10 Current Sense Threshold ($V_{(ISP1-ISN1)}$, $V_{(ISP2-ISN2)}$)	ISP1,2 = 24V ISP1,2 = 0V		6 6	10 11	15 16	mV mV
ISP1, ISP2 Input Current Bias Current	PWM1,2 = 2V (ACTIVE) PWM1,2 = 0V (STANDBY)			350 5	 8	µA µA
ISN1, ISN2 Input Current Bias Current	PWM1,2 = 2V (ACTIVE) PWM1,2 = 0V (STANDBY)			30 10		µA nA
CTRL1, CTRL2 Input Bias Current	V_{CTRL1}, V_{CTRL2} = 1V			20	200	nA
CTRL1, CTRL2 PWM Shutdown Threshold		●		100	150	mV
CTRL1, CTRL2 PWM Threshold Hysteresis				30		mV
FB1, FB2 Regulation Voltage (V_{FB})	ISP1,2 = 24V	●	1.163 1.17	1.18 1.18	1.197 1.19	V V
FB1, FB2 Overvoltage Threshold			V_{FB} + 43mV	V_{FB} + 53mV	V_{FB} + 63mV	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V, $V_{EN/UVLO}$ = 5V, CTRL1 = CTRL2 = 2V, PWM1 = PWM2 = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB1, FB2 OPENLED Threshold			V_{FB} – 43mV	V_{FB} – 53mV	V_{FB} – 63mV	V
FB1, FB2 SHORTLED Threshold		●		250	270	mV
FB1, FB2 Pin Input Bias Current	Current Out of Pin, FB = 1V			20	200	nA
Feedback Line Regulation	4V ≤ V_{IN1} ≤ 36V			0.001		%/V
T_{SET} Pin Voltage				630		mV
T_{SET} Pin Bias Current	Current Out of Pin, T_{SET} = 400mV			40	200	nA
Oscillator						
RT Pin Voltage				0.96		V
Switching Frequency	R_T = 357k R_T = 60.4k R_T = 27.4k	● ● ●	186 0.93 1.86	200 1.0 2.0	214 1.07 2.14	kHz MHz MHz
SYNC/CLKOUT Pin Resistance to GND				100		kΩ
SYNC/CLKOUT Input High Threshold			1.5			V
SYNC/CLKOUT Input Low Threshold					0.4	V
SYNC/CLKOUT Output Duty Cycle	CONFIG[6] = 1 (Clock Output Enabled)		30	50	70	%
SYNC/CLKOUT Output Voltage High	CONFIG[6] = 1 (Clock Output Enabled)			4		V
SYNC/CLKOUT Output Voltage Low	CONFIG[6] = 1 (Clock Output Enabled)			0.1	0.3	V
SYNC/CLKOUT Output Rise Time	$C_{SYNC/CLKOUT}$ = 50pF, CONFIG[6] = 1 (Clock Output Enabled)			40		ns
SYNC/CLKOUT Output Fall Time	$C_{SYNC/CLKOUT}$ = 50pF, CONFIG[6] = 1 (Clock Output Enabled)			20		ns
Logic						
$\overline{ALERT}$ Output Low	$I_{\overline{ALERT}}$ = 1mA				300	mV
PWM1, PWM2 Input High Voltage		●		1.18	1.3	V
PWM1, PWM2 Input Low Voltage		●	1.1	1.15		V
PWM1, PWM2 Resistance to GND				280		kΩ
Power Switch						
Top Switch On Resistance	I_{SW} = 1A			200		mΩ
Top Switch Current Limit		●	1.6	1.8	2	A
Bottom Switch On Resistance	I_{SW} = 1A			180		mΩ
Bottom Switch Current Limit			1.6	2	2.4	A
SW Leakage Current	V_{IN} = 36V, V_{SW} = 0V, 36V		–1.5		1.5	µA
Minimum Off Time			20	50	70	ns
Minimum ON Time			20	40	65	ns
PWMTG Gate Driver						
PWMTG ON Voltage ($V_{ISP1-PWMTG1}$, $V_{ISP2-PWMTG2}$)	ISP1,2 = 36V			7.5	9.5	V
PWMTG OFF Voltage ($V_{ISP1-PWMTG1}$, $V_{ISP2-PWMTG2}$)	ISP1,2 = 36V			0	0.3	V
PWMTG Turn-On Time	C_{LOAD} = 500pF, ISP1,2 = 36V			70		ns
PWMTG Turn-Off Time	C_{LOAD} = 500pF, ISP1,2 = 36V			40		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 12V, $V_{EN/UVLO}$ = 5V, CTRL1 = CTRL2 = 2V, PWM1 = PWM2 = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Port (Note 6)						
I²C Address	XXXX Bits Are Programmed by ADDR[1:2]	●		110XXXX[R/$\overline{W}$]		
V_{IHA}	High Level Input Voltage for Address Pins ADDR1, ADDR2	●	$INTV_{CC}$ – 0.8			V
V_{ILA}	Low Level Input Voltage for Address Pins ADDR1, ADDR2	●			0.6	V
R_{INH}	Resistance from ADDR1, ADDR2 to $INTV_{CC}$ to Set Chip Address Bit to 1	●			10	kΩ
R_{INL}	Resistance from ADDR1, ADDR2 to GND to Set Chip Address Bit to 0	●			10	kΩ
R_{INF}	Resistance from ADDR1, ADDR2 to GND or $INTV_{CC}$ to Set Chip Address Bit to Float	●	1			MΩ
SDA and SCL Input High Voltage		●	1.5			V
SDA and SCL Input Low Voltage		●			0.4	V
SDA and SCL Input High Current	SDA, SCL = 3.3V				50	nA
SDA and SCL Input Low Current	Current Out of Pin, SDA, SCL = 0V				50	nA
SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
Clock Operating Frequency					400	kHz
Bus Free Time Between Stop and Start Condition (t_{BUF})			1.3			µs
Hold Time After Repeated Start Condition ($t_{HD,SDA}$)			0.6			µs
Repeated Start Condition Set-Up Time ($t_{SU,STA}$)			0.6			µs
Stop Condition Set-Up Time ($t_{SU,STO}$)			0.6			µs
Data Hold Time Output ($t_{HD,DAT(O)}$)			0		900	ns
Data Hold Time Input ($t_{HD,DAT(I)}$)			0			ns
Data Set-Up Time ($t_{SU,DAT}$)			250			ns
SCL Clock Low Period (t_{LOW})			1.3			µs
SCL Clock High Period (t_{HIGH})			0.6			µs
Data Fall Time	C_B = Capacitance of One Bus Line (pF)		20 + 0.1C_B		300	ns
Data Rise Time	C_B = Capacitance of One Bus Line (pF)		20 + 0.1C_B		300	ns
Input Spike Suppress Pulse Width (t_{SP})					50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage source to the PWMTG pin or RT pin, otherwise permanent damage may occur.

Note 3: Do not apply a positive or negative voltage source to $INTV_{CC}$ pin, otherwise permanent damage may occur. I_{INTVCC} = 5mA is the maximum external load that can be applied. The internal load will be higher due to the power consumption of the IC.

Note 4: The LT3964E is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3964I is guaranteed to meet performance specifications over the –40°C to 125°C operating temperature range. The LT3964H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

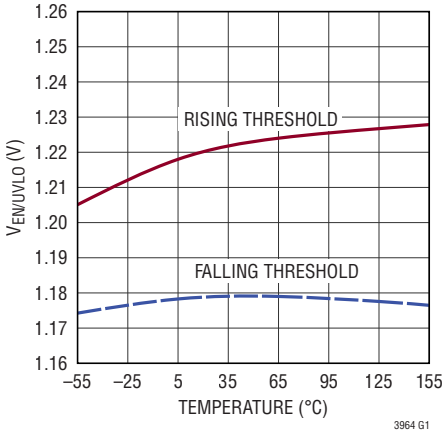
Note 5: The LT3964 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Note 6: All I²C serial port timing information is shown in Figure 15.

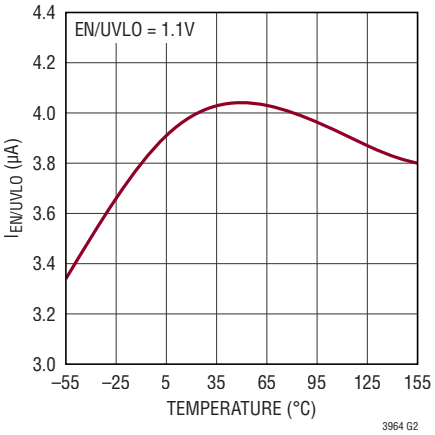
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

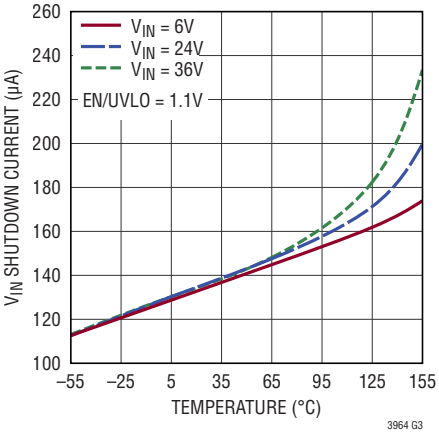
EN/UVLO Thresholds vs Temperature



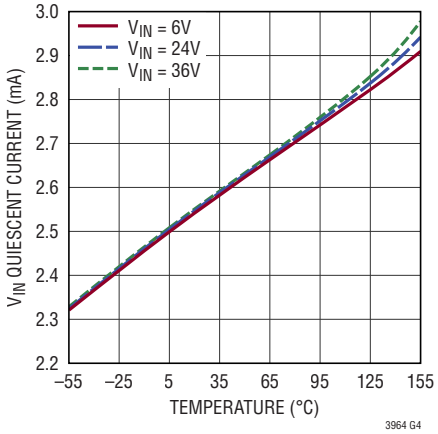
EN/UVLO Current vs Temperature



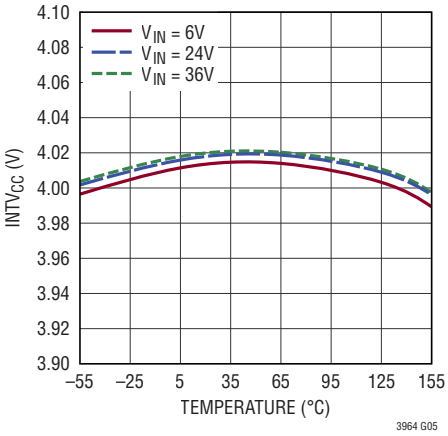
V_{IN} Shutdown Current vs Temperature



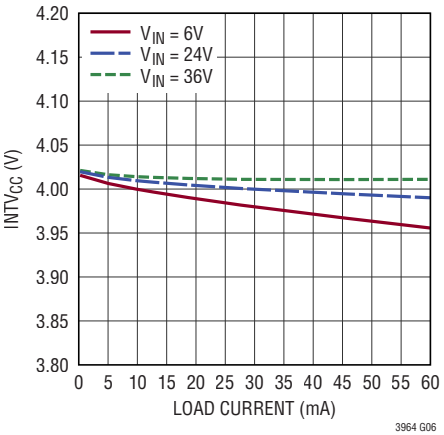
V_{IN} Quiescent Current vs Temperature



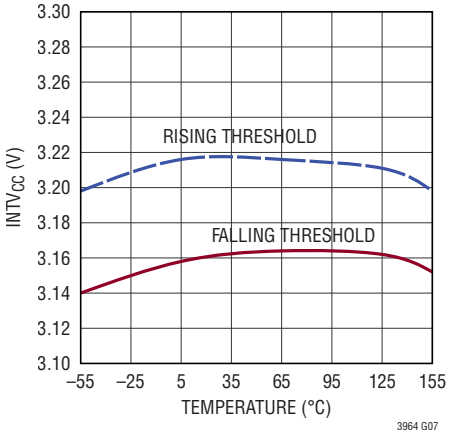
$INTV_{CC}$ vs Temperature ($3 \cdot V_{IN}$)



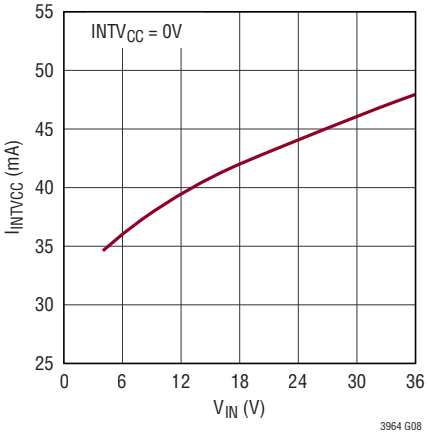
$INTV_{CC}$ vs Current ($3 \cdot V_{IN}$)



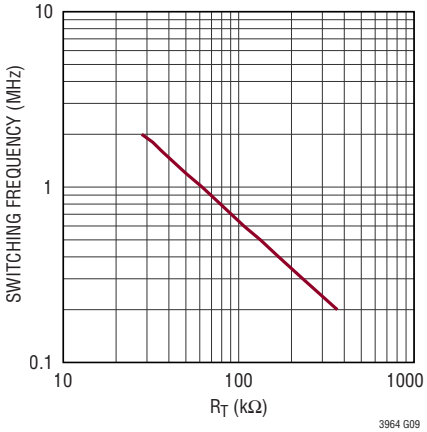
$INTV_{CC}$ UVLO vs Temperature



$INTV_{CC}$ Current Limit vs V_{IN}



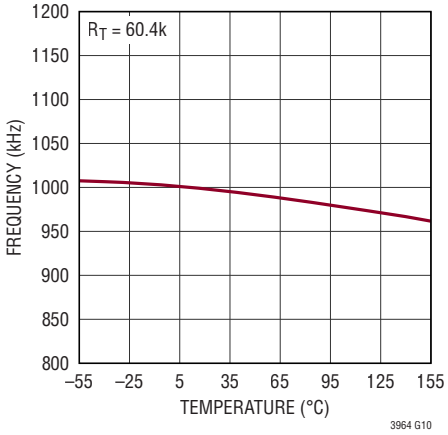
Switching Frequency vs R_T



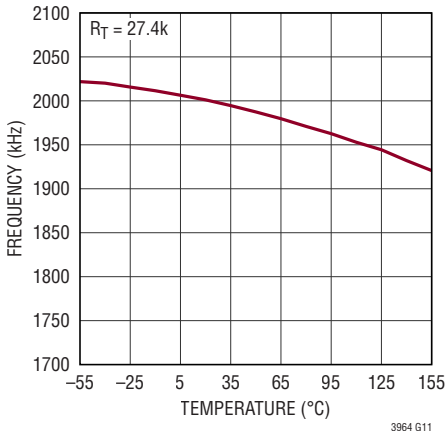
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

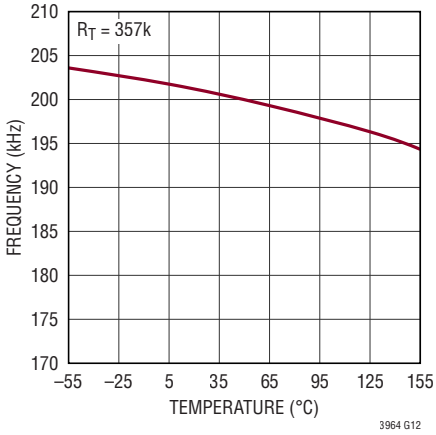
Frequency vs Temperature (1MHz)



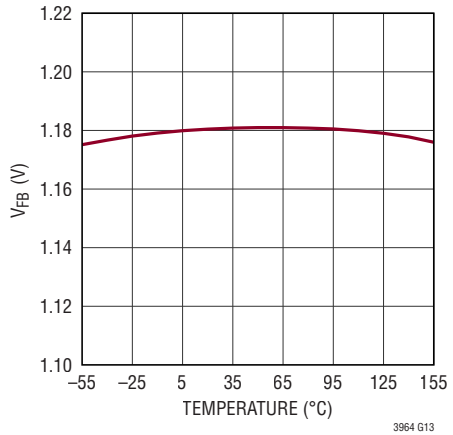
Frequency vs Temperature (2MHz)



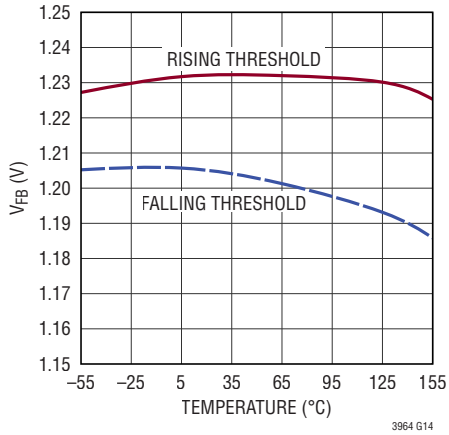
Frequency vs Temperature (200kHz)



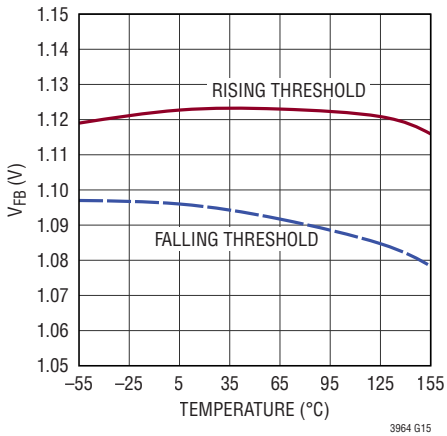
V_{FB} vs Temperature



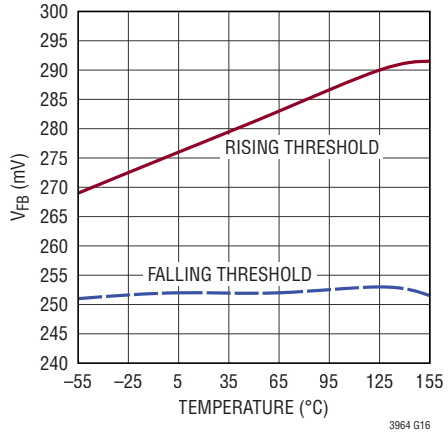
OVFB Threshold vs Temperature



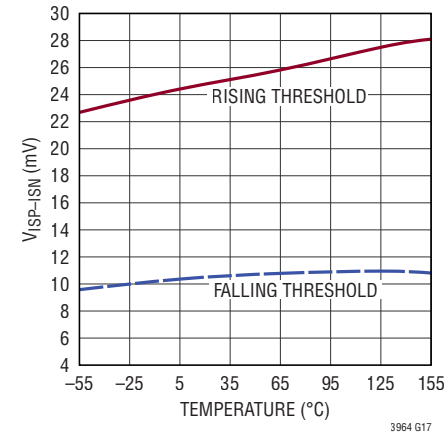
OPENLED Threshold vs Temperature



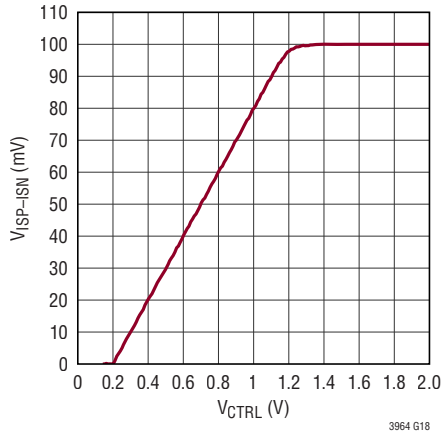
SHORTLED Threshold vs Temperature



C/10 Threshold vs Temperature



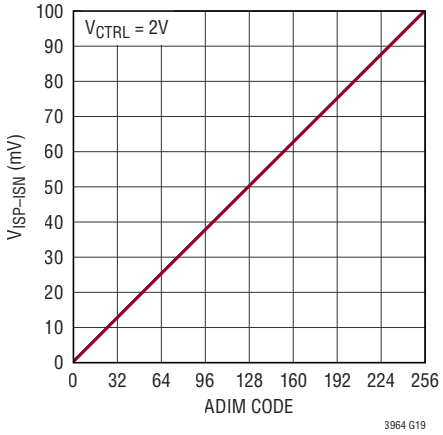
$V_{ISP–ISN}$ vs CTRL



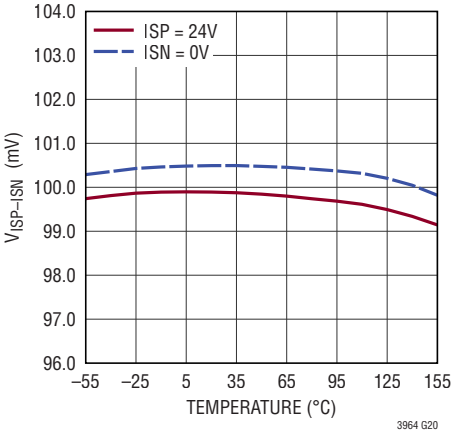
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

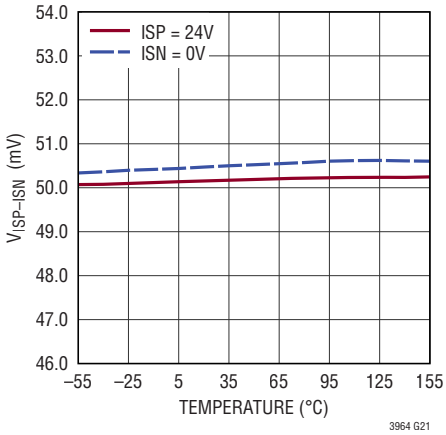
$V_{ISP–ISN}$ vs ADIM



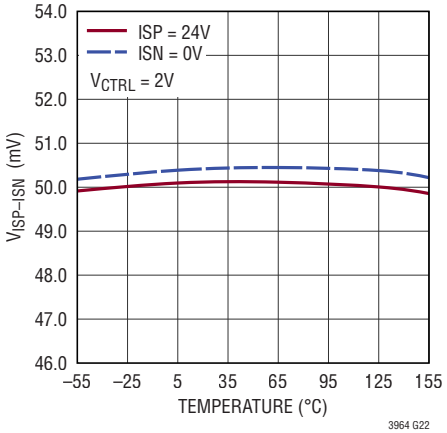
$V_{ISP–ISN}$ Full Scale vs Temperature



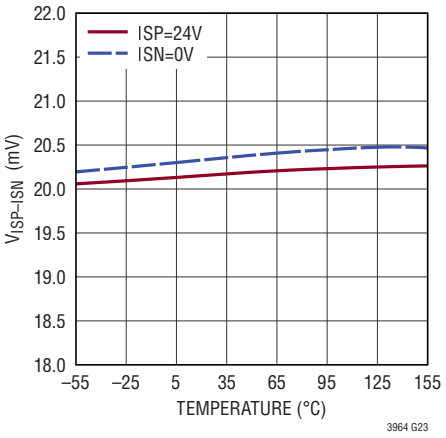
$V_{ISP–ISN}$ 1/2 Scale (V_{CTRL} = 0.7V) vs Temperature



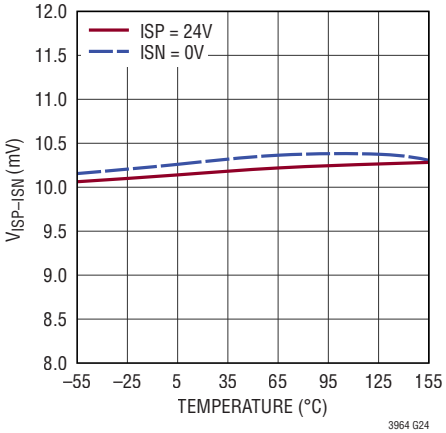
$V_{ISP–ISN}$ 1/2 Scale (ADIM = 0x7f) vs Temperature



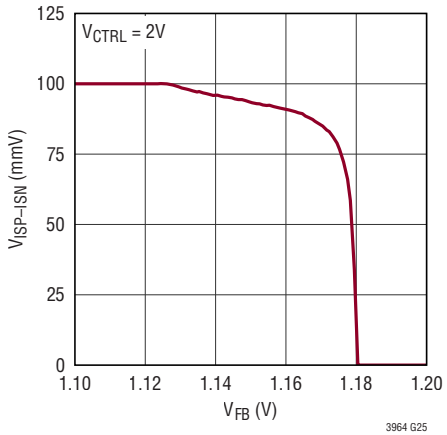
$V_{ISP–ISN}$ 1/5 Scale (V_{CTRL} = 0.4V) vs Temperature



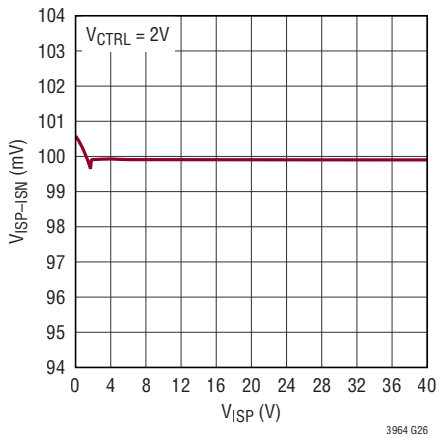
$V_{ISP–ISN}$ 1/10 Scale (V_{CTRL} = 0.3V) vs Temperature



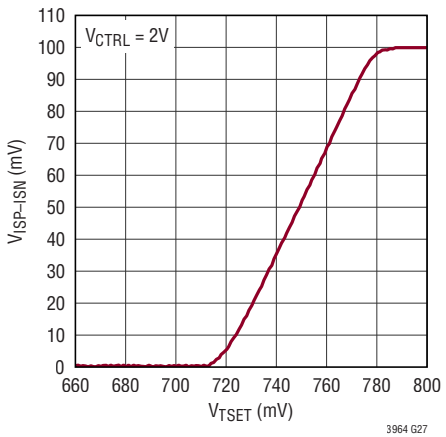
$V_{ISP–ISN}$ vs V_{FB}



$V_{ISP–ISN}$ vs V_{ISP}



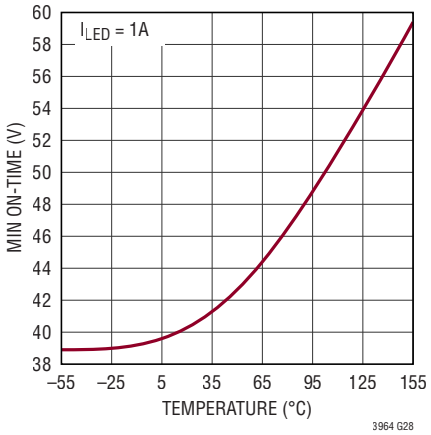
$V_{ISP–ISN}$ vs V_{TSET} at 90°C



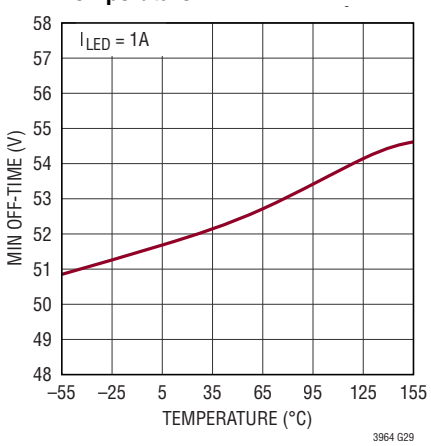
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

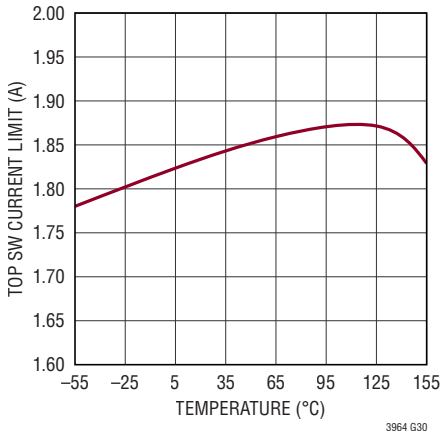
Minimum On-Time vs Temperature



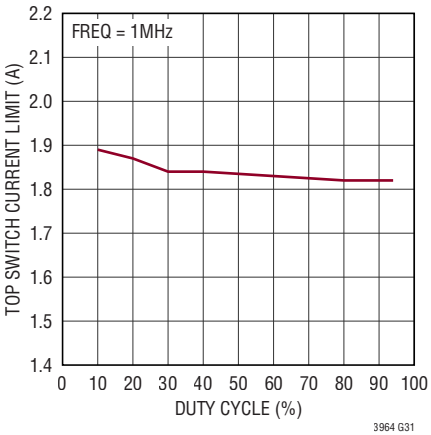
Minimum Off-Time vs Temperature



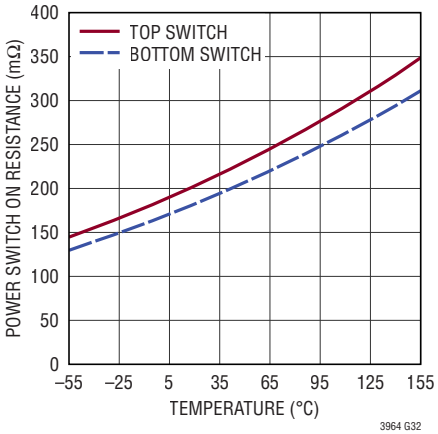
Top Switch Current Limit vs Temperature



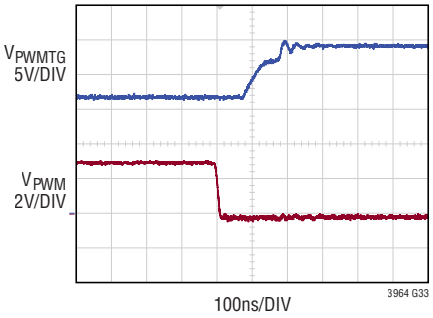
Top Switch Current Limit vs Duty Cycle



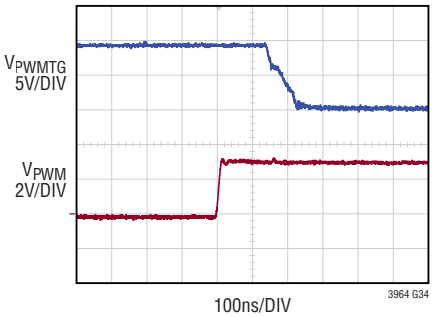
Power Switch On-Resistance vs Temperature



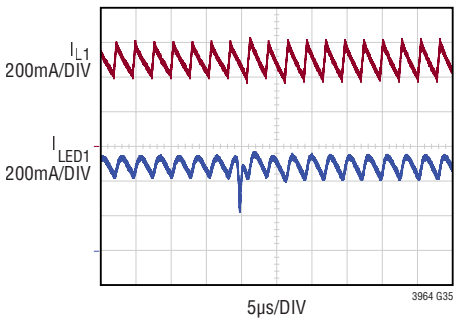
PWMTG Rising Edge



PWMTG Falling Edge

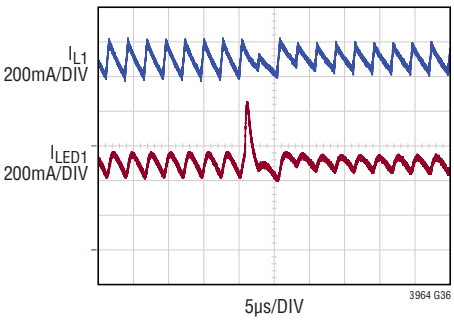


Transient Response at V_{IN} = 34V Zero LED On to One LED On



SEE MATRIX LED DRIVER ON PAGE 31

Transient Response at V_{IN} = 34V One LED On to Zero LED On



SEE MATRIX LED DRIVER ON PAGE 31

PIN FUNCTIONS

RT (Pin 1): Switching Frequency Adjustment Pin. Set the master clock frequency using a resistor to GND (for resistor values, see Typical Performance curve or Table 3). Do not leave the RT pin open.

CTRL1, CTRL2 (Pins 2, 3): Current Sense Threshold Adjustment Pins. The $V_{(ISP-ISN)}$ threshold is regulated by the internal 1.2V reference voltage, CTRL and ADIM[7:0] of the respective channel as follows:

$V_{(ISP-ISN)}$ = 0V, when V_{CTRL} < 0.2V

$V_{(ISP-ISN)}$ = [(V_{CTRL} –0.2V)/10]•(ADIM[7:0]+1)/256, when 0.2V ≤ V_{CTRL} ≤ 1.1V

$V_{(ISP-ISN)}$ = 100mV•(ADIM[7:0]+1)/256, when V_{CTRL} > 1.3V

For 1.1V < V_{CTRL} < 1.3V, the dependence of the current sense threshold upon V_{CTRL} transitions from a linear function to a constant value, reaching 98% of full scale value, 100mV•(ADIM[7:0]+1)/256, by V_{CTRL} = 1.2V. See Table 1 for detailed information. Do not leave this pin open.

EN/UVLO (Pin 4): Enable and Undervoltage Lockout Pin. An accurate 1.18V falling threshold with externally programmable hysteresis detects when power is OK to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 4µA pull-down current. Tie to 0.4V or less to disable the device.

$INTV_{CC}$ (Pin 5): Internal Low-Dropout Regulator Output. $INTV_{CC}$ is regulated to 4V, and must be bypassed with an external capacitor of at least 2.2µF. $INTV_{CC}$ is the power supply for the internal DMOS gate driver and control circuitry. Users may apply <5mA loads to $INTV_{CC}$. Overloading $INTV_{CC}$ can cause unintentional device shutdown from $INTV_{CC}$ current limiting or overheating due to power dissipation.

$\overline{ALERT}$ (Pin 6): Chip Alert Status Report Pin. An open-collector pull-down on $\overline{ALERT}$ asserts when any of the following conditions happen:

1. FB Overvoltage (V_{FB} > 1.233V);
2. OPENLED (V_{FB} > 1.127V and $V_{(ISP-ISN)}$ <10mV);
3. SHORTLED (V_{FB} < 0.25V);
4. LED Overcurrent ($V_{(ISP-ISN)}$ > 930mV);
5. $INTV_{CC}$ undervoltage; or
6. Thermal shutdown.

$\overline{ALERT}$ flag stays low until all alerts have been removed and unlatched.

PWM1, PWM2 (Pins 7, 8): PWM Input Signal Pin. A low signal turns off switching, reduces quiescent supply current, and drives PWMTG to the ISP level. PWM has an internal 280k pull-down resistor. If not used, connect this pin to $INTV_{CC}$.

SDA (Pin 9): Serial Data Line for I^2C Port. Open-drain output during read back.

SCL (Pin 10): Serial Clock Line for I^2C Port.

ADDR2 (Pin 11): Address Select Pin. This pin is configured as a three-state (LOW, HIGH, FLOAT) address control bit for the device I^2C address. See Table 14 for address selection.

ADDR1 (Pin 12): Address Select Pin. This pin is configured as a three-state (LOW, HIGH, FLOAT) address control bit for the device I^2C address. See Table 14 for address selection.

V_{IN2} (Pins 13, 14): Input Supply for Channel 2. May be driven by an independent supply, or connected to V_{IN1}. This signal must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN2} pin, and the negative terminal as close as possible to the PGND pin (Pin 37).

PIN FUNCTIONS

SW1, SW2 (Pins 16, 17, 30, 31): SW Pins. The SW pins are the outputs of the internal power switches of each channel. Tie each channel SW pins together and connect them to the appropriate inductor and boost capacitor. These nodes should be kept small on the PCB for good performance.

BST1, BST2 (Pins 18, 29): Boost Pins. These pins are used to provide a drive voltage, higher than the input voltage, to the topside power switch of each channel. Place a 0.1µF or larger boost capacitors as close as possible to the IC.

ISP1, ISP2 (Pins 19, 28): Connection Points for the Positive Terminals of the Current Feedback Resistors ($R_{LED1,2}$). Also serves as positive rails for PWMTG drivers.

ISN1, ISN2 (Pins 20, 27): Connection Points for the Negative Terminals of the Current Feedback Resistors ($R_{LED1,2}$).

PWMTG1, PWMTG2 (Pins 21, 26): Top Gate Driver Outputs. An inverted and level-shifted version of the PWM input signals. Used to drive the gate of an external PMOS transistor between V_{ISP} and V_{ISP}–7.5V to provide load-side on/off control, PWM dimming and fault-mode disconnect. Leave PWMTG unconnected if not used.

FB1, FB2 (Pins 23, 24): Voltage Loop Feedback Pins. The FB pin is intended for constant-voltage regulation or for LED protection/OPENLED detection. The LT3964 regulates the FB pins to 1.18V(NOMINAL). If the FB input is regulating the loop and $V_{(ISP-ISN)}$ is less than 10mV (Typical), the corresponding OPENLED bit in the chip status register is set and the $\overline{ALERT}$ pull-down is asserted. This action may signal an OPENLED fault for that channel. If FB is driven above 1.233V, the power switches are turned off for that channel, the corresponding OVFB bit in the chip status register is set, $\overline{ALERT}$ pull-down is asserted, and the PWMTG pin for that channel is driven high to protect the LEDs from an overcurrent event. If FB is driven below 0.25V, the power switches are turned off for that channel, the corresponding SHORTLED bit in the chip status register is set, $\overline{ALERT}$ pull-down is asserted, and the PWMTG pin for that channel is driven high to isolate the LED string from the power path. Do not tie these pins to GND.

V_{IN1} (Pins 33, 34): Input Supply. The V_{IN1} pins supply current to the LT3964 internal circuitry and to the internal topside power switch of Channel 1. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN1} pins, and the negative terminal as close as possible to the PGND pin (Pin 37).

T_{SET} (Pin 35): Junction Temperature Adjustment Pin. Programs LT3964 junction temperature breakpoint, beyond which LED currents will begin to decrease. An internal V_{PTAT} threshold (see Block Diagram) increases with junction temperature. When V_{PTAT} exceeds T_{SET} pin voltage, LED currents are decreased. If the function is not required, connect T_{SET} pin to $INTV_{CC}$ pin.

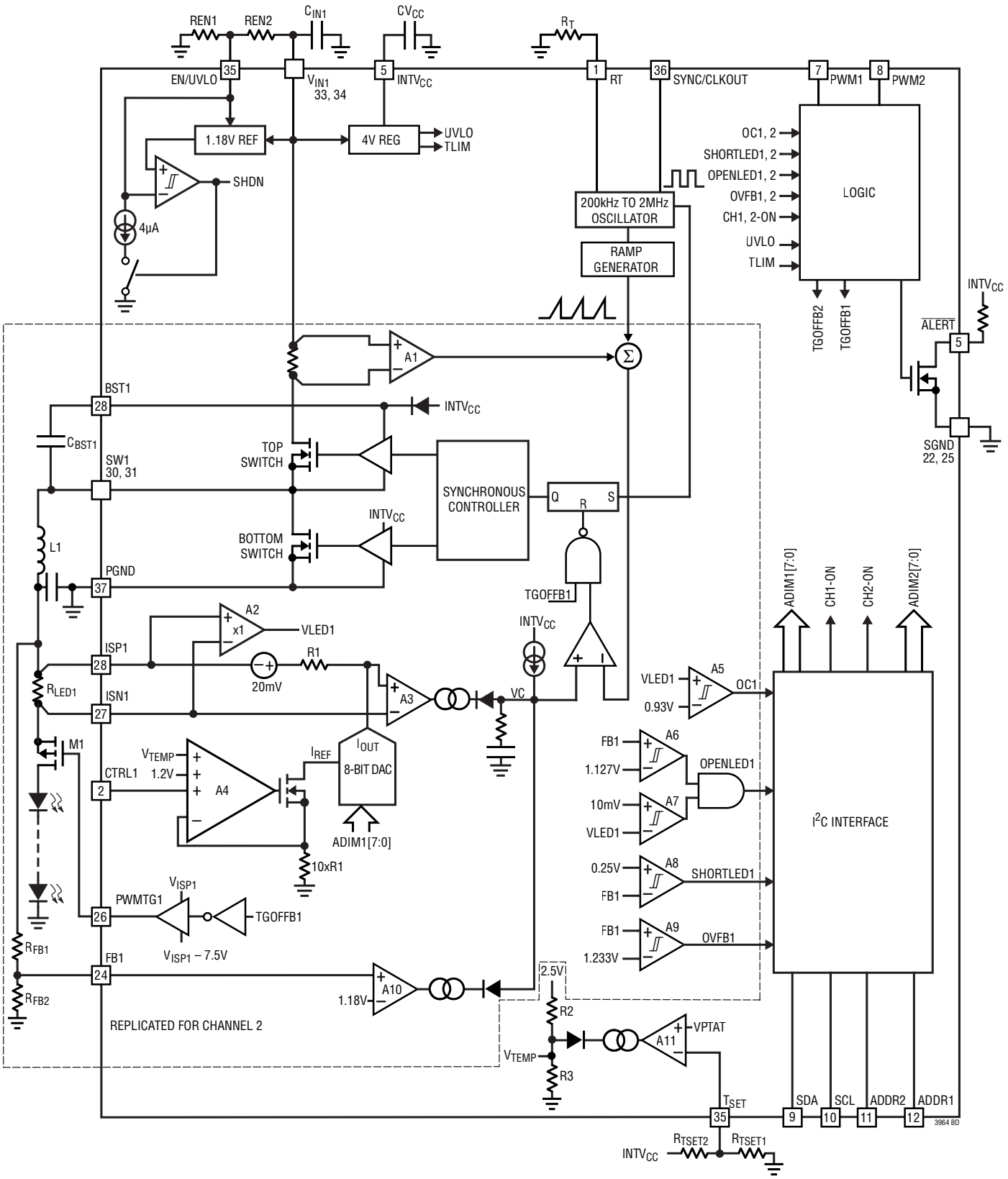
SYNC/CLKOUT (Pin 36): The SYNC/CLKOUT pin can be used to synchronize the internal oscillator to an external logic level signal. The R_T resistor should be chosen to program an internal switching frequency 10% slower than the SYNC pulse frequency. Use a 50% duty cycle waveform to drive this pin. When CONFIG[6] bit in the chip configuration register is set, a buffered version of the clock signal is driven out of the SYNC/CLKOUT pin. Note that the SYNC/CLKOUT pin is only meant to drive capacitive loads up to 50pF. If not used, tie this pin to GND with a 20k resistor.

SGND (Pins 22, 25): Chip Ground Pin.

PGND (Pin 37): Power Switch Ground. These pins are the return path of the internal bottom-side power switch. Place the negative terminal of the input capacitor as close to the PGND pins as possible.

NC (Pins 15, 32): No Connect Pin.

BLOCK DIAGRAM



OPERATION

The LT3964 is a dual constant-frequency, current mode step-down DC/DC converter with internal synchronous power switches. The operation of the LT3964 is best understood by referring to the Block Diagram of the IC.

In normal operation, with the PWM pin is low or CH1,2_ON signal is low, TGOFFB is disabled. The power switches are turned off, the PWMTG pin is pulled high to ISP to turn off the PMOS disconnect switch, and the ISP and ISN pin bias currents are reduced to several µA. When the PWM pin and CH1,2_ON signal transitions high, the PWMTG pin transitions low after a short delay. At the same time, the bottom switch is turned on for a short period of time to refresh the boost capacitor, followed by the top power switch turning on. A voltage input proportional to the top switch current is added to a stabilizing slope compensation ramp and the resulting top switch current sense signal is fed into the negative terminal of the PWM comparator. The current in the external inductor increases steadily during the time the top switch is on. When the switch current sense voltage exceeds the output of the error amplifier, labeled VC, the latch is reset and the switch is turned off. During the top switch off phase, the synchronous bottom switch is on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 2A (Typ) flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator. Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current or voltage in the load. The VC signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin and I^2C input ADIM[7:0]. In this manner, the error amplifier sets the correct top switch peak current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. The analog input at CTRL pin together with the digital input ADIM[7:0] can be used to provide a combination of temperature foldback protection via CTRL and analog dimming via I^2C, or a combination of analog dimming via CTRL pin and LED binning via I^2C.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the VC node is set by the amplified difference of the internal reference of 1.18V (typical) and the FB pin. If FB is lower than the reference voltage, the top switch current increases; if FB is higher than the reference voltage, the top switch demand current decreases. The LED current sense feedback interacts with the voltage feedback so that FB does not exceed the internal reference and the voltage between ISP and ISN does not exceed the threshold set by the product of the analog input at CTRL pin and the digital input ADIM[7:0] through I^2C. For accurate current or voltage regulation, it is necessary to ensure that under normal operating conditions, the appropriate loop is dominant. To deactivate the voltage loop entirely, FB can be set between 0.3V and 1.08V through a resistor network to $INTV_{CC}$ pin. To deactivate the LED current loop entirely, the ISP and ISN should be tied together and CTRL tied to $INTV_{CC}$.

Two LED specific functions featured on the LT3964 are controlled by the voltage feedback FB pin. First, when the FB pin exceeds a voltage 53mV lower (–4%) than the FB regulation voltage and $V_{(ISP-ISN)}$ is less than 10mV (Typical), the OPENLED bit, STATUS[1] or STATUS[5], is set in the channel status register. This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. When the FB pin drops below 0.25V (typical) after start-up, the SHORTLED bit, STATUS[2] or STATUS[6], is set by comparator A8. A blanking period occurs during start-up for the SHORTLED protection feature from the EN/UVLO toggle.

LT3964 features a PMOS disconnect switch driver. The PMOS disconnect switch can be used to improve the PWM dimming ratio, and operate as fault protection as well. Once a fault condition is detected, the PWMTG pin is pulled high to turnoff the PMOS switch. The action isolates the LED array from the power path, preventing excessive current from damaging the LEDs.

The I^2C interface is used to communicate between LT3964 and a microprocessor. LT3964 receives digital PWM dimming and analog dimming commands from a microprocessor and sends back the chip status, i.e., FB overvoltage (FB > 1.233V), output short (FB < 0.25V) after start-up, LED overcurrent ($V_{(ISP-ISN)}$ > 930mV), OPENLED (FB > 1.127V and ($V_{(ISP-ISN)}$ < 10mV).

APPLICATIONS INFORMATION

The following is a guide to selecting the external components and configuring the LT3964 according to the requirements of an application.

OPERATION MODE

The LT3964 has two operation modes: I²C mode (at least one address pin is NOT grounded) and non-I²C mode (both I²C address pins are grounded, i.e. ADDR1 = ADDR2 = GND).

In I²C mode, the LT3964 is initially set to be idle after power on reset. It will stay in idle until an updated PWM command is received via I²C interface.

In non-I²C mode, the LT3964 starts up right after the PWM pin input signal rising edge after power-on reset. Non-I²C mode allows customers to access all the registers except PWM dimming registers using the chip address (1100000 R/W).

PROGRAMMING LED CURRENT WITH THE CTRL PIN

The LED current is programmed by placing an appropriate value current sense resistor R_{LED} between the ISP and ISN pins. For best fault protection provided by the high side PMOS disconnect switch, sensing of the current should be done at the top of the LED string. The LED current is regulated by the internal 1.2V reference voltage, analog input at CTRL and digital input ADIM[7:0] of analog dimming register:

$$I_{LED} = \frac{100mV}{R_{LED}} \bullet \frac{ADIM[7:0]+1}{256}, V_{CTRL} > 1.3V$$

$$I_{LED} = \frac{V_{CTRL} - 0.2V}{10 \bullet R_{LED}} \bullet \frac{ADIM[7:0]+1}{256}, 0.2V < V_{CTRL} < 1.1V$$

$$I_{LED} = 0, V_{CTRL} < 200mV$$

When the CTRL pin voltage is between 1.1V and 1.3V, the LED current varies with CTRL, but departs from the previous equation by an increasing amount as the CTRL voltage increases. Ultimately, above 1.3V, the LED current no longer varies with CTRL. The typical $V_{(ISP-ISN)}$ threshold vs CTRL in terms of ADIM[7:0] is listed in Table 1.

Table 1. $V_{(ISP-ISN)}$ Threshold vs CTRL in Terms of ADIM[7:0]

V_{CTRL}(V)	$V_{(ISP-ISN)}$ (mV)
1.1	90 • (ADIM[7:0]+1)/256
1.15	94.4 • (ADIM[7:0]+1)/256
1.2	97.8 • (ADIM[7:0]+1)/256
1.25	99.4 • (ADIM[7:0]+1)/256
1.3	100 • (ADIM[7:0]+1)/256

The CTRL pin should not be left open (tie to $INTV_{CC}$ if not used). CTRL can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load as shown in Figure 1, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low.

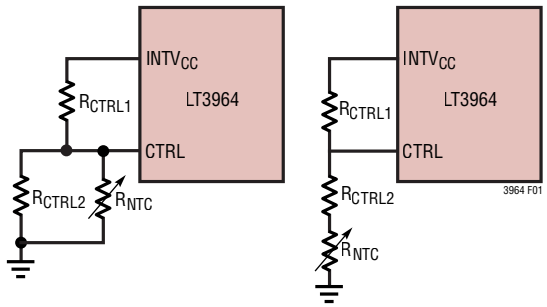


Figure 1. Setting CTRL with NTC Resistors

The digital input ADIM1[7:0] (for Channel 1) of analog dimming register shown in Table 2 can be accessed via I²C, which provides additional analog dimming. The default power-on value is 255.

The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor. For best accuracy, the amplitude of this ripple should be less than ±5mV.

SETTING SWITCHING FREQUENCY WITH THE RT PIN

The RT frequency adjust pin allows the user to program the switching frequency from 200kHz to 2MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses, and may not allow sufficiently high

APPLICATIONS INFORMATION

or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate R_T resistor value see Table 3. An external resistor from the RT pin to GND is required—do not leave this pin open.

Table 2. Channel 1 Analog Dimming Register

ANALOG DIMMING REGISTER[BIT]	VALUE	SETTING
ADIM1[0]	0 1*	0 +1/256 of the Current Set by CTRL
ADIM1[1]	0 1*	0 +1/128 of the Current Set by CTRL
ADIM1[2]	0 1*	0 +1/64 of the Current Set by CTRL
ADIM1[3]	0 1*	0 +1/32 of the Current Set by CTRL
ADIM1[4]	0 1*	0 +1/16 of the Current Set by CTRL
ADIM1[5]	0 1*	0 +1/8 of the Current Set by CTRL
ADIM1[6]	0 1*	0 +1/4 of the Current Set by CTRL
ADIM1[7]	0 1*	0 +1/2 of the Current Set by CTRL

*Denotes Default Power-On Value.

Table 3. R_T Resistance Range

SWITCHING FREQUENCY	R_T (kΩ)
2MHz	27.4
1.8MHz	32.4
1.6MHz	36.5
1.4MHz	42.2
1.2MHz	49.9
1MHz	60.4
800kHz	78.7
600kHz	107
400kHz	169
500kHz	133
300kHz	232
200kHz	357

FREQUENCY SYNCHRONIZING AND CLOCK

The LT3964 switching frequency can be synchronized to an external clock using the SYNC/CLKOUT pin. For proper operation, the R_T resistor should be chosen for a switching frequency 10% lower than the external clock frequency. Observation of the following guidelines about the SYNC waveform will ensure proper operation of this feature. Driving SYNC/CLKOUT with a 50% duty cycle waveform is always a good choice, otherwise, maintain the duty cycle between 20% and 60%. If the SYNC/CLKOUT pin is not used, it should be connected to GND through a 20k resistor or left floating (an internal 100k connects their pin to GND).

CLOCK SYNCHRONIZATION OF ADDITIONAL REGULATORS

The SYNC/CLKOUT pin of the LT3964 can be used to synchronize one or more other compatible switching regulator ICs. The frequency of the master LT3964 is set by the external R_T resistor, and the RT pin of all slave ICs must have a resistor tied to ground. It is preferable for all slave ICs to have the same internal free-running frequency. This CLKOUT function is disabled initially after power on reset. To enable this function, CONFIG[6] in the master LT3964's chip configuration register (see Table 11), has to be set to logic high via I^2C interface. Note that the SYNC/CLKOUT pin is only meant to drive capacitive loads up to 50pF.

UNDERSTANDING THE CURRENT LIMIT

The LT3964 has a peak current limit of 1.8A (typical). The inductor current, however, may exceed 1.8A when the frequency is high and the output voltage is low as in a short circuit. This is because there is a minimum on-time for which the SW pin will be driven high each switching period. The inductor current increases during this time, and if the frequency is high and the output voltage low, there may not be enough off-time remaining in each switching period for the inductor current to decrease back to the level at which it started. In this case, the net inductor current would increase with each switching period regardless of the state of the CTRL pin. To prevent an unbounded inductor current that would damage the LT3964, the on-time is prohibited until the current decreases to less than the valley current limit (2A typical). The peak current may increase to 1.8A (typical), but the off-time and the switching period are extended until the inductor current

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reaches equilibrium.

The above scenario generally ensues only when the output voltage is shorted to ground. When instead the LED string is shorted to ground, the voltage across the external PWMTG MOSFET (described later) is often high enough that the required on-time is greater than the minimum on-time. This means the inductor current can remain in regulation even at the highest switching frequency.

SELECTING AN INDUCTOR

The LT3964 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. The inductor must be rated for the current limit regardless of the intended application.

In applications with 1µF or larger output filter cap and fixed output load, a good first choice of inductor can be as follows:

$$L = \frac{V_{OUT}}{1.2A \bullet f_{SW}}$$

In the above equation, V_{OUT} is the output voltage and f_{SW} is the switching frequency.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L$$

where $I_{LOAD(MAX)}$ is the maximum output load for a given application, and ΔI_L is the inductor ripple current as calculated in the following equation:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

In applications that have dynamic and time-varying output loads, there is usually no output capacitor. The input voltage of these applications is fixed and generated from a boost converter. The inductor ripples must be limited to meet EMI requirement. For a given inductor ripple ΔI_L, the inductor should be selected as follows:

$$L = \frac{V_{IN}}{4 \bullet \Delta I_L \bullet f_{SW}}$$

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring high PWM dimming ratio, the value of the inductor may be lower. But be aware that the low inductance may result in discontinuous mode operation. The manufacturers featured in Table 4 are recommended sources of inductors.

Table 4. Inductor Manufacturers

MANUFACTURER	WEBSITE
Würth Elektronik	www.we-online.com
Coilcraft	www.coilcraft.com
Vishay Inter Technology	www.vishay.com

SELECTING AN OUTPUT CAPACITOR

In applications with fixed LED load, the output capacitor has two essential functions. It is first responsible for filtering the inductor current ripple so that the LED current will have relatively little ripple. It also stabilizes the LT3964's current loop, since the LED string impedance and output capacitor form the 2nd dominating pole in the loop, usually between 10kHz and 40kHz. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The sizing of the output capacitor depends on the chosen switching frequency, the inductor value and equivalent LED string impedance. Use of a X7R or X5R type ceramic capacitor is recommended. For good starting values, see the Typical Applications section. Consult factory applications for more detailed information.

When choosing a capacitor, special attention should be given to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required. Sources of quality ceramic capacitors are listed in Table 5.

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Table 5. Capacitor Manufacturers

MANUFACTURER	WEBSITE
Murata	www.murata.com
TDK	www.tdk.com
Kemet	www.kemet.com
Taiyo Yuden	www.t-yuden.com
AVX	www.avx.com

STABILIZING THE REGULATION LOOP

The LT3964 uses a transconductance error amplifier with internal compensation. Thus, the current loop has the fixed dominant pole and the zero internally. To compensate the loop, a 2nd pole has to be formed outside of LT3964. For applications with an output capacitor, the output capacitor and the equivalent impedance form the 2nd pole. For applications with dynamic and time-varying output loads that have no output capacitor, the 2nd pole has to be formed between 10kHz and 40kHz with the LED sensing resistor R_{LED} as shown in Figure 2. The time constant of the 2nd pole is $C_{FILT}(R_{LED} + R_{FILT})$. ISN pin has typical 30µA loading current. To keep ISP-ISN threshold DC offset less than 0.6mV (typical), R_{FILT} has to be less than 20Ω.

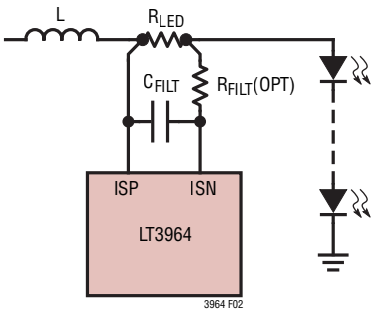

Figure 2. Forming 2nd Pole with R_{LED}

SELECTING THE INPUT CAPACITORS

Bypass the input of the LT3964 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT3964 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3964 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT3964 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3964. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3964 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3964's voltage rating. This situation can be easily avoided (see Analog Devices Application Note 88).

$INTV_{CC}$ REGULATOR

An internal low dropout (LDO) regulator produces the 4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT3964's circuitry and must be bypassed to ground with a minimum of 2.2µF X7R or X5R ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO.

PROGRAMMING INPUT UNDERVOLTAGE LOCKOUT

The LT3964 will stop switching and disable the PWMTG driver when the voltage at the EN/UVLO pin drops below precisely 1.18V, but internal circuitry will continue drawing current. A small 4µA pull-down current is active when EN/UVLO is below this threshold. Full shutdown is guaranteed when EN/UVLO is below 0.4V, and in full shutdown the LT3964 will draw less than 1µA.

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An external voltage source can be used to set the voltage at EN/UVLO and enable or disable the LT3964 at will. Alternatively, a resistor network can be placed between V_{IN} and EN/UVLO as shown in Figure 3. The following equations should be used to determine the values of the resistor:

$$V_{IN(FALLING)} = 1.18V \bullet \frac{R_{EN1}+R_{EN2}}{R_{EN1}}$$

$$V_{IN(RISING)} = 1.23V \bullet \frac{R_{EN1}+R_{EN2}}{R_{EN1}} + 4\mu A \bullet R_{EN2}$$

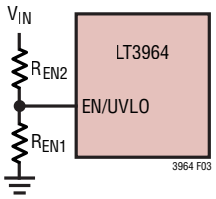

Figure 3. EN/UVLO Resistor Configuration

USING THE T_{SET} PIN FOR THERMAL PROTECTION

The LT3964 contains a special programmable thermal regulation loop that limits the internal junction temperature of the part. This thermal regulation feature provides important protection at high ambient, and allows a give application to be optimized for typical, not worst-case, ambient temperatures with the assurance that the LT3964 will automatically protect itself and the LED strings under worst-case conditions.

The operation of the thermal loop is simple. As the ambient temperature increases, so does the internal junction temperature is reached, the LT3964 begins to linearly reduce the LED current, as needed, to try and maintain this temperature. This can only be achieved when the ambient temperature stays below the desired maximum junction temperature. If the ambient temperature continues to rise past the programmed maximum junction temperature, the LEDs current will be reduced to approximately zero.

While this feature is intended to directly protect the LT3964, it can also be used to derate the LED current at high temperatures. Since there is a direct relationship between the LED current and LT3964 junction temperature, the T_{SET} function also provides some LED current derating at high temperatures.

Two external resistors program the maximum IC junction temperature using a resistor divider from the $INTV_{CC}$ pin, as shown in Figure 4. Choose the ratio R_{TSET1} and R_{TSET2} for the desired junction temperature. Figure 5 shows the relationship of T_{SET} voltage to junction temperature.

A 10nF capacitor in parallel with R_{TSET1} is recommended if the T_{SET} node picks up switching noise due to bad PCB layout practice.

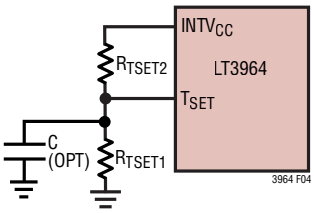

Figure 4. Programming the T_{SET}

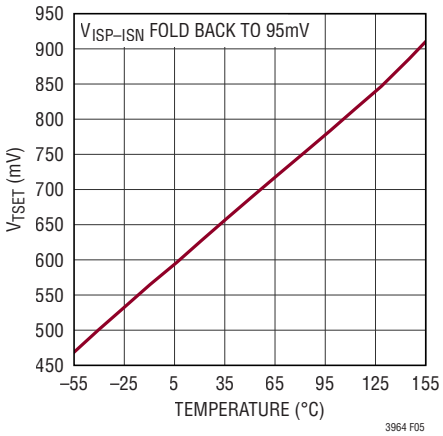

Figure 5. T_{SET} Pin Threshold vs Junction Temperature

SELECTING A MOSFET FOR PWM DIMMING

Pulse-width-modulation of the LED current is an effective way to control the brightness of the light without varying its color. The brightness can also be adjusted with finer resolution this way than by varying the current level.

The LT3964 features a PWMTG driver that is intended for a high-voltage PMOS switch in position to effect PWM dimming by connecting and disconnecting the string of LEDs from the output capacitor and the current sense resistor. When the switch is open and the string is disconnected, the LED current will be zero. In contrast to a low-side NMOS driver, this feature eliminates the need for a dedicated return path for the LED current in automotive applications or other grounded-chassis systems.

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A high side PMOS disconnected switch with a minimum VTH of –1V to –2V is recommended in most LT3964 applications. The drain-source voltage rating of the chosen PMOS should be greater than the maximum output voltage set by the FB pin and ID rating should be above I_{LED}. A diode with anode connected to ground and cathode to the drain of the PWMTG MOSFET as D1 shown in Figure 6 can protect that device from overvoltage caused by excessive inductance in the LED string. Table 6 lists three recommended manufacturers of PMOS devices.

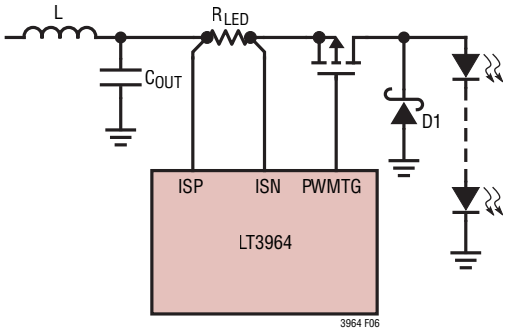

Figure 6. Catch Diode for Short Circuit Protection with Disconnect PMOS

Table 6. PMOS Manufacturers

MANUFACTURER	WEBSITE
Infineon Technologies	www.infineon.com
Vishay Inter Technology	www.vishay.com
Renesas Electronics	www.am.renesas.com

PROGRAMMING OUTPUT VOLTAGE (CONSTANT-VOLTAGE REGULATION) OR OUTPUT CLAMP

For applications that have fixed LED loads and output capacitor, the LT3964's voltage feedback pin FB can be used to program the OPENLED clamp voltage by selecting the values of R_{FB1} and R_{FB2} (see Figure 7) according to the following equation:

$$V_{OUT} = 1.18V \bullet \frac{R_{FB1}+R_{FB2}}{R_{FB1}}$$

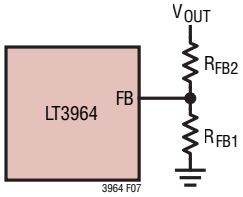

Figure 7. FB Resistor Configuration for Applications with Output Capacitor

If the OPENLED clamp voltage is programmed correctly using the resistor divider, then FB pin should never exceed 1.08V to guarantee that the LED current is only regulated by CTRL pin when the LEDs are connected. For best performance, set OPENLED clamp voltage about 10% higher than the maximum LED string voltage.

If the output voltage is near the maximum when the LED string breaks, it may take too long for the feedback loop to adjust the inductor current and avoid overcharging the output. Thus it is possible that the FB voltage can exceed the 1.18V regulation voltage momentarily. However, if the FB voltage exceeds 1.233V (typical), the overvoltage lockout threshold, the LT3964 will immediately stop switching and the PWMTG driver is turned off. Meanwhile, the STATUS[4] bit (for Channel 1) or STATUS[0] bit (for Channel 2) in the chip status register is written to logic high, and the $\overline{ALERT}$ pin is also asserted.

For applications with wide dynamic and time-varying LED loads, a 100nF capacitance is recommended at output node. However, if output node can still overshoot beyond V_{IN} during open circuit (OPENLED), then a Schottky diode is required to clamp output to V_{IN} shown in Figure 8. The BV rating of the Schottky has to be higher than maximum V_{IN}. Another Schottky diode is recommended to protect ISP and ISN from ringing below ground due to the excessive inductance in the LED string. To avoid falsely triggering SHORTLED (F_B < 250mV), a resistor from $INTV_{CC}$ to F_B is included to disable this feature.

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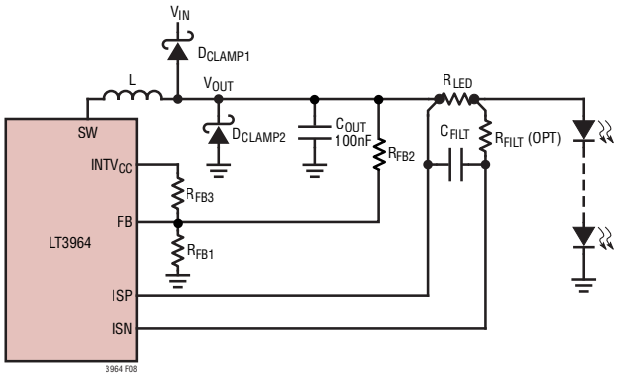

Figure 8. Output Clamp for Applications with No Output Capacitor

OPENLED DETECTION

To detect open-circuit condition at the output, the LT3964 monitors both output voltage and current. When FB exceeds V_{FB} – 53mV and $V_{(ISP-ISN)}$ is less than 10mV, the OPENLED status bit, STATUS[5] for (Channel 1) or STATUS[1] for (Channel 2) in the chip status register, is written to logic 1, and the $\overline{ALERT}$ pin is also asserted.

SHORTLED AND OVERCURRENT PROTECTION FEATURE

The resistor network formed by R_{FB1} and R_{FB2} also defines the criteria for short circuit (SHORTLED). For the LT3964, a short circuit is when FB is less than 250mV after initial start-up. STATUS[6] (for Channel 1) or STATUS[2] (for Channel 2) in the chip status register is set at the same time.

An application without direct output sensing is shown in Figure 6. LT3964 also monitors output overcurrent ($V_{(ISP-ISN)}$ > 930mV typically) to decide output short. Once an overcurrent is detected, STATUS[7] bit (for Channel 1) or STATUS[3] bit (for Channel 2) in the chip status register is set and $\overline{ALERT}$ pin will be pulled low simultaneously.

In both cases, LT3964 stops switching and pulls PWMTG high intermediately to disconnect the LED array from the power path as shown in Figure 9.

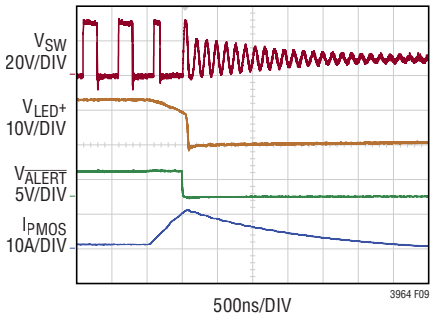

Figure 9. PWMTG Response to Short Circuit Fault

LT3964 has two different ways to respond to SHORTLED or OC fault: hiccup or latchoff. The default is hiccup. Once a fault is detected, an internal fault timer starts. When the timer expires and the fault disappears, the LT3964 will re-startup. The PWMTG is pulled high, and switching starts after a fixed internal soft start time. Figures 10 and 11 show the LT3964 response to a short circuit fault in hiccup mode. In I²C mode, the $\overline{ALERT}$ pin is kept asserted even though the fault is removed, whereas the $\overline{ALERT}$ pin is de-asserted in non-I²C mode.

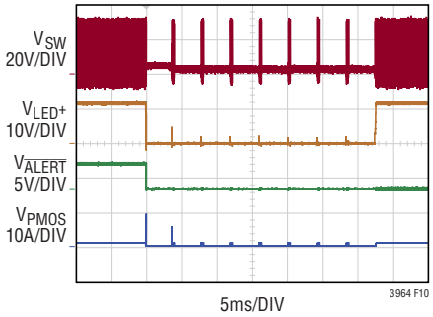

Figure 10. Hiccup Response to Short Circuit Fault in I²C Mode

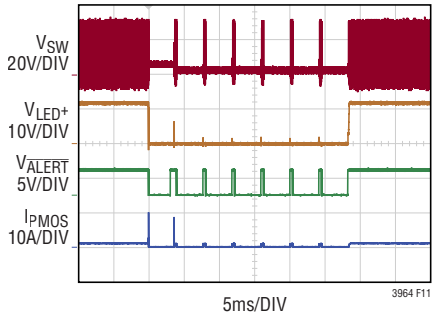

Figure 11. Hiccup Response to Short Circuit Fault in Non-I²C Mode

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Latch-off mode is another way that the LT3964 can be programmed to respond to faults. When a fault happens, the CONFIG[7] in the chip configuration register (see Table 11) is set via I^2C, and LT3964 will stop switching and pull PWMTG pin high immediately. LT3964 will stay non-switching even if all faults have been removed as shown in Figure 12. To exit latchoff mode, the EN/UVLO pin must be toggled low to high.

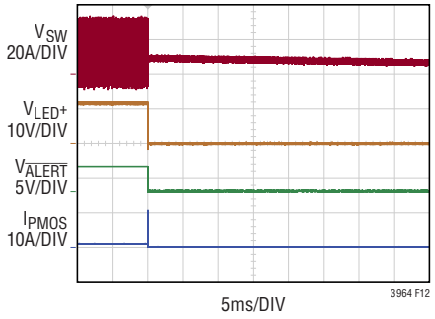

Figure 12. Latch-off Response to a Short Circuit Fault

PRECAUTIONS REGARDING REVERSED INPUT CURRENT

LT3964 is not designed to run a large reversed input current, greater than 200mA continuously, from SW pin to the V_{IN} pin through the top switch when the top switch is in off state. This cautionary note explains the situation where this potentially damaging condition can develop, and what measures can be taken to protect the top switch if this condition is likely. Small negative inductor currents, 100mA or less, are expected and acceptable for periods less than a switching cycle. This is expected during normal operation at low LED current. One event that causes large, potentially damaging negative inductor currents to flow through the parasitic body diode of the top switch is a ground fault on the supply when the output is charged. This input fault event is not common, but the user should be aware of it. The three conditions which, when seen together, are more likely to lead to a potentially damaging reverse current level while the top switch is off are:

1. The buck output voltage is almost equal to V_{IN} supply;
2. The output voltage is high at the beginning of the switching cycle; and
3. The inductor current is close to zero when the low side turns on briefly to charge the BST capacitor

The reason these three conditions can lead to sustained negative inductor current is because when the bottom switch is ON, big voltage is seen across inductor to cause a large negative inductor ripple even for 40ns period of time (bottom switch minimum ON time). After the bottom switch turns off, both switches are in off state for the remaining switch cycle. Thus the negative inductor current continues to flow backwards through the top switch body diode for an extended period of time due to little voltage across the inductor. The V_{IN} equal to V_{OUT} condition can be encountered during an OPENLED event if the constant voltage regulation is set close to V_{IN}; and alternatively, if V_{IN} drops to a level where the LED V_f is close to V_{IN}. In the former instance (OPENLED) the switching will be discontinuous since there is no load, so inductor current is likely going negative during BST refresh cycle when low switch is on. If this operational condition is expected (i.e., $V_{OUT}/(V_{OUT} - V_{IN}) > 10$), a 10µH or larger value inductor will prevent generating a large negative inductor current during brief pulse on the synchronous FET. For applications that are running at high die temperature over 125°C, a Schottky diode is strongly suggested to provide extra protection and bypass negative inductor current around the top switch, as shown in Figure 13.

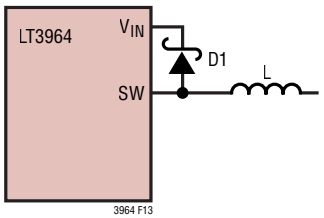

Figure 13. Reverse Input Current Protection

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CHANNEL-LEVEL $\overline{\text{ALERT}}$ REPORTING

When a channel-level fault happens, the LT3964 will set the corresponding reporting bit in the chip status register (see Table 7), which is also latched until the master sends a command to reset it. If the corresponding bit in the chip status register (see Table 8) is high, LT3964 will report this fault by pulling down the $\overline{\text{ALERT}}$ pin.

Table 7. Chip Status Register

CHIP STATUS REGISTER[BIT]	VALUE	SETTING
STATUS[0]	0* 1	Ch1 Output Voltage Normal Ch1 Output Overvoltage (OVFB)
STATUS[1]	0* 1	Ch1 LED Normal Ch1 LED Open (OPENLED)
STATUS[2]	0* 1	Ch1 LED Normal Ch1 LED Shorted (SHORTLED)
STATUS[3]	0* 1	Ch1 Output Current Normal Ch1 Output Overcurrent (OC)
STATUS[4]	0* 1	Ch2 Output Voltage Normal Ch2 Output Overvoltage (OVFB)
STATUS[5]	0* 1	Ch2 LED Normal Ch2 LED Open (OPENLED)
STATUS[6]	0* 1	Ch2 LED Normal Ch2 LED Shorted (SHORTLED)
STATUS[7]	0* 1	Ch2 Output Current Normal Ch2 Output Overcurrent (OC)

*Denotes Default Power-On Value.

Table 8. Chip Status Enable Register

CHIP STATUS ENABLE REGISTER[BIT]	VALUE	SETTING
STATEN[0]	0 1*	Disable Reporting Ch1 OVFB Enable Reporting Ch1 OVFB
STATEN [1]	0 1*	Disable Reporting Ch1 OPENLED Enable Reporting Ch1 OPENLED
STATEN [2]	0 1*	Disable Reporting Ch1 SHORTLED Enable Reporting Ch1 SHORTLED
STATEN [3]	0 1*	Disable Reporting Ch1 OC Enable Reporting Ch1 OC
STATEN [4]	0 1*	Disable Reporting Ch2 OVFB Enable Reporting Ch2 OVFB
STATEN [5]	0 1*	Disable Reporting Ch2 OPENLED Enable Reporting Ch2 OPENLED
STATEN [6]	0 1*	Disable Reporting Ch2 SHORTLED Enable Reporting Ch2 SHORTLED
STATEN [7]	0 1*	Disable Reporting Ch2 OC Enable Reporting Ch2 OC

*Denotes Default Power-On Value.

The LT3964 will respond to the master alert response inquiry (ARI) by sending back the chip address. If operated in I^2C mode, the $\overline{\text{ALERT}}$ pin is kept asserted until the transfer is successfully completed. After that, the LT3964 will not respond to future ARI requests until a new alert event occurs and $\overline{\text{ALERT}}$ pin is asserted again. Once the master receives the chip address, the master will decide whether to read back the full alert information from LT3964 and reset the chip status register. To minimizing the alert reporting, LT3964 doesn't report the same fault over again if the corresponding STATUS bit is not cleared.

In non-I^2C mode, the LT3964 reports faults independent of the I^2C register. Whenever LT3964 detects OVFB and OPENLED faults, the $\overline{\text{ALERT}}$ pin is asserted. SHORTLED and OC faults usually keep $\overline{\text{ALERT}}$ pin asserted until the internal soft-start fault timer expires and the faults have been removed.

PWM DIMMING CONTROL FOR BRIGHTNESS

PWM dimming is used to modulate the LED current between zero and full current to achieve a precisely programmed average current, without the possibility of color shift that occurs at low current in LEDs. To make PWM dimming more accurate, the switch demand current is stored on the internal VC node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase. The minimum PWM on or off time depends on the choice of operating frequency set by the RT input. For best current accuracy, the minimum PWM high time should be at least two switching cycles (1µs for f_{SW} = 2MHz).

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A low duty cycle PWM signal can cause excessive start-up times if it were allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated, the LT3964 will ignore a logical disable by the PWM input signal. The device will continue to soft-start with switching and TG enabled until either the internal soft-start time expires or the output current reaches one-fifth of the full-scale current. At this point the device will begin following the dimming control as designated by PWM pin input or PWM input via I^2C.

The internal PWM dimming signal is controlled by both PWM pin input (PWMEXT) and I^2C PWM registers (CH1PWM1, CH1PWM2, CH2PWM1, CH2PWM2). In non-I^2C mode, the PWM registers output are set to 1 permanently, thus the internal PWM dimming signal is only gated by PWMEXT. In I^2C mode, PWM registers are initially set to 0 after power on reset. It can be updated according to intended dimming frequency and dimming duty cycle. The PWM registers for Channel 1 shown in Tables 9 and 10 have the following outputs:

$$\text{PWM Frequency} = \frac{f_{SW}}{2^{(SCALE[2:0]+6)}}$$

$$\text{PWM Duty Cycle} = \frac{CH1_ON[SCALE[2:0]+5:0]}{2^{(SCALE[2:0]+6)}}$$

where f_{SW} is the switching frequency. For example, if SCALE[2:0] = 7, then the PWM frequency is $f_{SW}/8192$, and the PWM duty cycle is CH1_ON[12:0]/8192. If SCALE[2:0] = 0, then PWM frequency is $f_{SW}/64$. The higher order bits, CH1_ON[12:6], are neglected and PWM duty cycle is defined by CH1_ON[5:0]/64.

Note the maximum achievable PWM duty cycle set by PWM registers is 8191/8192. To achieve 100% PWM dimming, the CONFIG[3]/[2] in the chip configuration register has to be cleared. Usually PWM registers offer better PWM dimming performance as the dimming control signals are aligned up with the internal clock.

The LT3964 can drive a LED string in either PWM (pulse width modulation) mode or BAM (Bit Angle Modulation) mode that is set by the combination of CONFIG[3]/[2] and CONFIG[1]/[0] as shown in Tables 11 and 12. Bit Angle Modulation (BAM) is a LED drive technique that can be used with fixed or variable frequency modulation. In essence, the LED is driven by a pulse train that is the binary word defining the value of required intensity. Each bit of the pulse train is stretched by a ratio defined by the binary significance of each bit (CH1_ON[bit] or CH2_ON[bit]). Table 13 shows the ratio by which each bit is stretched, and Figure 14 shows an BAM example for CH1_ON[6:0] = 001101b and SCALE[2:0] = 000b.

Table 9. Channel 1 (CH1) PWM Register 1 (CH1PWM1)

CH1 PWM REGISTER1[BIT]	VALUE	SETTING
CH1PWM1[0]	0* 1	PWMON Time 5th MSB CH1_ON[8] = 0 PWMON Time 5th MSB CH1_ON [8] = 1
CH1PWM1[1]	0* 1	PWMON Time 4th MSB CH1_ON [9] = 0 PWMON Time 4th MSB CH1_ON [9] = 1
CH1PWM1[2]	0* 1	PWMON Time 3rd MSB CH1_ON[10] = 0 PWMON Time 3rd MSB CH1_ON [10] = 1
CH1PWM1[3]	0* 1	PWMON Time 2nd MSB CH1_ON[11] = 0 PWMON Time 2nd MSB CH1_ON [11] = 1
CH1PWM1[4]	0* 1	PWMON Time MSB CH1_ON[12] = 0 PWMON Time MSB CH1_ON[12] = 1
CH1PWM1[5]	0* 1	PWMON FREQ Scalar LSB SCALE[0] = 0 PWMON FREQ Scalar LSB SCALE[0] = 1
CH1PWM1[6]	0* 1	PWMON FREQ Scalar 2nd MSB SCALE[1] = 0 PWMON FREQ Scalar 2nd MSB SCALE[1] = 1
CH1PWM1[7]	0* 1	PWMON FREQ Scalar MSB SCALE[2] = 0 PWMON FREQ Scalar MSB SCALE[2] = 1

*Denotes Default Power-On Value for I^2C Mode. PWMON Denotes PWM-ON TIME. FREQ Denotes PWM Frequency.

APPLICATIONS INFORMATION

Table 10. Channel 1 (CH1) PWM Register 2 (CH1PWM2)

CH1 PWM REGISTER2 [BIT]	VALUE	SETTING
CH1PWM2[0]	0* 1	PWMON Time LSB CH1_ON[0] = 0 PWMON Time LSB CH1_ON[0] = 1
CH1PWM2[1]	0* 1	PWMON Time 12th MSB CH1_ON[1] = 0 PWMON Time 12th MSB CH1_ON[1] = 1
CH1PWM2[2]	0* 1	PWMON Time 11th MSB CH1_ON[2] = 0 PWMON Time 11th MSB CH1_ON[2] = 1
CH1PWM2[3]	0* 1	PWMON Time 10th MSB CH1_ON[3] = 0 PWMON Time 10th MSB CH1_ON[3] = 1
CH1PWM2[4]	0* 1	PWMON Time 9th MSB CH1_ON[4] = 0 PWMON Time 9th MSB CH1_ON[4] = 1
CH1PWM2[5]	0* 1	PWMON Time 8th MSB CH1_ON[5] = 0 PWMON Time 8th MSB CH1_ON[5] = 1
CH1PWM2[6]	0* 1	PWMON Time 7th MSB CH1_ON[6] = 0 PWMON Time 7th MSB CH1_ON[6] = 1
CH1PWM2[7]	0* 1	PWMON Time 6th MSB CH1_ON[7] = 0 PWMON Time 6th MSB CH1_ON[7] = 1

*Denotes Default Power-On Value for I^2C Mode.

Table 11. Chip Configuration Register

CHIP CONFIGURATION REGISTER [BIT]	VALUE	SETTING
CONFIG[0]	0* 1	Channel 2 PWM Mode Channel 2 BAM Mode
CONFIG[1]	0* 1	Channel 1 PWM Mode Channel 1 BAM Mode
CONFIG[2]	0 1*	Channel 2 PWM Registers' Output Disabled (Always On) Channel 2 PWM Registers' Output Enabled
CONFIG[3]	0 1*	Channel 1 PWM Registers' Output Disabled (Always On). Channel 1 PWM Registers' Output Enabled
CONFIG[4]	x	Not Used
CONFIG[5]	x	No Used
CONFIG[6]	0* 1	Clock Output Disabled Clock Output Enabled
CONFIG[7]	0* 1	Latchoff Mode Disabled Latchoff Mode Enabled

*Denotes Default Power-On Value for I^2C Mode. BAM Denotes Bit Angle Modulation.

Table 12. I^2C PWM Dimming Setting

CONFIG[3]/[2]	CONFIG[1]/[0]	ACTION
1	1	Bit Angle Modulation
1	0	Regular Pulse Width Modulation
0	x	I^2C PWM Dimming Disabled (Always On)

Table 13. Stretch Ratio of Each PWMON Bit

BIT POSITION	STRETCHED BY
CH1_ON[12]	4096
CH1_ON[11]	2048
CH1_ON[10]	1024
CH1_ON[9]	512
CH1_ON[8]	256
CH1_ON[7]	128
CH1_ON[6]	64
CH1_ON[5]	32
CH1_ON[4]	16
CH1_ON[3]	8
CH1_ON[2]	4
CH1_ON[1]	2
CH1_ON[0]	1

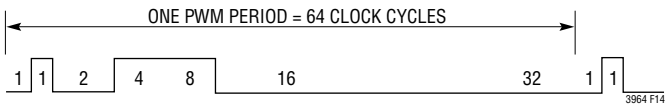


Figure 14. BAM Example

APPLICATIONS INFORMATION

I²C OPERATION

I²C Interface

The LT3964 communicates with a bus master using the standard I²C 2-wire interface. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LT3964 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL have TTL thresholds (min 1.5V high threshold and max 0.4V low threshold). I²C internal logic gates are powered from $INTV_{CC}$. When $INTV_{CC}$ is below approximately 3.2V, the I²C serial port is reset to power-on states and registers are set to default values.

I²C Bus Speed

The I²C port operates at speeds up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I²C START and STOP Conditions

Figure 15 shows I²C port timing information. A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LT3964, the master may transmit a STOP condition that commands the LT3964 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LT3964 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LT3964 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LT3964 is written to, it acknowledges its write address and subsequent register address and data bytes. When reading from the LT3964, it acknowledges its read address and 8-bit status byte. An acknowledge pulse (active LOW) generated by the LT3964 lets the master know that the latest byte of information was transferred. The master generates the clock cycle and releases the SDA line (HIGH) during the acknowledge clock cycle. The LT3964 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

I²C Device Addressing

Eight distinct bus addresses are configurable using ADDR2 and ADDR1 pins. Table 14 shows the correspondence between ADDR2 and ADDR1 pin states and addresses. The least significant bit of the address byte, known as the read/write bit, is 0 when writing data to the LT3964 and 1 when reading from it. There is also one global address available at 0001100R/W to send or inquire information from all slaves on the same I²C bus (see I²C broadcast mode for more information).

Table 14. Slave Address Map (110 A3 A2 A1 A0 R/W)

ADDR2	ADDR1	A3	A2	A1	A0
GND	FLOAT	0	0	0	1
GND	$INTV_{CC}$	0	0	1	1
FLOAT	GND	0	1	0	0
FLOAT	FLOAT	0	1	0	1
FLOAT	$INTV_{CC}$	0	1	1	1
$INTV_{CC}$	GND	1	1	0	0
$INTV_{CC}$	FLOAT	1	1	0	1
$INTV_{CC}$	$INTV_{CC}$	1	1	1	1
GND*	GND	0	0	0	0

*Non-I²C Mode: Internal PWM Dimming Function is Disabled.

APPLICATIONS INFORMATION

I²C Sub-Addressed Writing

The LT3964 has 9 command registers that can be accessed by the I²C port via a sub-addressed writing system. Each write cycle of the LT3964 consists of a series of three bytes beginning with the LT3964 write address. The second byte is the sub-address of the command register being written to. The sub-address is a pointer to the register where the data in the third byte will be stored. The third byte is the data to be written to the just-received sub-address.

I²C Bus Write Operation

The master initiates communication with the LT3964 with a START condition and the LT3964 write address. If the address matches that of the LT3964, the LT3964 returns an acknowledge pulse. The master should then deliver the sub-address. Again the LT3964 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledgement by the LT3964. If desired a REPEAT-START condition may be initiated by the master where another device on the I²C bus is addressed. The LT3964 remembers the valid data it has received. Once all the devices on the I²C have been addressed and sent valid data and a global STOP has been sent, the LT3964 will update its command latches with the data it has received. Figure 16 shows the LT3964 I²C serial port write pattern.

I²C Sub-Addressed Reading

The LT3964 I²C interface supports random address reading of the I²C command and status registers. Before reading a register, the register's sub-address must be written. Send a START condition followed by the LT3964 write address followed by the sub-address of the register to be read. The sub-address is now stored as a pointer to the register. Send a REPEAT-START condition followed by the LT3964 read address. Following the acknowledgment of its read address the LT3964 returns one bit of information for each of the next 8-clock cycles. A STOP condition is not required for the read operation. The read sub-address is stored until a new sub-address is written. Verify the data written to the internal data hold latches prior to committing data to the command registers by reading back the data before sending a STOP condition. Continuously poll a register by repeatedly sending a START condition followed by the LT3964 read address, and then clocking the data out after the read address acknowledge. Figure 17 shows the LT3964 I²C serial port read pattern.

I²C Command and Status Registers

There are nine I²C command/status registers and three read-only I²C part number registers in the LT3964. All of the information for these registers is shown in Tables 15.

I²C Broadcast (BCMODE)

The BCMODE write command (0001 1000) is used to synchronize the PWM dimming cycles among the multiple LT3964 slaves on the I²C bus. The LT3964 slaves must be operating with a common external clock in order to be synchronized. The command does not modify any register bits. It only resets each channel counter to synchronize the dimming cycles.

APPLICATIONS INFORMATION

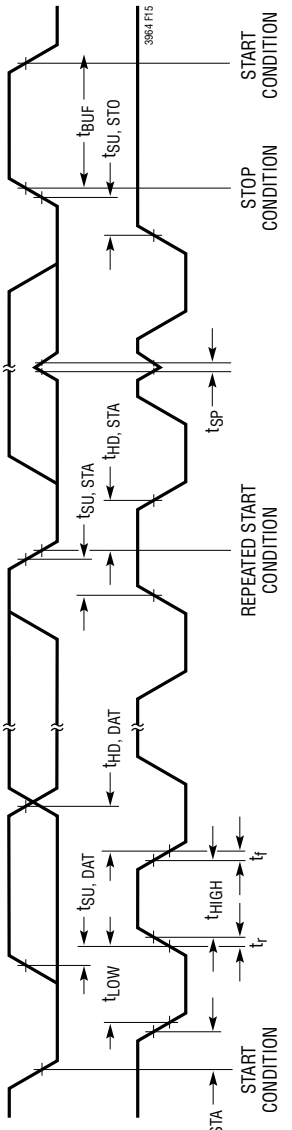


Figure 15. I²C Serial Port Timing

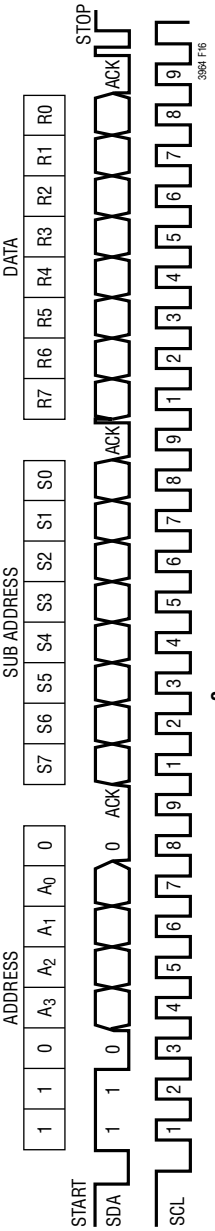


Figure 16. LT3964 I²C Serial Port Multiple Write Pattern

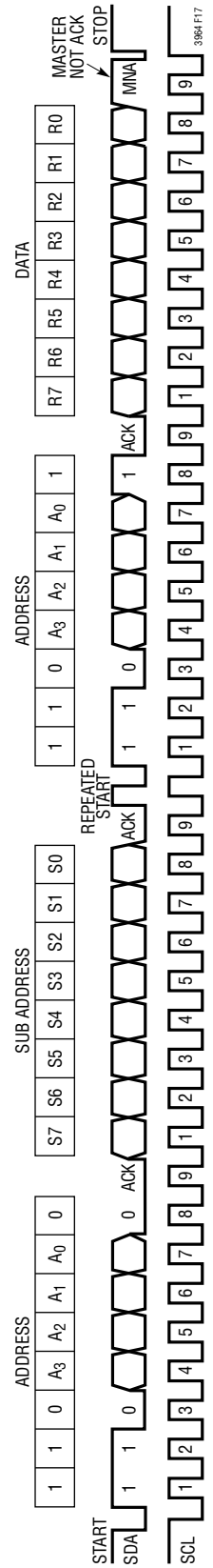


Figure 17. LT3964 I²C Serial Port Read Pattern

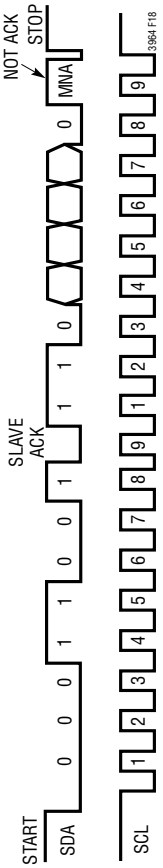


Figure 18. LT3964 I²C Serial Port Broadcast Read Pattern

APPLICATIONS INFORMATION

Table 15. LT3964 Command Register Table

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x01	CONFIG	Latchoff Mode Enable Bit 0 = Disabled 1 = Enabled	Clock Output Enable Bit 0 = Disabled 1 = Enabled	Not Used	Not Used	Channel 1 Pulse Dim Enable Bit 0 = Disabled (Always On) 1 = Enabled	Channel 2 Pulse Dim Enable Bit 0 = Disabled (Always On) 1 = Enabled	Channel 1 Pulse Dim Type Bit 0 = PWM Mode 1 = BAM Mode	Channel 2 Pulse Dim Type Bit 0 = PWM Mode 1 = BAM Mode	00xx 1100
0x02	CH1PWM1	Channel 1 PWM FREQ Scalar MSB	Channel 1 PWM FREQ Scalar 2nd MSB	Channel 1 PWM FREQ LSB	Channel 1 PWM ON Time MSB	Channel 1 PWM ON Time 2nd MSB	Channel 1 PWM ON Time 3rd MSB	Channel 1 PWM ON Time 4th MSB	Channel 1 PWM ON Time 5th MSB	0000 0000
0x03	CH1PWM2	Channel 1 PWM ON Time 6th MSB	Channel 1 PWM ON Time 7th MSB	Channel 1 PWM ON Time 8th MSB	Channel 1 PWM ON Time 9th MSB	Channel 1 PWM ON Time 10th MSB	Channel 1 PWM ON Time 11th MSB	Channel 1 PWM ON Time 12th MSB	Channel 1 PWM ON Time LSB	0000 0000
0x04	CH2PWM1	Channel 2 PWM FREQ Scalar MSB	Channel 2 PWM FREQ Scalar 2nd MSB	Channel 2 PWM FREQ LSB	Channel 2 PWM ON Time MSB	Channel 2 PWM ON Time 2nd MSB	Channel 2 PWM ON Time 3rd MSB	Channel 2 PWM ON Time 4th MSB	Channel 2 PWM ON Time 5th MSB	0000 0000
0x05	CH2PWM2	Channel 2 PWM ON Time 6th MSB	Channel 2 PWM ON Time 7th MSB	Channel 2 PWM ON Time 8th MSB	Channel 2 PWM ON Time 9th MSB	Channel 2 PWM ON Time 10th MSB	Channel 2 PWM ON Time 11th MSB	Channel 2 PWM ON Time 12th MSB	Channel 2 PWM ON Time LSB	0000 0000
0x06	ADIM1	Channel 1 Analog Dimming MSB	Channel 1 Analog Dimming 2nd MSB	Channel 1 Analog Dimming 3rd MSB	Channel 1 Analog Dimming 4th MSB	Channel 1 Analog Dimming 5th MSB	Channel 1 Analog Dimming 6th MSB	Channel 1 Analog Dimming 7th MSB	Channel 1 Analog Dimming LSB	1111 1111
0x07	ADIM2	Channel 2 Analog Dimming MSB	Channel 2 Analog Dimming 2nd MSB	Channel 2 Analog Dimming 3rd MSB	Channel 2 Analog Dimming 4th MSB	Channel 2 Analog Dimming 5th MSB	Channel 2 Analog Dimming 6th MSB	Channel 2 Analog Dimming 7th MSB	Channel 2 Analog Dimming LSB	1111 1111
0x08	STATEN	Channel 2 Overcurrent Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 2 SHORTLED Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 2 OPENLED Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 2 Overvoltage Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 1 Overcurrent Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 1 SHORTLED Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 1 OPENLED Reporting Enable Bit 0 = Disabled 1 = Enabled	Channel 1 Overvoltage Reporting Enable Bit 0 = Disabled 1 = Enabled	1111 1111
0x09	STATUS	Channel 2 Overcurrent Reporting Bit 0 = NO 1 = YES	Channel 2 SHORTLED Reporting Bit 0 = NO 1 = YES	Channel 2 OPENLED Reporting Bit 0 = NO 1 = YES	Channel 2 Overvoltage Reporting Bit 0 = NO 1 = YES	Channel 1 Overcurrent Reporting Bit 0 = NO 1 = YES	Channel 1 SHORTLED Reporting Bit 0 = NO 1 = YES	Channel 1 OPENLED Reporting Bit 0 = NO 1 = YES	Channel 1 Overvoltage Reporting Bit 0 = NO 1 = YES	0000 0000

APPLICATIONS INFORMATION

The BCMODE read command (0001 1001) is used to inquire about which LT3964 slave on the bus is sending the alert (see Alert Response Protocol section for details). This command is two bytes long. The first byte is the broadcast read address 00011001. The second byte $110A_3A_2A_1A_00$ is sent by the alerting slave, where $A_3A_2A_1A_0$ is an input logic value from the programmable address select pins ADDR2 and ADDR1 shown in Table 14. Figure 18 shows LT3964 BCMODE read pattern.

$\overline{\text{ALERT}}$ RESPONSE PROTOCOL

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt. The master initiates the ARA procedure with a START condition and the special 7-bit ARA bus address (0001100) followed by the read bit (R) = 1. If the LT3964 is asserting the $\overline{\text{ALERT}}$ pin, it acknowledges and responds by sending its 7-bit bus address ($110A_3A_2A_1A_0$) and a 0. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LT3964 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LT3964 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LT3964 will de-assert its $\overline{\text{ALERT}}$ pin and will not respond to further ARA requests until a new alert event occurs.

DESIGNING THE PRINTED CIRCUIT BOARD

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Usually, large switched currents flow through the local input capacitors and the V_{IN} and GND pins. The loops traveled by these currents should be made as small as possible by keeping the capacitors as close as possible to these pins. These capacitors, as well as the large inductor, should be placed on the same side of the board as the LT3964 and connected on the same layer. Other large, bulk input capacitors can be safely placed farther from the chip and on the other side of the board.

Create a Kelvin ground network by keeping the ground connection for all of the other components separate. It should only join the ground for the input and output capacitors and the return path for the LED current at the exposed pad. To keep thermal resistance low, extend the ground plane as much as possible, and thermal vias under and near the LT3964 to additional ground planes within the circuit board and on the bottom side.

There are a few other aspects of the board design that improve performance. Likewise minimizing the area of the SW and BST nodes reduces noise. The traces for FB pins should be kept short to lessen the susceptibility of these high impedance nodes to noise. Minimizing the connections from the external current sense resistor R_{LED} to the ISP and ISN pins are essential for current regulation accuracy. The $INTV_{CC}$ bypass capacitor as well as the BST capacitor should be placed as closely as possible to their respective pins.

Figure 19 shows the simplified two sided layout of power component placement with traces, ground plane and via locations. Note that the 4-layer layout is recommended for best performance. Please contact the factory for the reference layout design.

APPLICATIONS INFORMATION

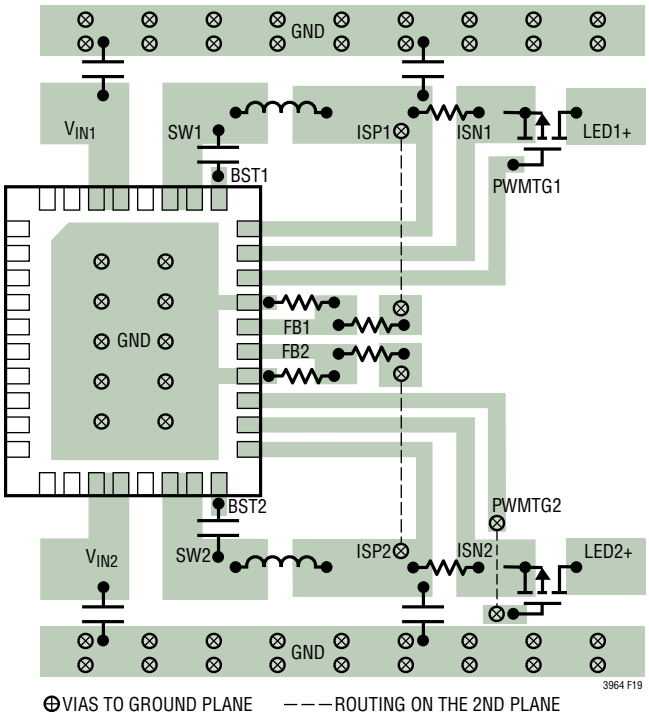
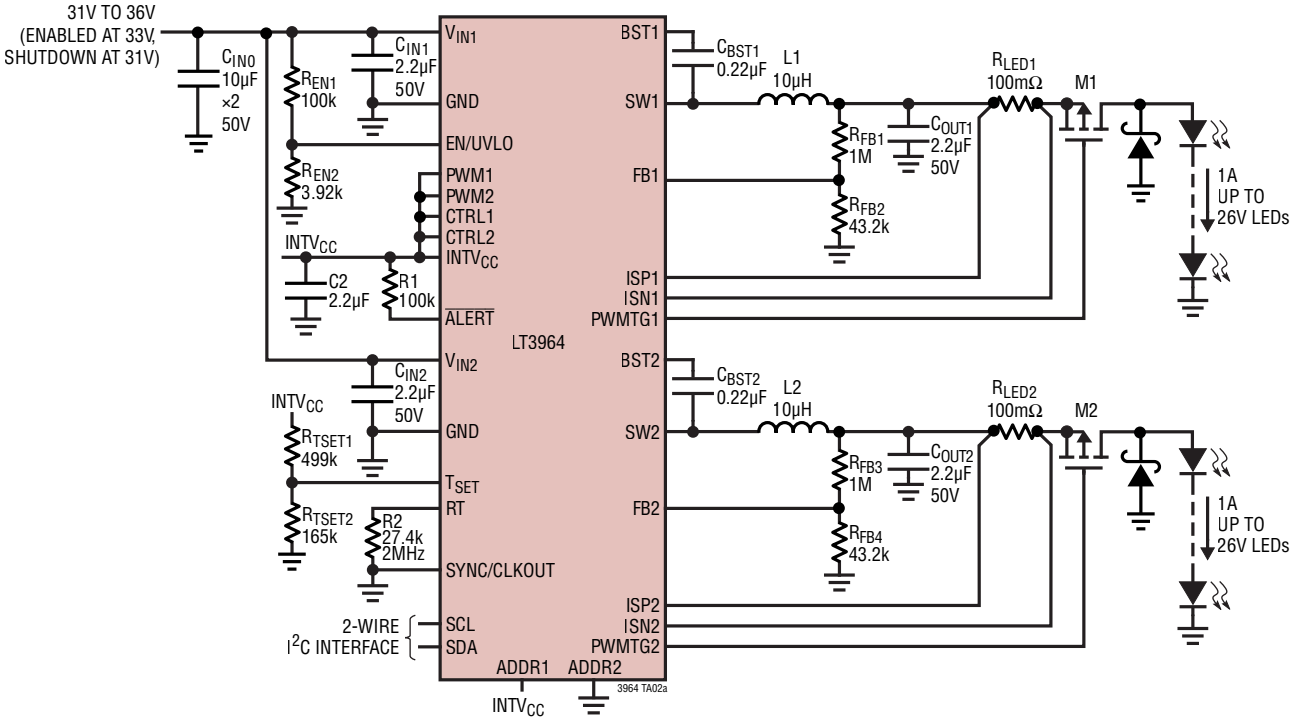


Figure 19. Simplified Layout for Dual Buck LED Driver

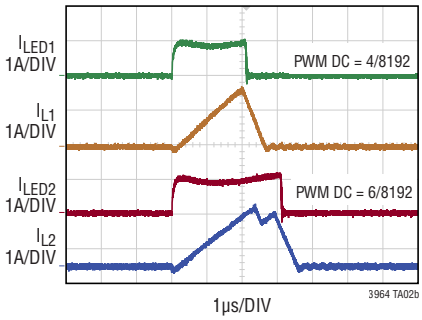
TYPICAL APPLICATIONS

Short-LED Robust, 50W Dual Buck 1A LED Driver with Internal PWM Dimming



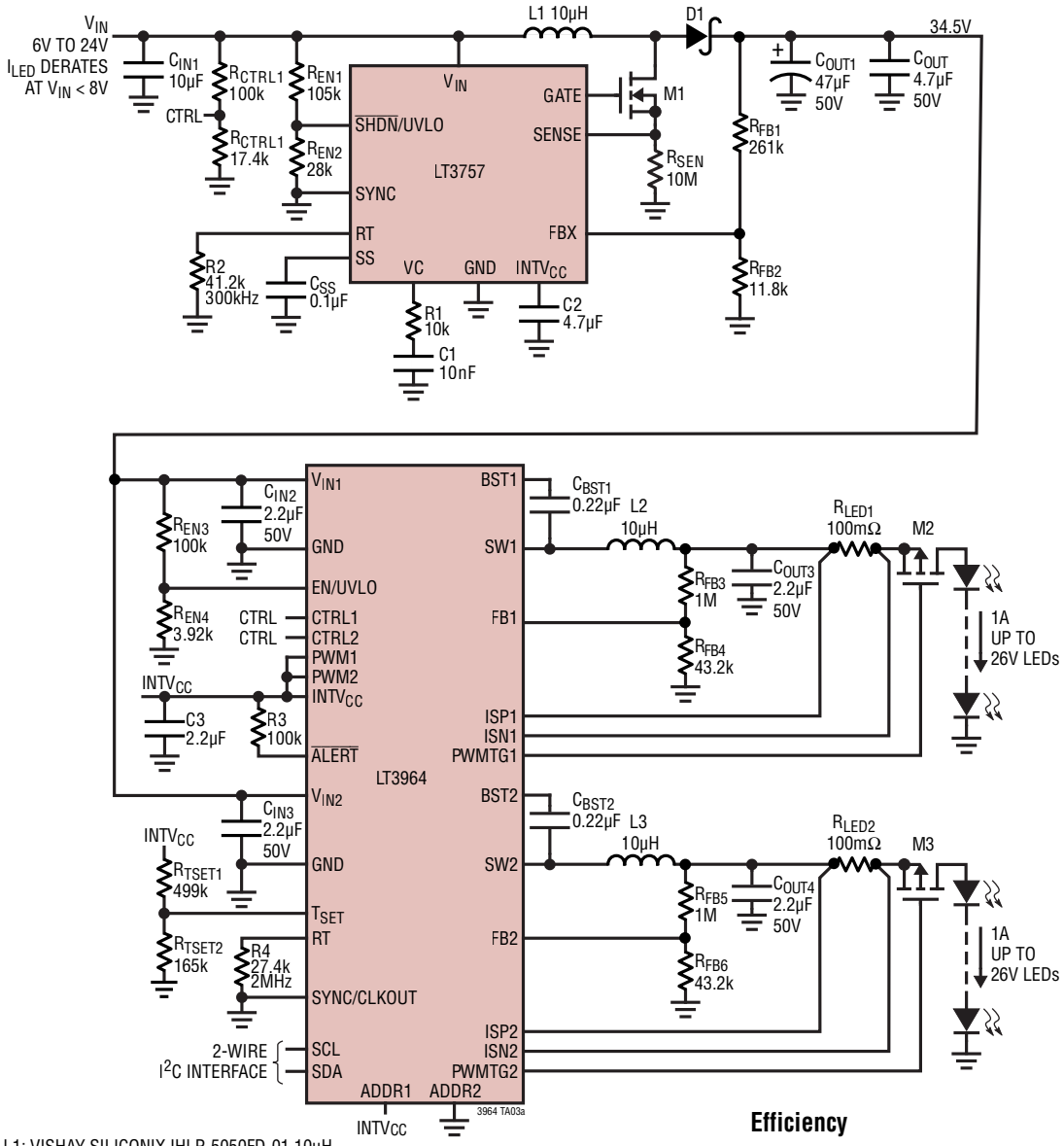
L1, L2: WURTH 74437349100
M1, M2: VISHAY Si2319CDS

PWM Dimming at V_{IN} = 34V



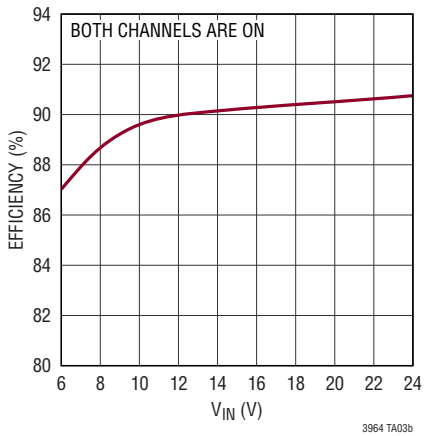
TYPICAL APPLICATIONS

Multi-Channel Boost Buck LED Driver



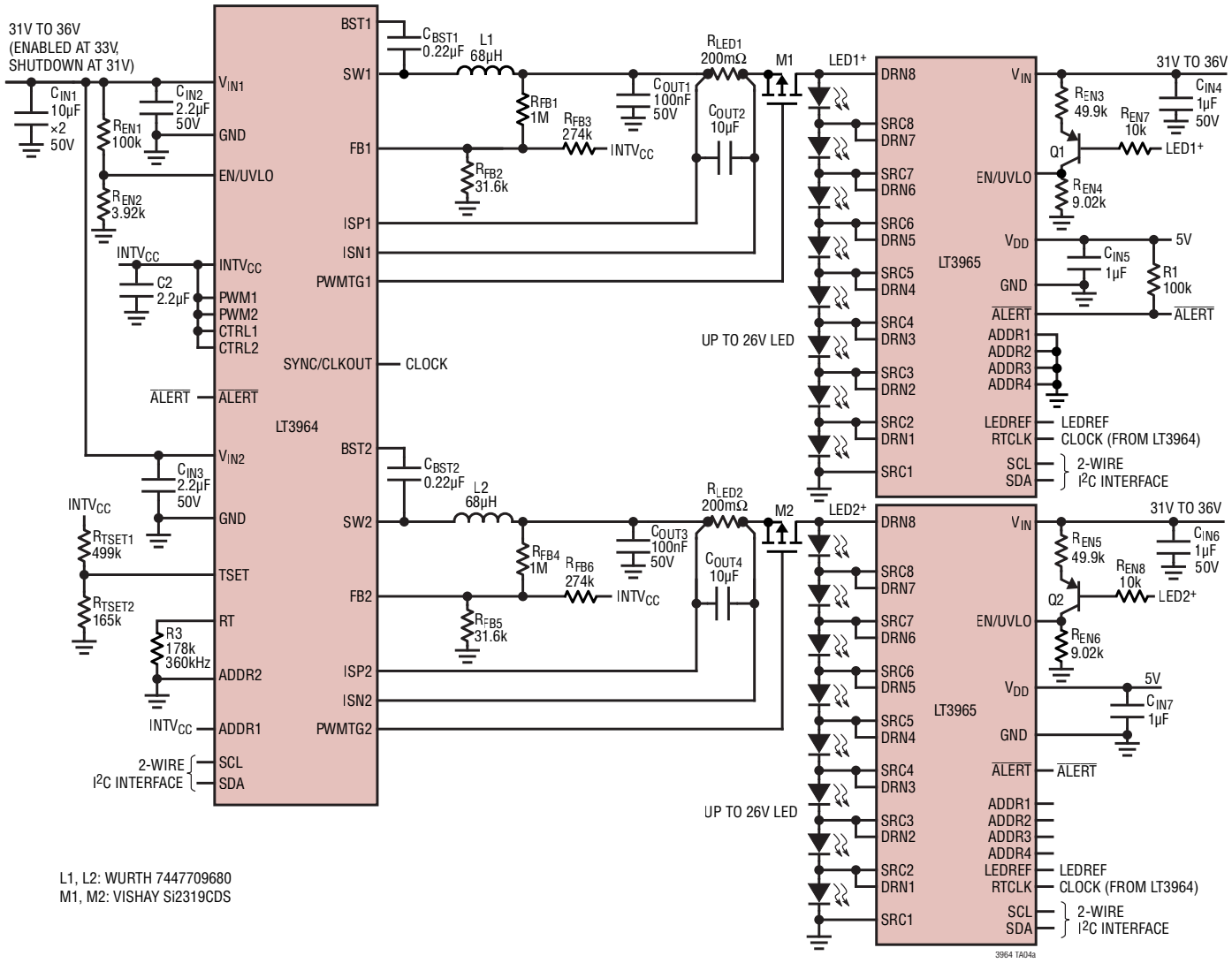
L1: VISHAY SILICONIX IHLP-5050FD-01 10µH
L2, L3: WURTH 74437349100
M1: INFINEON BSC030N04NS
M2, M3: VISHAY Si2319CDS
D1: DIODES PDS1040

Efficiency



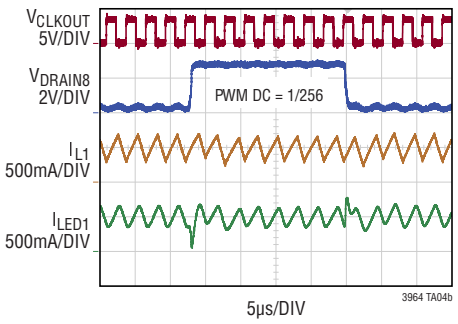
TYPICAL APPLICATIONS

Matrix LED Driver

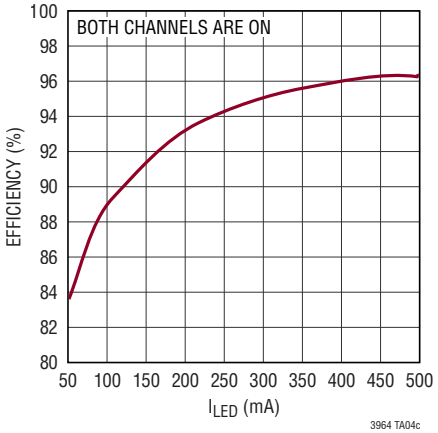


L1, L2: WURTH 7447709680
M1, M2: VISHAY Si2319CDS

Single LED PWM Dimming at V_{IN} = 34V



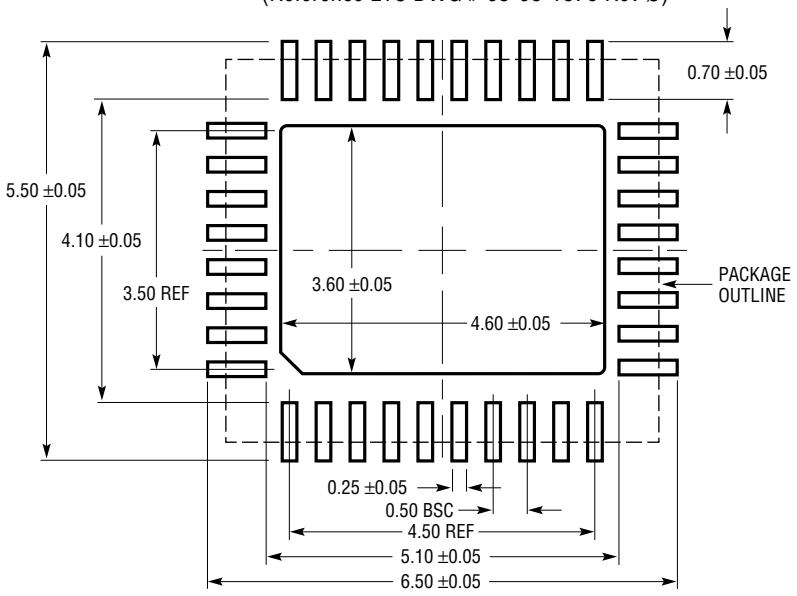
Efficiency, V_{IN} = 34V



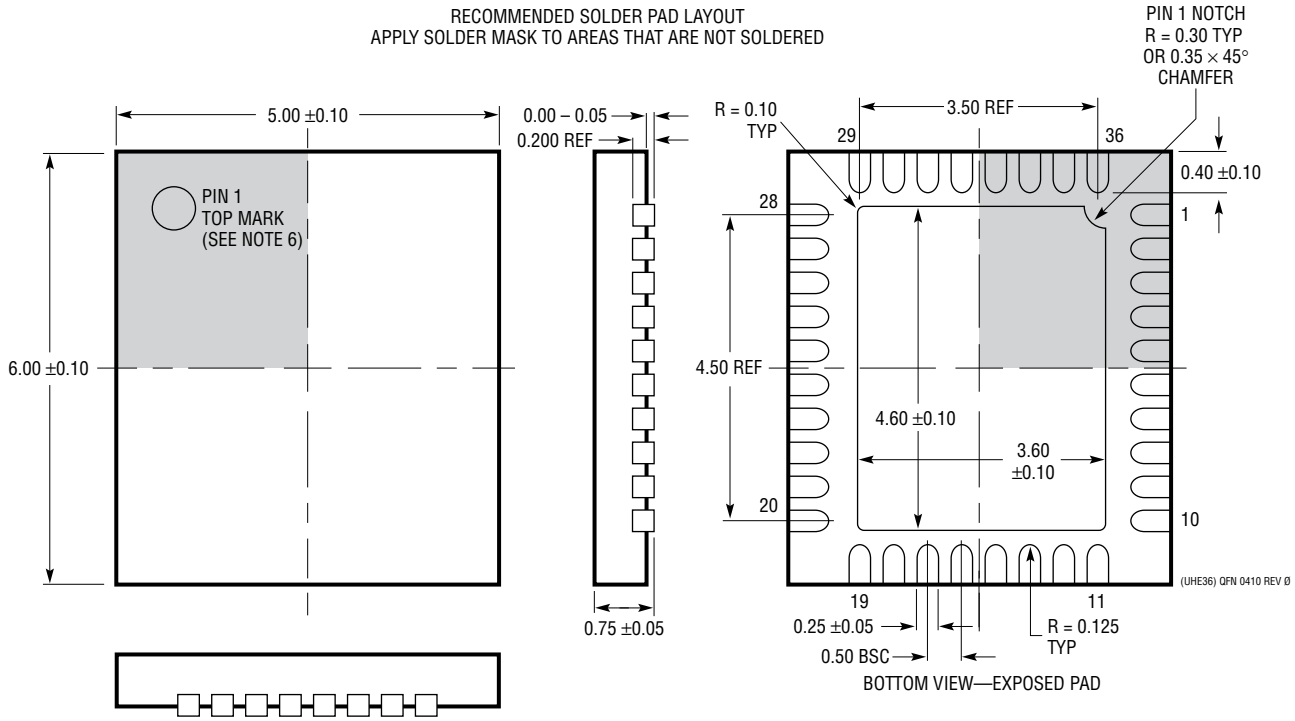
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3964#packaging for the most recent package drawings.

UHE Package
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1876 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/17	Block Diagram: corrected MOSFET symbol orientation for top switch, bottom switch and M1 MOSFETs.	12
B	3/18	Note 2: RT pin added.	5

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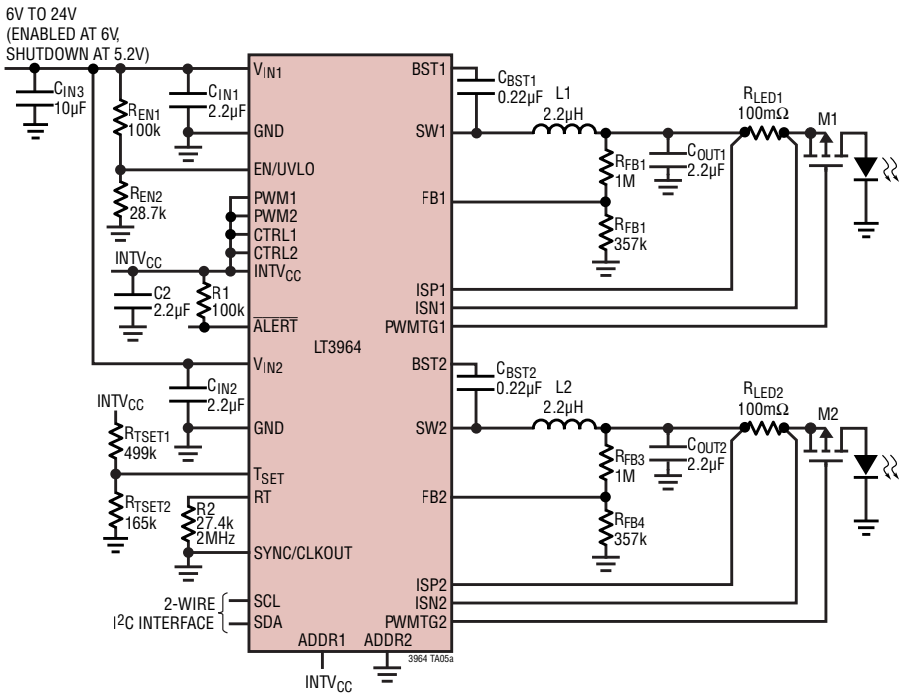
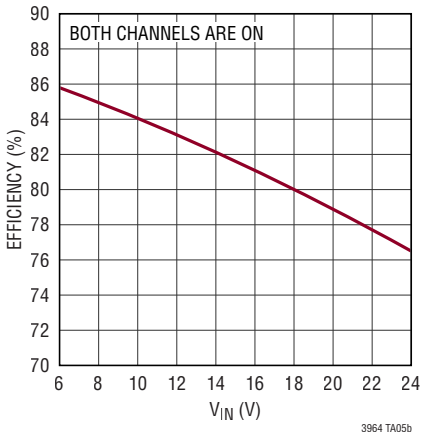
TYPICAL APPLICATION

Dual 1A Single LED Driver



L1, L2: COILCRAFT XAL4020-222MEB
M1, M2: VISHAY Si2365EDS

Efficiency, I_{LED} = 1A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3922	36V, 2A Synchronous Step-Up LED Driver	$V_{IN(MIN)}$ = 2.8V, $V_{IN(MAX)}$ = 36V, V_{OUT} = 40V, 128:1 Internal Dimming and 5,000:1 External Dimming, ISD = 1µA, 4mm × 5mm QFN-28
LT3932	36V, 2A Synchronous Step-Down LED Driver	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, V_{OUT} = 0V to 36V, 128:1 Internal Dimming and 5,000:1 External Dimming, ISD = 1µA, 4mm × 5mm QFN-28
LT3952	60V, 4A Synchronous Step-Up LED Driver	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, V_{OUT} = 0V to 60V, 5:1 Internal Dimming and 4,000:1 External Dimming, ISD = 1µA, TSSOP-28E
LT3795	High Side 110V, 1MHz LED Driver with 3,000:1 PWM Dimming with Spread Spectrum Frequency Modulation	$V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 110V, V_{OUT} = $110V_{MAX}$, 3000:1 PWM, 20:1 Analog, ISD = <1µA, TSSOP-28E
LT3956	$80V_{IN}/80V_{OUT}$, I_{SW} = 3.3A, 1MHz LED Driver with 3,000:1 PWM Dimming	$V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 80V, V_{OUT} = $40V_{MAX}$, 3000:1 PWM, 20:1 Analog, ISD = <1µA, 5mm × 6mm QFN-36
LT3761	High Side 100V, 1MHz LED Controller with 3,000:1 PWM Dimming and Internal PWM Generator	$V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 60V, V_{OUT} = $80V_{MAX}$, 3000:1 PWM, 20:1 Analog, ISD = <1µA, MSOP-16E
LT3755/ LT3755-1/ LT3755-2	High Side 75V, 1MHz LED Controller with 3,000:1 PWM Dimming	$V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 40V, V_{OUT} = 5V to 75V, 3000:1 PWM, 20:1 Analog, ISD = <1µA, 3mm × 3mm QFN-16 and MSOP-16E
LT3756/ LT3756-1/ LT3756-2	High Side 100V, 1MHz LED Controller with 3,000:1 PWM Dimming	$V_{IN(MIN)}$ = 6.0V, $V_{IN(MAX)}$ = 100V, V_{OUT} = 5V to 100V, 3000:1 PWM, 20:1 Analog, ISD = <1µA, 3mm × 3mm QFN-16 and MSOP-16E

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