300 mA, Low Quiescent Current, CMOS Linear Regulator

Data Sheet **ADP172**

FEATURES

- Maximum output current: 300 mA
- Input voltage range: 1.6 V to 3.6 V
- Low quiescent current
  - I_{GND} = 23 µA with 0 mA load
  - I_{GND} = 170 µA with 300 mA load
- Low shutdown current: <1 µA
- Low dropout voltage: 50 mV at 300 mA load
- Output voltage accuracy: ±1%
- Up to 31 fixed-output voltage options available from 0.8 V to 3.0 V
- Accuracy over line, load, and temperature: ±3%
- Stable with small 1 µF ceramic output capacitor
- PSRR performance of 70 dB at 10 kHz and 73 dB at 1 kHz
- Low noise: 30 µV rms at V_{OUT} = 0.8 V
- Current limit and thermal overload protection
- Logic-controlled enable
- Tiny 4-ball, 0.5 mm pitch WLCSP package

APPLICATIONS

- Mobile phones
- Digital camera and audio devices
- Portable and battery-powered equipment
- DSP/FPGA/microprocessor supplies
- Post dc-to-dc regulation

TYPICAL APPLICATION CIRCUITS

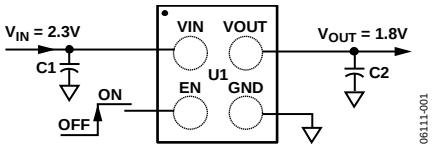

Figure 1. ADP172 with Fixed Output Voltage, 1.8 V

GENERAL DESCRIPTION

The ADP172 is a low voltage input, low quiescent current, low-dropout (LDO) linear regulator that operates from 1.6 V to 3.6 V and provides up to 300 mA of output current. The low 50 mV dropout voltage at 300 mA load improves efficiency and allows operation over a wide input voltage range. The low 23 µA of quiescent current at no load makes the ADP172 ideal for battery-operated portable equipment.

The ADP172 is capable of 31 fixed-output voltage options, ranging from 0.8 V to 3.0 V. The ADP172 is optimized for stable operation with small 1 µF ceramic output capacitors. Ideal for powering digital processors, the ADP172 exhibits good transient performance and occupies minimal board space. Compared with commodity-type LDOs, the ADP172 provides 20 dB to 40 dB better power supply rejection ratio (PSRR) at 100 kHz, making the ADP172 an ideal power source for analog-to-digital converter (ADC) mixed-signal processor systems and allowing use of smaller size bypass capacitors. In addition, low output noise performance without the need for an additional bypass capacitor further reduces printed circuit board (PCB) component count.

Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP172 is available in a tiny 4-ball, 0.5 mm pitch WLCSP for the smallest footprint solution to meet a variety of portable power applications.

Rev. E

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SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 1.6 V (whichever is greater), EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	1.6		3.6	V
OPERATING SUPPLY CURRENT[1]	I_{GND}	I_{OUT} = 0 µA		23		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			60	µA
		I_{OUT} = 1 mA		50		µA
		I_{OUT} = 1 mA, T_J = −40°C to +125°C			100	µA
		I_{OUT} = 150 mA		130		µA
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			210	µA
		I_{OUT} = 300 mA		170		µA
		I_{OUT} = 300 mA, T_J = −40°C to +125°C			260	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.1		µA
		EN = GND, V_{IN} = 3.6 V, T_J = −40°C to +85°C			2	µA
		EN = GND, V_{IN} = 3.6 V, T_J = 85°C to 125°C			25	µA
OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		1 mA < I_{OUT} < 300 mA, V_{IN} = (V_{OUT} + 0.5 V) to 3.6 V	−2		+1.5	%
		1 mA < I_{OUT} < 300 mA, V_{IN} = (V_{OUT} + 0.5 V) to 3.6 V, T_J = −40°C to +125°C	−3		+1.5	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 3.6 V, T_J = −40°C to +125°C	−0.25		+0.25	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 300 mA		0.001		%/mA
		I_{OUT} = 1 mA to 300 mA, T_J = −40°C to +125°C			0.005	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 10 mA, V_{OUT} ≥ 1.8 V		2		mV
		I_{OUT} = 10 mA, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			7	mV
		I_{OUT} = 150 mA, V_{OUT} ≥ 1.8 V		25		mV
		I_{OUT} = 150 mA, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			50	mV
		I_{OUT} = 300 mA, V_{OUT} ≥ 1.8 V		50		mV
		I_{OUT} = 300 mA, V_{OUT} ≥ 1.8 V, T_J = −40°C to +125°C			100	mV
START-UP TIME[4]	$t_{START-UP}$	V_{OUT} = 1.8 V		120		µs
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}		400	450	800	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
Logic High Voltage	V_{IH}	1.6 V ≤ V_{IN} ≤ 3.6 V	1.2			V
Logic Low Voltage	V_{IL}	1.6 V ≤ V_{IN} ≤ 3.6 V			0.4	V
Leakage Current Voltage	$V_{I-LEAKAGE}$	EN = VIN or GND		0.1		µA
		EN = VIN or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			1.5	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	0.7			V
Hysteresis	$UVLO_{HYS}$			80		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 3.0 V		72		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.8 V		50		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.2 V		40		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 0.8 V		30		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{IN} = 3.6 V, I_{OUT} = 10 mA, V_{OUT} = 0.8 V		73		dB
		10 kHz, V_{IN} = 3.6 V, I_{OUT} = 10 mA, V_{OUT} = 0.8 V		70		dB
		10 kHz, V_{IN} = (V_{OUT} + 1 V), I_{OUT} = 10 mA to 300 mA		50		dB
		100 kHz, V_{IN} = (V_{OUT} + 1 V), I_{OUT} = 10 mA to 300 mA		47		dB

[1] The current from the external resistor divider network in the case of adjustable voltage output (as with the ADP172) should be subtracted from the ground current measured.
[2] Based on an end-point calculation using 1 mA and 300 mA loads. See Figure 4 for typical load regulation performance for loads less than 1 mA.
[3] Applies only for output voltages above 1.6 V. Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.
[4] Start-up time is defined as the time between the rising edge of EN and VOUT at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_J = −40°C to +125°C	0.45			µF
CAPACITOR ESR	R_{ESR}	T_J = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.45 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +4.0 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +4.0 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply only individually, not in combination. The ADP172 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. PCB. Refer to JESD51-7 for detailed information regarding board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The *Guidelines for Reporting and Using Electronic Package Thermal Information: JESD51-12* states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package—factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
4-Ball, 0.5 mm Pitch WLCSP	260	58	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

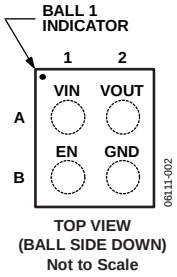

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
A2	VOUT	Output Voltage Adjust Input. Connect the midpoint of an external divider from VOUT to GND to this pin to set the output voltage
B1	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

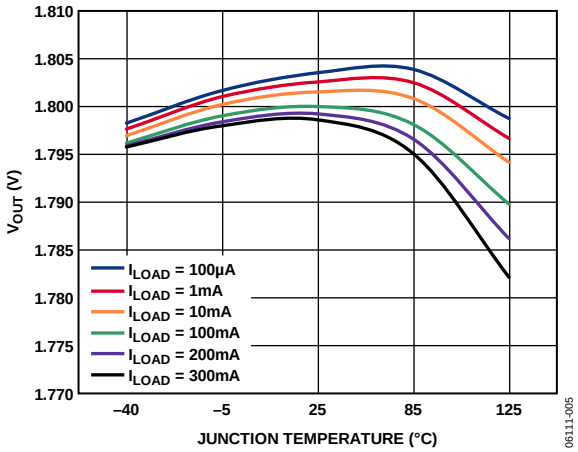

Figure 3. Output Voltage vs. Junction Temperature

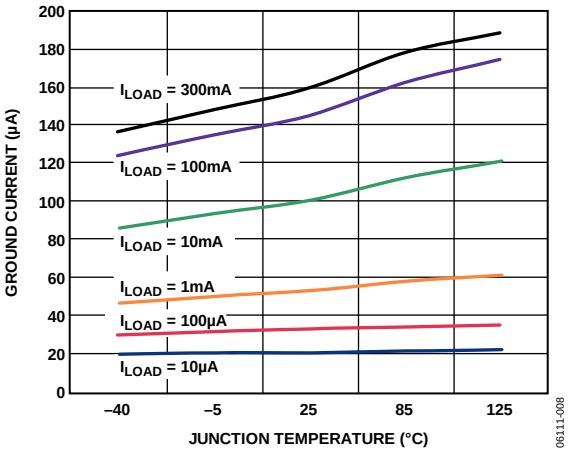

Figure 6. Ground Current vs. Junction Temperature

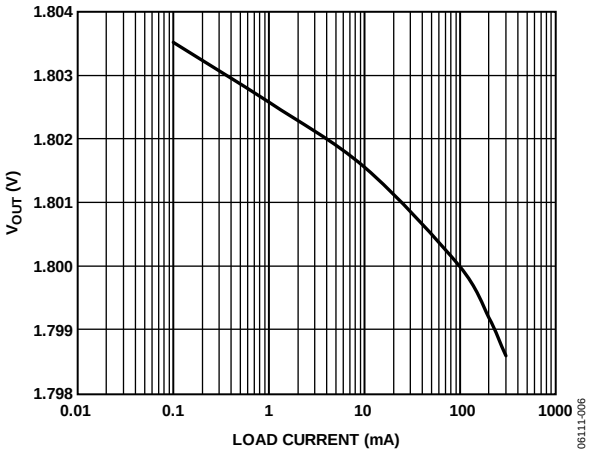

Figure 4. Output Voltage vs. Load Current

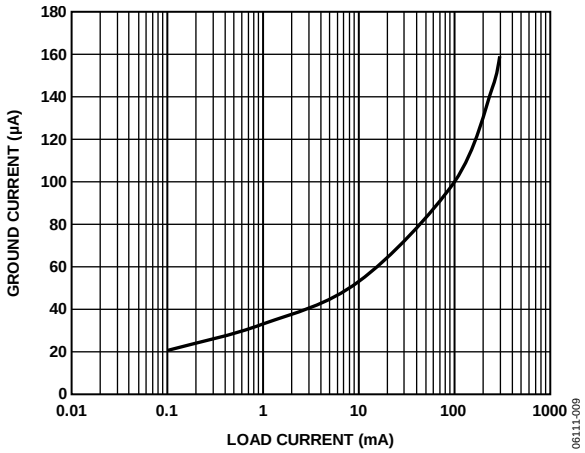

Figure 7. Ground Current vs. Load Current

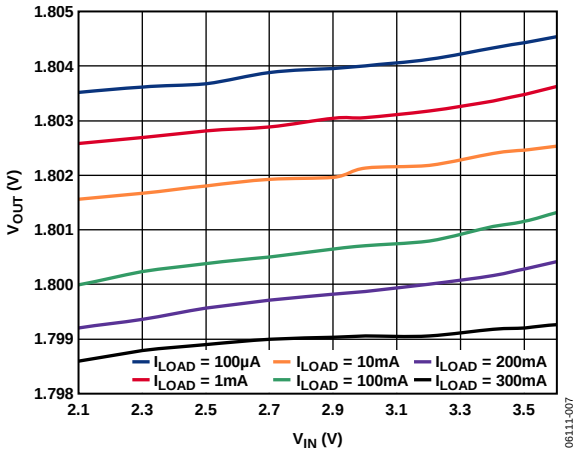

Figure 5. Output Voltage vs. Input Voltage

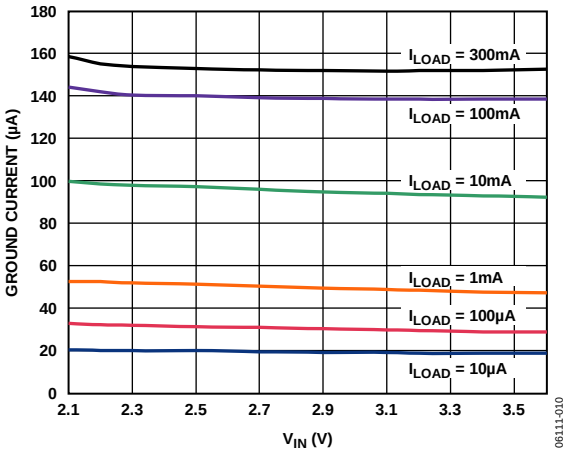

Figure 8. Ground Current vs. Input Voltage

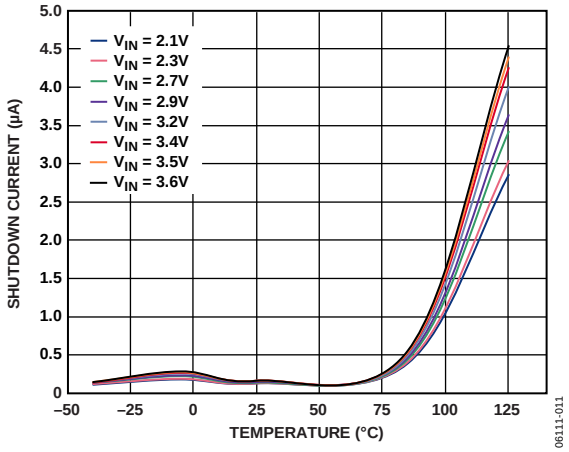

Figure 9. Shutdown Current vs. Temperature at Various Input Voltages

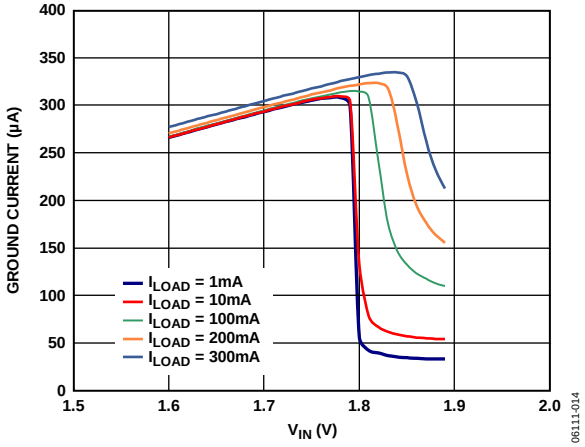

Figure 12. Ground Current vs. Input Voltage (in Dropout)

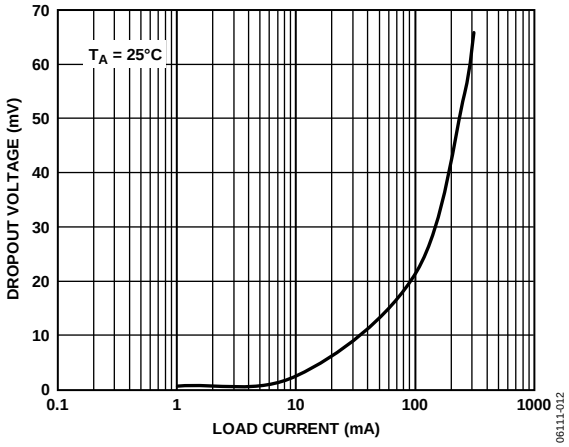

Figure 10. Dropout Voltage vs. Load Current

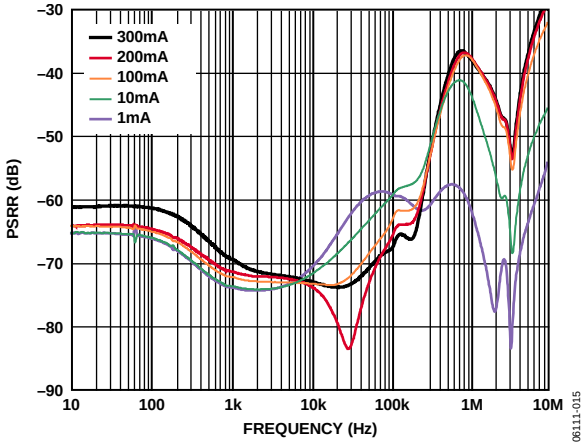

Figure 13. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 0.8 V

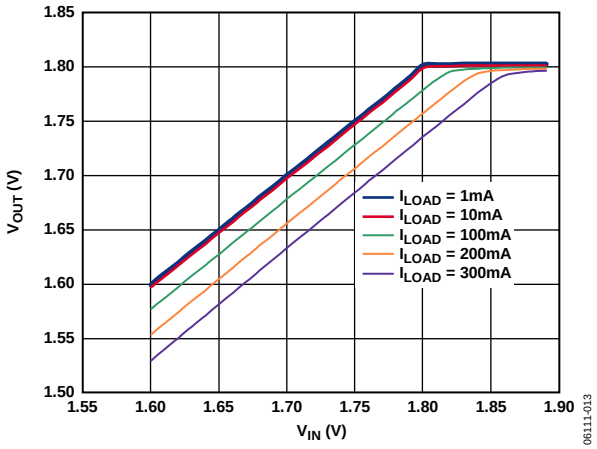

Figure 11. Output Voltage vs. Input Voltage (in Dropout)

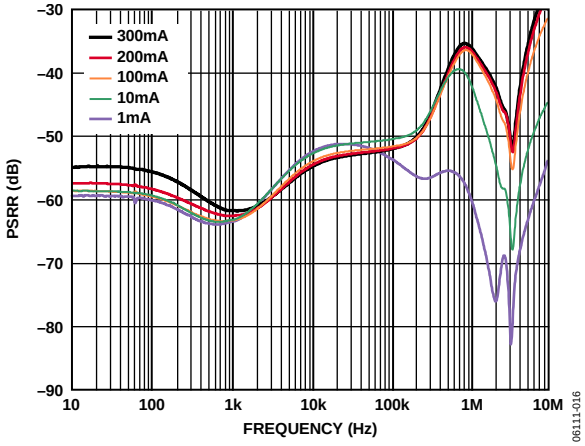

Figure 14. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.8 V

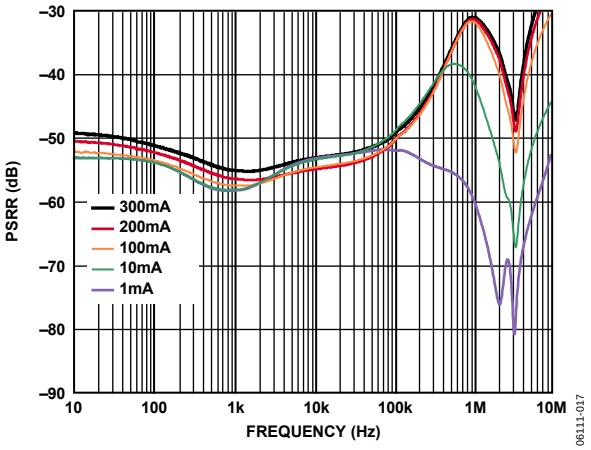

Figure 15. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.0 V

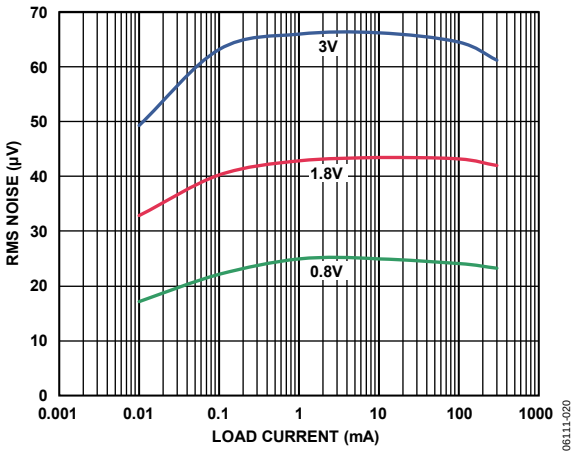

Figure 18. RMS Noise vs. Load Current and Output Voltage

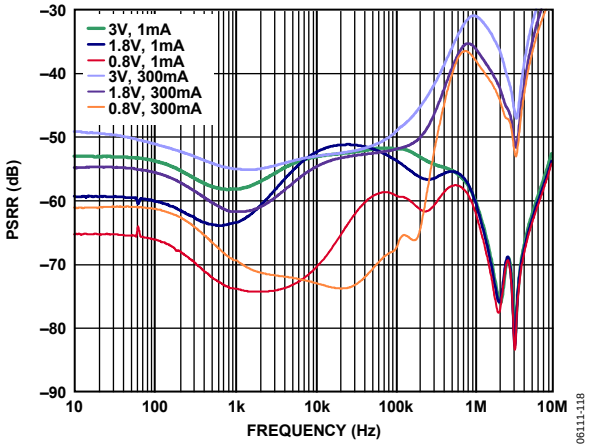

Figure 16. Power Supply Rejection Ratio vs. Frequency, Various Output Voltages and Load Currents

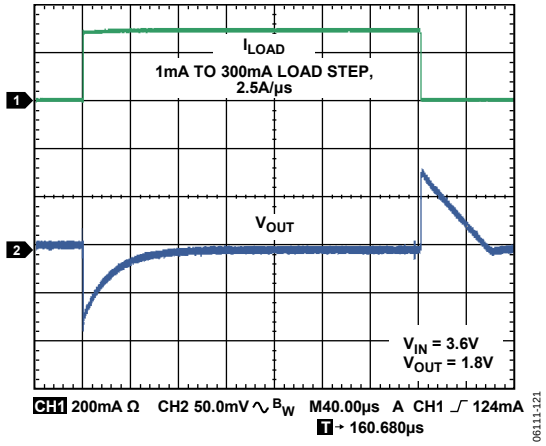

Figure 19. Load Transient Response, C_{IN} and C_{OUT} = 1 µF

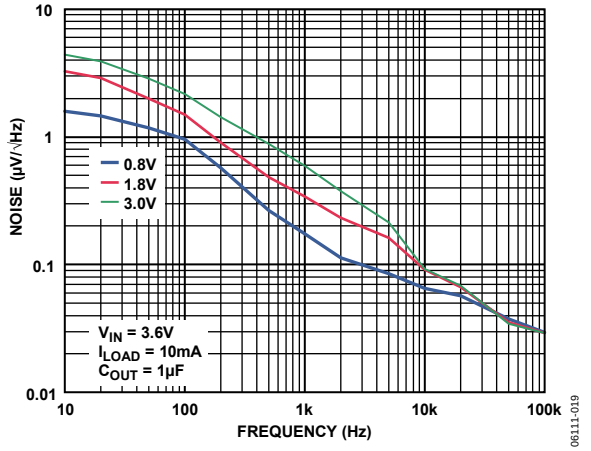

Figure 17. Output Noise Spectrum

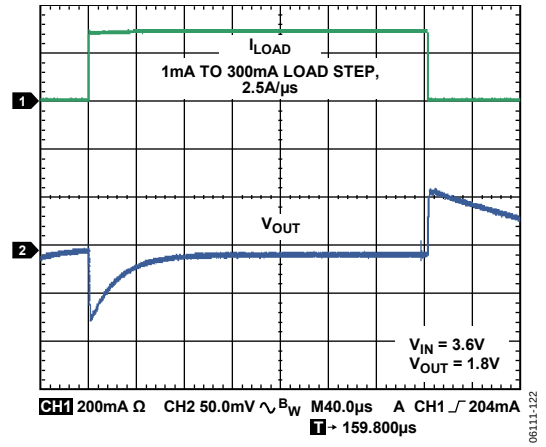

Figure 20. Load Transient Response, C_{IN} and C_{OUT} = 4.7 µF

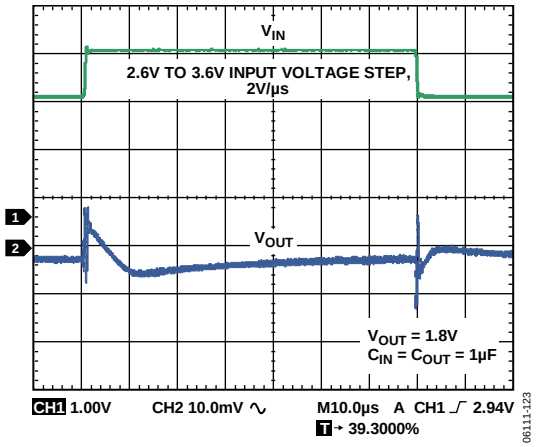

Figure 21. Line Transient Response, Load Current = 1 mA

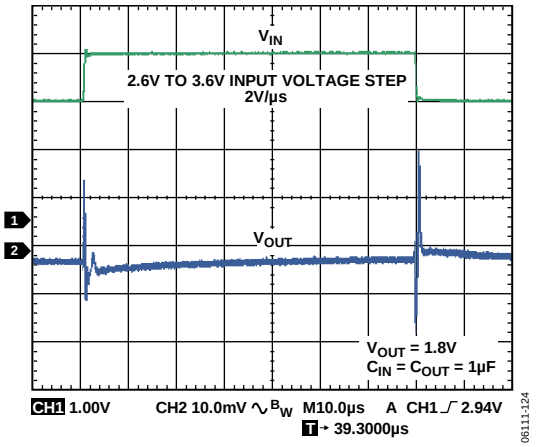

Figure 22. Line Transient Response, Load Current = 300 mA

THEORY OF OPERATION

The ADP172 is a low quiescent current, low-dropout linear regulator that operates from 1.6 V to 3.6 V and can provide up to 300 mA of output current. Drawing a low 170 µA of quiescent current (typical) at full load makes the ADP172 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP172 provides excellent transient performance.

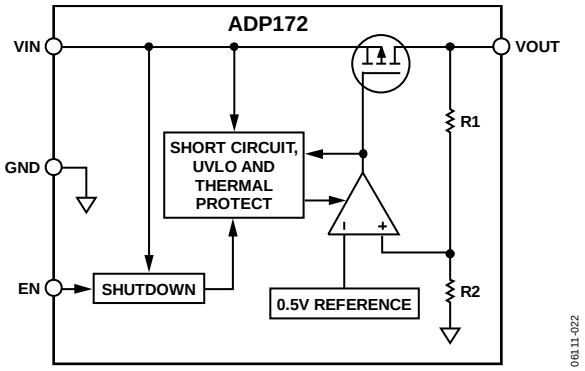

Figure 23. ADP172 Internal Block Diagram

Internally, the ADP172 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP172 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP172 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP172. The transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP172 to large changes in load current. Figure 24 and Figure 25 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

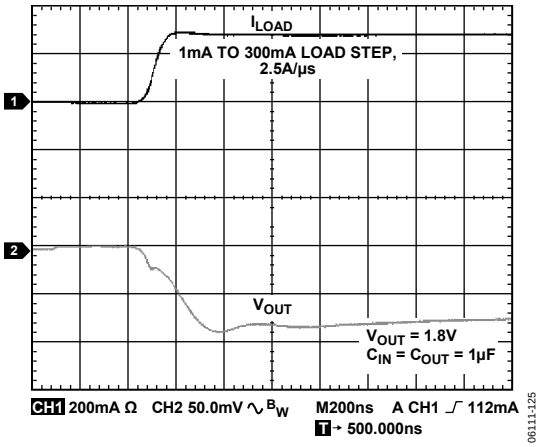

Figure 24. Output Transient Response, C_{OUT} = 1 µF

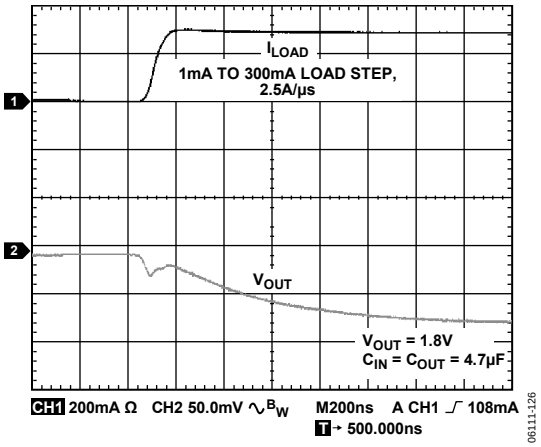

Figure 25. Output Transient Response, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance is encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP172, as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temper-ature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. An X5R or X7R dielectric with a voltage rating of 6.3 V or 10 V is recommended. The Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

Figure 26 depicts the capacitance vs. bias voltage characteristics of a 0402, 1 µF, 10 V X5R capacitor. The variance of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits less capacitance variance over bias voltage. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

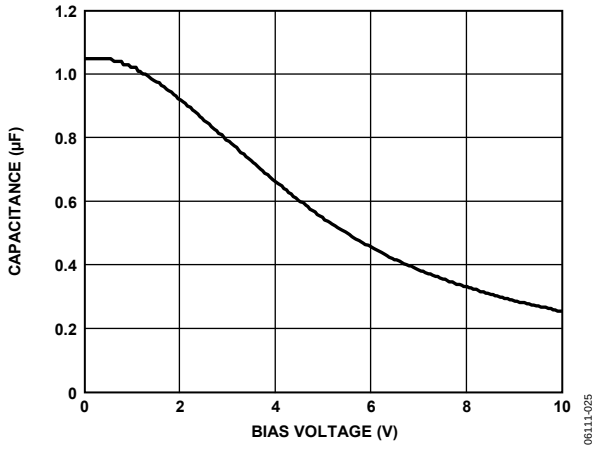

Figure 26. Capacitance vs. Bias Voltage Characteristics

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 26.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP172, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP172 has an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 1.2 V. This ensures that the ADP172 inputs and the output behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP172 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 27, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

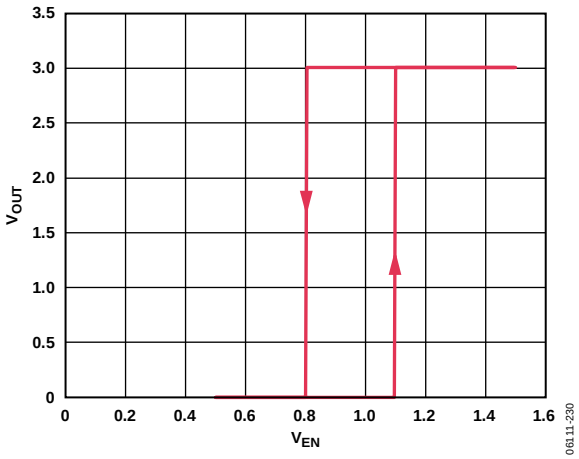

Figure 27. ADP172 Typical EN Pin Operation

As shown in Figure 27, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 28 shows typical EN active/inactive thresholds when the input voltage varies from 1.6 V to 3.6 V.

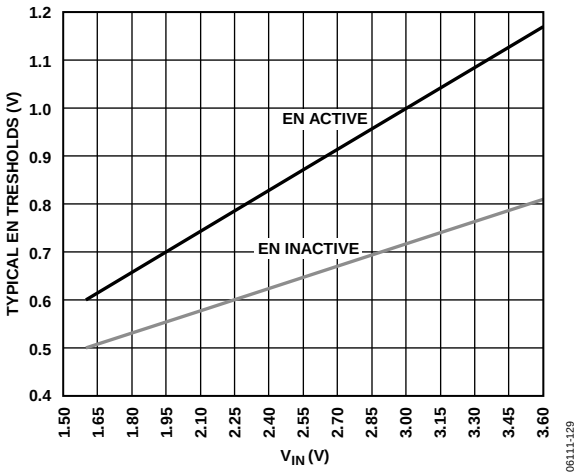

Figure 28. Typical EN Pin Thresholds vs. Input Voltage

The ADP172 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 1.8 V option is approximately 120 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 29, the start-up time is dependent on the output voltage setting.

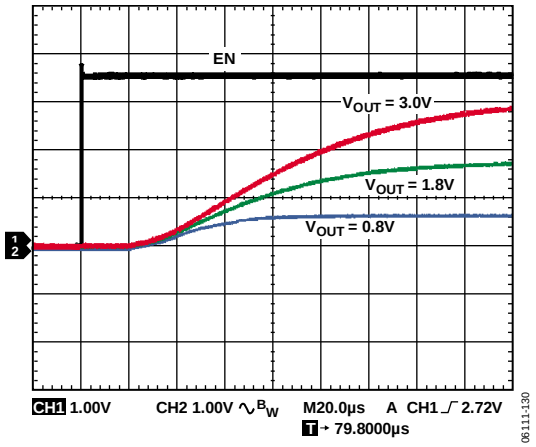

Figure 29. Typical Start-Up Time

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP172 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP172 is designed to limit the current when the output load reaches 450 mA (typical). When the output load exceeds 450 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to 0. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP172 limits the current so that only 450 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to 0. As the junction temperature cools and drops below 135°C, the output turns on and conducts 450 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 450 mA and 0 mA, which continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP172 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used and the amount of copper to which the GND pin of the package is soldered on the PCB. Table 6 shows typical θ_{JA} values of the 4-ball WLCSP package for various PCB copper sizes.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	260
50	159
100	157
300	153
500	151

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP172 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 30 to Figure 35 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

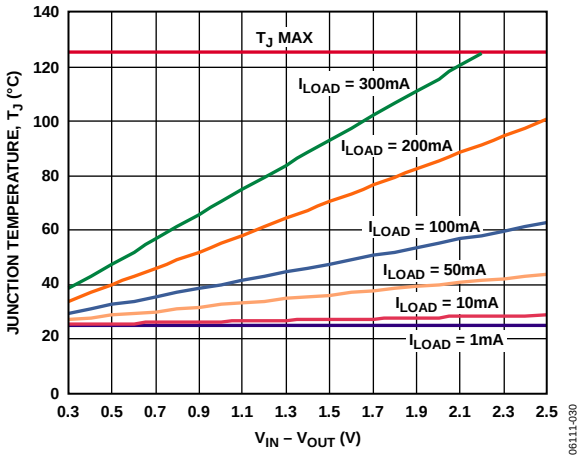

Figure 30. 500 mm² of PCB Copper, T_A = 25°C

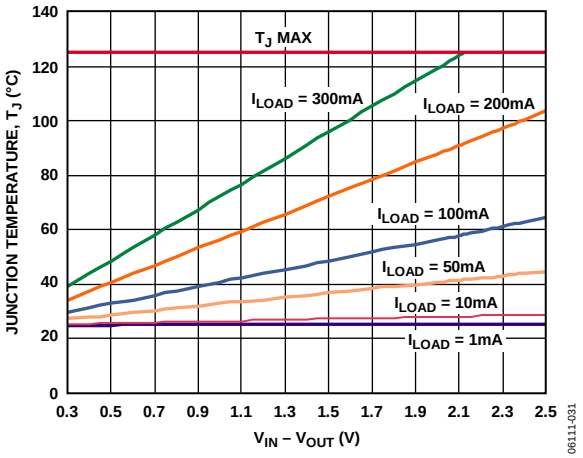

Figure 31. 100 mm² of PCB Copper, T_A = 25°C

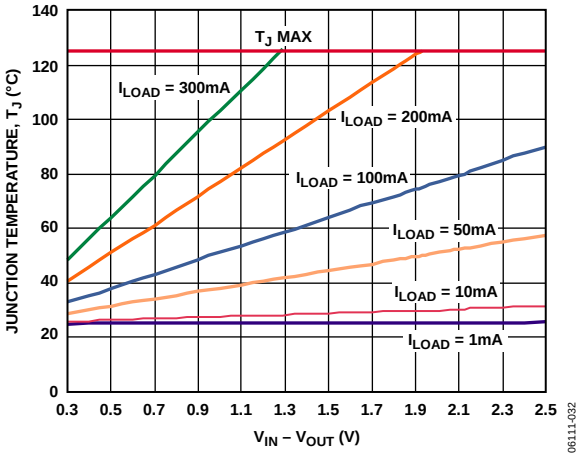

Figure 32. 0 mm² of PCB Copper, T_A = 25°C

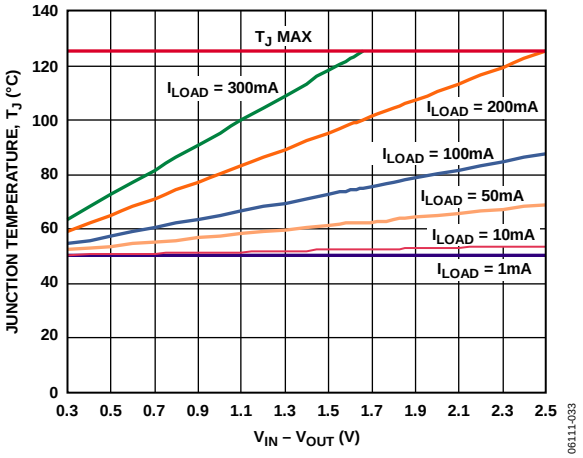

Figure 33. 500 mm² of PCB Copper, T_A = 50°C

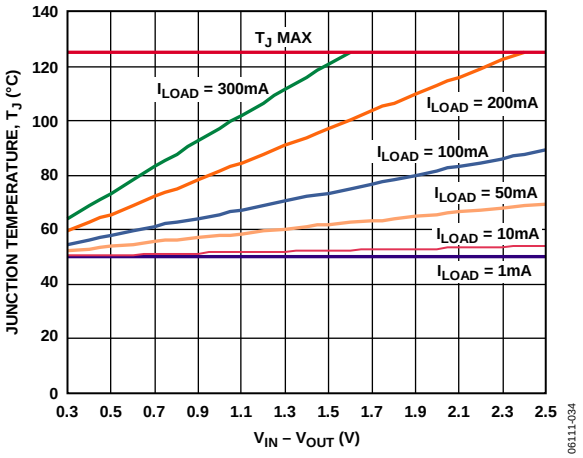

Figure 34. 100 mm² of PCB Copper, T_A = 50°C

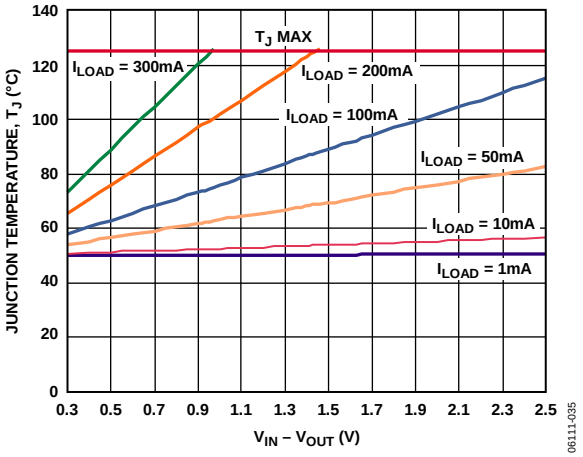

Figure 35. 0 mm² of PCB Copper, T_A = 50°C

In cases where board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 36). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 58°C/W for the 4-Ball WLCSP package.

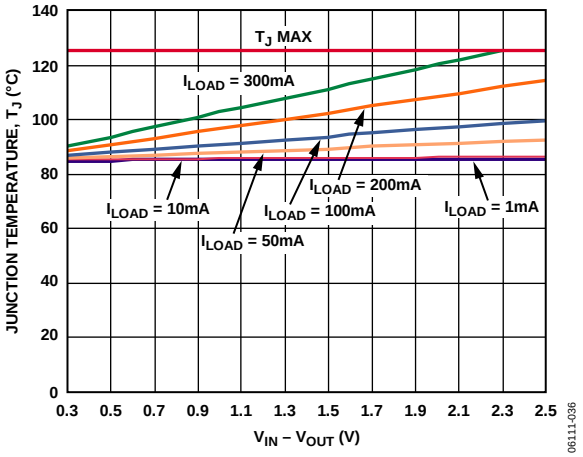

Figure 36. T_A = 85°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP172. However, as can be seen from Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution for boards on which area is limited.

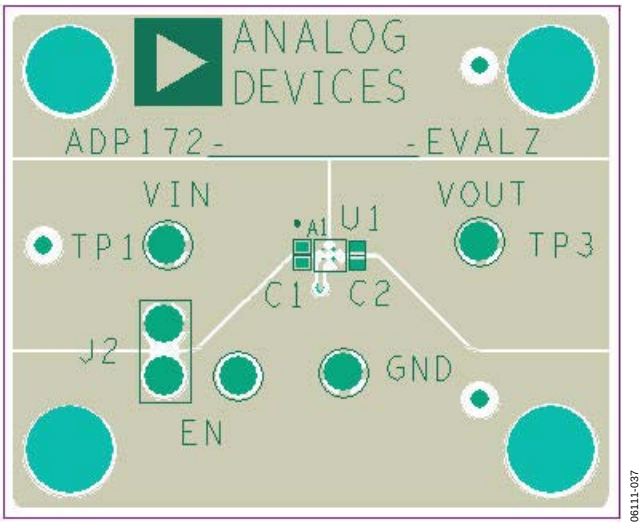

Figure 37. Example ADP172 PCB Layout

OUTLINE DIMENSIONS

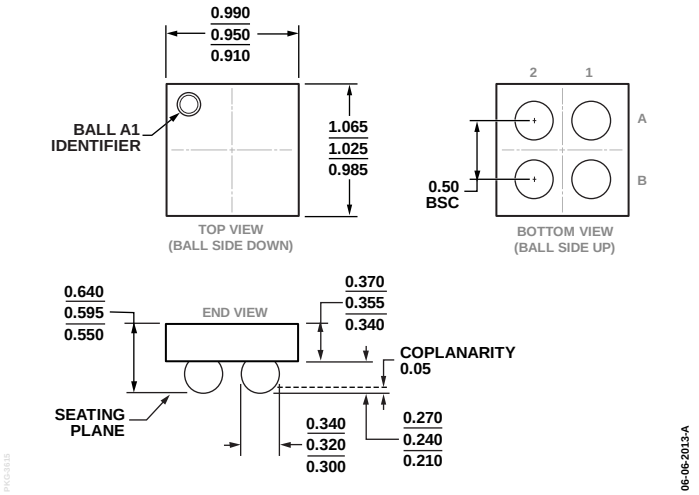

Figure 38. 4-Ball, Wafer Level Chip Scale Package [WLCSP]
(CB-4-4)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP172ACBZ-1.0-R7	−40°C to +125°C	1.0	4-Ball WLCSP	CB-4-4	6V
ADP172ACBZ-1.2-R7	−40°C to +125°C	1.2	4-Ball WLCSP	CB-4-4	51
ADP172ACBZ-1.26-R7	−40°C to +125°C	1.26	4-Ball WLCSP	CB-4-4	6E
ADP172ACBZ-1.5-R7	−40°C to +125°C	1.5	4-Ball WLCSP	CB-4-4	5J
ADP172ACBZ-1.65-R7	−40°C to +125°C	1.65	4-Ball WLCSP	CB-4-4	BD
ADP172ACBZ-1.7-R7	−40°C to +125°C	1.7	4-Ball WLCSP	CB-4-4	CH
ADP172ACBZ-1.8-R7	−40°C to +125°C	1.8	4-Ball WLCSP	CB-4-4	5X
ADP172ACBZ-0.9-R7	−40°C to +125°C	0.9	4-Ball WLCSP	CB-4-4	CV
ADP172ACBZ-2.1-R7	−40°C to +125°C	2.1	4-Ball WLCSP	CB-4-4	6B
ADP172ACBZ-2.9-R7	−40°C to +125°C	2.9	4-Ball WLCSP	CB-4-4	91
ADP172ACBZ-3.0-R7	−40°C to +125°C	3.0	4-Ball WLCSP	CB-4-4	6Z
ADP172ACB-1.2-EVALZ		1.2	Evaluation Board		
ADP172ACB-1.5-EVALZ		1.5	Evaluation Board		
ADP172ACB-1.8-EVALZ		1.8	Evaluation Board		
ADP172ACB-3.0-EVALZ		3.0	Evaluation Board		
ADP172ACB1.26-EVALZ		1.26	Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact your local Analog Devices, Inc., sales or distribution representative.

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