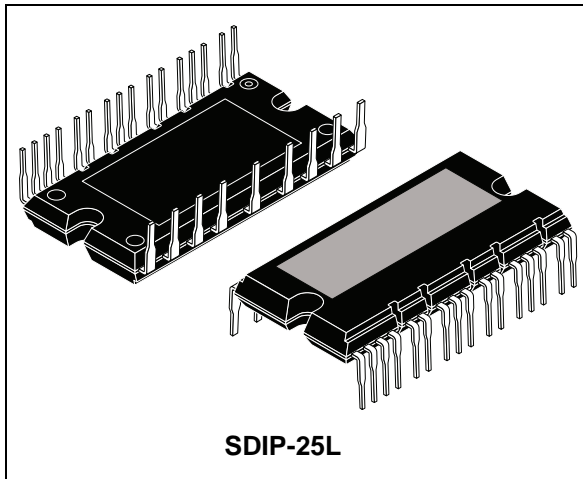


SLLIMM™ small low-loss intelligent molded module IPM, 3-phase inverter, 10 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Features

- IPM 10 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBT
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down resistor
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- 5 k Ω NTC thermistor for temperature control
- UL recognized: UL1557 file E81734

Table 1. Device summary

| Order code | Marking | Package | Packing |
|--------------|------------|----------|---------|
| STGIPS10K60A | GIPS10K60A | SDIP-25L | Tube |

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1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

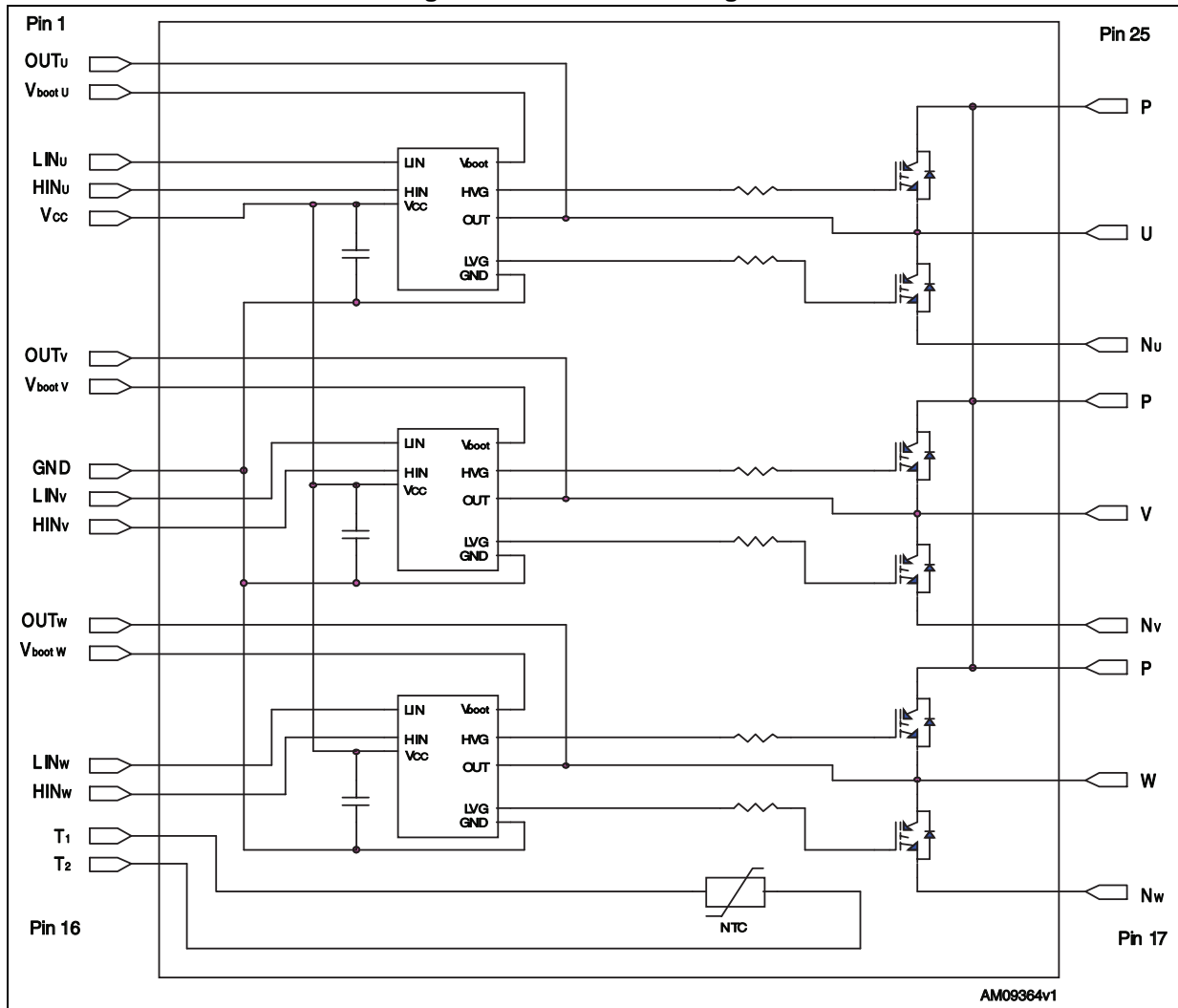
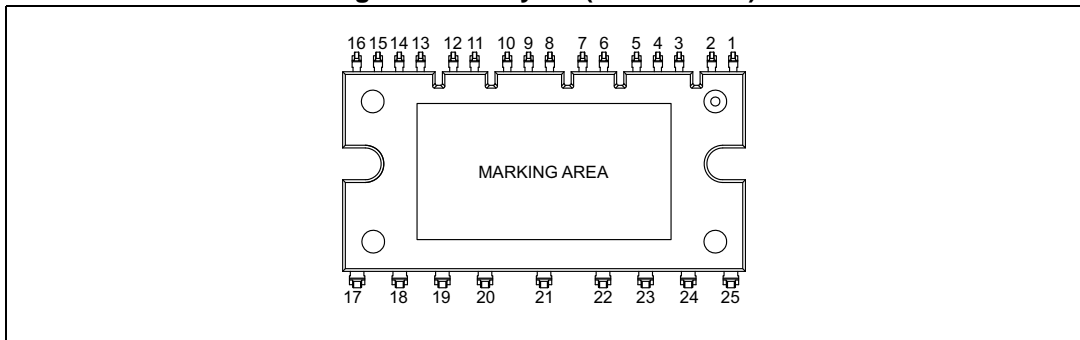


Table 2. Pin description

| Pin | Symbol | Description |
|-----|---------------------|--|
| 1 | OUT _U | High side reference output for U phase |
| 2 | V _{boot U} | Bootstrap voltage for U phase |
| 3 | LIN _U | Low side logic input for U phase |
| 4 | HIN _U | High side logic input for U phase |
| 5 | V _{CC} | Low voltage power supply |
| 6 | OUT _V | High side reference output for V phase |
| 7 | V _{boot V} | Bootstrap voltage for V phase |
| 8 | GND | Ground |
| 9 | LIN _V | Low side logic input for V phase |
| 10 | HIN _V | High side logic input for V phase |
| 11 | OUT _W | High side reference output for W phase |
| 12 | V _{boot W} | Bootstrap voltage for W phase |
| 13 | LIN _W | Low side logic input for W phase |
| 14 | HIN _W | High side logic input for W phase |
| 15 | T ₁ | NTC thermistor terminal 1 |
| 16 | T ₂ | NTC thermistor terminal 2 |
| 17 | N _W | Negative DC input for W phase |
| 18 | W | W phase output |
| 19 | P | Positive DC input |
| 20 | N _V | Negative DC input for V phase |
| 21 | V | V phase output |
| 22 | P | Positive DC input |
| 23 | N _U | Negative DC input for U phase |
| 24 | U | U phase output |
| 25 | P | Positive DC input |

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------|---------------|
| V_{PN} | Supply voltage applied between P - N_U , N_V , N_W | 450 | V |
| $V_{PN(surge)}$ | Supply voltage (surge) applied between P - N_U , N_V , N_W | 500 | V |
| V_{CES} | Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$) | 600 | V |
| $\pm I_C^{(2)}$ | Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$ | 10 | A |
| $\pm I_{CP}^{(3)}$ | Each IGBT pulsed collector current | 20 | A |
| P_{TOT} | Each IGBT total dissipation at $T_C = 25^\circ\text{C}$ | 33 | W |
| t_{scw} | Short-circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_j = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN(1)} = 5\text{ V}$ | 5 | μs |

1. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$.
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature.

Table 4. Control part

| Symbol | Parameter | Min. | Max | Unit |
|---------------|--|-----------------|------------------|------|
| V_{OUT} | Output voltage applied between OUT_U , OUT_V , OUT_W - GND | $V_{boot} - 18$ | $V_{boot} + 0.3$ | V |
| V_{CC} | Low voltage power supply | - 0.3 | 18 | V |
| V_{boot} | Bootstrap voltage | - 0.3 | 618 | V |
| V_{IN} | Logic input voltage applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$ | - 0.3 | $V_{CC} + 0.3$ | V |
| dV_{OUT}/dt | Allowed output slew rate | 50 | 50 | V/ns |

Table 5. Total system

| Symbol | Parameter | Value | Unit |
|-----------|---|------------|------------------|
| V_{ISO} | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$) | 2500 | V |
| T_J | Power chips operating junction temperature | -40 to 150 | $^\circ\text{C}$ |
| T_C | Module case operating temperature | -40 to 125 | $^\circ\text{C}$ |

2.2 Thermal data

Table 6. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|--|-------|------|
| R_{thJC} | Thermal resistance junction-case single IGBT max. | 3.8 | °C/W |
| | Thermal resistance junction-case single diode max. | 5.5 | °C/W |

3 Electrical characteristics

$T_j = 25^\circ\text{C}$ unless otherwise specified.

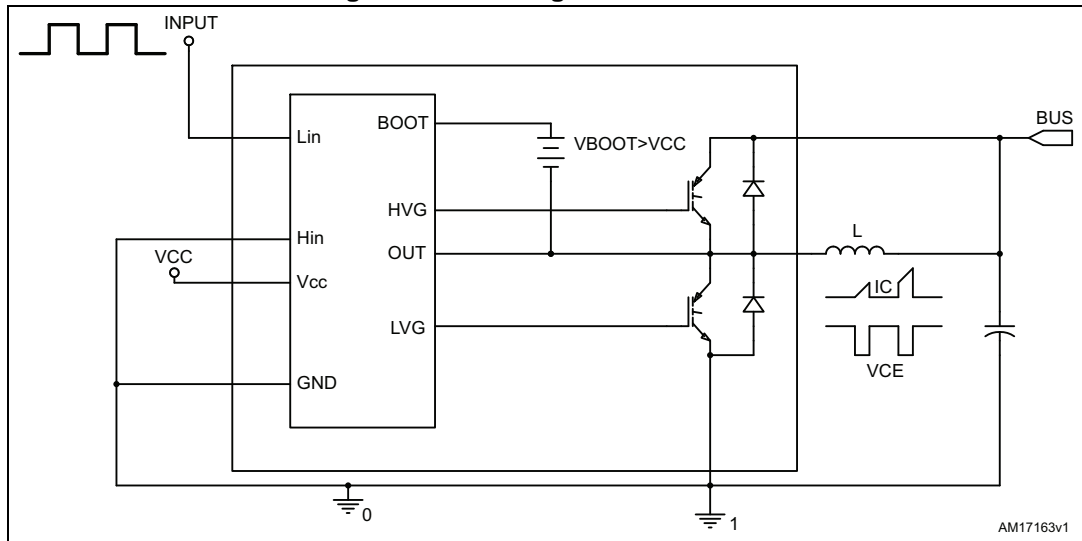
Table 7. Inverter part

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|---|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 5\text{ V}$, $I_C = 5\text{ A}$ | - | 2.1 | 2.5 | V |
| | | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 5\text{ V}$, $I_C = 5\text{ A}$, $T_j = 125^\circ\text{C}$ | - | 1.8 | | |
| I_{CES} | Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state") | $V_{CE} = 550\text{ V}$ $V_{CC} = V_{boot} = 15\text{ V}$ | - | | 150 | μA |
| V_F | Diode forward voltage | $V_{IN}^{(1)} = 0$ "logic state", $I_C = 5\text{ A}$ | - | | 1.9 | V |
| Inductive load switching time and energy | | | | | | |
| t_{on} | Turn-on time | $V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 5\text{ A}$ (see Figure 4) | - | 320 | - | ns |
| $t_{c(on)}$ | Crossover time (on) | | - | 70 | - | |
| t_{off} | Turn-off time | | - | 430 | - | |
| $t_{c(off)}$ | Crossover time (off) | | - | 135 | - | |
| t_{rr} | Reverse recovery time | | - | 130 | - | |
| E_{on} | Turn-on switching losses | | - | 65 | - | μJ |
| E_{off} | Turn-off switching losses | | - | 75 | - | |

1. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$.

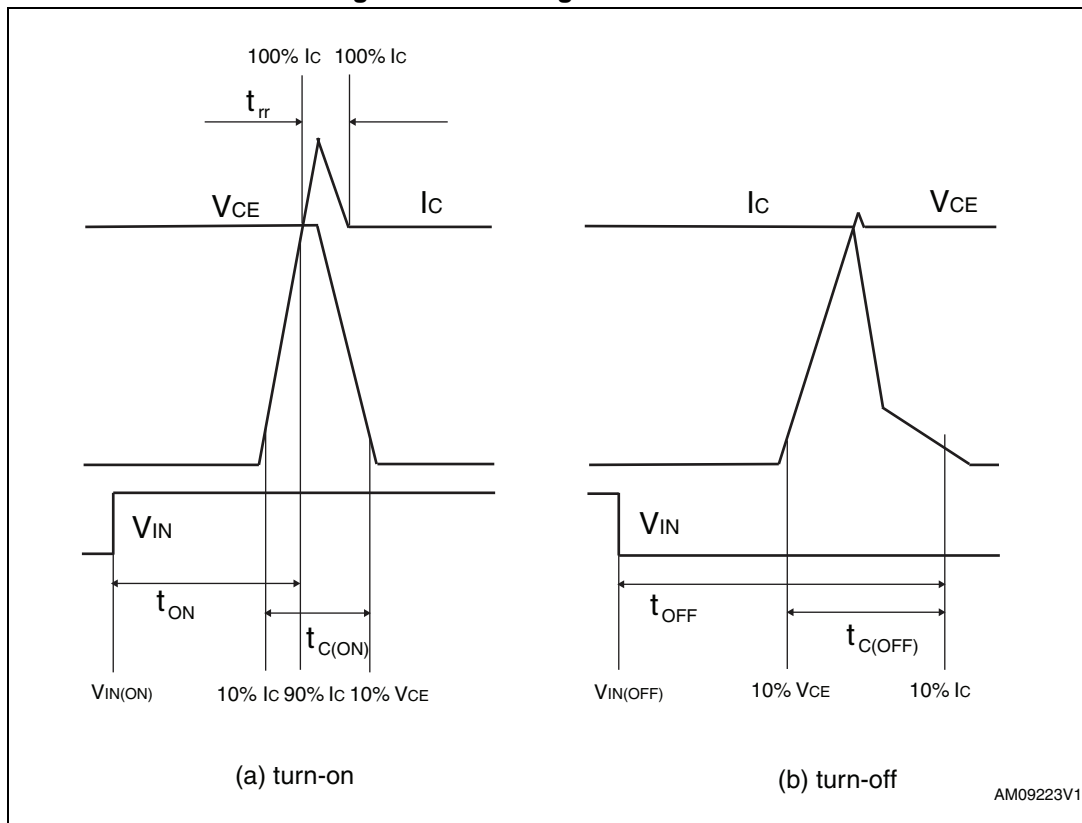
Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit



AM17163v1

Figure 4. Switching time definition



AM09223V1

3.1 Control part

Table 8. Low supply voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|-------------------------|------|------|------|------|
| V_{CCthON} | Under voltage turn on threshold | | 9.1 | 9.6 | 10.1 | V |
| $V_{CCthOFF}$ | Under voltage turn off threshold | | 7.9 | 8.3 | 8.8 | V |
| V_{CChys} | Under voltage hystereses | | 0.9 | | | V |
| I_{qccu} | Under voltage quiescent supply current | $V_{CC} < 7.9\text{ V}$ | | 0.75 | 1.2 | mA |
| I_{qcc} | Quiescent current | $V_{CC} = 15\text{ V}$ | | 1 | 1.5 | mA |

Table 9. Bootstrap supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|----------------------------------|--------------------------|------|------|------|---------------|
| V_{boot_thON} | Under voltage turn on threshold | | 8.5 | 9.5 | 10.5 | V |
| V_{boot_thOFF} | Under voltage turn off threshold | | 7.2 | 8.3 | 9.2 | V |
| V_{boot_hys} | Under voltage hystereses | | 0.9 | | | V |
| I_{qboot} | Quiescent current | | | | 250 | μA |
| $R_{DS(on)}$ | Bootstrap driver on resistance | $V_{CC} > 12.5\text{ V}$ | | 125 | | Ω |

Table 10. Logic input ⁽¹⁾ ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------|--------------------------------|------------------------------|------|------|------|---------------|
| V_{il} | Low level logic input voltage | | | | 1.1 | V |
| V_{ih} | High level logic input voltage | | 1.8 | | | V |
| I_{il} | Low level logic input current | $V_{IN}^{(2)} = 0\text{ V}$ | -1 | | | μA |
| I_{ih} | High level logic input current | $V_{IN}^{(1)} = 15\text{ V}$ | | 20 | 70 | μA |

1. See [Figure 9: Dead time and interlocking definition](#).
2. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$

3.1.1 NTC thermistor

Table 11. NTC thermistor

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit. |
|------------------|-----------------------|--------------------|------|------|------|-------|
| R ₂₅ | Resistance | T = 25 °C | | 5 | | kΩ |
| R ₁₂₅ | Resistance | T = 125 °C | | 300 | | Ω |
| B | B-constant | T = 25 °C to 85 °C | | 3340 | | K |
| T | Operating temperature | | -40 | | 125 | °C |

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B \left(\frac{1}{T} - \frac{1}{298} \right)}$$

Where T are temperatures in Kelvin.

Figure 5. NTC resistance vs. temperature

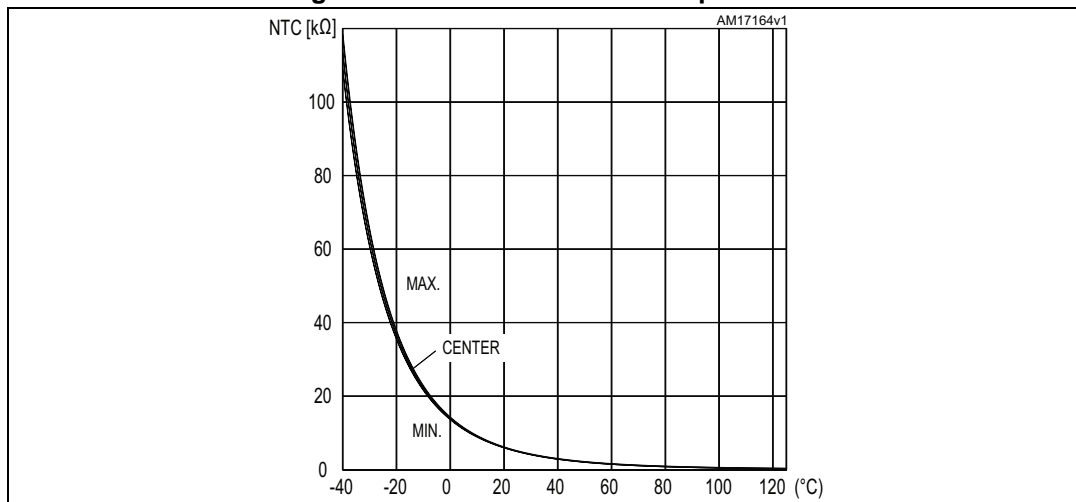


Figure 6. NTC resistance vs. temperature (zoom)

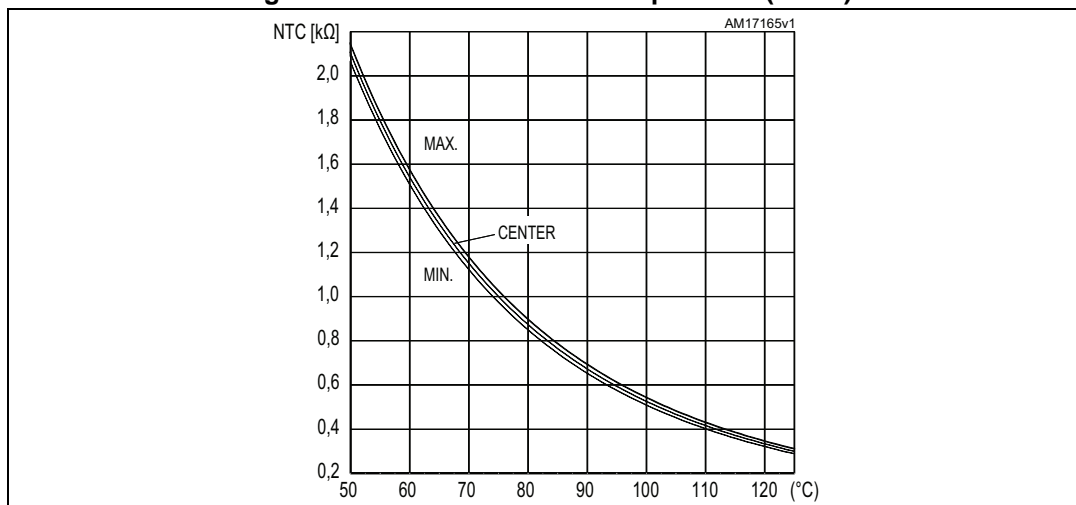


Figure 7. Maximum $I_{C(RMS)}$ current vs. switching frequency (1)

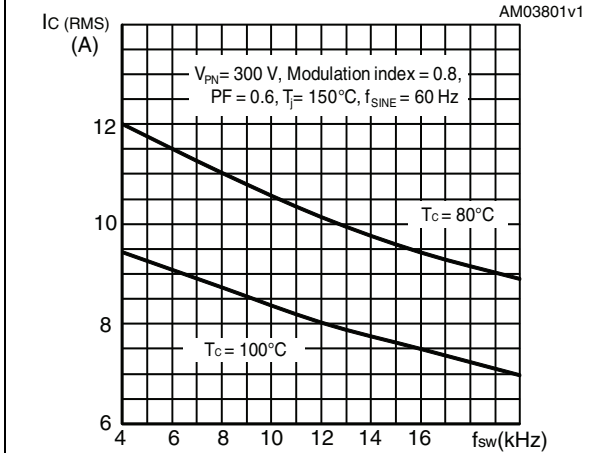
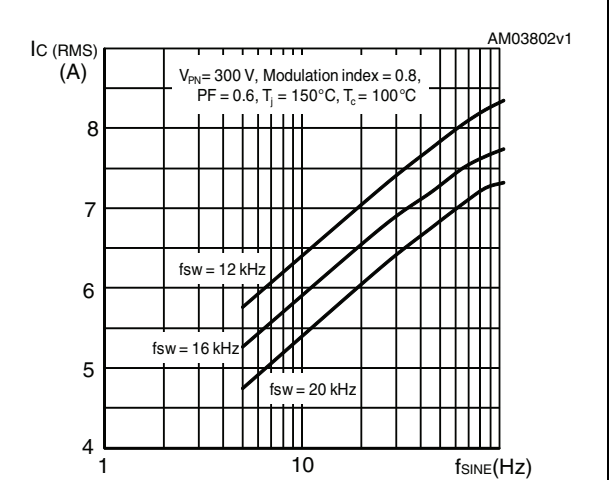
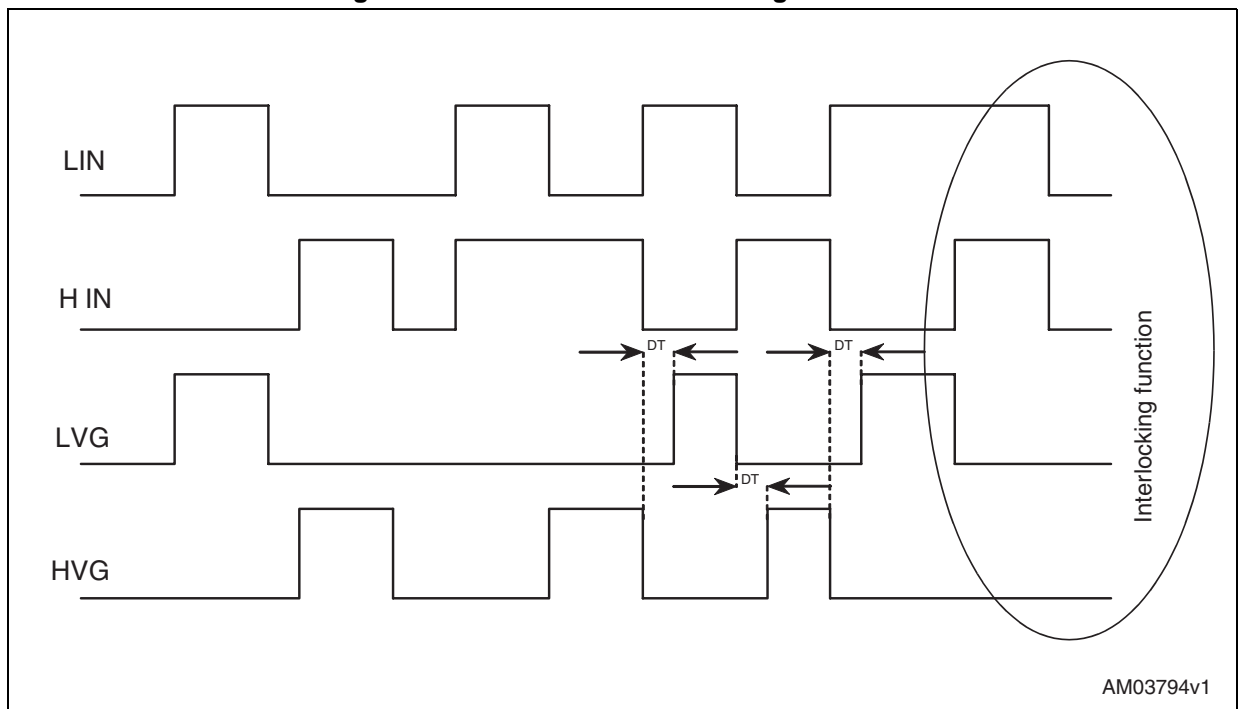


Figure 8. Maximum $I_{C(RMS)}$ current vs. f_{SINE} (1)



1. Simulated curves refer to typical IGBT parameters and maximum R_{thj-c} .

Figure 9. Dead time and interlocking definition



Minimum recommended dead time (DT) between low and high side logic input: 1 μs .

4.1 Recommendations

- Input signal HIN,LIN are active-high logic. A 500 k Ω (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

Table 12. Recommended operating conditions

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------|------------------------------------|---|------|------|------|---------|
| V_{PN} | Supply Voltage | Applied between P-Nu, Nv, Nw | | 300 | 400 | V |
| V_{CC} | Control supply voltage | Applied between V_{CC} -GND | 12 | 15 | 17 | V |
| V_{BS} | High side bias voltage | Applied between V_{BOOTi} - OUT_i for $i = U, V, W$ | 11.5 | | 17 | V |
| t_{dead} | Blanking time to prevent Arm-short | For each input signal | 1 | | | μ s |
| f_{PWM} | PWM input signal | -40°C < T_c < 100°C -40°C < T_j < 125°C | | | 20 | kHz |
| T_c | Case operation temperature | | | | 100 | °C |

Refer to AN3338 for further details.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

5.1 SDIP-25L package information

Figure 11. SDIP-25L package outline

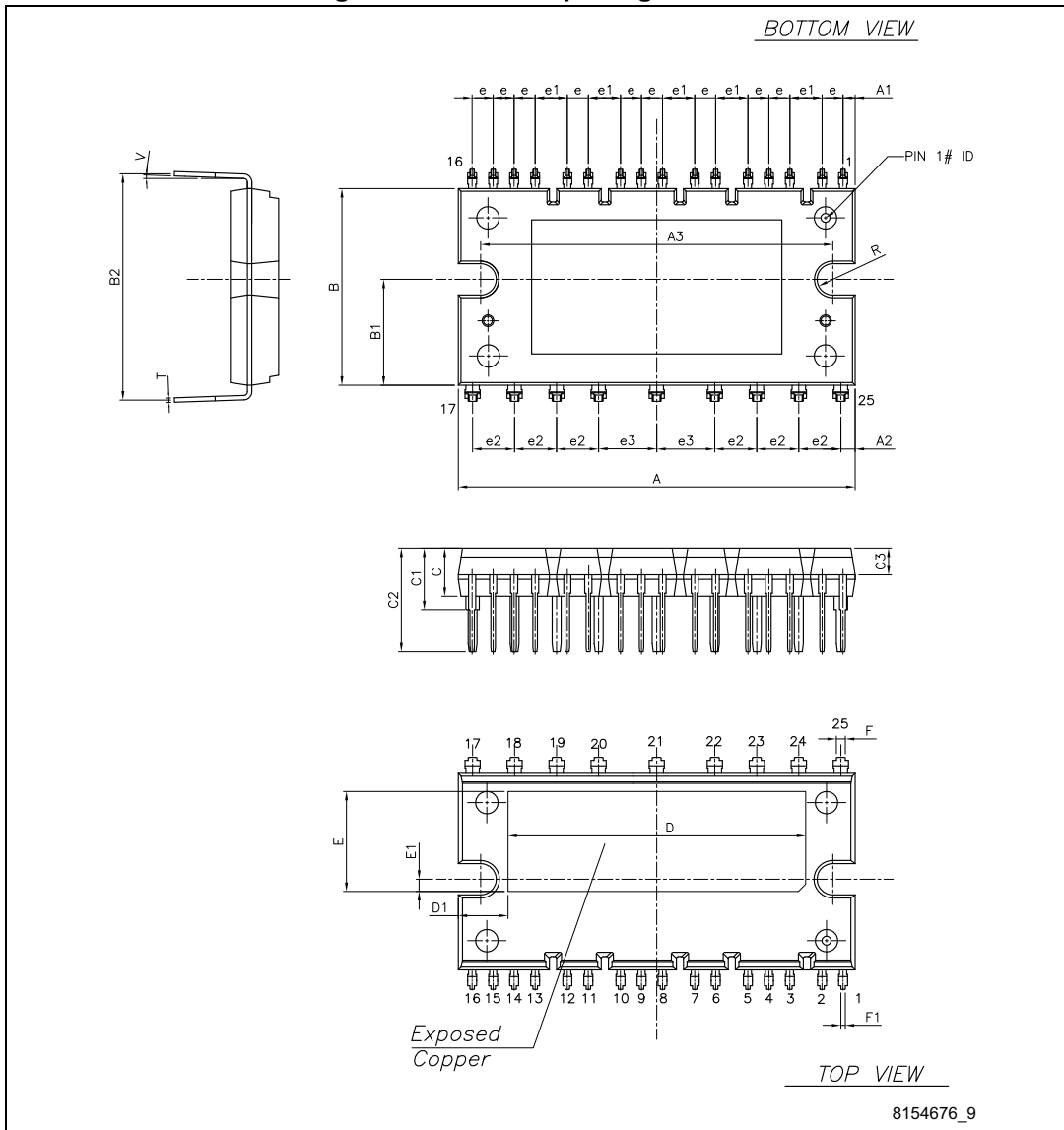
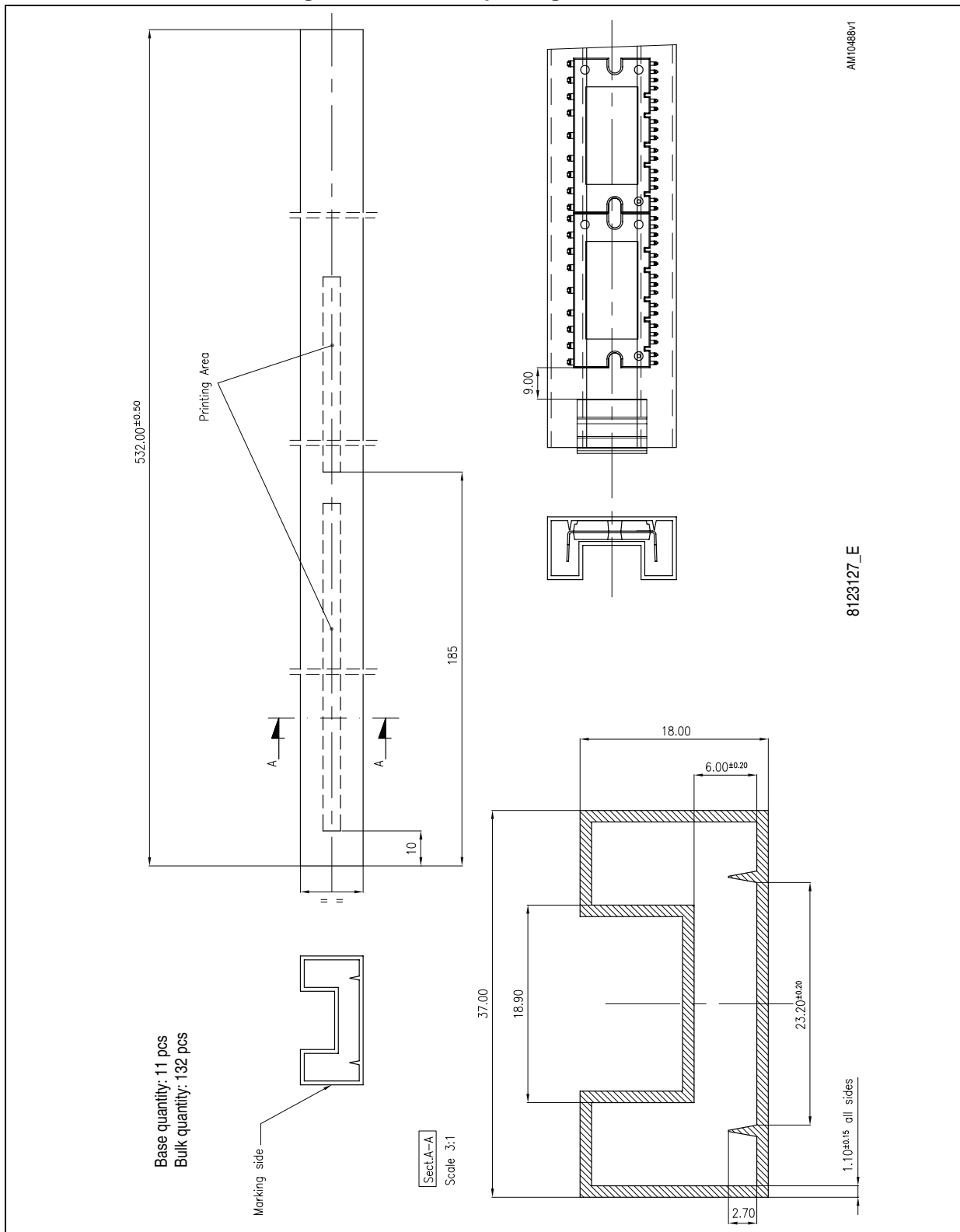


Table 13. SDIP-25L mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 43.90 | 44.40 | 44.90 |
| A1 | 1.15 | 1.35 | 1.55 |
| A2 | 1.40 | 1.60 | 1.80 |
| A3 | 38.90 | 39.40 | 39.90 |
| B | 21.50 | 22.00 | 22.50 |
| B1 | 11.25 | 11.85 | 12.45 |
| B2 | 24.83 | 25.23 | 25.63 |
| C | 5.00 | 5.40 | 6.00 |
| C1 | 6.50 | 7.00 | 7.50 |
| C2 | 11.20 | 11.70 | 12.20 |
| C3 | 2.90 | 3.00 | 3.10 |
| e | 2.15 | 2.35 | 2.55 |
| e1 | 3.40 | 3.60 | 3.80 |
| e2 | 4.50 | 4.70 | 4.90 |
| e3 | 6.30 | 6.50 | 6.70 |
| D | | 33.30 | |
| D1 | | 5.55 | |
| E | | 11.20 | |
| E1 | | 1.40 | |
| F | 0.85 | 1.00 | 1.15 |
| F1 | 0.35 | 0.50 | 0.65 |
| R | 1.55 | 1.75 | 1.95 |
| T | 0.45 | 0.55 | 0.65 |
| V | 0° | | 6° |

5.2 Packing information

Figure 12. SDIP-25L packing information



6 Revision history

Table 14. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 16-Apr-2009 | 1 | Initial release. |
| 11-May-2009 | 2 | Added Figure 7 and Figure 8 . |
| 17-Jul-2009 | 3 | Reduced $V_{CE(sat)}$ value on Table 7 . |
| 06-Apr-2010 | 4 | Document promoted from preliminary data to datasheet. Inserted Figure 3: Switching time test circuit and Table 12: Recommended operating conditions . Updated Table 5: Total system , Table 6: Thermal data , Table 7: Inverter part , Figure 5: NTC resistance vs. temperature , Figure 7: Maximum IC(RMS) current vs. switching frequency , Figure 8: Maximum IC(RMS) current vs. fSINE (1) and Section 5: Package information . |
| 15-Jun-2010 | 5 | Updated Table 7: Inverter part . Minor text changes to improve readability. |
| 17-Nov-2010 | 6 | Updated Table 3, 5, 11 and 12 . Modified Figure 7 and Figure 8 . |
| 07-Mar-2011 | 7 | Updated title with SLLIMM™ in cover page, added SDIP-25L tube dimensions Figure 12 on page 16 . |
| 04-Nov-2011 | 8 | Updated title with SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter - 10 A, 600 V short-circuit rugged IGBT in cover page and SDIP-25L mechanical data Table 13 on page 14 , Figure 11 on page 14 . |
| 28-Aug-2012 | 9 | Modified: Min. and Max. value Table 4 on page 5 . Updated: Table 13 on page 14 , Figure 11 on page 14 and Figure 12 on page 16 . Added: Figure 13 on page 17 . |
| 02-May-2013 | 10 | Modified: Figure 3 on page 8 and Figure 5 on page 10 . Added: Figure 6 on page 10 . |
| 13-Apr-2015 | 11 | Text edits and formatting changes throughout document Updated Figure 2: Pin layout (bottom view) Updated Section 5: Package information |

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