

N-channel 80 V, 5.2 mΩ typ., 100 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

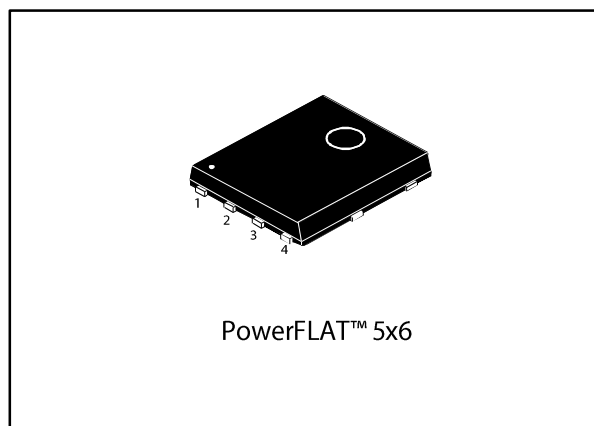
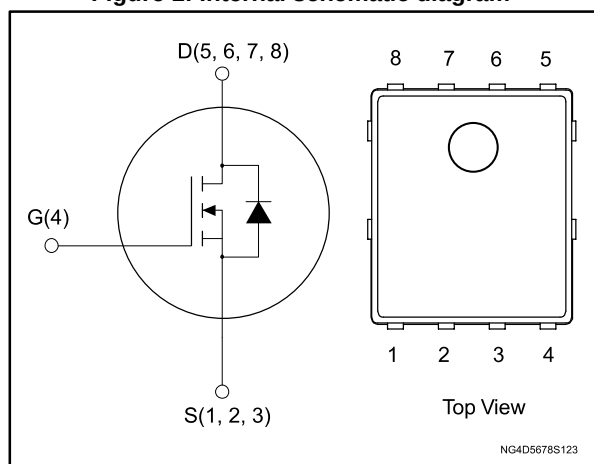


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL100N8F7	80 V	6.1 mΩ	100 A	120 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL100N8F7	100N8F7	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	100	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	71	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	400	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	20	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	14	A
$I_{DM}^{(3)(2)}$	Drain current (pulsed)	80	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	120	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.8	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	220	mJ
T_J	Operating junction temperature	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature		$^{\circ}\text{C}$

Notes:

⁽¹⁾This value is rated according to R_{thj-c} .

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾This value is rated according to $R_{thj-pcb}$.

⁽⁴⁾Starting $T_J=25^{\circ}\text{C}$, $I_D=25\text{ A}$, $V_{DD}=40\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.25	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	80			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 80 V			1	μA
		V _{GS} = 0, V _{DS} = 80 V, T _C = 125 °C			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 10 A		5.2	6.1	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 40 V, f = 1 MHz	-	3435	-	pF
C _{oss}	Output capacitance		-	653	-	pF
C _{rss}	Reverse transfer capacitance		-	57	-	pF
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 20 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	46.8	-	nC
Q _{gs}	Gate-source charge		-	23.4	-	nC
Q _{gd}	Gate-drain charge		-	11.2	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 10 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	49	-	ns
t _r	Rise time		-	95	-	ns
t _{d(off)}	Turn-off delay time		-	60	-	ns
t _f	Fall time		-	32	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0$, $I_{SD} = 20$ A	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 20$ A, $di/dt = 100$ A/ μ s	-	48.6		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60$ V (see Figure 15 : <i>"Test circuit for inductive load switching and diode recovery times"</i>)	-	58.6		nC
I_{RRM}	Reverse recovery current		-	2.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

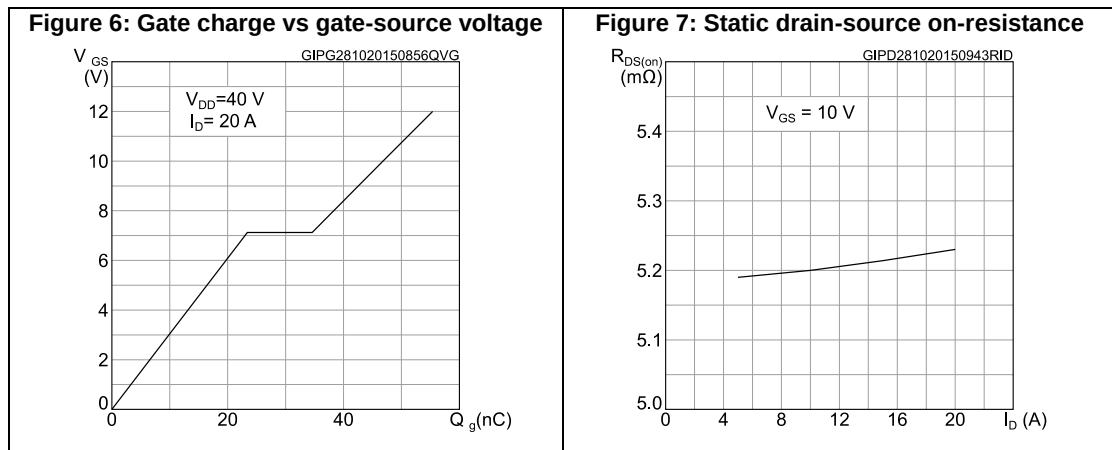
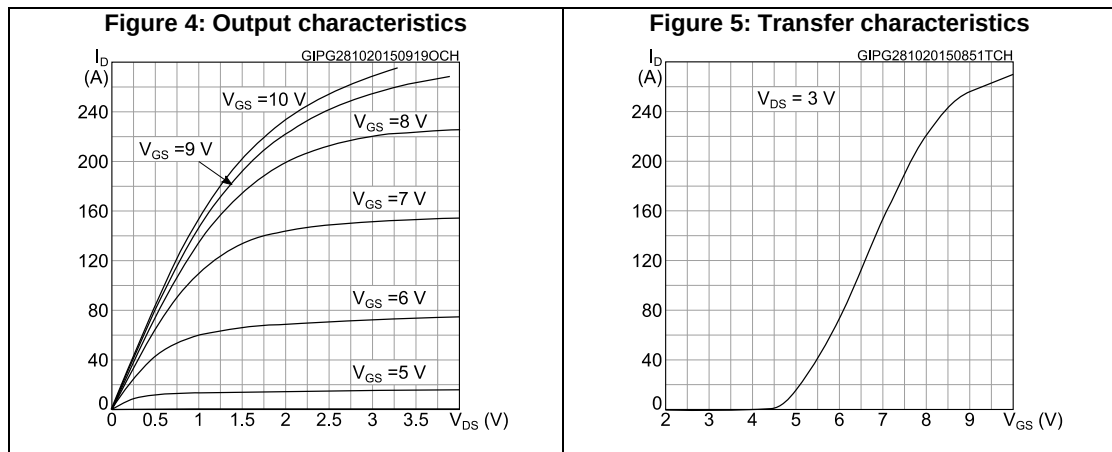
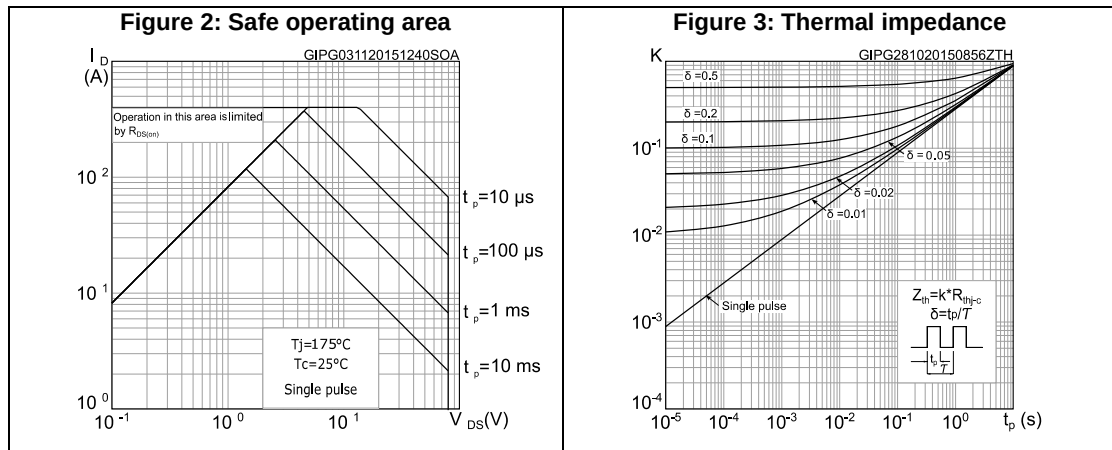


Figure 8: Capacitance variations

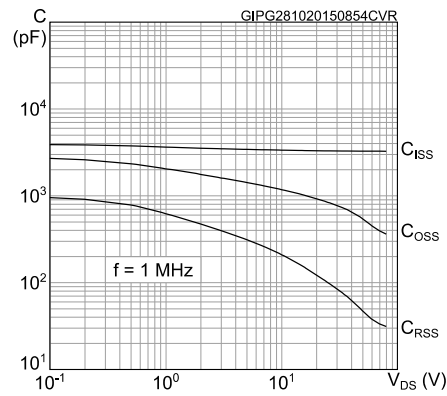


Figure 9: Normalized gate threshold voltage vs temperature

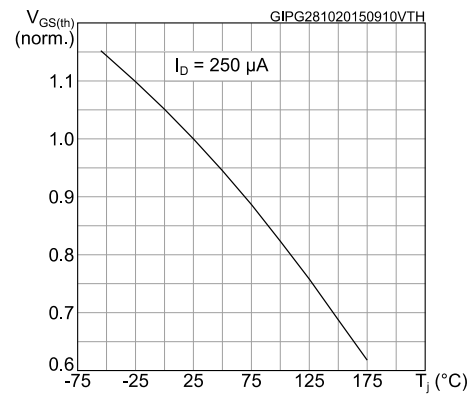


Figure 10: Normalized on-resistance vs temperature

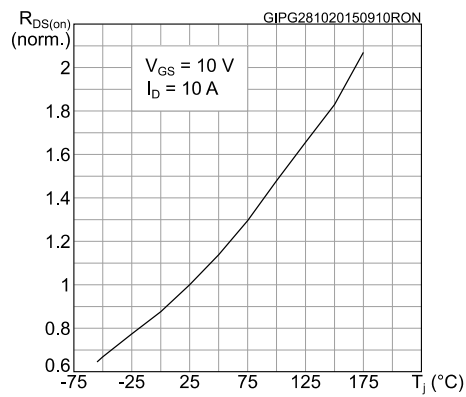


Figure 11: Normalized V(BR)DSS vs temperature

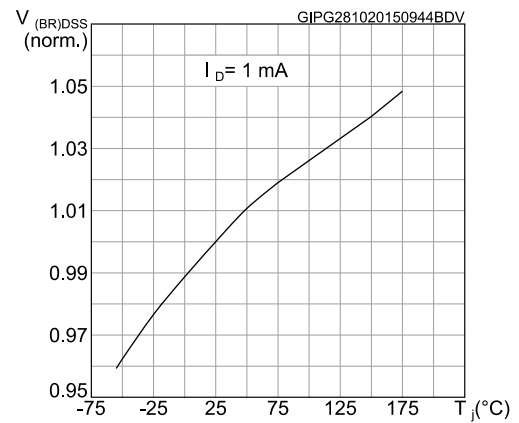
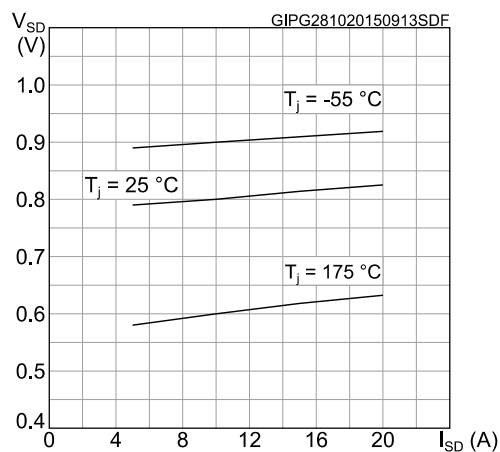
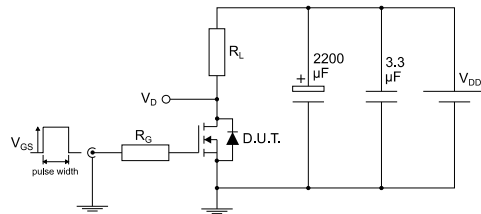


Figure 12: Source-drain diode forward characteristics



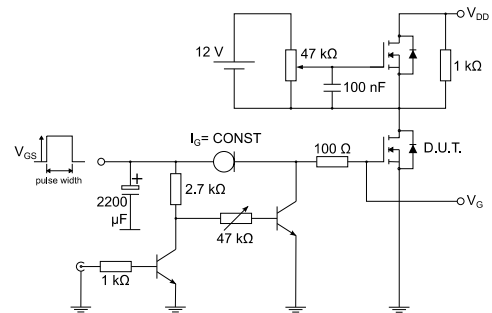
3 Test circuits

Figure 13: Test circuit for resistive load switching times



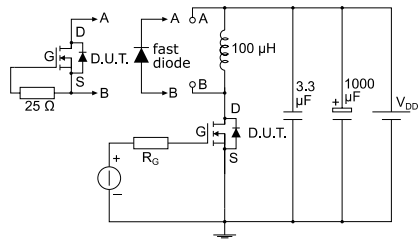
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Figure 14: Test circuit for gate charge behavior



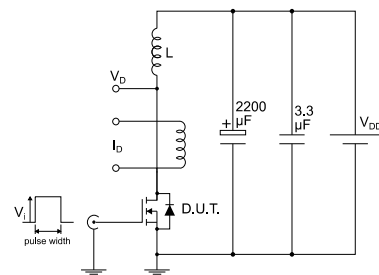
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Figure 15: Test circuit for inductive load switching and diode recovery times



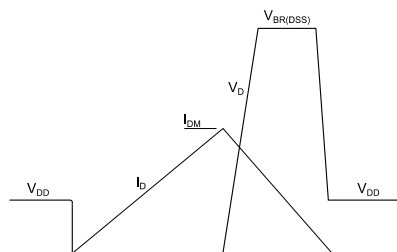
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Figure 16: Unclamped inductive load test circuit



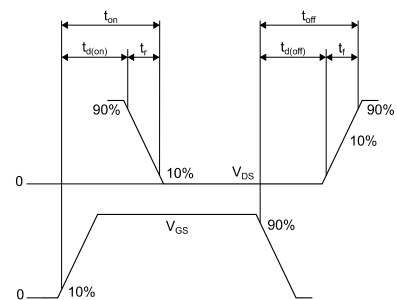
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

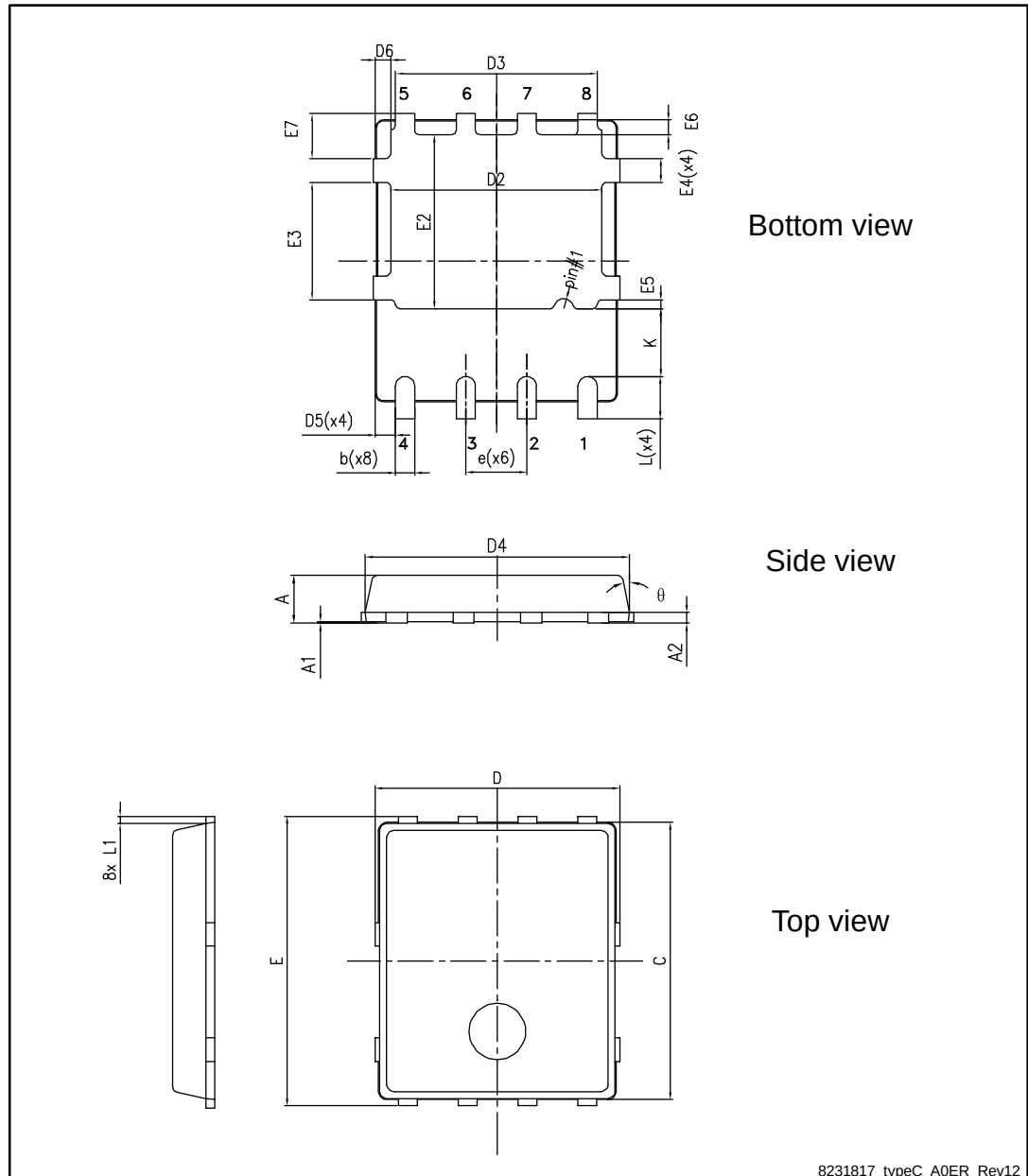
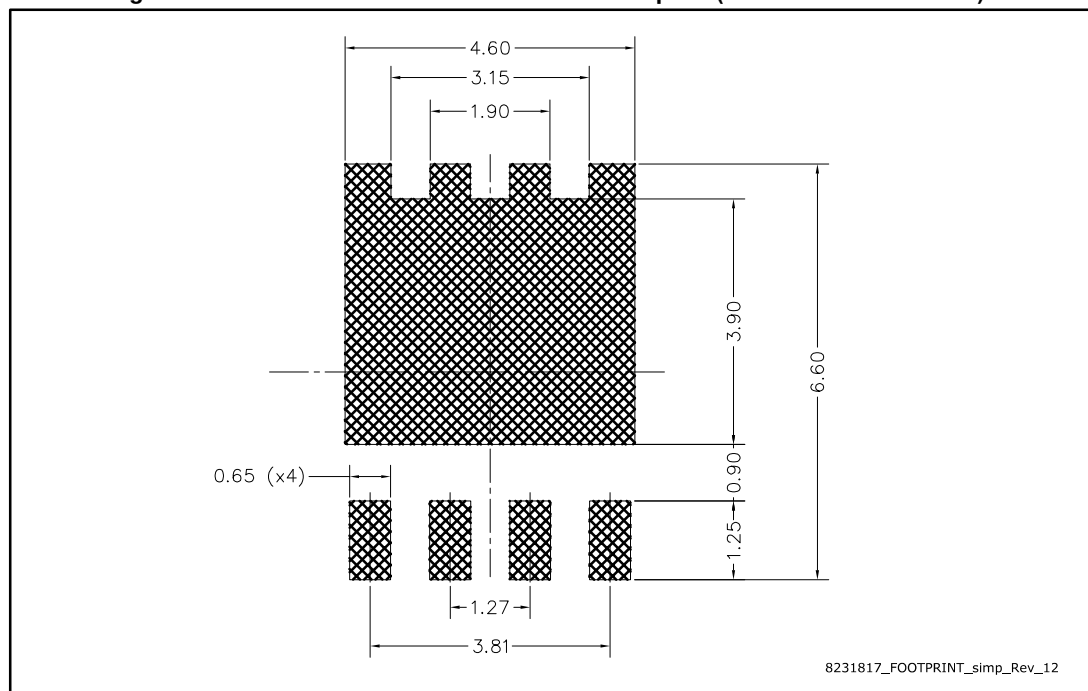


Table 8: PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.715		1.015
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 type C packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

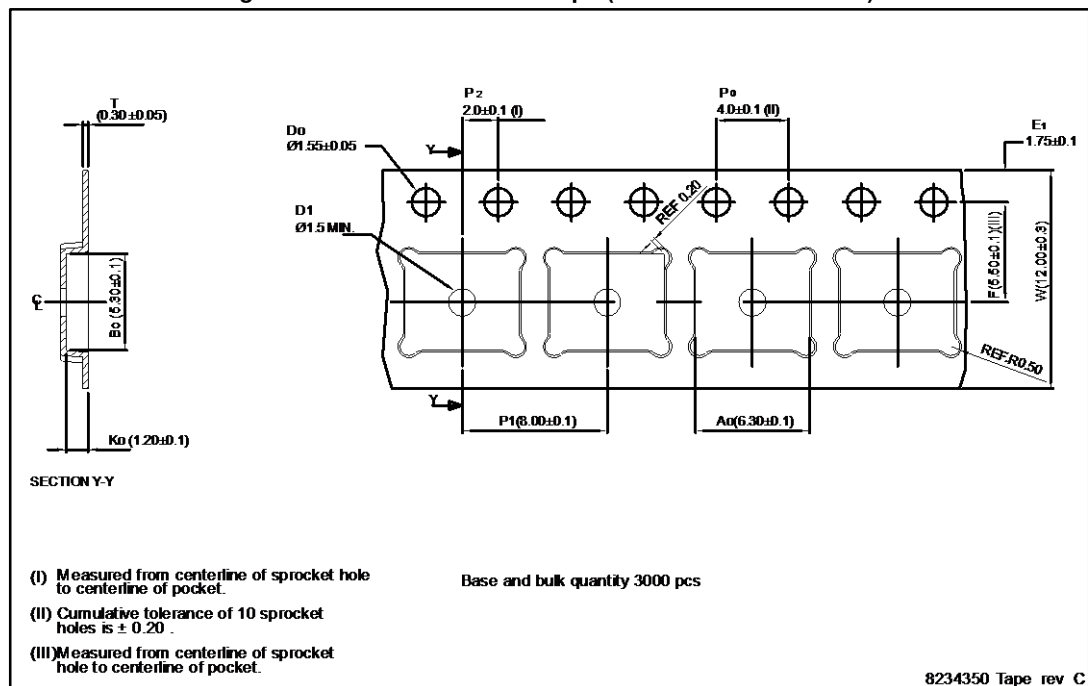


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

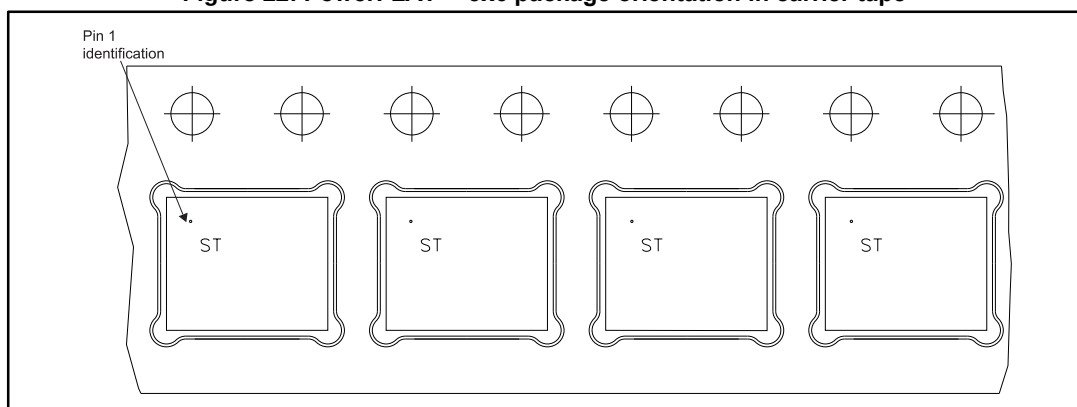
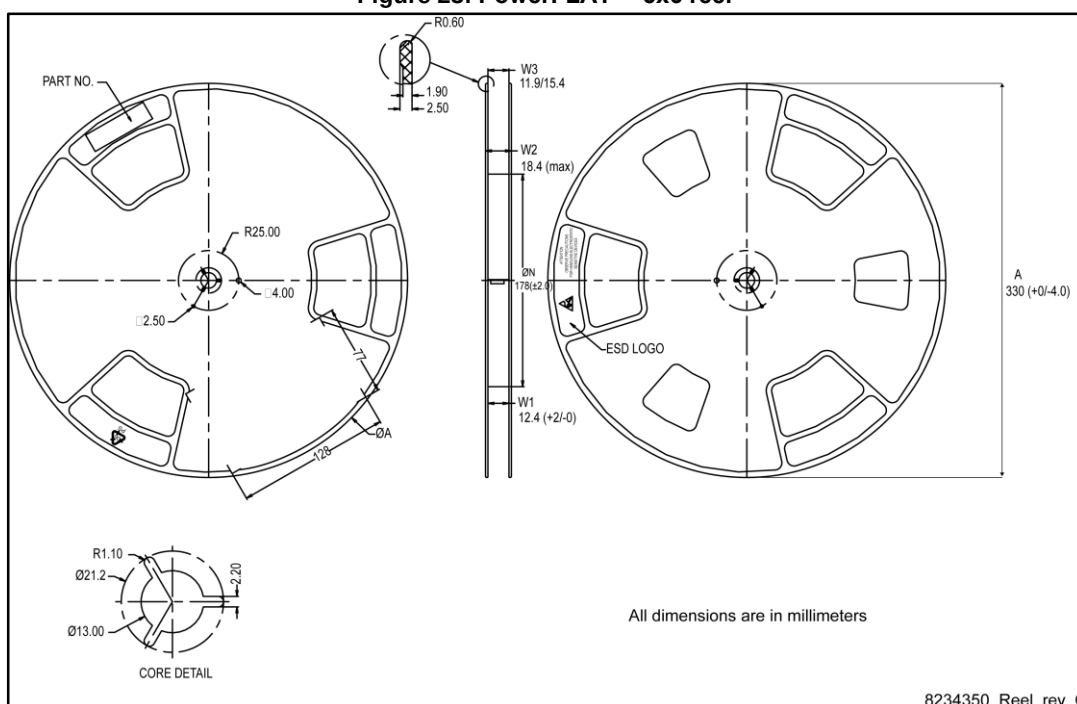


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
21-Oct-2014	1	Initial release.
03-Nov-2015	2	Modified: Table 2: "Absolute maximum ratings" , Table 5: "Dynamic", Table 6: "Switching times" and Table 7: "Source drain diode". Added: Section 4.1: "Electrical characteristics (curves)". Minor text changes
03-Dec-2015	3	Document status promoted from preliminary to production data.

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