# MAUC-011003

## Up Converter
## 27.5 - 33.4 GHz

Rev. V1

### Features

- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Doubler, and RF Buffer
- 12 dB Conversion Gain
- 20 dBm Input Third Order Intercept (IIP3)
- -45 dBm (2x) LO Leakage (at RF Port)
- Variable Gain with Adjustable Bias
- Lead-Free 4 mm, 24 Lead QFN Package
- RoHS^ Compliant and 260°C Reflow Compatible

### Description

The MAUC-011003 is an integrated up-converter assembled in a lead-free 4 mm 24-lead PQFN plastic package. This device has a typical conversion gain of 12 dB, and an image rejection of 15 dBc. This up-converter includes a LO doubler, LO buffer amplifier, and RF buffer amplifier. Variable gain can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and 2×LO leakage over the gain control range. The output IP3 is 32 dBm at maximum gain.

The MAUC-011003 is ideally suited for 28 and 32 GHz band point-to-point radios under both LSB and USB operation and Ka-Band VSAT applications.

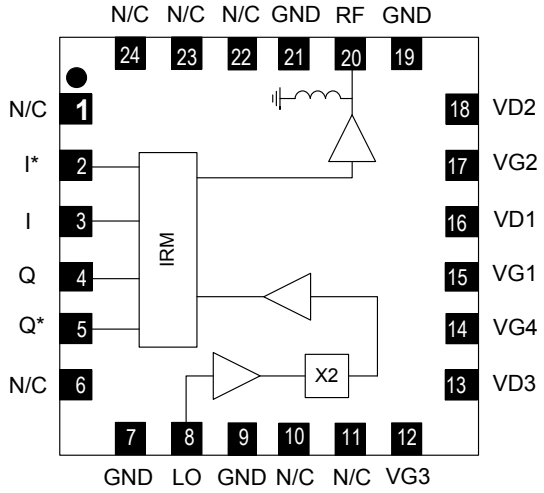
Each device is 100% RF tested to ensure performance compliance.

### Ordering Information[1]

| Part Number | Package |
|---|---|
| MAUC-011003-TR0500 | 500 Piece Reel |
| MAUC-011003-001SMB | Sample Board |

1. Reference Application Note M513 for reel size information.

### Functional Schematic




### Pin Configuration[2]

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | N/C | 13 | VD3 |
| 2 | I* | 14 | VG4 |
| 3 | I | 15 | VG1 |
| 4 | Q | 16 | VD1 |
| 5 | Q* | 17 | VG2 |
| 6 | N/C | 18 | VD2 |
| 7 | GND | 19 | GND |
| 8 | LO | 20 | RF |
| 9 | GND | 21 | GND |
| 10 | N/C | 22 | N/C |
| 11 | N/C | 23 | N/C |
| 12 | VG3 | 24 | N/C |
| | | 25 | Paddle[3] |

2. For optimum RF performance, all N/C's should be terminated to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

^ Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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### Electrical Specifications: LO = 0 dBm, IF = -10 dBm @ 2 GHz, $V_D1,2^4$ = 4 V, $V_D3^4$ = 3 V, $I_D1 + I_D2$ = 240 mA, $I_D3$ = 140 mA, $V_G4$ = -3 V, $T_A$ = 25°C

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Frequency Range (RF) | GHz | 27.5 | - | 33.4 |
| Frequency Range (LO) | GHz | 12 | - | 18.45 |
| LO Input Power (PLO) | dBm | - | 0 | - |
| Conversion Gain | dB | 8.5 | 12.0 | 14.0 |
| Image Rejection | dBc | - | 15 | - |
| Input IP3 | dBm | - | 20 | - |
| Output IP3 ($P_{IN}$ = -10 dBm/tone) | dBm | 28 | 32 | - |
| Spurious (2xLO) [tuned - IF voltages ~ 0.2 V] | dBm | - | -45 | - |
| Spurious (1xLO) | dBm | - | -55 | - |
| Gate Voltages ($V_G1$,$V_G2$,$V_G3$)[4] | V | -1.0 | - | -0.1 |
| Gate Current ($I_G1 + I_G2$) | mA | -2.0 | - | 0 |
| Gate Current ($I_G3$) | mA | -0.5 | - | 0 |

4. Apply gate voltages prior to drain voltages. First turn on $V_G4$ = -3 V. Then adjust $V_G1$, $V_G2$ and $V_G3$ between -1.0 and -0.1 V to achieve specified drain current. Typical current (380 mA) = 240 ($I_D1 + I_D2$) + 140 ($I_D3$) . Refer to App Note [1] for biasing details.

### Absolute Maximum Ratings[5,6,7]

| Parameter | Absolute Max. |
|---|---|
| Drain Voltage | 4.3 V |
| Gate Bias Voltage ($V_G$1,2,3) | -1.5 V < $V_G$ < 0 V |
| Gate Bias Voltage ($V_G4$) | -4.0 V < $V_G$ < 0 V |
| Input Power | 10 dBm |
| LO Input Power | 13 dBm |
| Storage Temperature | -55°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Junction Temperature | +150°C |

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x $10^6$ hours.

### Handling Procedures

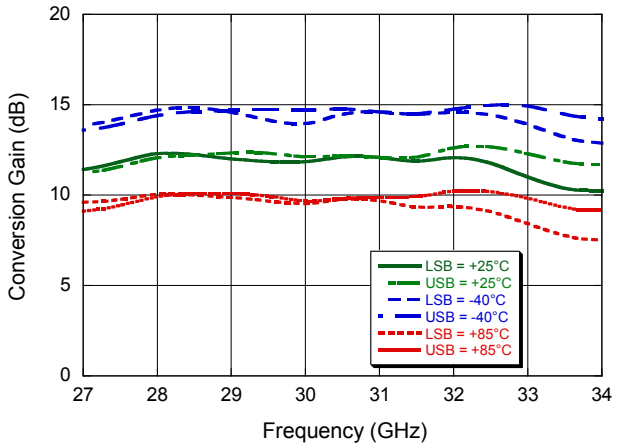
Please observe the following precautions to avoid damage:

### Static Sensitivity

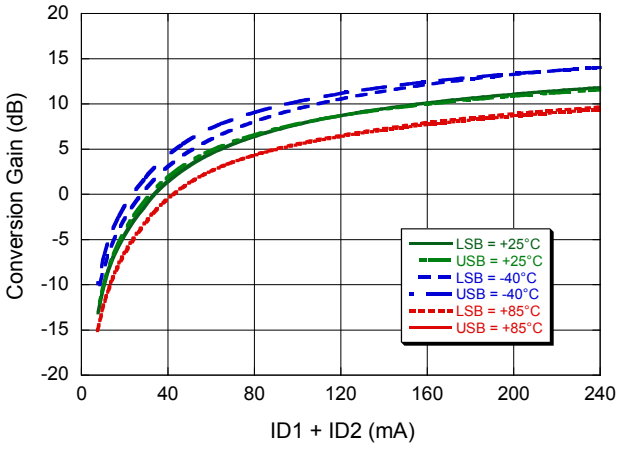
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these static sensitive devices.

## Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, $P_{DC}$ = 1.38 W

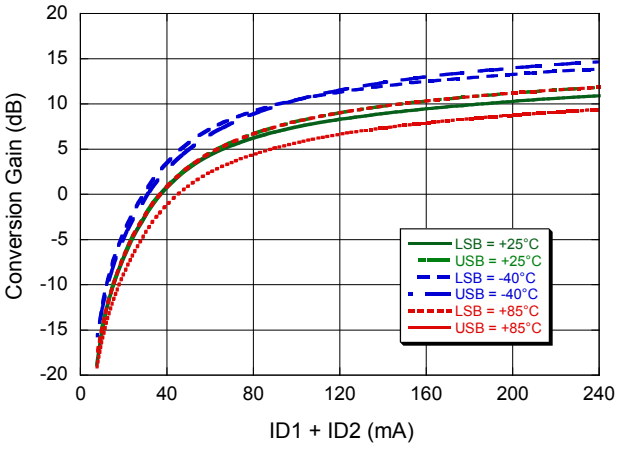
***Conversion Gain***



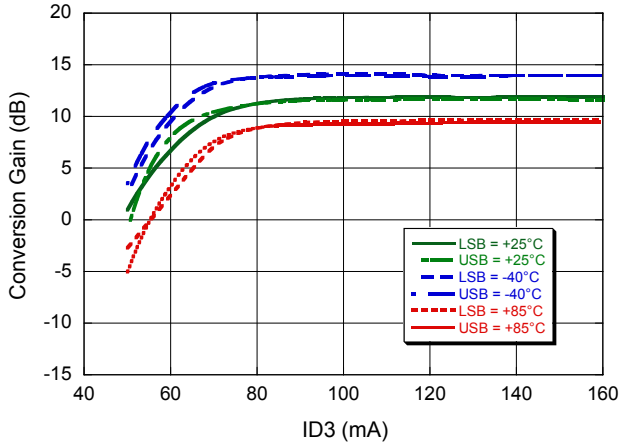

***Conversion Gain @ 27.5 GHz***



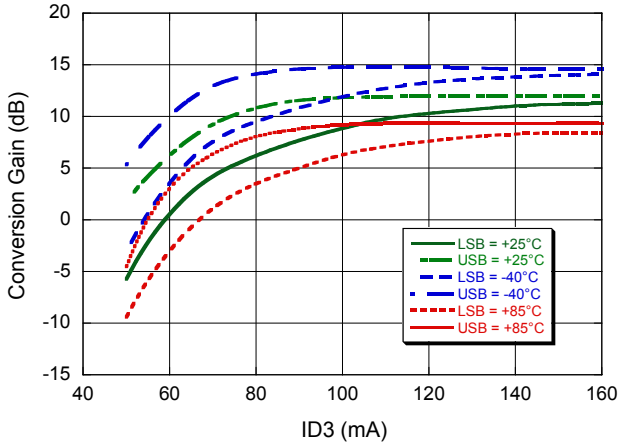

***Conversion Gain @ 33.5 GHz***




***Conversion Gain @ 27.5 GHz***

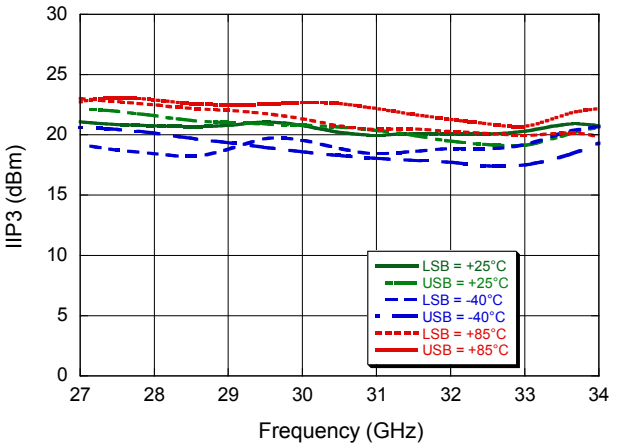



***Conversion Gain @ 33.5 GHz***

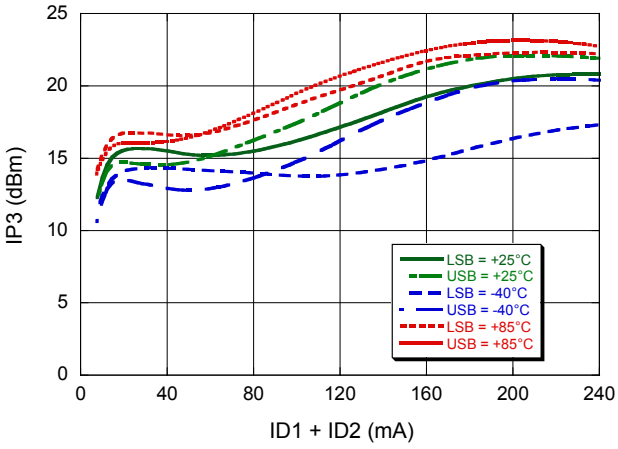


## Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, $P_{DC}$ = 1.38 W

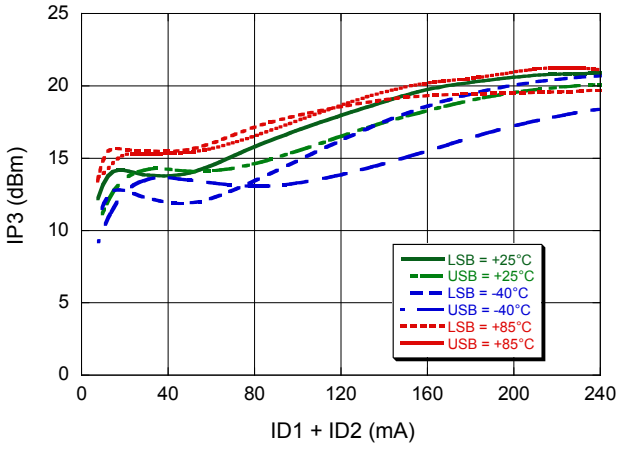
***Input IP3***



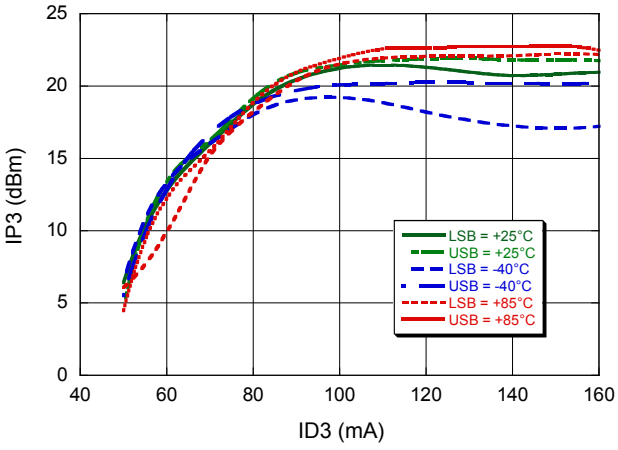

***Input IP3 @ 27.5 GHz***



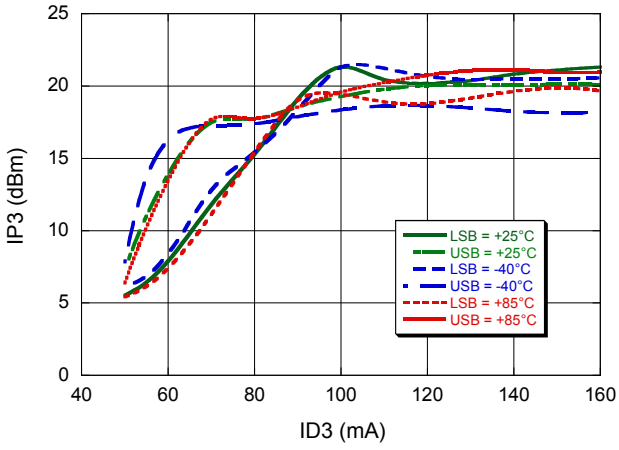

***Input IP3 @ 33.5 GHz***




***Input IP3 @ 27.5 GHz***

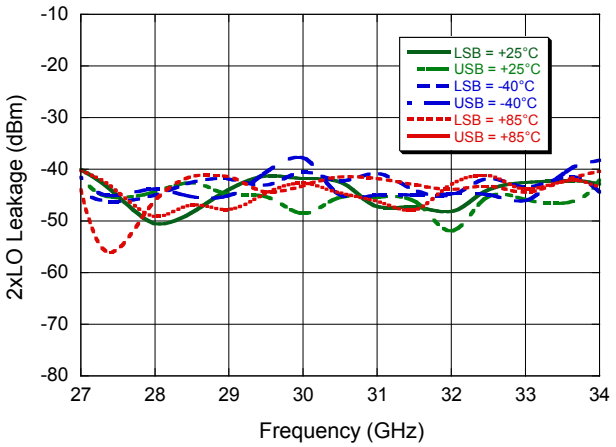



***Input IP3 @ 33.5 GHz***



## Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, $P_{DC}$ = 1.38 W

***2xLO Leakage***




***1xLO Leakage***

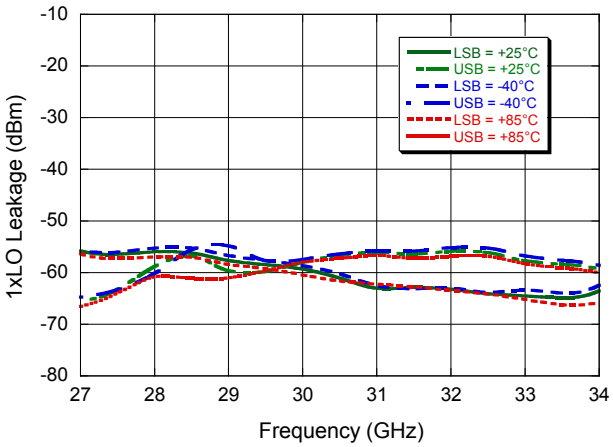
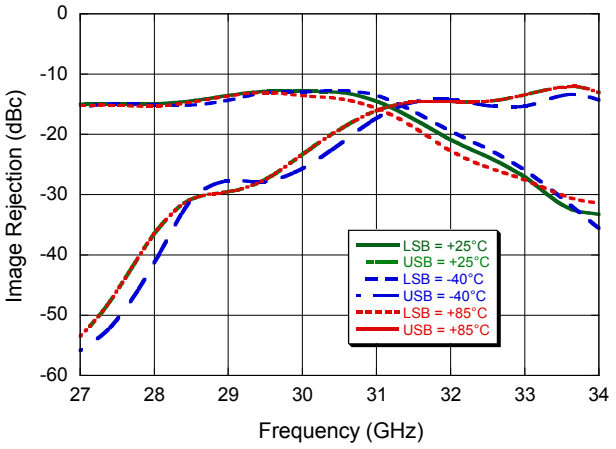



***Image Rejection***

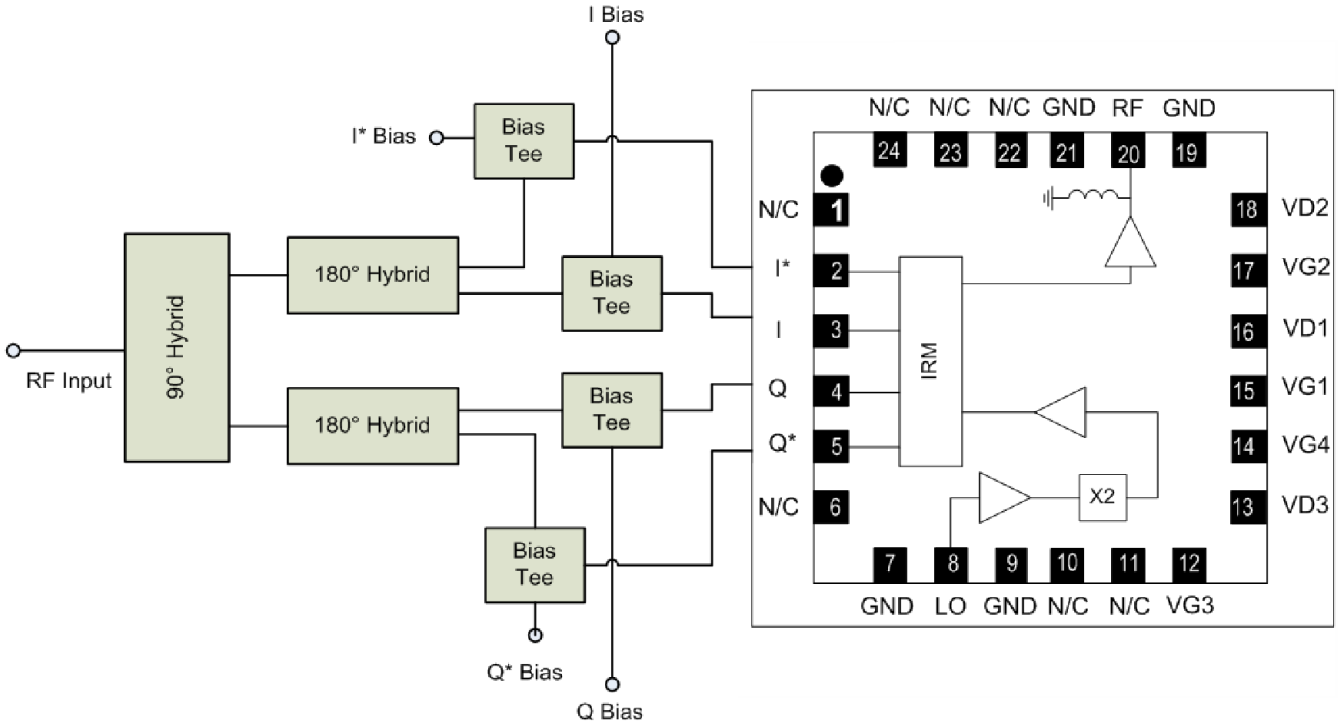


## App Note [1] Biasing

Apply negative gate bias before applying positive drain bias. MAUC-011003 is operated by biasing $V_D1$ and $V_D2$ at 4 V and $V_D3$ at 3 V. The drain currents are set to 90 mA, 150 mA, and 140 mA respectively. $V_G4$ requires a fixed voltage bias of nominally -3 V. In order to maintain the best performance over temperature it is recommended to use active bias on $V_G1$, $V_G2$ and $V_G3$ to keep the currents in $V_D1$, $V_D2$ and $V_D3$ constant. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current.

## App Note [2] IF Inputs

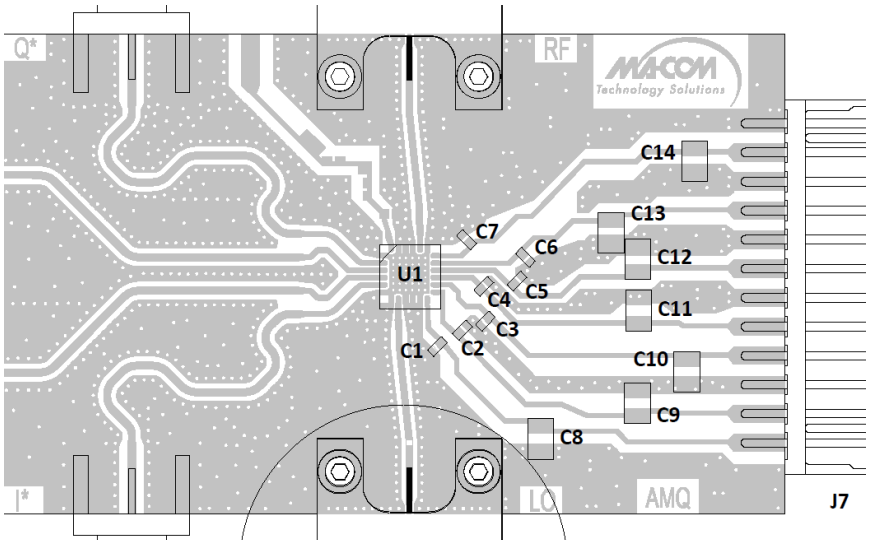
The IF input to the typical configuration is through a 90° hybrid coupler. The hybrid splits the IF input into in-phase and quadrature-phase components which feed into two 180° hybrid couplers splitting into 4 signals. These four signals enter the MAUC-011003 on I/I*,Q/Q* IF inputs. For highest gain, best image rejection and lowest noise figure, all the 4 IF inputs should be used.



## App Note [3] Board Layout

As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF (C1 - C7) and 1 µF (C8 - C14) on each of the bias lines are recommended placed a distance further away.

### Recommended Board Layout



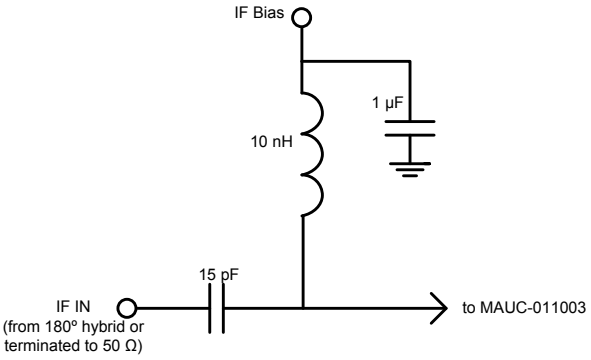

## App Note [4] IF Bias Tuning

To obtain optimum 2xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (I, Q, I*, Q*). DC bias is implemented by adding simple bias tees to each of the four IF ports. The diagram below shows a typical bias tee design used.

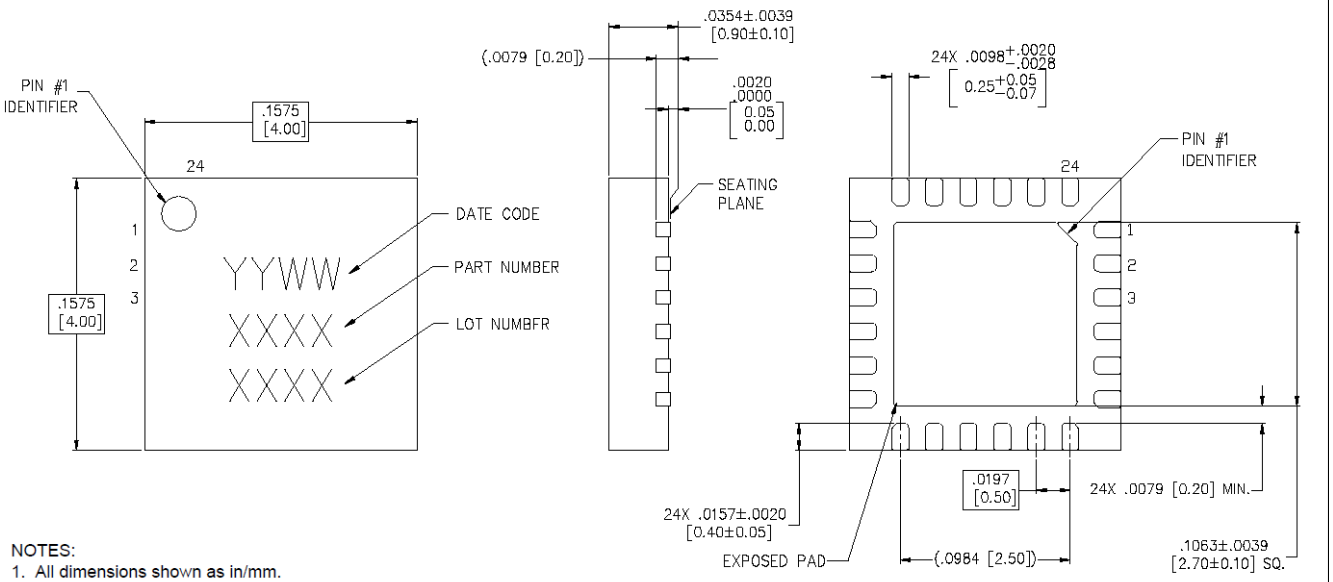
If the I and Q ports are used for the IF input, the I* and Q* ports are DC biased and terminated into 50 Ω. A typical tuning arrangement is to apply a fixed 0.3 V DC bias to both the used IF input ports: I, Q. The remaining two IF ports which have been terminated to 50 Ω tuning independently for minimum 2xLO leakage.

For minimum 2xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.

### Typical Configuration



## *Lead-Free* 4 mm 24-Lead PQFN †




NOTES:
1. All dimensions shown as in/mm.
2. Reference S2083 application note for PCB footprint information.
3. Reference JEDEC MO-220, VAR. VGGD-6 for additional dimensional and tolerance information.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin.