# CCM Boost LED Driver with Sub-Microsecond PWM Dimming and Open Loop Protection

## Features

- Switch-mode controller for single switch converters
  - Boost
  - SEPIC
- Current loop closed with sub-microsecond PWM dimming pulses supports PWM dimming >20kHz
- High PWM dimming ratio (>10,000:1)
- Internal 40V linear regulator
- Internal ±2% voltage reference
- Programmable constant frequency operation
- Programmable slope compensation
- Programmable soft start
- 10V, +0.25A/-0.5A MOSFET gate drivers
- Hiccup mode protection for both short circuit and open circuit conditions
- Latching protection from open loop
- Active-Low, open-drain output to indicate a fault condition

## Applications

- LED backlights for LCD Displays

## General Description

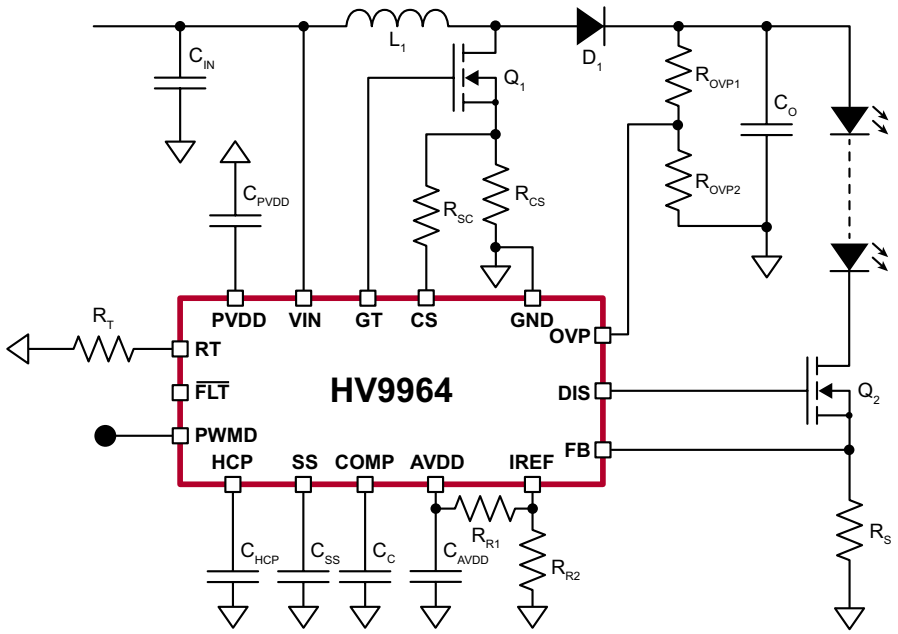
The HV9964 is a current mode control LED driver IC designed to control single switch PWM converters (boost or SEPIC) in a constant frequency mode. The controller uses a peak current-mode control scheme (with programmable slope compensation) and includes an internal transconductance amplifier to accurately control the output current over all line and load conditions. The IC also provides a load switch gate drive output, which can be used to disconnect the LEDs in case of a fault condition using an external load switch. The 10V external FET drivers allow the use of standard level FETs. The low voltage 5V AVDD is used to power the internal logic and also acts as a reference voltage to set the current level.

The HV9964 features Supertex' proprietary PWM dimming control algorithm achieving a dimming pulse of a few hundred nanoseconds from a continuous conduction mode (CCM) or discontinuous-conduction mode (DCM) boost converter, while maintaining the instantaneous LED constant current determined by the reference voltage input. This feature permits dimming frequency outside of the audible range. The feature can also yield a wide dimming ratio in excess of 10,000:1 at low dimming frequency.

The HV9964 provides a full protection feature set, including output-short and open-circuit protection with auto-restart, and latching open-loop protection with an open-drain flag output.

The HV9964 is powered by a built-in 40V linear regulator.

## Typical Boost Application Circuit

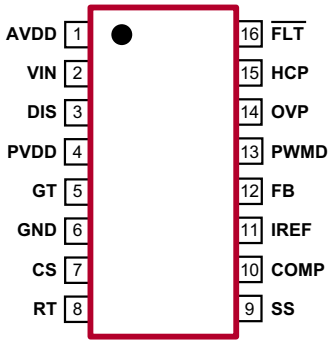


## Ordering Information

| Part Number | Package Options | Packing |
|---|---|---|
| HV9964NG-G | 16-Lead SOIC | 45/Tube |
| HV9964NG-G M934 | 16-Lead SOIC | 2500/Reel |

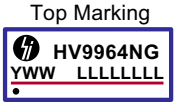
*-G indicates package is RoHS compliant ('Green')*

## Pin Description

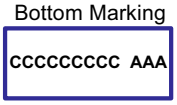



**16-Lead SOIC (NG)**

Top Marking




Bottom Marking




Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

*Package may or may not include the following marks: Si or*

**16-Lead SOIC (NG)**

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| VIN to GND | -0.5V to +45V |
| PVDD to GND | -0.3V to +12V |
| GT, DIS to GND | -0.3V to (PVDD +0.3V) |
| AVDD to GND | -0.3V to 6.0V |
| IREF to GND | -0.3V to 3.0V |
| All other pins to GND | -0.3V to ($AV_{DD}$ +0.3V) |
| Junction temperature | +150°C |
| Storage ambient temperature range | -65°C to +150°C |
| Continuous power dissipation *($T_A$ = +25°C)* | 1000mW |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Typical Thermal Resistance

| Package | $\theta_{ja}$ |
|---|---|
| 16-Lead SOIC | 83°C/W |

## Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < $T_A$ < +125°C, otherwise the specifications are at $T_A$ = 25°C. $V_{IN}$ = 24V, $C_{PVDD}$ = 1.0µF, $C_{AVDD}$ = 1.0µF, $C_{GT}$ = 1.0nF, $C_{RT}$ = 1.0nF, $C_{DIS}$ = 330pF unless otherwise noted.)*

| Sym | Description | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **Input** | | | | | | | |
| $V_{INDC}$ | Input DC supply voltage range | - | 9.0 | - | 40 | V | DC input voltage |
| $I_{INSD}$ | Shut-down mode supply current | - | - | - | 1.5 | mA | PWMD = GND |
| **Internal Regulator for Gate Drivers** | | | | | | | |
| $PV_{DD}$ | Internally regulated voltage | - | 9.5 | 10 | 10.5 | V | $V_{IN}$ = 12 - 40V, $f_S$ = 500kHz, PWMD = $V_{DD}$ |
| $UVLO_{RISE}$ | $V_{DD}$ under voltage lockout threshold | * | 6.65 | - | 7.20 | V | $PV_{DD}$ rising |
| $UVLO_{HYST}$ | $V_{DD}$ under voltage hysteresis | - | - | 500 | - | mV | $PV_{DD}$ falling |
| $PV_{DD,MIN}$ | Minimum $V_{DD}$ voltage | * | 8.0 | - | - | V | $V_{IN}$ = 9.0V, PWMD = $V_{DD}$, $f_S$ = 500kHz, $C_{GT}$ = 2.0nF |

## Electrical Characteristics *(cont.)*

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| Sym | Description | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **Internal Low Voltage Regulator** | | | | | | | |
| $AV_{DD}$ | Internally regulated voltage | * | 4.9 | 5.0 | 5.1 | V | $V_{IN}$ = 9 - 40V, PWMD = $V_{DD}$ |
| $I_{AVDD\_ext}$ | External current draw | - | 0 | - | 500 | µA | --- |
| **PWM Dimming** | | | | | | | |
| $V_{PWMD(lo)}$ | PWMD input low voltage | * | - | - | 0.8 | V | --- |
| $V_{PWMD(hi)}$ | PWMD input high voltage | * | 2.0 | - | - | V | --- |
| $t_d$ | Latching delay time | - | - | 100 | - | ns | --- |
| $R_{PWMD}$ | PWMD pull down resistor | - | 50 | 100 | 150 | kΩ | $V_{PWMD}$ = 3.3V |
| **GT Output** | | | | | | | |
| $I_{SOURCE}$ | Short circuit current, sourcing | - | 0.25 | - | - | A | $V_{GT}$ = 0V |
| $I_{SINK}$ | Sinking current | - | 0.50 | - | - | A | $V_{GT}$ = 10V |
| $T_{RISE}$ | Output rise time | - | - | 34 | - | ns | PVDD = 10V |
| $T_{FALL}$ | Output fall time | - | - | 13 | - | ns | PVDD = 10V |
| **Over Voltage Protection** | | | | | | | |
| $V_{OVP,rising}$ | Over voltage rising trip point | * | 1.94 | 2.00 | 2.06 | V | OVP rising |
| $V_{OVP,HYST}$ | Over voltage hysteresis | - | - | 0.20 | - | V | OVP falling |
| **Hiccup Timer** | | | | | | | |
| $K_{HCP+}$ | Multiplier for charging current | - | - | 0.50 | - | - | $C_{HCP}$ = 10nF – 100nF; 10µA current @ 100kHz switching frequency |
| $K_{HCP-}$ | Multiplier for discharging current | - | - | 0.75 | - | - | $C_{HCP}$ = 10nF – 100nF; 15µA current @ 100kHz switching frequency |
| $V_{FC}$ | Voltage level to start gate driver | - | - | 1.8 | - | V | --- |
| $V_{DLY}$ | Voltage level for open loop detection | - | - | 2.0 | - | V | --- |
| $V_{RST}$ | Voltage level restart HCP timer | - | - | 0.1 | - | V | --- |
| $I_{DIS}$ | Discharging current (pull down FET) | - | 10 | - | - | mA | $V_{TMR}$ = 5.0V |
| **Soft Start** | | | | | | | |
| $K_{SS+}$ | Multiplier for charging current | - | - | 0.5 | - | - | $C_{SS}$ = 1nF - 10nF; 10µA current @ 100kHz switching frequency |
| $I_{SS-}$ | Discharging current | - | 1.0 | - | - | mA | $V_{SS}$ = 5.0V |

***Note:***

*# Denotes specifications guaranteed by design*

## Electrical Characteristics *(cont.)*

*((The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < $T_A$ < +125°C, otherwise the specifications are at $T_A$ = 25°C. $V_{IN}$ = 24V, $C_{PVDD}$ = 1.0µF, $C_{AVDD}$ = 1.0µF, $C_{GT}$ = 1.0nF, $C_{RT}$ = 1.0nF, $C_{DIS}$ = 330pF unless otherwise noted.)*

| Sym | Description | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **Slope Compensation** | | | | | | | |
| $I_{SLOPE}$ | Peak current out of CS pin | - | 150 | 180 | 216 | µA | --- |
| $T_{SETTLING}$ | Settling time for current sourced | - | - | - | 800 | ns | --- |
| **Current Sense** | | | | | | | |
| $T_{BLANK}$ | Leading edge blanking | * | 100 | - | 250 | ns | --- |
| $T_{DELAY1}$ | Delay to output of output comparator | - | - | - | 200 | ns | COMP = $AV_{DD}$, 50mV overdrive at CS |
| $R_{div}$ | Internal resistor divider ratio – COMP to CS | # | - | 1/12 | - | - | --- |
| $V_{OFFSET}$ | Comparator offset voltage | - | -10 | - | +10 | mV | --- |
| **Internal Transconductance Opamp** | | | | | | | |
| GB | Gain-bandwidth product | # | - | 1.0 | - | MHz | 75pF capacitance at COMP pin |
| $A_V$ | Open loop DC gain | - | 65 | - | - | dB | Output open |
| $V_{CM}$ | Input common-mode range | # | -0.3 | - | 3.0 | V | --- |
| $V_{COMP}$ | Output voltage range | # | 0.7 | - | $AV_{DD}$ -0.7 | V | $A_V$ > 50dB |
| $G_m$ | Transconductance | - | - | 1.5 | - | mA/V | --- |
| $V_{OFFSET}$ | Input offset voltage | * | -3.0 | - | 3.0 | mV | --- |
| $I_{COMP+}$ | COMP sink current | # | - | 0.2 | - | mA | $V_{FB}$ = AVDD, $V_{IREF}$ = 0, $V_{COMP}$ = 0 |
| $I_{COMP-}$ | COMP source current | # | - | 0.2 | - | mA | $V_{FB}$ = 0V, $V_{IREF}$ = AVDD, $V_{COMP}$ = AVDD -0.7V |
| $I_{BIAS}$ | Input bias current | # | - | 0.5 | 1.0 | nA | --- |
| $I_{COMP,DIS}$ | Discharging current | - | 10 | - | - | mA | $V_{COMP}$ = 5.0V |
| **Oscillator** | | | | | | | |
| $f_{OSC1}$ | Oscillator frequency | * | 88 | 100 | 112 | kHz | RT = 193kΩ |
| $f_{OSC2}$ | Oscillator frequency | * | 440 | 500 | 560 | kHz | RT = 39kΩ |
| $F_{OSC}$ | Output frequency range | # | 88 | - | 560 | kHz | --- |
| $D_{MAX}$ | Maximum duty cycle | * | 87 | - | 93 | % | --- |

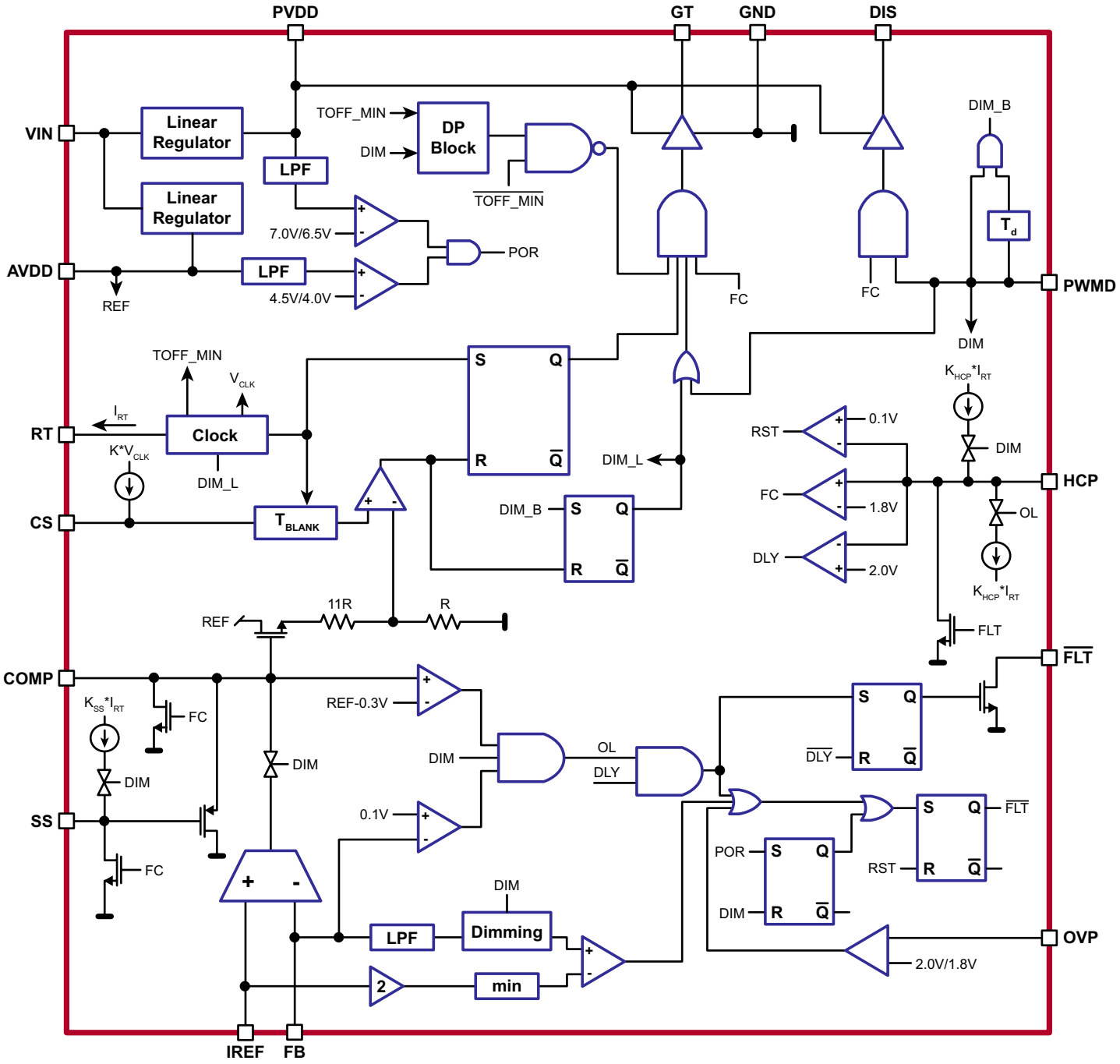
***Note:***
*# Denotes specifications guaranteed by design*

## Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < $T_A$ < +125°C, otherwise the specifications are at $T_A$ = 25°C. $V_{IN}$ = 24V, $C_{PVDD}$ = 1.0µF, $C_{AVDD}$ = 1.0µF, $C_{GT}$ = 1.0nF, $C_{RT}$ = 1.0nF, $C_{DIS}$ = 330pF unless otherwise noted.)*

| Sym | Description | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **Output Short Circuit** | | | | | | | |
| $G_{SC}$ | Gain for short circuit comparator | - | 1.8 | 2.0 | 2.2 | - | --- |
| $V_{OMIN}$ | Minimum output voltage of the gain stage | * | 0.14 | 0.20 | 0.26 | V | $I_{REF}$ = GND |
| $T_{OFF}$ | Propagation time for short circuit detection | - | - | - | 250 | ns | PWMD = $V_{DD}$, $I_{REF}$ = 400mV; FB step from 0 to 900mV; $\overline{FLT}$ goes from high to low; no capacitance at DIS pin |
| $T_{RISE,DIS}$ | DIS output rise time | - | - | - | 100 | ns | 330pF capacitance at DIS pin |
| $T_{FALL,DIS}$ | DIS output fall time | - | - | - | 100 | ns | 330pF capacitance at DIS pin |
| $T_{BLANK,SC}$ | Blanking time | * | 500 | - | 700 | ns | --- |
| **Fault Monitor** | | | | | | | |
| $V_{\overline{FLT}(LOW)}$ | $\overline{FLT}$ low voltage | - | 0 | - | 0.3 | V | $I_{FLT}$ = 1.0mA |
| **Open Loop Detection** | | | | | | | |
| $V_{FB(TH)}$ | FB threshold voltage | - | 85 | - | 115 | mV | --- |
| $V_{COMP\ (TH)}$ | COMP threshold voltage | - | AVDD -0.3 | - | - | V | --- |

## Functional Block Diagram



## Power Topology

The HV9964 is a switch-mode LED driver designed to control a boost or SEPIC converter in a constant frequency mode. The IC includes internal linear regulators, which enables it to operate at input voltages from 9 to 40V. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, and accurate control of the LED current. It also includes logic to enable enhanced PWM dimming which allows dimming ratios in excess of 10,000:1.

## Power Supply to the IC (VIN, PVDD and AVDD)

The HV9964 can be powered directly from its VIN pin that takes a voltage up to 40V. There are two linear regulators within the HV9964 – a 10V linear regulator (PVDD), which is used for the two FET drivers, and a 5.0V linear regulator (AVDD) which supplies power to the rest of the control logic. The IC also has a built in under-voltage lockout which shuts off the IC if the voltage at either VDD pin falls below its UVLO threshold. Both VDD pins must by bypassed by a low ESR capacitor (≥0.1µF) for proper operation. The input current drawn from the external power supply (or VIN pin) is a sum of the 1.5mA (max) current drawn by the all the internal circuitry and the current drawn by the gate driver (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 1.5mA + Q_{G1} \bullet f_S + Q_{G2} \bullet f_{PWMD}$$

In the above equation, $f_S$ is the switching frequency of the converter, $f_{PWMD}$ is the frequency of the applied PWM dimming signal, $Q_{G1}$ is the gate charge of the external boost FET and $Q_{G2}$ is the gate charge of the load switch (both of which can be obtained from the FET datasheets). The AVDD pin can also be used as a reference voltage to set the LED current using a resistor divider to the IREF pin.

## Timing Resistor (RT)

The switching frequency of the converter is set by connecting a resistor between RT and GND. The resistor value can be determined as:

$$R_T \approx \frac{1}{f_S \bullet 52pF} + 880\Omega$$

The oscillator is also timed to the PWM dimming signal to improve the PWM dimming performance. The oscillator is turned off when PWMD is low and is enabled when PWMD goes high.

## PWM Dimming

PWM dimming in the HV9964 can be accomplished using a TTL compatible square wave source at the PWMD pin. The HV9964 has an enhanced PWM dimming capability, which allows PWM dimming to widths a few hundred nanoseconds with no drop in the LED current. The enhanced PWM dimming performance of the HV9964 can be best explained by considering typical boost converter circuits without this functionality. When the PWM dimming pulse becomes very short, the boost converter is turned off before the input current can reach its steady state value. This causes the input power to drop, which is manifested in the output as a drop in the LED current (Figure. 1b; for a CCM design).

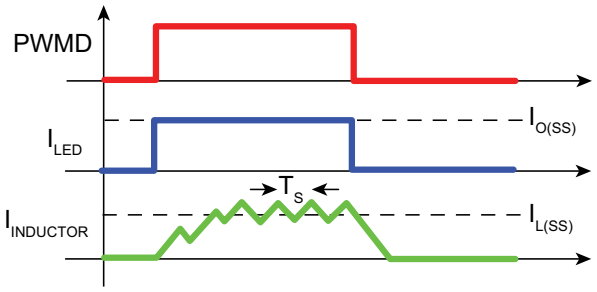



**Figure 1a: PWM dimming width much greater than switching period $T_S$**

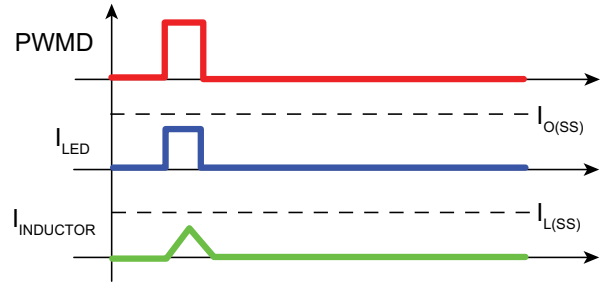



**Figure 1b: Sub-$T_S$ PWM dimming width**

In Figures 1a and 1b, $I_{O(SS)}$ and $I_{L(SS)}$ refer to the steady state values (PWMD = 100%) for the output current and inductor current respectively. As it can be seen, the inductor current does not rise high enough to trip the CS comparator. This causes the closed loop amplifier to lose control over the LED current, and the COMP output rails to VDD.

In the HV9964, however, this problem is overcome by keeping the boost converter running even though the PWMD pulse has ended. This is to ensure enough power delivered to the output. Thus, the amplifier still has control over the LED current, and the LED current is in regulation as shown in Figure 2.

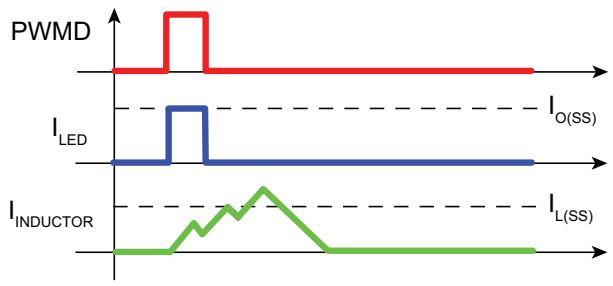



**Figure 2: Sub-$T_S$ PWM dimming width with the HV9964**

Note that the GT output is not limited by its maximum duty cycle $D_{MAX}$ past the PWMD signal trailing edge. The gate is kept active until the corresponding CS reference is met by $I_{INDUCTOR}$. When the PWMD signal is high, the GT and DIS pins are enabled, and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across itself. The DIS pin goes low, turning off the disconnect switch. However, the GT output is kept active.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The chosen filter capacitor should be large enough so that it can absorb the inductor energy without significant change of the voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD becomes high again.

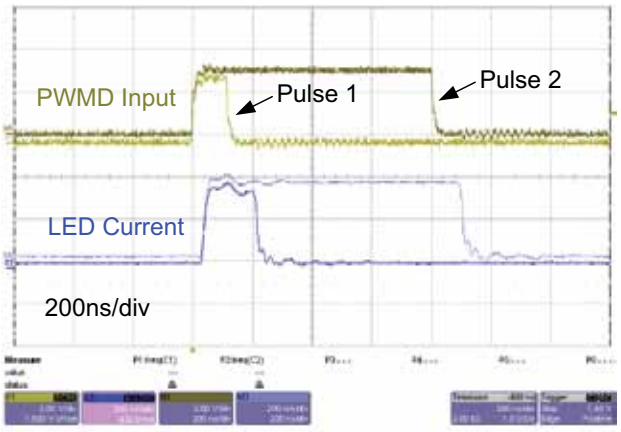



**Figure 3: Deep PWM dimming performance: LED current maintained in regulation**

## Current Sense (CS)

The current sense input is used to sense the source current of the switching FET. The CS input of the HV9964 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on. The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 12 (11R:1R). This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is AVDD - 0.7V, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current. The current sense resistor $R_{CS}$ should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For discontinuous conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is chosen as:

$$R_{CS} = \frac{AVDD - 0.7V}{12 \bullet I_{SAT}}$$

where $I_{SAT}$ is the maximum desired peak inductor current. For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. This factor must also be accounted for when determining $R_{CS}$ (see Slope Compensation section).

## Slope Compensation

Choosing a slope compensation that is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles. The HV9964 slope compensation circuit uses an external resistor $R_{SC}$ at CS pin to program the voltage slew rate. The current sourced out of the CS pin is proportional to the internal oscillator ramp. This current ramp has a peak value of 180µA. Therefore, the slope compensation ramp is programmed as:

$$DS = \frac{dV_{CS}}{dt} = R_{SC} \bullet 180\mu A \bullet f_S$$

where $f_S$ is switching frequency.

Assuming a down slope of DS (A/µs) for the inductor current, the current sense resistor can be computed as:

$$R_{CS} = \frac{AVDD - 0.7V}{12} \bullet \frac{1}{\frac{DS}{2f_S} + I_{SAT}}$$

The slope compensation resistor is chosen to provide the required amount of slope compensation required to maintain stability.

$$R_{SC} = \frac{DS}{f_S \bullet 180\mu A}$$

## Soft Start

Soft start of the LED current can be achieved by connecting a capacitor at the SS pin. The rate of voltage rise of SS pin limits the LED current's rate of rise. Upon start-up, the capacitance at the COMP network is being charged by the 200µA sourcing current of the transconductance amplifier. Without the soft-start function, this larger current would cause the COMP voltage to increase faster than the boost converter's response time, causing overshoots in the LED current during start-up. The SS pin is used to prevent these LED current overshoots by limiting the COMP voltage slew rate. A capacitor at the soft start pin programs this slew rate.

$$\frac{dV_{SS}}{dt} = \frac{2V}{C_{SS} \bullet R_T}$$

The HV9964 includes a latch which clamps the SS pin to ground, but releases it upon the first PWMD rising edge after power-on. This ensures soft start for the LED current independent of the power sequencing between VIN and PWMD.

## DIS Output

The DIS pin is used to control a load switch when driving boost and SEPIC converters. In the case of boost converters, when there is a short circuit fault at the output, there is a direct path from the input source to ground which can cause high currents to flow. The load switch is used to interrupt this path and prevent damage to the converter. The load switch also helps to disconnect the output filter capacitors for the boost and SEPIC converters from the LED load during PWM dimming and enables a fast dimming transitions.

## Fault Conditions and Hiccup Timer

The HV9964 is a robust controller which can protect the LEDs and the LED driver in case of fault conditions. The HV9964 includes both open LED protection and output short circuit protection. In both cases, the HV9964 shuts down and attempts a restart. The hiccup time is programmed by the capacitor at the HCP pin. When a fault condition is detected, both GT and DIS outputs are disabled. The COMP, SS and HCP pins are pulled to GND. Once the voltage at the HCP pin falls below 0.1V, and the fault condition(s) have disappeared, the capacitor at the HCP pin is released and is charged slowly by a current source proportional to the $R_T$ current. The HCP timing capacitor is programmed as:

$$C_{HCP} \approx \frac{t_{HICCUP}}{R_T}$$

Once the capacitor is charged to 1.8V, the COMP and SS pins are released and GT and DIS pins are allowed to turn on. The HV9964 resumes operation, beginning with the soft-start mode ensuring smooth recovery of the LED current.

## Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the gate and DIS outputs are pulled low. As soon as the load switch is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This behavior of the HV9964 allows the LED driver to recover from accidental shorts without having to power the IC down. Note that the power rating of the LED current sense resistor has to be chosen adequately to be able to survive a persistent fault condition.

The power rating of the resistor can be determined using:

$$P_{RS} \geq \frac{I_{SAT}^2 R_S (T_{BLANK,CS} + T_{OFF})}{R_T} = \frac{I_{SAT}^2 R_S \bullet 0.95\mu s}{R_T}$$

where $I_{SAT}$ is the saturation current of the disconnect FET.

## Open Loop Detection

The HV9964 includes protection circuitry disabling the boost converter when there is a short circuit between the anode and cathode of the LED string. However, if the string is shorted to ground, the sense resistor $R_S$ is bypassed, causing the IC to lose the feedback signal. The voltage at FB becomes 0V, and COMP rails to the AVDD potential. Nevertheless, the boost converter keeps on running, producing a potentially damaging LED current.

To detect and to prevent this type of a fault, an open loop detection circuit is added. If COMP > AVDD - 0.3V, and FB < 0.1V simultaneously, then a discharge current of 15µA is activated at

the HCP pin. With a 10µA sourcing current and a 15µA sinking current, the total current discharging the HCP capacitor is 5µA. This current will discharge the HCP capacitor from AVDD to 2.0V. When the voltage at HCP drops below 2.0V, the IC interprets it as an open loop condition, issues a logic low state at the $\overline{FLT}$ output, and shuts GT and DIS down. The discharge time provides a programmable delay to the detection event. This delay time is needed because the open loop condition may happen during startup when the SS capacitance is insufficient. To prevent misinterpretation of this condition as the current loop open, the delay is introduced.

It is recommended, that the input supply voltage is shut off by the host upon issuing $\overline{FLT}$ low, as shutting the HV9964 off may not necessarily interrupt the current in the LED string in the case of a partial short circuit to chassis.

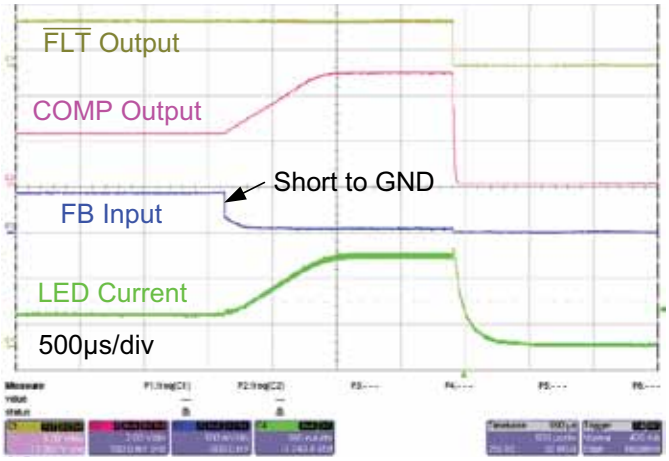


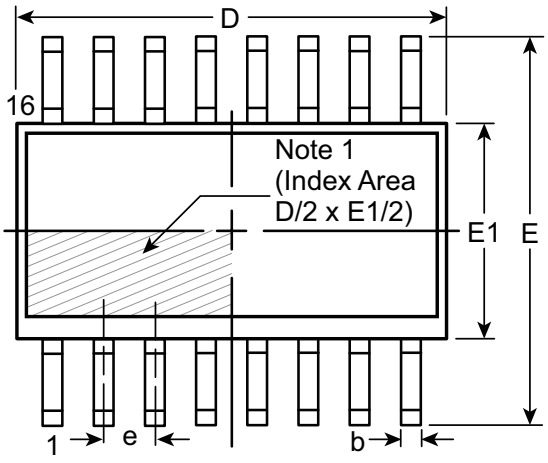

**Figure 8: Wiring short circuit to GND: detection and shutdown.**

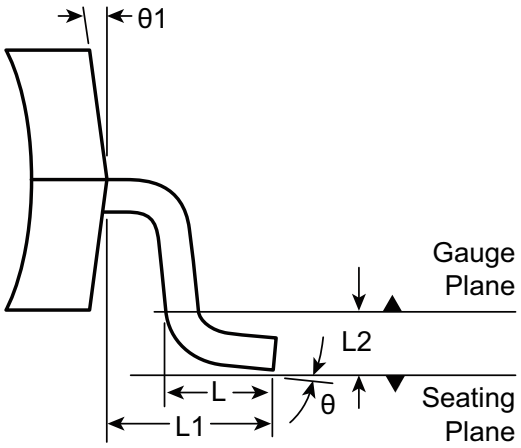
## Pin Description (16-Lead SOIC)

| Pin # | Name | Description |
|---|---|---|
| 1 | AVDD | This is a power supply pin for all internal control circuits. This voltage is also used as the reference voltage both internally and externally. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF). |
| 2 | VIN | This pin is the input of a 40V high voltage regulator. |
| 3 | DIS | This pin is used to drive an external load switch which disconnects the load from the circuit during a fault condition or during PWM dimming to achieve a very high dimming ratio. |
| 4 | PVDD | This pin is a regulated 10V supply for the two gate drivers (DIS and GT). It must be bypassed with a low ESR capacitor to GND (at least 1.0µF). |
| 5 | GT | This is the gate driver output for the switching FET. |
| 6 | GND | Ground return for all the low power analog internal circuitry as well as the gate drivers. This pin must be connected to the return path from the input. |
| 7 | CS | This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time. |
| 8 | RT | This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode. The switching frequency is synchronized to the PWMD input and oscillator will turn on once PWMD goes high. This pin must be bypassed to AVDD using a 1.0nF capacitor. |
| 9 | SS | This pin is used to provide soft start upon turn-on of the IC. A capacitor at this pin programs the soft start time. |
| 10 | COMP | Stable Closed loop control can be accomplished by connecting a compensation network between COMP and GND. |
| 11 | IREF | The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the AVDD pin. Connecting a voltage greater than 1.25V at this pin will disable the short circuit comparator. |
| 12 | FB | This pin provides output current feedback to the HV9964 by using a current sense resistor. |
| 13 | PWMD | When this pin is pulled to GND (or left open), switching of the HV9964 is disabled. When an external TTL high level is applied to it, switching will resume. |
| 14 | OVP | This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 1.25V, the gate output of the HV9964 is turned off and DIS goes low. The IC will turn on when the voltage at the pin goes below 1.125V. |
| 15 | HCP | This pin provides the hiccup timer in case of a fault. A capacitor at this pin programs the hiccup time. |
| 16 | $\overline{\text{FLT}}$ | This open-drain, active-low output indicates the presence of a fault condition. |

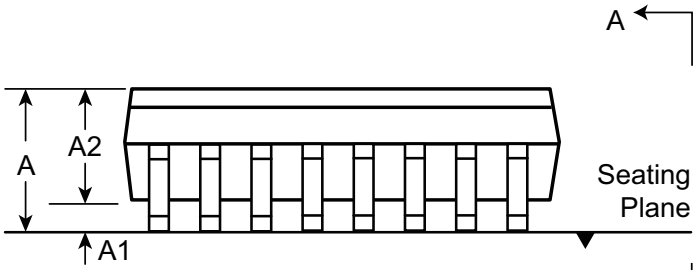
# 16-Lead SOIC (Narrow Body) Package Outline (NG)

***9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch***

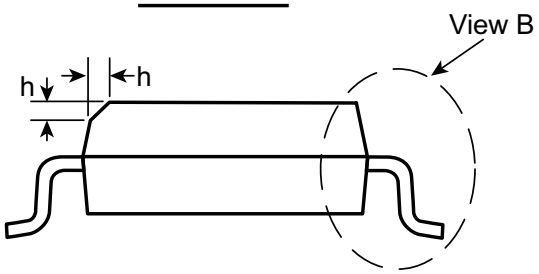



## Top View




## View B




***Note:***

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 9.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | $0^O$ | $5^O$ |
| | NOM | - | - | - | - | 9.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 10.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | $8^O$ | $15^O$ |

*JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.*
** This dimension is not specified in the JEDEC drawing.*
***Drawings are not to scale.***
***Supertex Doc. #:*** *DSPD-16SONG, Version G041309.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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