TLE4961-3L

High Precision Automotive Hall Effect Latch

Data Sheet

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2012-07-18	

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Table of Contents

List of Figures

List of Tables

1 Product Description

1.1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Bipolar Hall Effect Latch	3.0~32 V	1.6 mA	High B_{OP}:7.5 mT B_{RP}:-7.5 mT	Open Drain Output	-40°C to 170°C

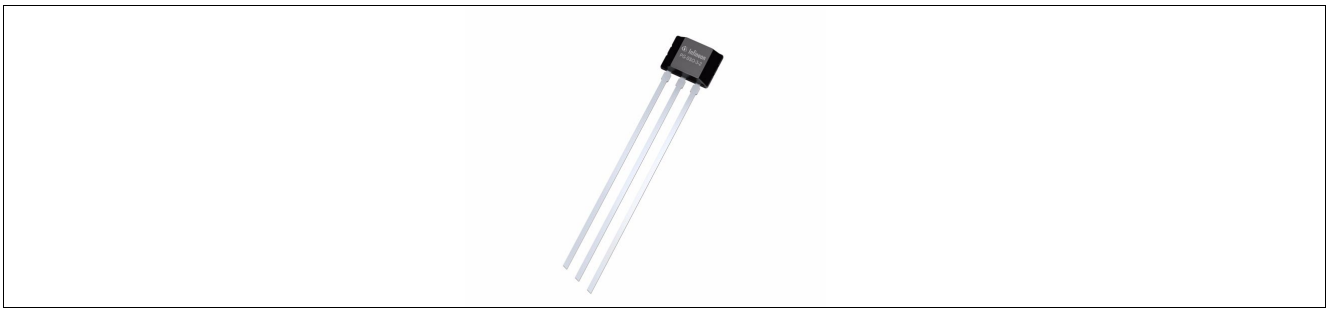

Figure 1-1 Image of TLE4961-3L in the PG-SSO-3-2 Package

1.2 Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent & overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35 µs)
- High ESD performance
- Leaded package PG-SSO-3-2 (TLE4961-3L)

1.3 Target Applications

Target applications for the TLE496x Hall switch family are all applications which require a high precision Hall switch with an operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

The magnetic behavior as a latch and switching thresholds of typical ±7.5 mT make the device especially suited for the use with a pole wheel for index counting applications as e.g. power closing and window lifter.

Table 1-1 Ordering Information

Product Name	Product Type	Ordering Code	Package
TLE4961-3L	Hall Latch	SP000848034	PG-SSO-3-2

2 Functional Description

2.1 General

The TLE4961-3L is an integrated Hall effect latch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

2.2 Pin Configuration (top view)

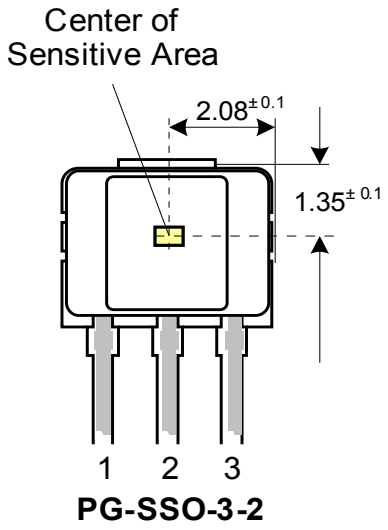

Figure 2-1 Pin Configuration and Center of Sensitive Area

2.3 Pin Description

Table 2-1 Pin Description PG-SSO-3-2

Pin No.	Symbol	Function
1	VDD	Supply voltage
2	GND	Ground
3	Q	Output

2.4 Block Diagram

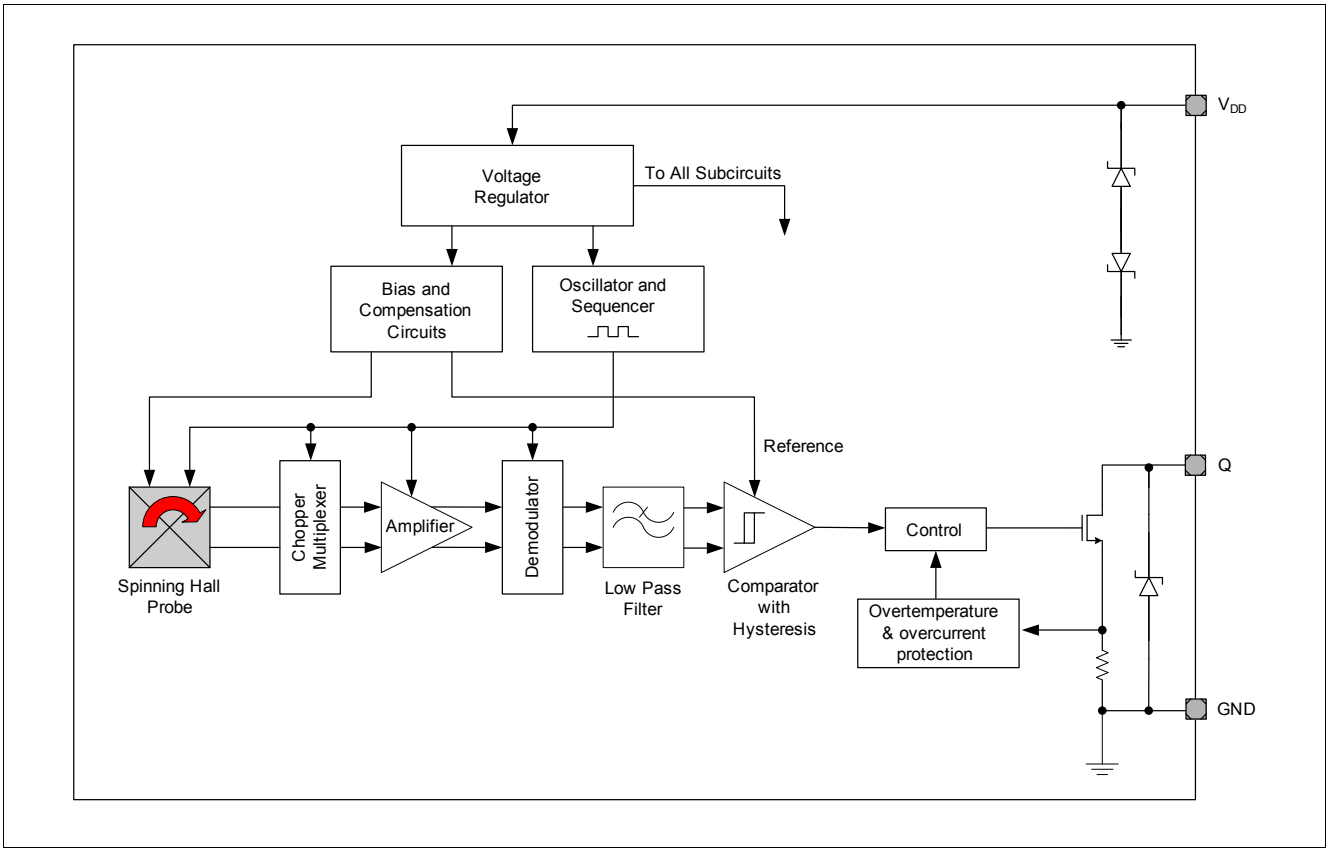

Figure 2-2 Functional Block Diagram TLE4961-3L

2.5 Functional Block Description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

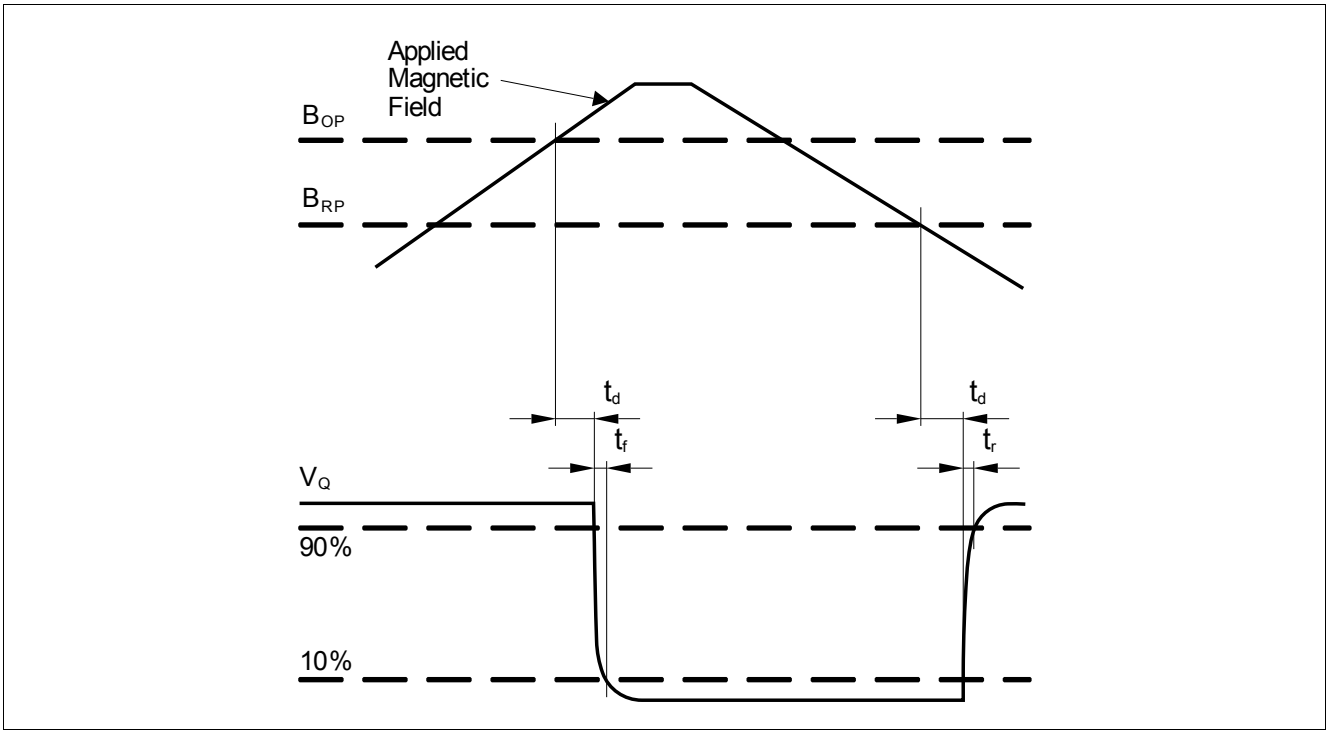

Figure 2-3 Timing Diagram TLE4961-3L

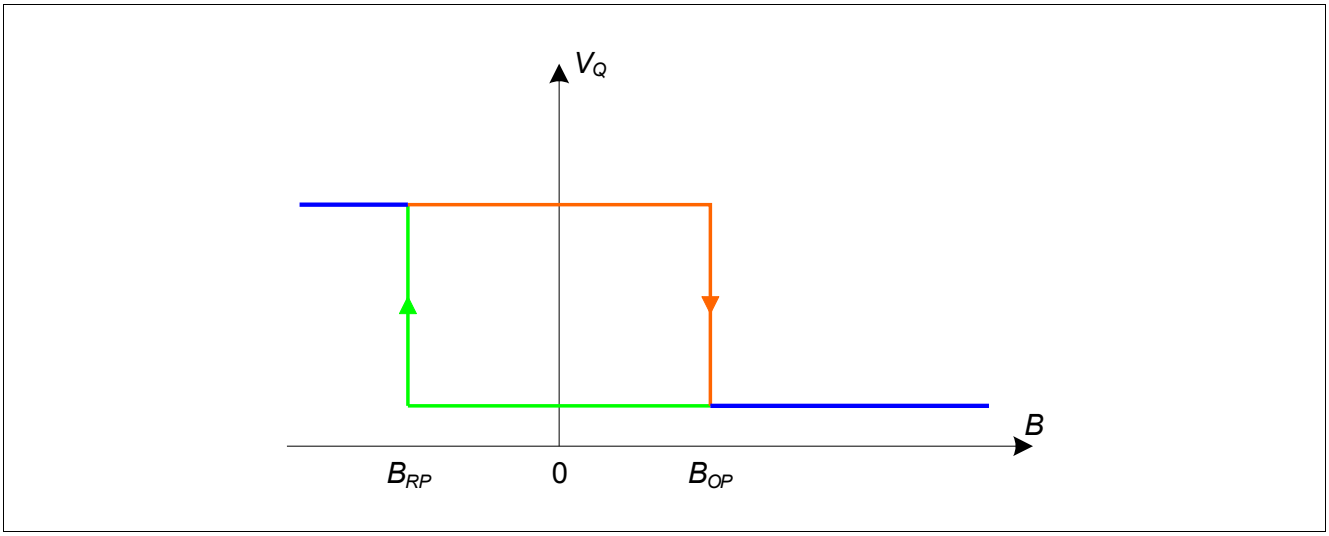

Figure 2-4 Output Signal TLE4961-3L

2.6 Default Start-up Behavior

The magnetic thresholds exhibit a hysteresis $B_{HYS} = B_{OP} - B_{RP}$. In case of a power-on with a magnetic field B within hysteresis ($B_{OP} > B > B_{RP}$) the output of the sensor is set to the pull up voltage level (V_Q) per default. After the first crossing of B_{OP} or B_{RP} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD}.

This means for $B > B_{OP}$ the output is switching, for $B < B_{RP}$ and $B_{OP} > B > B_{RP}$ the output stays at V_Q.

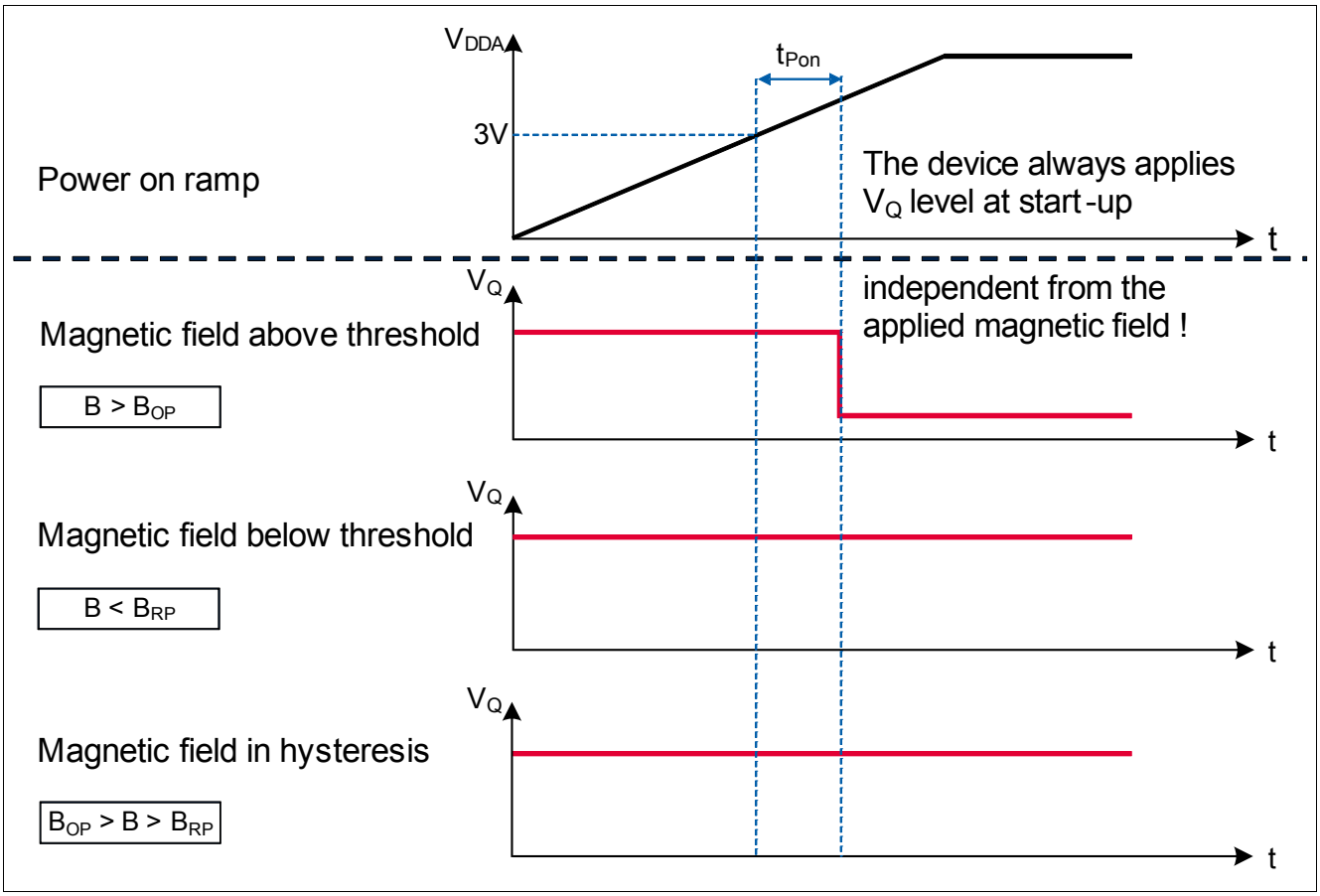

Figure 2-5 Illustration of the Start-up Behavior of the TLE4961-3L

3 Specification

3.1 Application Circuit

The following **Figure 3-1** shows one option of an application circuit. As explained above the resistor R_S can be left out (see **Figure 3-2**). The resistor R_Q has to be in a dimension to match the applied V_S to keep I_Q limited to the operating rage of maximum 25 mA.

e.g.:

V_S = 12 V

I_Q = 12 V/1200 Ω = 10 mA

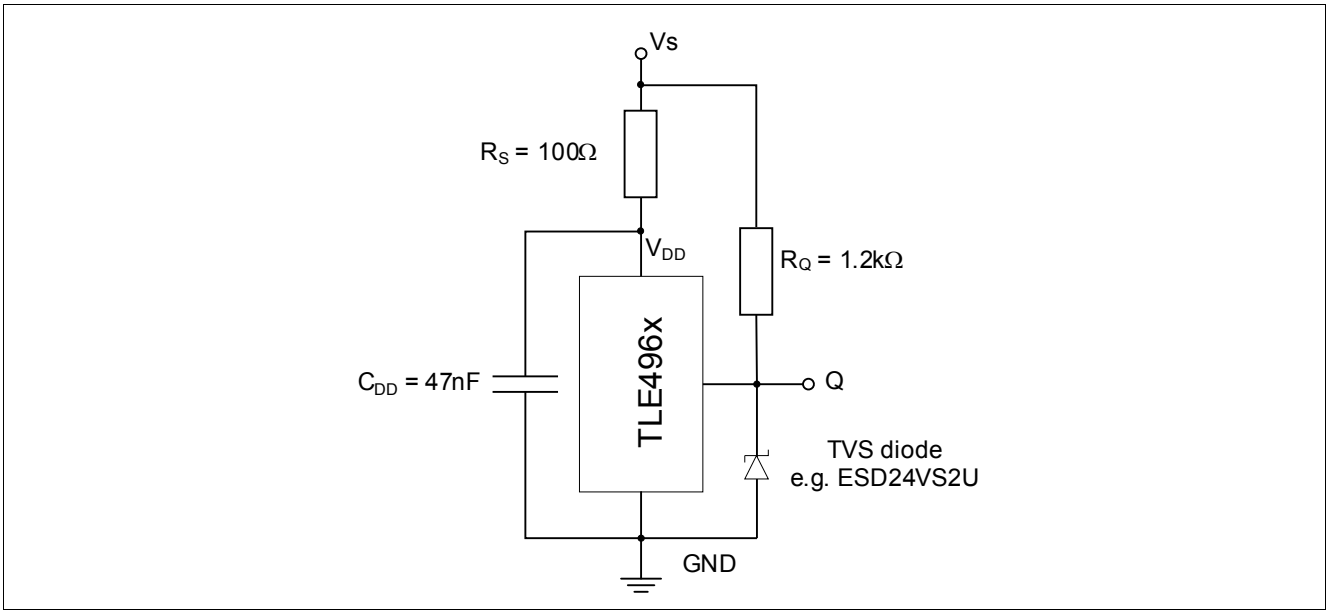

Figure 3-1 Application Circuit 1: With External Resistor

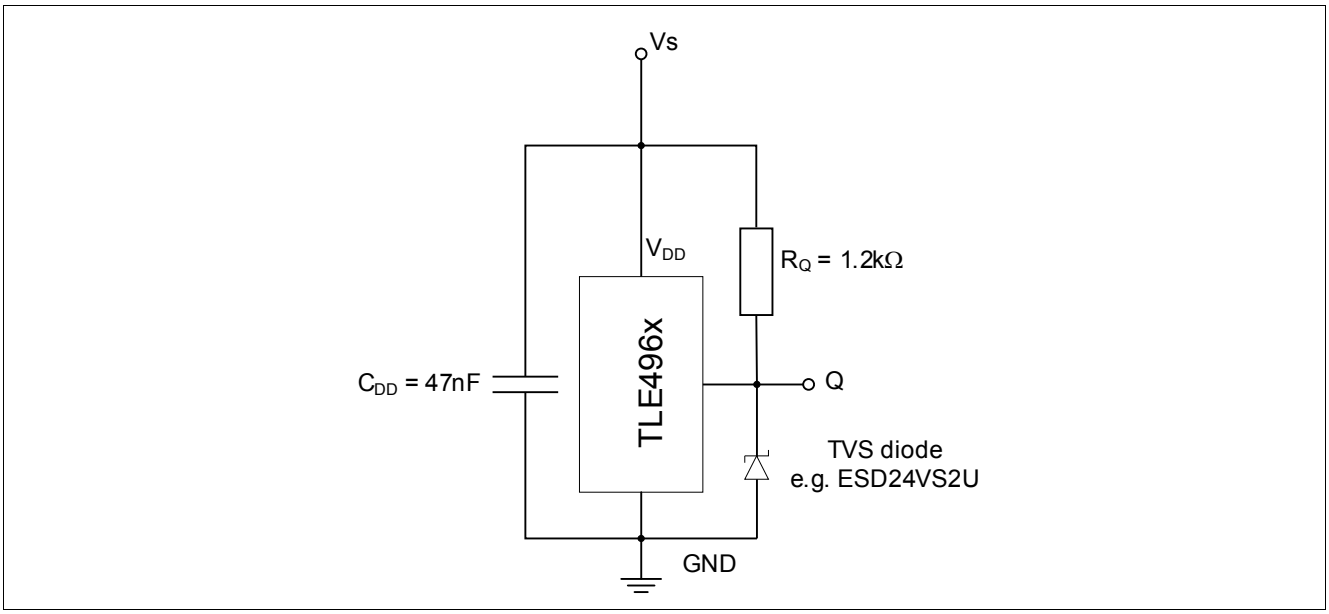

Figure 3-2 Application Circuit 2: Without External Resistor

3.2 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage[1)]	V_{DD}	-18		32 42	V	 10h, no external resistor required
Output voltage	V_Q	-0.5		32	V	
Reverse output current	I_Q	-70			mA	
Junction temperature[1)]	T_J	-40		155 165 175 195	°C	for 2000h (not additive) for 1000h (not additive) for 168h (not additive) for 3 x 1h (additive)
Storage temperature	T_S	-40		150	°C	
Thermal resistance Junction ambient	R_{thJA}			200	K/W	for PG-SSO-3-2 (2s2p)
Thermal resistance Junction lead	R_{thJL}			150	K/W	for PG-SSO-3-2

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (SSO3 example):
e.g for: V_{DD} = 12 V, I_S = 2.5 mA, V_{QSAT} = 0.5 V, I_Q = 20 mA
Power dissipation: P_{DIS} = 12 V x 2.5 mA + 0.5 V x 20 mA = 30 mW + 10 mW = 40 mW
Temperature $\Delta T = R_{thJA} \times P_{DIS}$ = 200 K/W x 40 mW = 8 K
For T_A = 150 °C: $T_J = T_A + \Delta T$ = 150 °C + 8 K = 158 °C

Table 3-2 ESD Protection[1)] (TA = 25°C)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM)[2)]	V_{ESD}	-7		7	kV	R = 1.5 kΩ, C = 100 pF
ESD voltage (SDM)[3)]		-1		1		
ESD voltage (system level)[4)]		-15		15		with circuit shown in Figure 3-1 & Figure 3-2

1) Characterization of ESD is carried out on a sample basis, not subject to production test.
2) Human Body Model (HBM) tests according to EIA/JESD22-A114.
3) Socket device model (SDM) tests according to EOS/ESD-DS5.3-1993.
4) Gun test (2kΩ / 330pF or 330Ω / 150pF) according to ISO 10605-2008.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4961-3L.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 3-3 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0		32[1)]	V	
Output voltage	V_Q	-0.3		32	V	
Junction temperature	T_j	-40		170	°C	
Output current	I_Q	0		25	mA	
Magnetic signal input frequency[2)]	f_{SW}	0		10	kHz	

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to V_{DD} = 12 V and TA = 25°C. The below listed specification is valid in combination with the application circuit shown in **Figure 3-1** and **Figure 3-2**

Table 3-4 General Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	
Reverse current	I_{SR}		0.05	1	mA	for V_{DD} = -18 V
Output saturation voltage	V_{QSAT}		0.2	0.5	V	I_Q = 20 mA
			0.24	0.6	V	I_Q = 25 mA
Output leakage current	I_{QLEAK}			10	µA	
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited & thermal shutdown
Output fall time[1)]	t_f	0.17	0.4	1	µs	1.2 kΩ / 50 pF, see **Figure 2-3**
Output rise time[1)]	t_r	0.4	0.5	1	µs	1.2 kΩ / 50 pF, see **Figure 2-3**
Output jitter[1)2)]	t_{QJ}		0.35	1	µs	For square wave signal with 1 kHz
Delay time[1)3)]	t_d	12	15	30	µs	see **Figure 2-3**
Power-on time[1)4)]	t_{PON}		80	150	µs	V_{DD} = 3 V, B ≤ B_{RP} - 0.5 mT or B ≥ B_{OP} + 0.5 mT
Chopper frequency[1)]	f_{OSC}		350		kHz	

1) Not subject to production test, verified by design/characterization.

2) Output jitter is the 1σ value of the output switching distribution.

3) Systematic delay between magnetic threshold reached and output switching.

4) Time from applying V_{DD} = 3.0 V to the sensor until the output is valid.

Table 3-5 Magnetic Characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	5.0	8.1	11.1	mT	
		25	4.6	7.5	10.4		
		170	3.6	6.2	8.8		
Release point	B_{RP}	-40	-11.1	-8.1	-5.0	mT	
		25	-10.4	-7.5	-4.6		
		170	-8.8	-6.2	-3.6		
Hysteresis	B_{HYS}	-40	12.0	16.2	22.2	mT	
		25	11.2	15.0	20.8		
		170	9.3	12.4	17.6		
Effective noise value of the magnetic switching points[1)]	B_{Neff}	25		62		µT	
Temperature compensation of magnetic thresholds[2)]	T_C			-1200		ppm/K	

1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents a the rms-value and corresponds therefore to a 1 σ probability of normal distribution. Consequently a 3 σ value corresponds to 99.7% probability of appearance.

2) Not subject to production test, verified by design/characterization.

Field Direction Definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

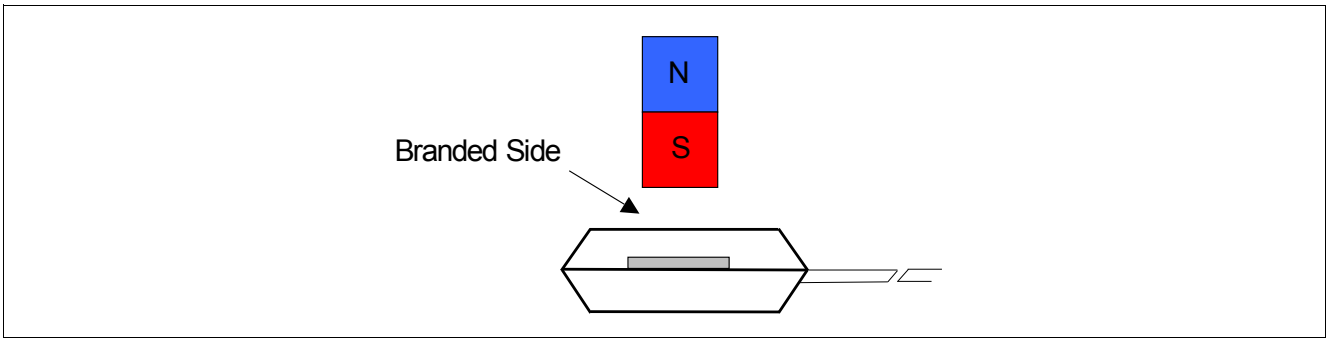

Figure 3-3 Definition of Magnetic Field Direction PG-SSO-3-2

3.5 Electro Magnetic Compatibility

Characterization of Electro Magnetic Compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.

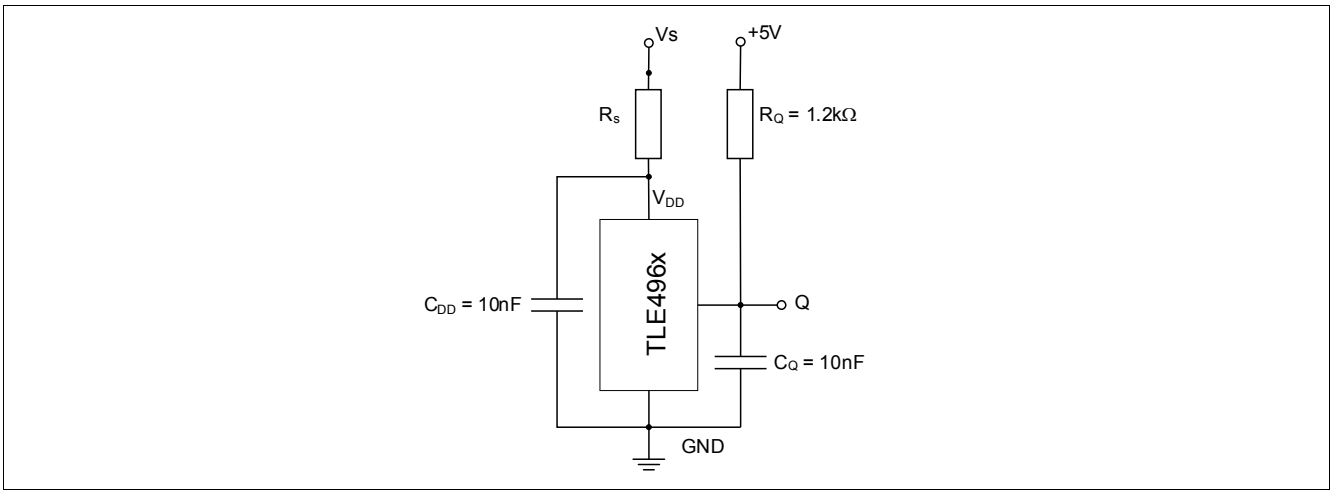

Figure 3-4 EMC Test Circuit

Ref: ISO 7637-2 (Version 2004), test circuit **Figure 3.4** (with external resistor, R_S = 100 Ω)

Table 3-6 Magnetic Compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-100 V	C
Testpulse 2a[1)]		60 V/110 V	A/C
Testpulse 2b		10 V	C
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4[2)]		-7 V / -5.5 V	A
Testpulse 5b[3)]		U_S = 86.5 V / U_S* = 28.5 V	A

1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.
3) A central load dump protection of 42 V is used. Us* = 42 V-13.5 V.

Ref: ISO 7637-2 (Version 2004), test circuit **Figure 3.4** (without external resistor, R_S = 0Ω)

Table 3-7 Electro Magnetic Compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-50 V	C
Testpulse 2a[1)]		50 V	A
Testpulse 2b		10 V	C
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4[2)]		-7 V / 5.5 V	A
Testpulse 5b[3)]		U_S = 86.5 V / U_S* = 28.5 V	A

1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.
3) A central load dump protection of 42 V is used. Us* = 42 V-13.5 V.

4 Package Information

The TLE4961-3L is available in the through-hole leaded package PG-SSO-3-2.

4.1 Package Outline PG-SSO-3-2

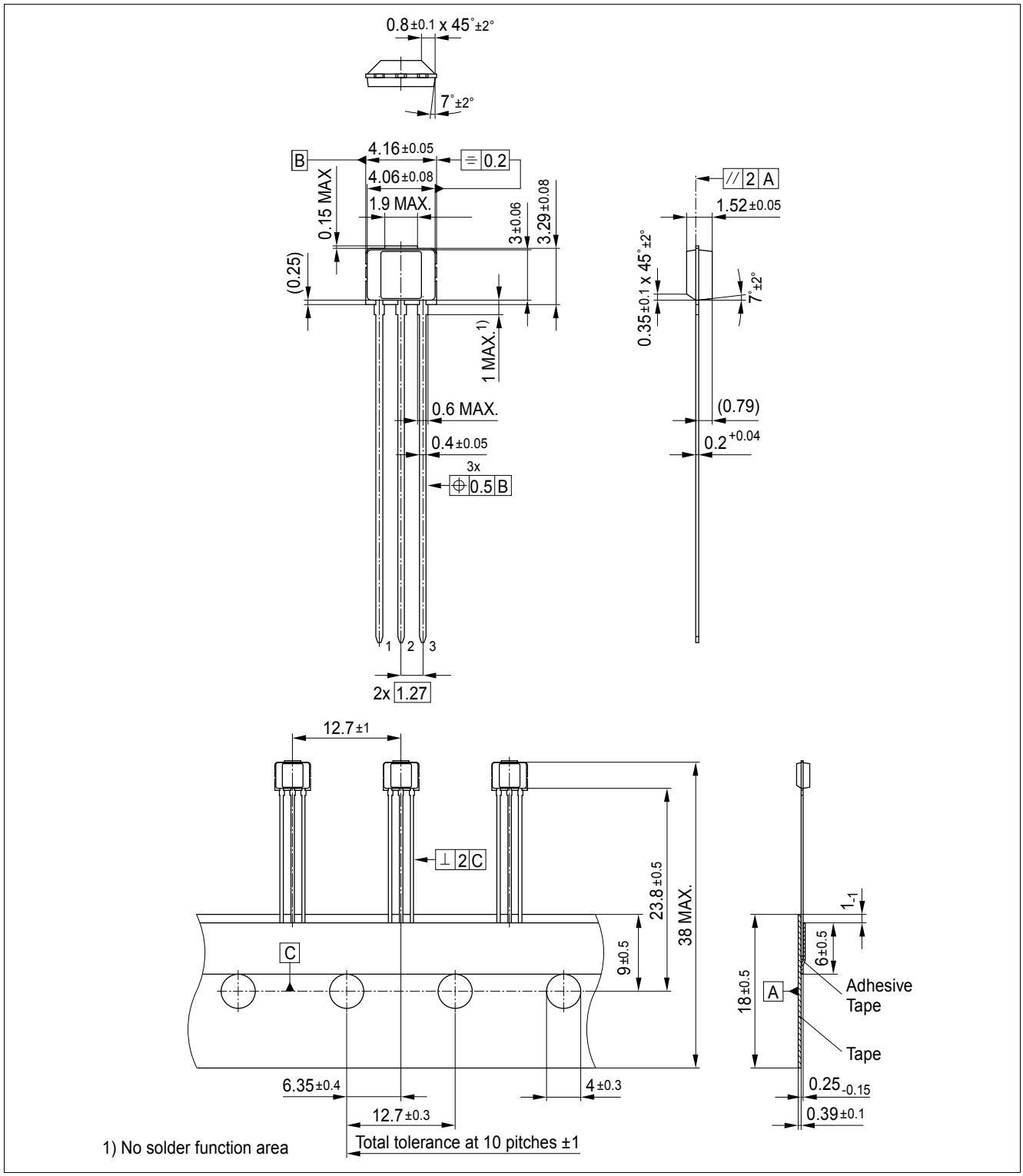

Figure 4-1 PG-SSO-3-2 Package Outline (All Dimensions in mm)

4.2 PG-SSO-3-2 Distance between Chip and Package

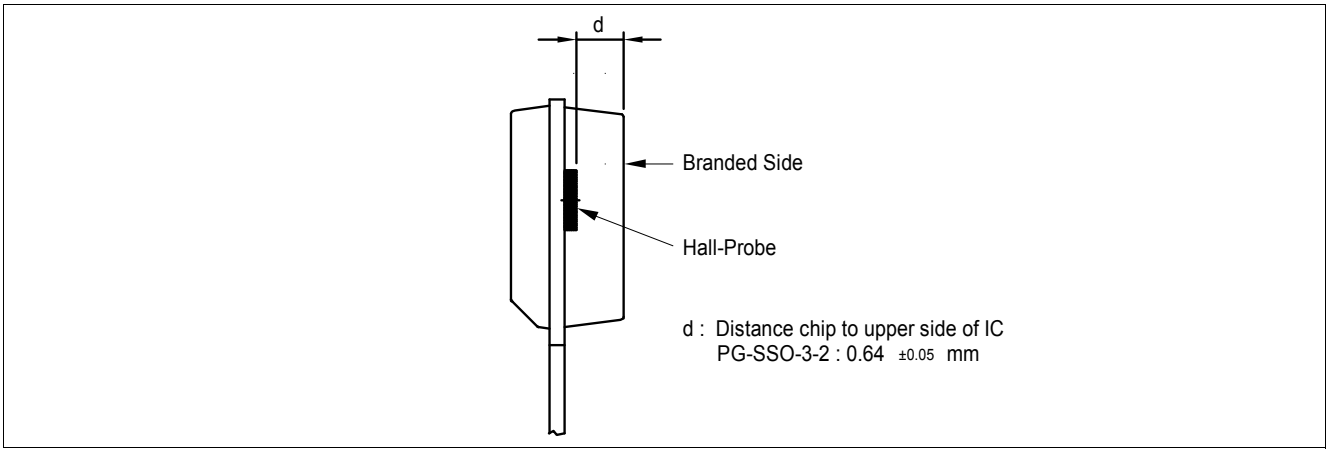

Figure 4-2 Distance between Chip and Package

4.3 Package Marking

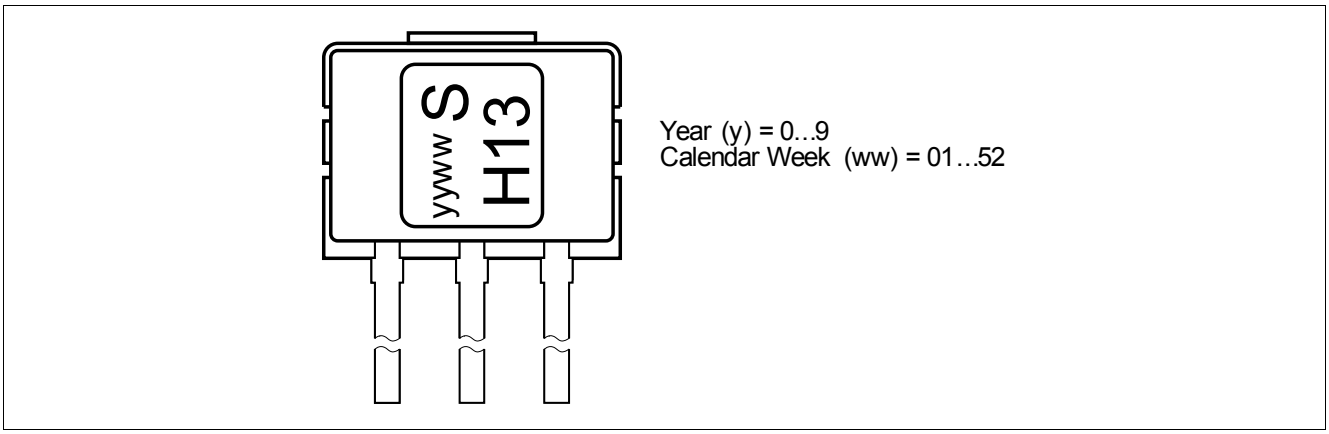

Figure 4-3 Marking of TLE4961-3L

5 Graphs of the Magnetic Parameters

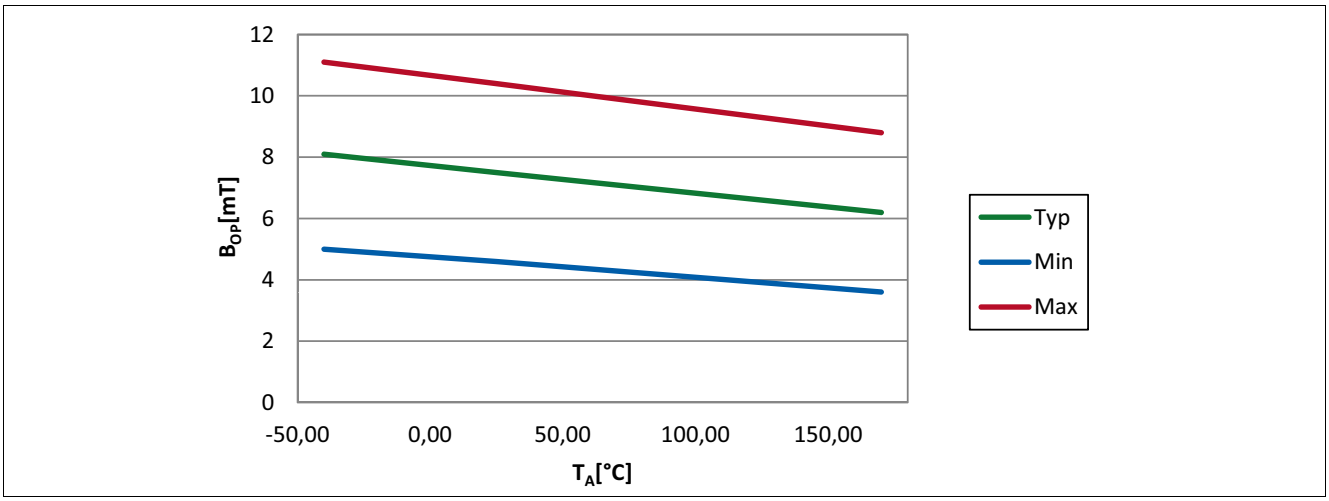

Figure 5-1 Operating Point (B_{OP}) of the TLE4961-3L over Temperature

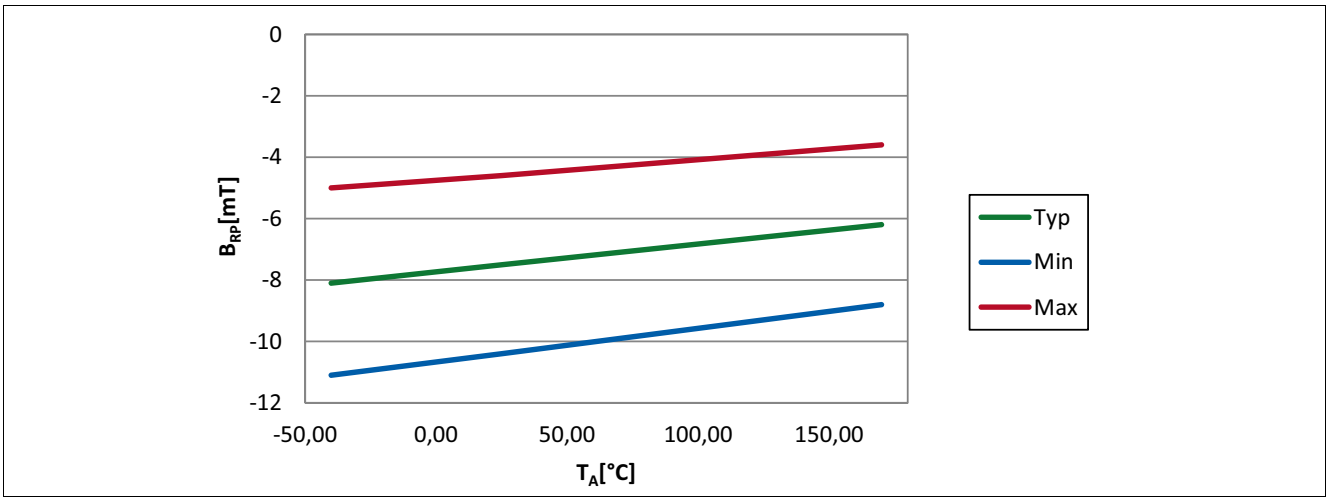

Figure 5-2 Release Point (B_{RP}) of the TLE4961-3L over Temperature

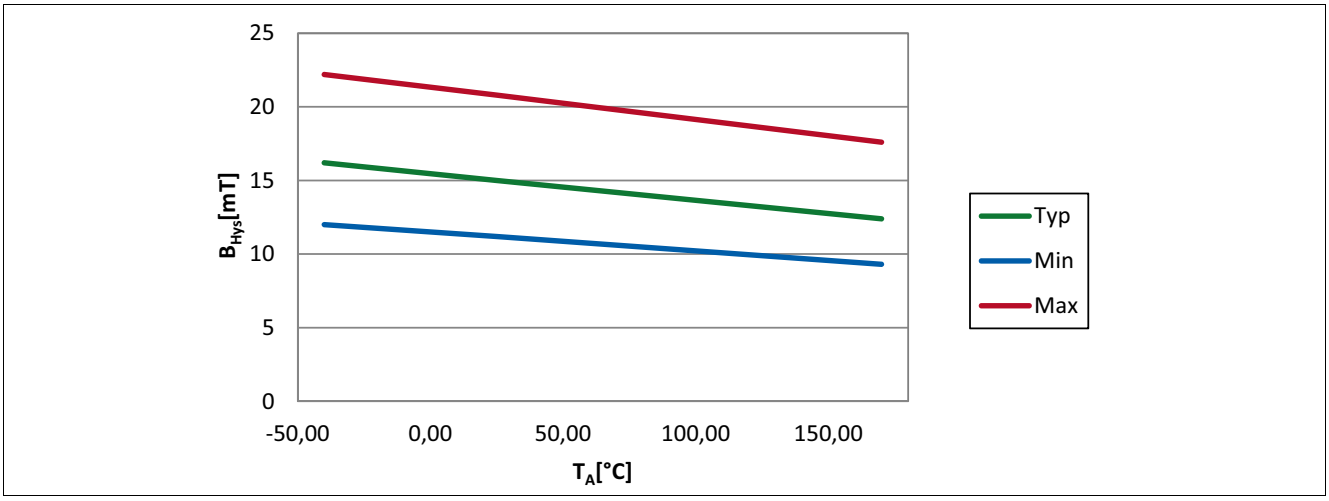

Figure 5-3 Hysteresis (B_{Hys}) of the TLE4961-3L over Temperature

6 Graphs of the Electrical Parameters

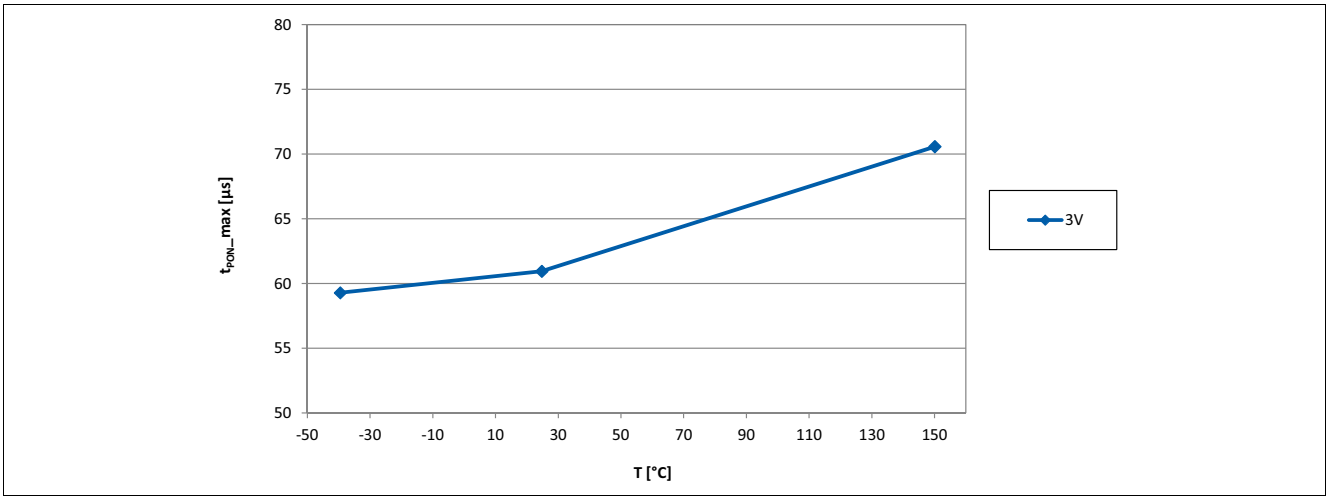

Figure 6-1 Power On Time t_{PON} of the TLE4961-3L over Temperature

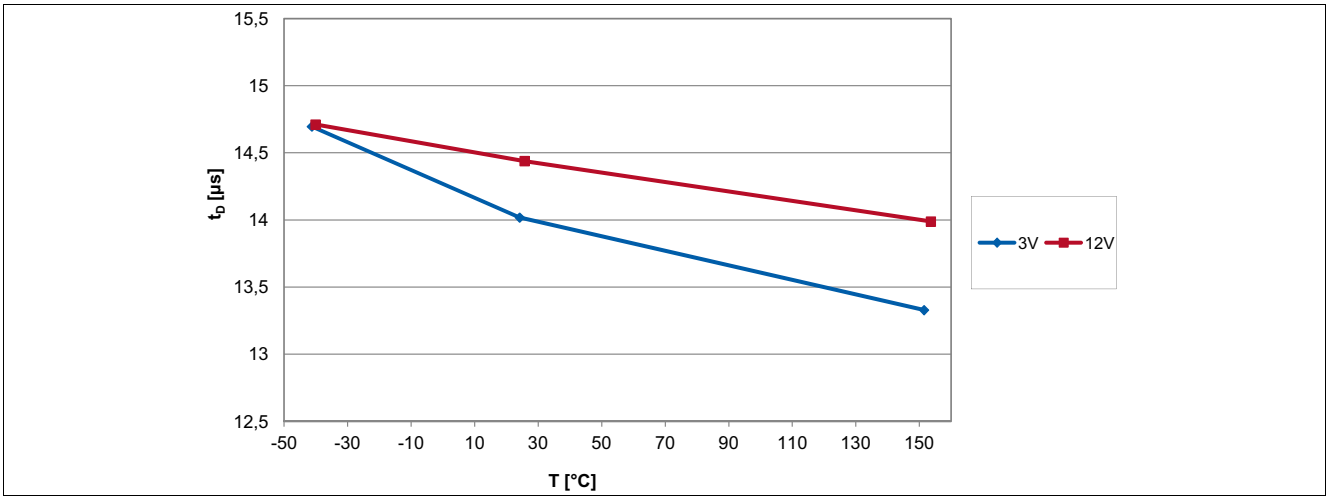

Figure 6-2 Signal Delay Time of the TLE4961-3L over Temperature

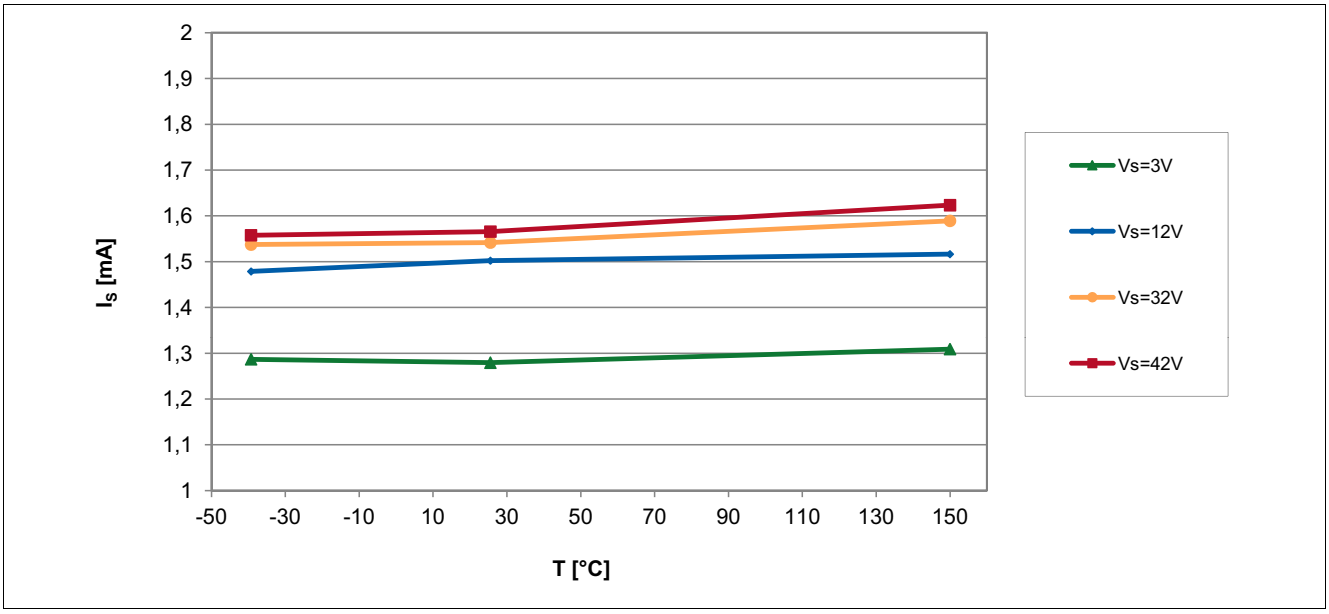

Figure 6-3 Supply Current of the TLE4961-3L over Temperature

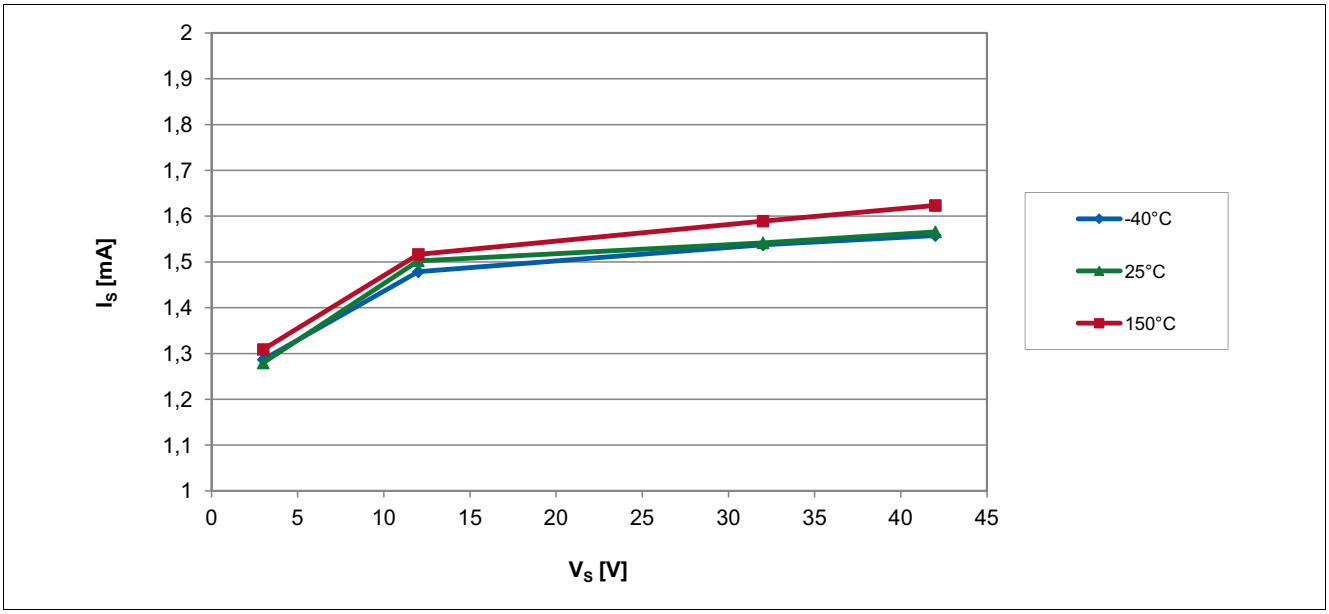

Figure 6-4 Supply Current of the TLE4961-3L over Supply Voltage

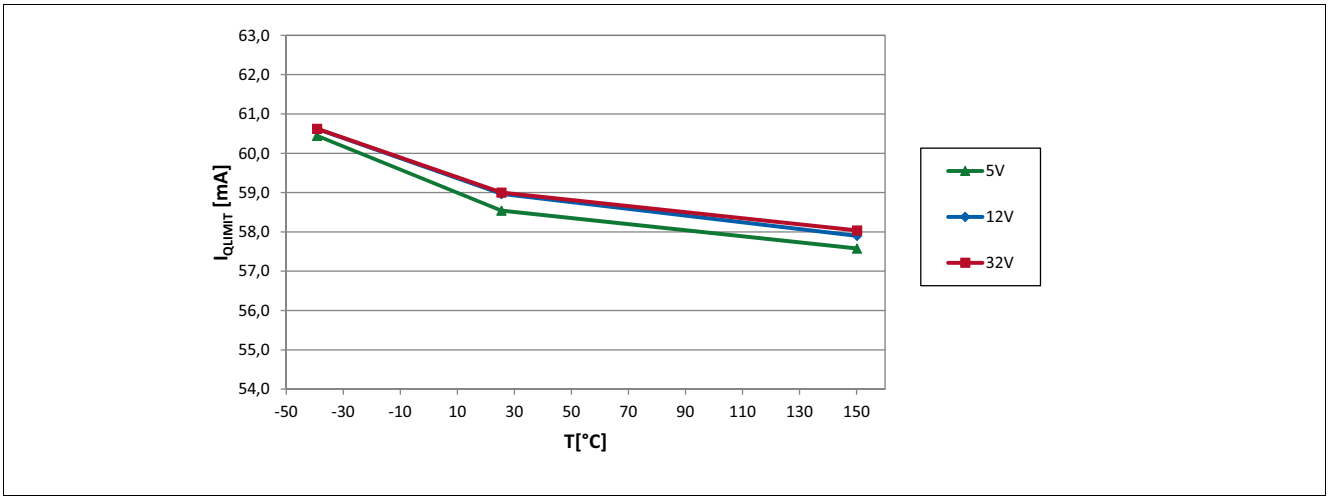

Figure 6-5 Output Current Limit of the TLE4961-3L over Temperature

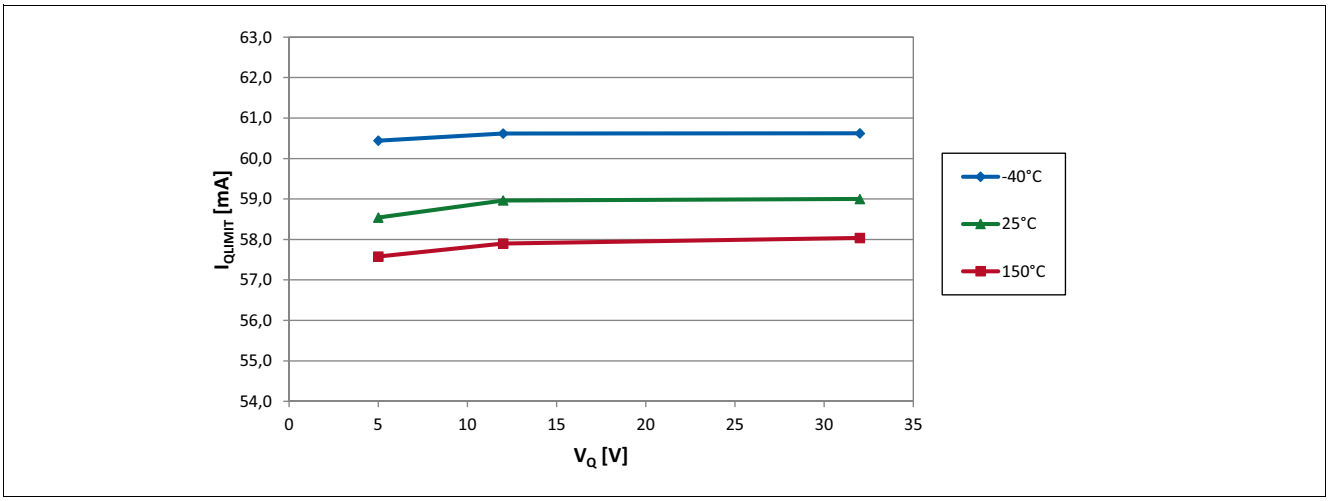

Figure 6-6 Output Current Limit of the TLE4961-3L over applied Pull-up Voltage

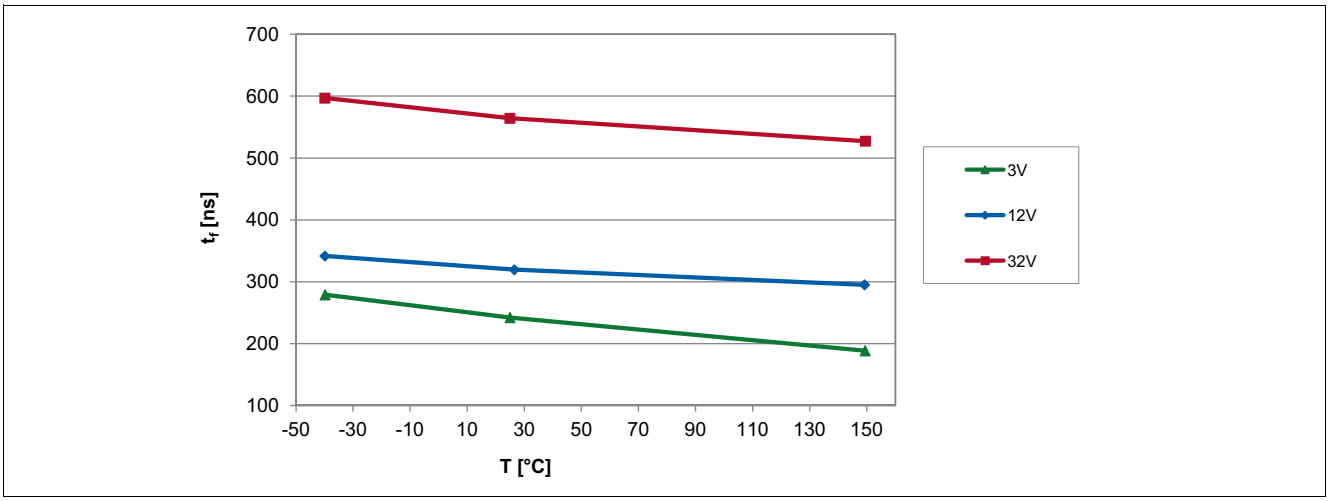

Figure 6-7 Output Fall Time of the TLE4961-3L over Temperature

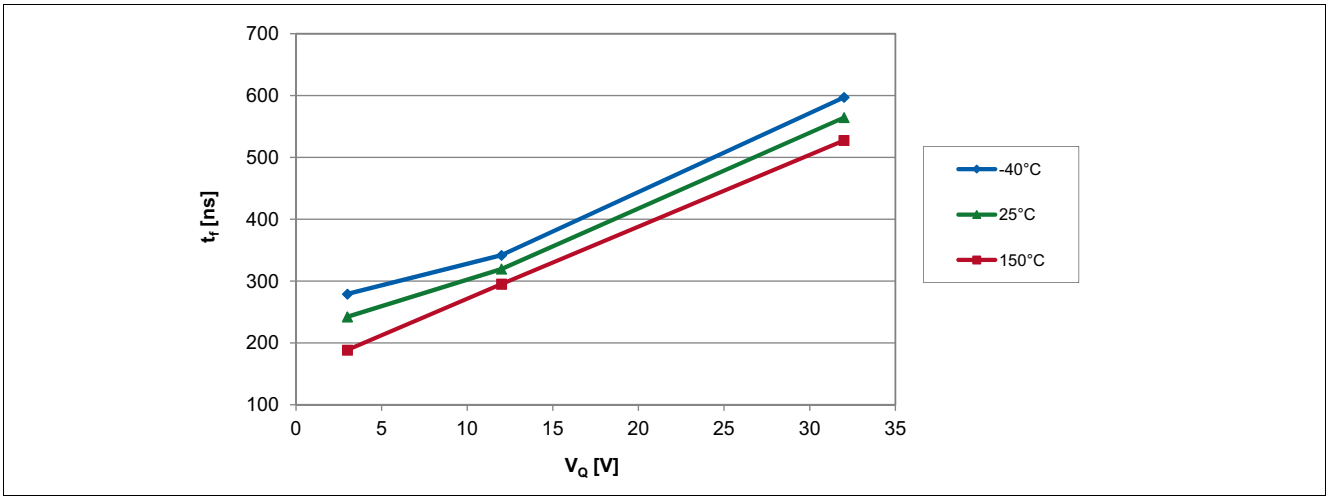

Figure 6-8 Output Fall Time of the TLE4961-3L over applied Pull-up Voltage

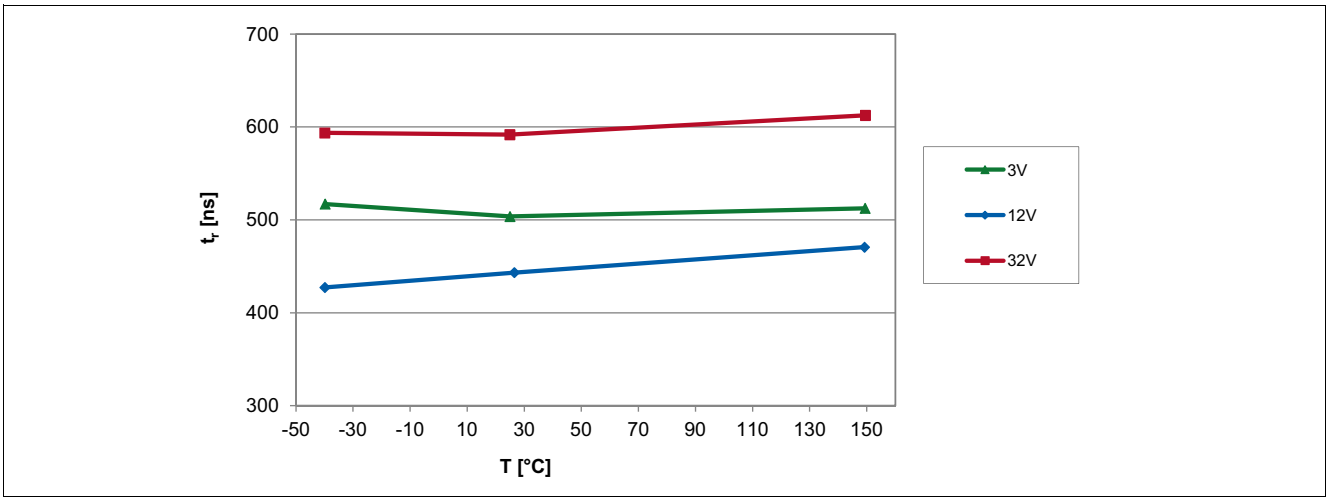

Figure 6-9 Output Rise Time of the TLE4961-3L over Temperature

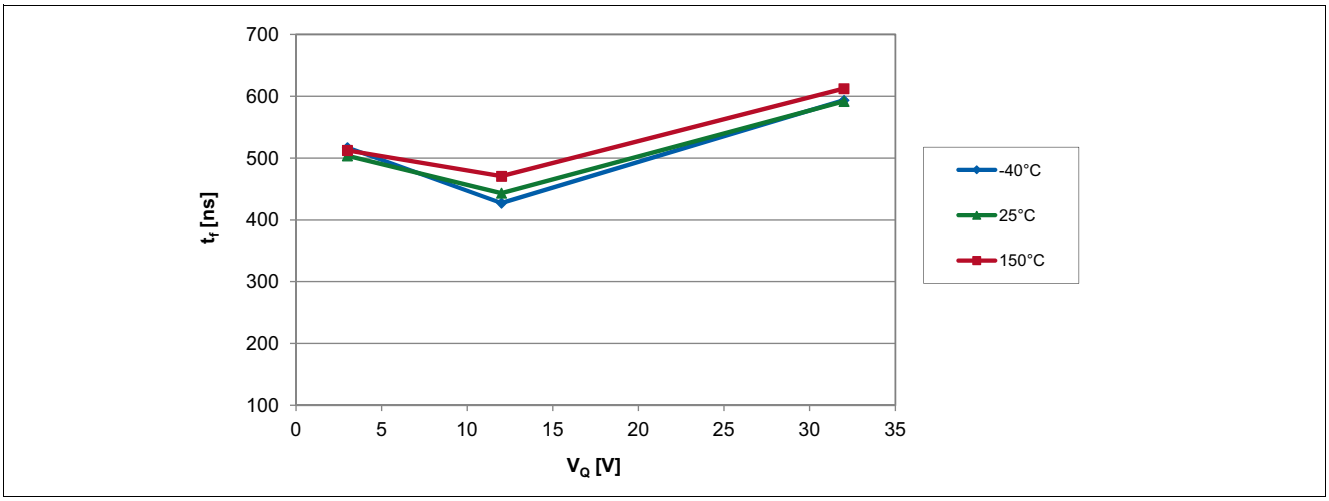

Figure 6-10 Output Rise Time of the TLE4961-3L over applied Pull-up Voltage

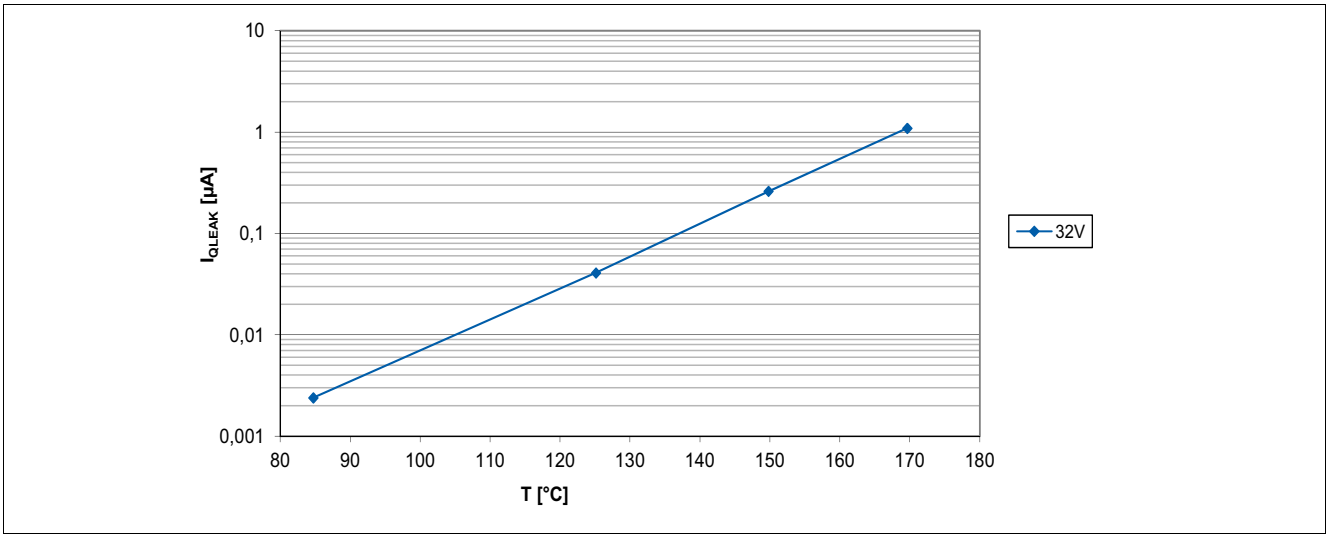

Figure 6-11 Output Leakage Current of the TLE4961-3L over Temperature

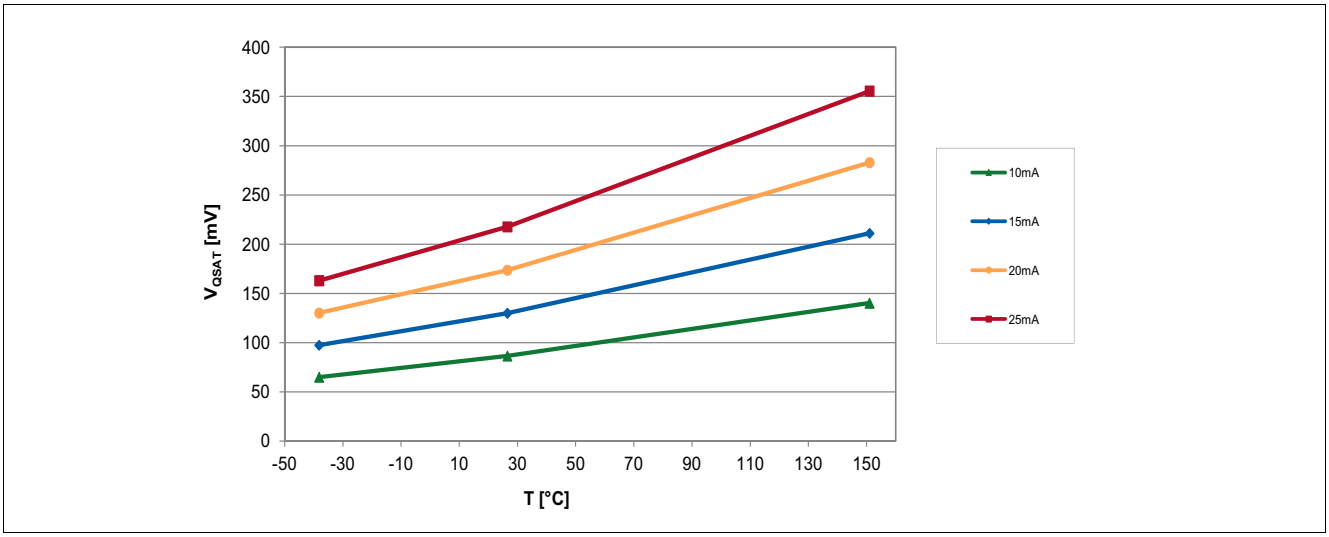

Figure 6-12 Saturation Voltage of the TLE4961-3L over Temperature

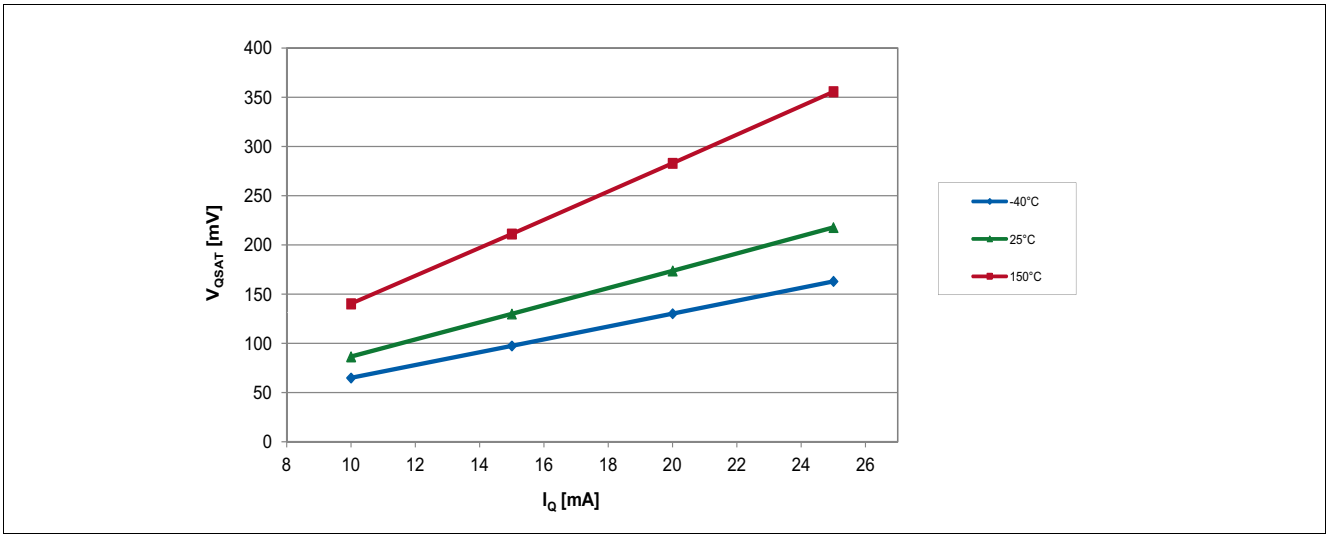

Figure 6-13 Saturation Voltage of the TLE4961-3L over Output Current

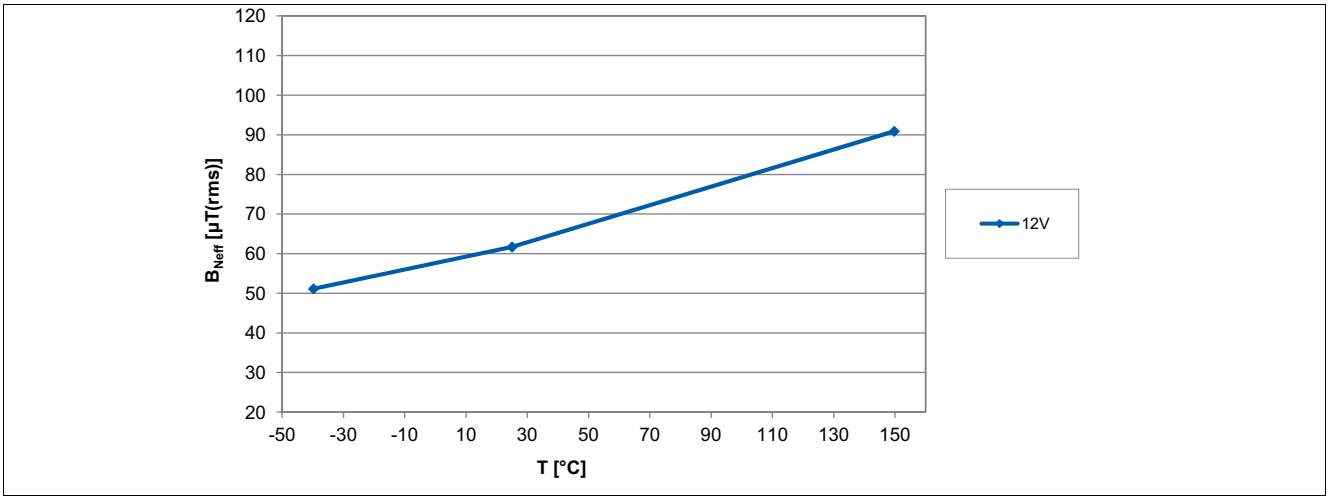

Figure 6-14 Effective Noise of the TLE4961-3L Thresholds over Temperature

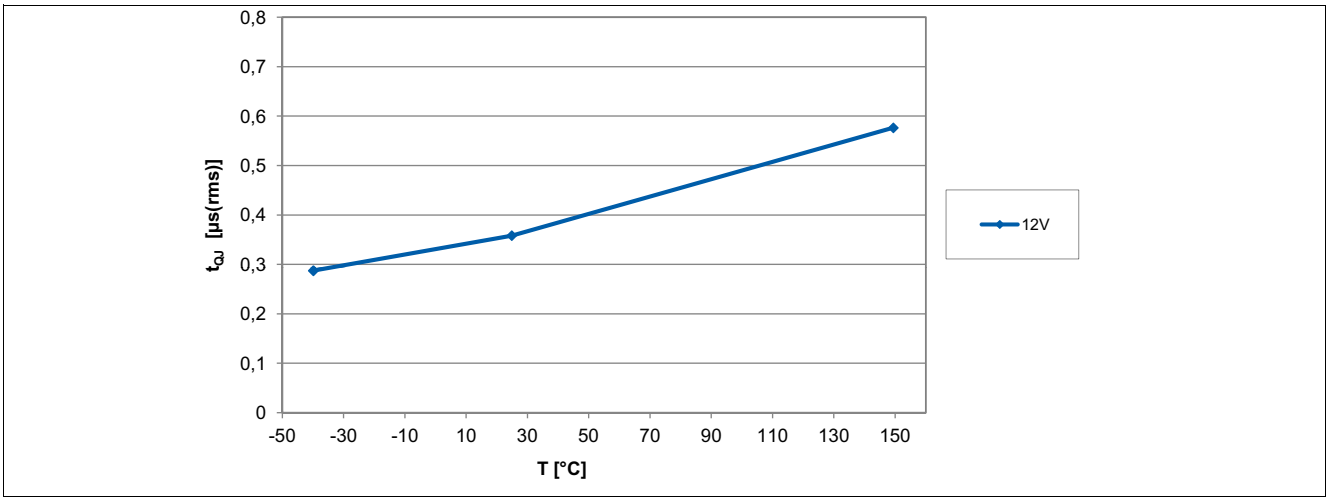

Figure 6-15 Output Signal Jitter of the TLE4961-3L over Temperature

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