ANALOG DEVICES

EVAL-AD7768-4FMCZ User Guide
UG-921

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Evaluation Board for the AD7768-4 24-Bit, 4-Channel, Simultaneous Sampling, 256 kSPS, Sigma-Delta ADC with Power Scaling

FEATURES

Full featured evaluation board for the AD7768-4
PC control in conjunction with the SDP-H1
   system demonstration platform (EVAL-SDP-CH1Z)
PC software control and data analysis
Time and frequency domain
Standalone hardware capability

ONLINE RESOURCES

Evaluation Kit Contents
   EVAL-AD7768-4FMCZ evaluation board
   Evaluation software CD for the AD7768-4
Documents Needed
   AD7768-4 data sheet
   EVAL-AD7768-4FMCZ user guide
Required Software
   AD7768-4 evaluation software

EQUIPMENT NEEDED

EVAL-AD7768-4FMCZ evaluation board
EVAL-SDP-CH1Z system demonstration platform
External 7 V to 9 V bench top power supply
DC/AC signal source (Audio Precision® or similar high
   performance signal source)
USB cable
PC running Windows with USB 2.0 port

GENERAL DESCRIPTION

The EVAL-AD7768-4FMCZ evaluation kit features the AD7768-4 24-bit, 256 kSPS, analog-to-digital converter (ADC). A 7 V to 9 V external bench top supply is regulated to 5 V and 3.3 V to supply the AD7768-4 and support components. The EVAL-AD7768-4FMCZ board connects to the USB port of the PC via a connection to the SDP-H1 motherboard, EVAL-SDP-CH1Z.

The AD7768-4 evaluation software fully configures the AD7768-4 device register functionality and provides dc and ac time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EVAL-AD7768-4FMCZ is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the AD7768-4 over a USB cable through the EVAL-SDP-CH1Z system demonstration platform (SDP).

Full specifications on the AD7768-4 are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

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REVISION HISTORY

3/16—Revision 0: Initial Version

EVAL-AD7768-4FMCZ QUICK START GUIDE

To begin using the EVAL-AD7768-4FMCZ evaluation board, take the following steps:

1. Ensure that the EVAL-SDP-CH1Z SDP-H1 board is disconnected from the USB port of the PC. Install the evaluation board software from the CD included in the evaluation board kit. Restart the PC after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)

2. Connect the SDP-H1 board to the evaluation board (unpowered). Figure 1 illustrates the connection: J4 of the SDP-H1 board adapts to the receiving socket on the EVAL-AD7768-4FMCZ printed circuit board (PCB).

3. Ensure that the boards are connected firmly together.

4. Apply power to the evaluation board via the supplied 9 V dc adapter at J1 (LK1 in Position B). Alternatively, supply an external voltage in the range of 7 V to 9 V from a bench top power supply using the J3 connector (LK1 in Position A).

5. Connect the 12 V dc supply to the SDP-H1 board, and then connect to the PC using the supplied USB cable. For Windows® XP, the PC may need to search for the SDP drivers. Choose to automatically search for the drivers for the SDP-H1 board if prompted by the operating system.

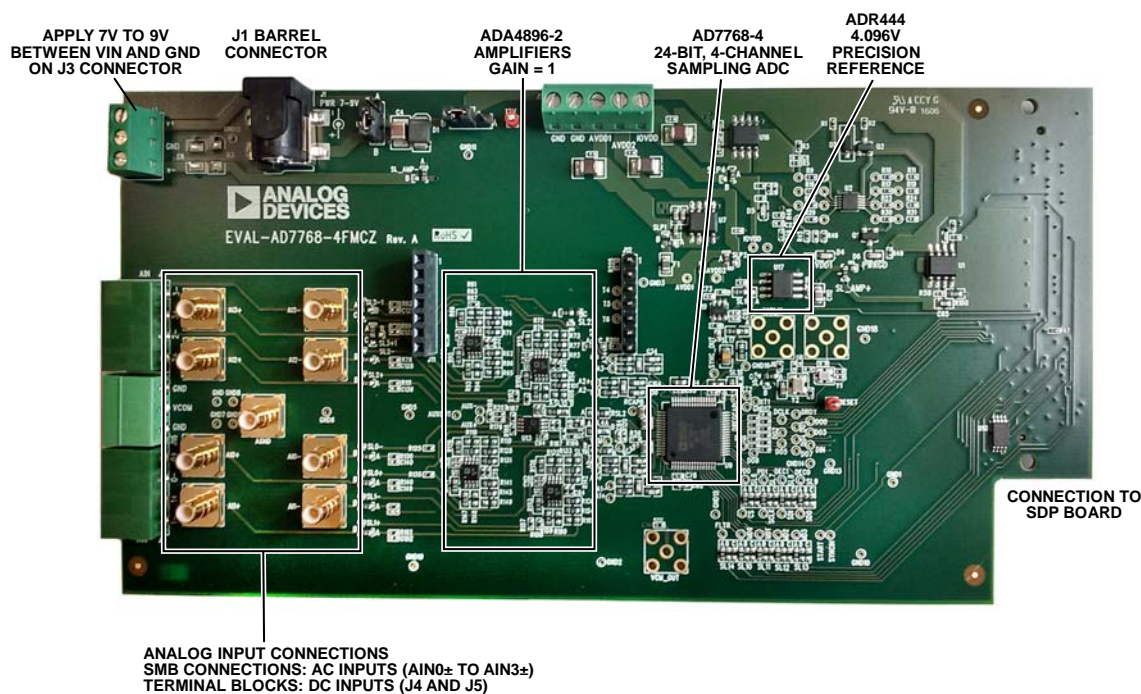6. Launch the AD7768-4 evaluation software from the **Analog Devices** subfolder in the **Programs** menu.

Figure 1. EVAL-AD7768-4FMCZ Evaluation Board

ANALOG INPUTS AND FRONT-END CIRCUIT

As shown in Figure 1, the AIN0± to AIN3± analog inputs are accessible through either the SMBs or the terminal blocks.

Figure 2 shows these connectors and details the eight main solder links that route the inputs from either the terminal blocks or the SMBs for each of the signals.

In the default board configuration, the input terminals are connected through to the ADA4896-2 on each of the ADC channels.

The ADR444 4.096 V low noise reference is used by default, allowing an absolute input range of 0||4.096 V on each input.

The ADA4896-2 amplifiers are not terminated at the inputs for any particular source impedances.

The on-board, common-mode voltage source on the AD7768-4 is used to bias the input signal. The default condition is V_{CM} = (AVDD1 − AVSS)/2.
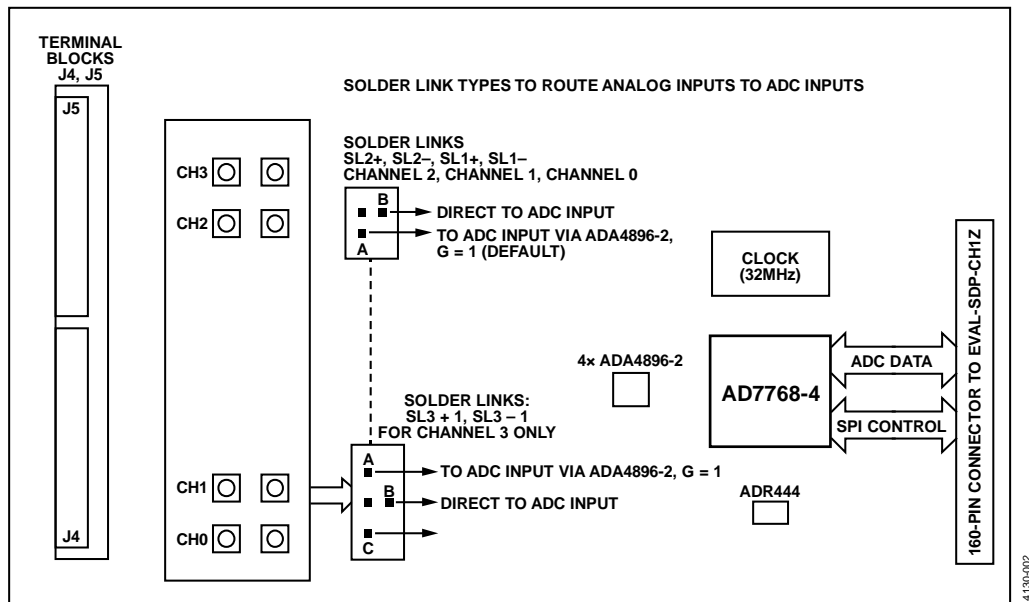

Figure 2. Analog Inputs: Input Connectors, Solder Links, and Amplifiers

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7768-4 is a 4-channel, simultaneously sampling, Σ-Δ ADC. The AD7768-4 offers an ADC per channel and synchronized sampling. The ADC power scaling is as required for the application, catered for by selecting one of the following modes of operation:

- Fast: 256 kSPS maximum, 110.8 kHz input bandwidth, 59 mW per channel
- Median: 128 kSPS maximum, 55.4 kHz input bandwidth, 32 mW per channel
- Economy: 32 kSPS maximum, 13.8 kHz input bandwidth, 12.2 mW per channel

The AD7768-4 offers extensive digital filtering:

- Wideband: low ripple, antialiasing, low pass filter with sharp roll off, and full attenuation at Nyquist frequency.
- Sinc response: sinc5 filter, low latency path for dc measurements or control loops.

Within these filter options, the user can select a decimation rate of 32, 64, 128, 256, 512, or 1024.

Embedded analog functionality on each ADC channel simplifies system design. A precharge buffer on each analog input reduces analog input current.

Complete specifications for the AD7768-4 are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details about the EVAL-SDP-CH1Z SDP-H1 board are available on the Analog Devices, Inc., website at www.analog.com.

HARDWARE LINK OPTIONS

The default link options are listed in Table 1. The board can be configured to operate from a bench top power supply via Connector J3, or from a 9 V dc adapter via Connector J1. The supply required for the AD7768-4 comes from the on-board low dropout regulators (LDOs), which generate their input voltage from J1 or J3 depending on the setting of LK1. Alternatively, the board can be powered by setting LK2 to Position A when used in conjunction with the SDP-H1 board (see Table 3 for details).

Table 1. Default Link and Solder Link Options

Link No.	Default Option	Description
LK1	A	LK1 selects the input voltage source.
		Position A: J3 is selected.
		Position B: J1 is selected.
LK2	B	LK2 selects the input from EVAL-SDP-CH1Z board.
		Position A: 12 V input from EVAL-SDP-CH1Z.
		Position B: external power supply from either J1 or J3.
SL1	A	SL1 selects between pin or SPI mode operation of the AD7768-4.
		Position A: SPI mode.
		Position B: pin mode (pin mode is not compatible with the evaluation software and currently untested on evaluation board).
SL2	B	FORMAT0 pin.
		Position A: IOVDD.
		Position B: DGND.
SL4	A	Clock terminal source selection. To choose the Y1 crystal oscillator, do not populate SL4. R253, R254, C46, and C45 must be populated. SL4A must be configured to the crystal oscillator.
		Position A: selects CMOS Oscillator Y2.
		Position B: unpopulated terminals (J6 and J7).
		Position C: SDP MCLK.
SL4A	A	Clock select (CLK_SEL) pin.
		CMOS clock option on Pin 32.
		Crystal oscillator or LVDS option.
SL5	Soldered 0 Ω resistor	Shorts $\overline{SYNC\_OUT}$ to $\overline{SYNC\_IN}$ to allow sync pulses on $\overline{START}$ to be synchronously applied to $\overline{SYNC\_IN}$.
SL6	A	Pin 16: ST0/$\overline{CS}$.
		Position A: $\overline{CS}$ pin in SPI mode.
		Position B: Channel 0 to Channel 3 power down (pin mode).
		Position C: Channel 0 to Channel 3 enabled (pin mode).

Link No.	Default Option	Description
SL7	A	Pin 17: ST1/SCLK. Position A: SCLK in SPI mode. Position B: pin mode.
SL8	A	Pin 18: DEC1/SDI. Position A: SDI in SPI mode. Position B: IOVDD. Position C: GND.
SL9	A	Pin 19: DEC0/SDO. Position A: SDO in SPI mode. Position B: IOVDD. Position C: GND.
SL10	A	Pin 12: MODE0/GPIO0. Position A: GPIO to SDP. Position B: GND. Position C: IOVDD.
SL11	A	Pin 13: MODE1/GPIO1. Position A: GPIO to SDP. Position B: GND. Position C: IOVDD.
SL12	A	Pin 14: MODE2/GPIO2. Position A: GPIO to SDP. Position B: GND. Position C: IOVDD.
SL13	A	Pin 15: MODE3/GPIO3. Position A: GPIO to SDP. Position B: GND. Position C: IOVDD.
SL14	A	Pin configuration mode. AD7768-4 evaluation kit software runs from SPI mode; select the filter via the register map. This link selects the filter mode (only available in pin mode). Position A: GPIO4. Position B: sinc5 fast settling filter. Position C: wideband low ripple filter.
SL15	A	Select common-mode voltage to bias input signals to one of the following. Position A: OP2177 buffered VCM output. Position B: VCM output from AD7768-4.
SL16	B	Select reference path from ADR444 to REFx+. Position A: bypass external reference buffer. Position B: ADR444 input into ADA4841-1 reference buffer.
SL17	B	Select reference path from ADR444 to REFx+. Position A: bypass external reference buffer. Position B: select output from ADA4841-1 reference buffer.
SL18	Unsoldered	Shorts IOVDD to DREGCAP, only for IOVDD = 1.8 V operation; see the AD7768-4 data sheet.
SL19	A	External common-mode buffer input selection. Position A: AD7768-4 VCM pin. Position B: AVDD1 used for common-mode selection, R166 (0 Ω) and R167 (not inserted) can be used as voltage dividers.
SL22, SL23		Selects the output from Channel 3 amplifier driver option. Position A: ADA4896-2. Position B: bypass driver. Position C: amplifier driver board header via the J11 and J12 connectors.

Link No.	Default Option	Description
SLP1	A	AVDD1 input selector.
		Position A: ADP7118ARDZ-5.0 5 V LDO.
		Position B: external AVDD1 input (J2, Pin 3).
SLP2	A	AVDD2 LDO selector.
		Position A: ADP7118ARDZ-5.0 5 V LDO.
		Position B: external AVDD2 input (J2, Pin 4).
SLP4	A	IOVDD input selector.
		Position A: ADP7118ARDZ-3.3 3.3 V LDO.
		Position B: external AVDD2 input (J2, Pin 5), 2.25 V to 3.6 V, 1.8 V.
SL_AMP+	A	ADA4896-2 positive supply voltage.
		Position A: AVDD1 ADP7118ARDZ-5.0 supply.
		Position B: external supply to board, J1 or J3 input depending on LK1 position.
SL_AMP−	A	ADA4896-2 negative supply voltage.
		Position A: evaluation board ground plane.
		Position B: external supply to board, J1 or J3 input depending on LK1 position, on-board ADA4896-2 are shorted to ground and VSS pins, replace with capacitors for bipolar amplifier supplies.
SL2+ to SL0+, SL2− to SL0−	A	Selects the input driver for Channel 2, Channel 1, and Channel 0.
		Position A: ADA4896-2.
		Position B: bypass driver.
SL3+, SL3−	A	Selects the input driver for Channel 3.
		Position A: ADA4896-2.
		Position B: bypass driver.
		Position C: external amplifier driver board header via the J11 and J12 connectors.

On-Board Connectors

Table 2 provides information about the external connectors on the EVAL-AD7768-4FMCZ.

Table 2. On-Board Connectors

Connector	Function
J1	Wall wart (dc plug) power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.
J2	Connector for supplying AVDD1, AVDD2, IOVDD, AVSS, and AGND externally.
J3	Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.
J4	4-pin connector for input to Channel 2 and Channel 3.
J5	4-pin connector for input to Channel 0 and Channel 1.
J6	SMA/SMB connector for XTAL2 (CLKIN/LVDS).
J7	SMA/SMB connector for XTAL1 (LVDS).
J11	Optional external connector for driver daughter board. Channel 3.
J12	Optional external connector for driver daughter board. Channel 3.
J13, J14	8-pin connector for input to Channel 0 to Channel 3.
J15	Unpopulated VCM SMA connector.
AI0+ to AI3+	Analog input SMA positive terminal for Channel 0 to Channel 3.
AI0− to AI3−	Analog input SMA negative terminal for Channel 0 to Channel 3.
P1	Connector on the underside of the EVAL-AD7768-4FMCZ board that mates with the EVAL-SDP-CH1Z controller board.

POWER SUPPLIES

The evaluation board requires that an external power supply, either a bench top supply or a wall wart (dc plug) supply, be applied to J1 or J3 (see Table 3 for more information). Linear regulators generate the required power supply levels from the applied V_{IN} rail. The regulators used are the 5 V ADP7118 (U1 and U7), which supply AVDD1, the on-board amplifiers and reference, and the 3.3 V ADP7118 (U16), which delivers 3.3 V to the IOVDD pin of the AD7768-4.

SERIAL DATA INTERFACE

The AD7768-4 evaluation board outputs conversion results to the EVAL-SDP-CH1Z SDP-H1 board via the four data output pins, DOUT0 to DOUT3. The serial data interface also includes signals such as SCLK, DCLK, and $\overline{DRDY}$ (all are outputs).

SERIAL CONFIGURATION INTERFACE

The AD7768-4 is configured by the SDP-H1 board via a 4-wire SPI interface. SL1 must be shorted to Position A for this mode to be active.

POWERING DOWN THE SYSTEM DEMONSTRATION PLATFORM

When disconnecting the SDP-H1 evaluation platform and powering down the system, make sure to first exit the evaluation software. Then, press the reset button on the SDP-H1 board before disconnecting the 12 V supply and then the USB. Failure to follow this procedure can cause damage to the SDP-H1 board.

Table 3. AD7768-4 Power Supply[1]

Power Supply (V_{IN}) Source	Voltage Range	Function
J1	7 V to 9 V	Wall wart (dc plug) supply to the evaluation board. Supplies LDOs that create the 5 V and 3.3 V rails. It also supplies the ADR444 external reference. Ensure that both LK1 and LK2 are set to Position B when the external power supply is applied to this connector.
J3	7 V to 9 V	Bench top supply to the evaluation board. Supplies LDOs that create 5 V and 3.3 V rails. It also supplies the ADR444 external reference and on-board amplifiers. Ensure that LK1 is set to Position A when the external power supply is applied to this connector and LK2 is set to Position B.
EVAL-SDP-CH1Z	12 V	If using the EVAL-SDP-CH1Z, power can be taken from this board and supplied to the LDOs. Set LK2 to Position A.

[1] Only a single supply is required.

SOCKETS/CONNECTORS

Table 4. Connector Details

Connector	Function	Connector Type	Manufacturer/Part No.	Order No.
J1	Wall wart (dc plug) power supply voltage input. Apply 7 V.	2 mm, dc power connector	Kycon KLDX-SMT2-0202-A	Mouser 806-KLDX-SMT20202A
J2	Apply voltage within data sheet specified ranges and GND (0 V) to this connector to power the evaluation board. J2 is the connector for supplying AVDD1, AVDD2, IOVDD, AVSS, and AGND externally.	5-pin socket terminal block	Lumberg FRE 05	Farnell 1217310
J3	Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.	3-pin socket terminal block, 3.81 mm pitch	Phoenix Contact MC 1,5/3-G-3,81	Farnell 3704737
J6	SMA/SMB connector for XTAL2 (CLKIN/LVDS).	Straight PCB mount SMB/SMA jack	Tyco 1-1337482-0	Not inserted
J7	SMA/SMB connector for XTAL1 (LVDS).	Straight PCB mount SMB/SMA jack	Tyco 1-1337482-0	Not inserted
J4	4-pin connector for input to Channel 2 to Channel 3.	4-pin socket terminal block, 3.81 mm pitch	Multicomp, MC000130	Farnell 2008110
J5	4-pin connector for input to Channel 0 to Channel 1.	4-pin socket terminal block, 3.81 mm pitch	Multicomp, MC000130	Farnell 2008110
J11	Optional external connector for additional driver board, Channel 3.	7-way, 2.54 mm, vertical socket	Samtec SSW-107-01-T-S	Farnell 1803478
J12	Optional external connector for additional driver board, Channel 3.	7-way, 2.54 mm, through hole header	Samtec TLW-107-05-G-S	Farnell 1668499
J15	Unpopulated VCM SMA connector.	Straight PCB mount SMB/SMA jack	Tyco 1-1337482-0	Farnell 3704737
AI0+ to AI3+	Analog input SMA positive terminal for Channel 0 to Channel 3.	Straight PCB mount SMB/SMA jack	Tyco 1-1337482-0	Farnell 1206013
AI0− to AI3−	Analog input SMA negative terminal for Channel 0 to Channel 3.	Straight PCB mount SMB/SMA jack	Tyco 1-1337482-0	Farnell 1206013
P1	Connection to EVAL-SDP-CH1Z controller board.	160-pin, 10 mm, male, VITA 57 connector	Samtec ASP-134604-01	Farnell 2433507

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and SDP-H1 board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

Connect the EVAL-SDP-CH1Z SDP-H1 board to P1 (bottom) on the EVAL-AD7768-4FMCZ evaluation board.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7768-4FMCZ evaluation kit includes a CD containing software to be installed on the PC before using the evaluation board.

There are two parts to the installation:

- AD7768-4 evaluation board software installation
- EVAL-SDP-CH1Z system demonstration platform board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and SDP-H1 board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC. When disconnecting the board, it is important to follow the power-down sequence outlined in the Powering Down the System Demonstration Platform section.

Installing the Evaluation Board Software

To install the evaluation board software,

1. With the SDP-H1 board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7768-4-4**.
3. A dialog box appears requesting permission to allow the program to make changes to the PC. Click **Yes**.

Figure 3. Evaluation Board Software Installation:
Granting Permission for Program to Make Changes

4. Select the location to install the software, and then click **Next**. Figure 4 shows the default installation locations, which are displayed when the window opens. To select a different installation location, click **Browse**.

Figure 4. Evaluation Board Software Installation:
Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, select **I accept the License Agreement**, and then click **Next**.
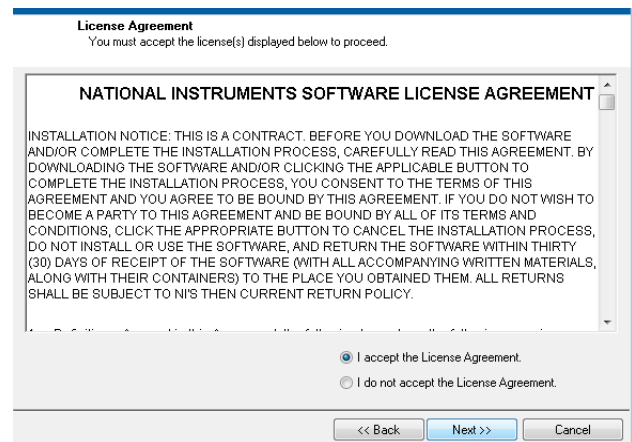
Figure 5. Evaluation Board Software Installation:
Accepting the License Agreement

6. A summary of the installation is displayed. Click **Next** to continue.
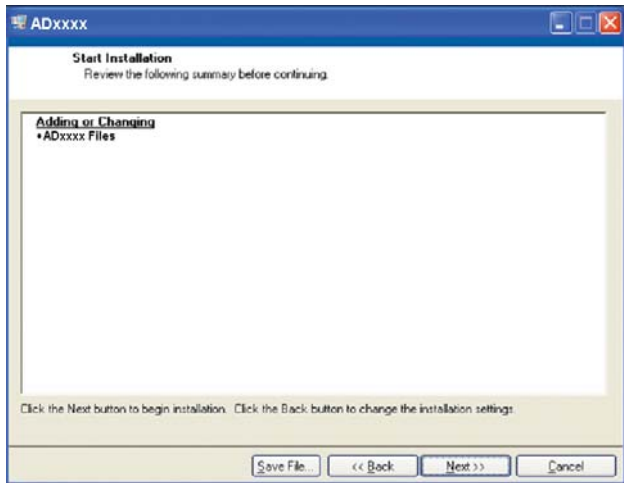
Figure 6. Evaluation Board Software Installation: Reviewing a Summary of the Installation

7. A dialog box informs you when the installation is complete. Click **Next**.
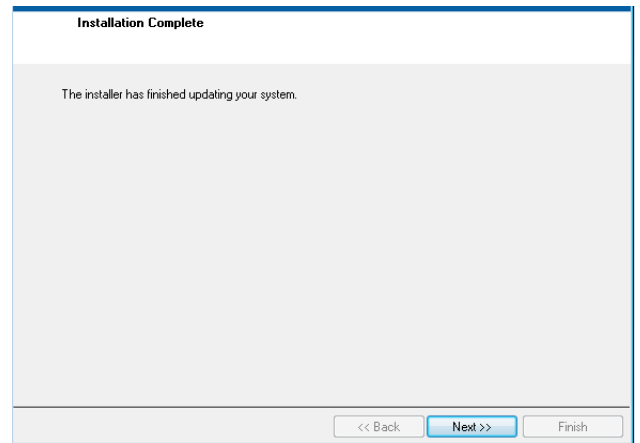
Figure 7. Evaluation Board Software Installation: Indicating When the Installation is Complete

Installing the System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window displays for the installation of the SDP drivers.

1. With the EVAL-SDP-CH1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.
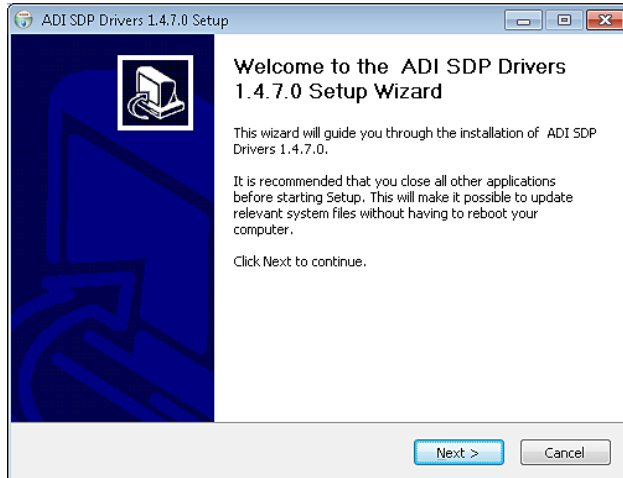
Figure 8. SDP Drivers Setup: Beginning the Drivers Installation

2. Select the location to install the drivers, and then click **Next**.
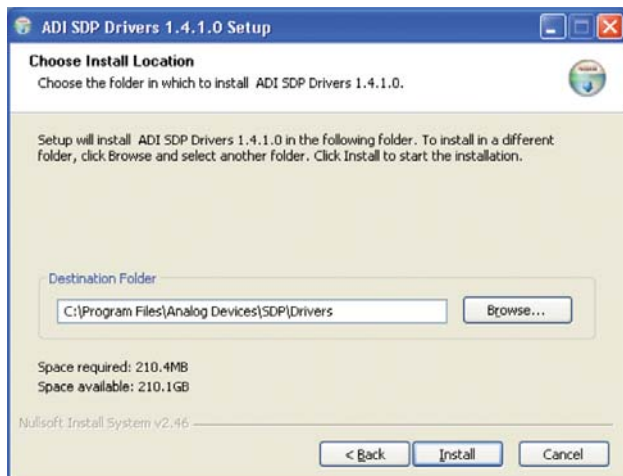
Figure 9. SDP Drivers Setup: Selecting the Location for Drivers Installation

3. Click **Install** to confirm that you want to install the drivers.
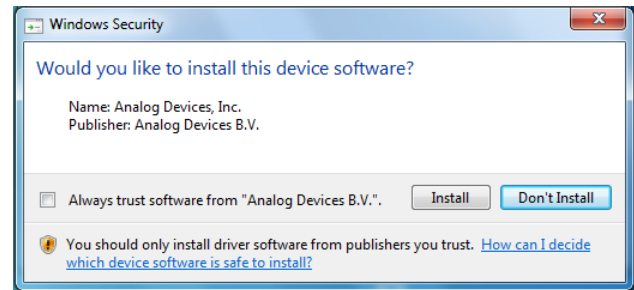
Figure 10. SDP Drivers Setup: Granting Permission to Install Drivers

4. To complete the drivers installation, click **Finish**, which closes the installation wizard.
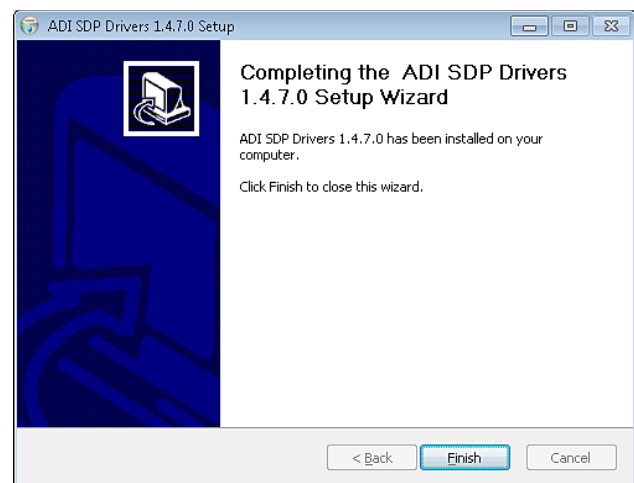
Figure 11. SDP Drivers Setup: Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart your computer.
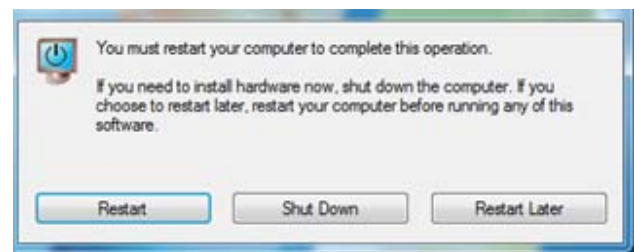
Figure 12. SDP Drivers Setup: Restarting the Computer

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Hardware sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the EVAL-SDP-CH1Z SDP-H1 board is plugged into the PC. (If using Windows XP, the PC may need to search for the SDP drivers. Choose to automatically search for the drivers for the SDP board if prompted by the operating system.)
2. Check that the SDP-H1 board is connected to the PC correctly using the **Device Manager** of the PC.
   a. Access the **Device Manager** as follows:
      i. Right-click **My Computer** and then click **Manage**.
      ii. A dialog box appears asking for permission to allow the program to make changes to the computer. Click **Yes**.
      iii. The **Computer Management** box appears. Click **Device Manager** from the list of **System Tools** (see Figure 13).
   b. The SDP-H1 board appears under **ADI Development Tools**, which indicates that the driver software is installed and that the board is connected to the PC correctly.
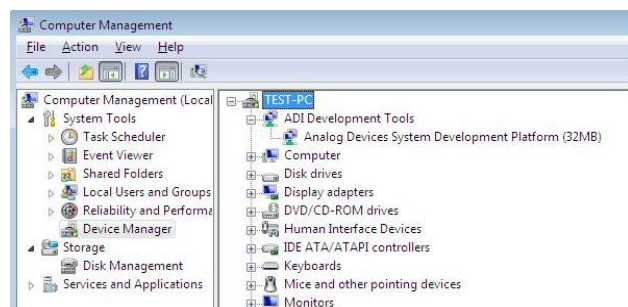
Figure 13. Device Manager: Checking That the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7768-4 software as follows:

1. From the Start menu, click **Programs** > **Analog Devices** > **AD7768-4 Evaluation Software**. The main window of the software then displays.
2. If the AD7768-4 evaluation system is not connected to the USB port via the SDP-H1 when the software is launched, a connectivity error displays prompting the user to choose an evaluation board (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.
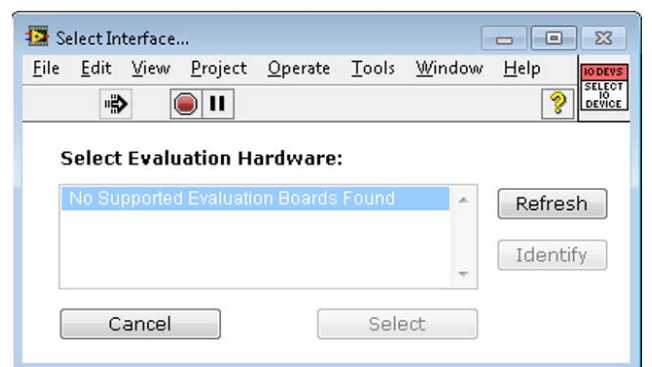
Figure 14. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the SDP-H1 board connected to the PC is detected, and then the main window appears (see Figure 15).

SOFTWARE OPERATION
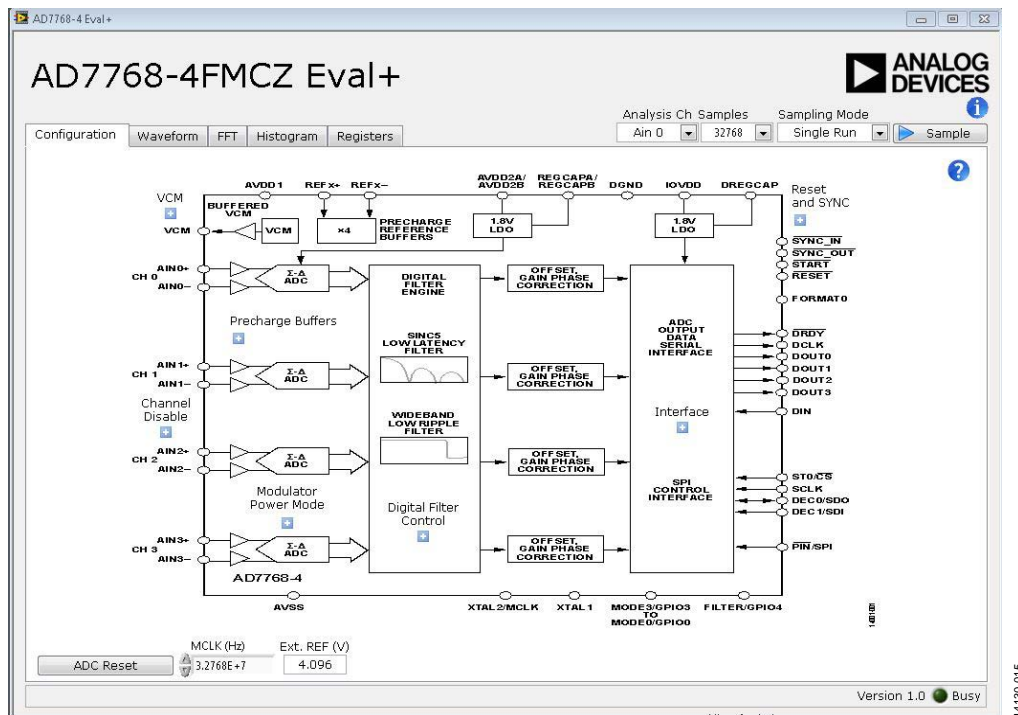
Figure 15. Evaluation Software Main Window

Overview of the Main Window

The main window contains the significant control buttons and analysis indicators of the evaluation software.

Configuration Tab and AD7768-4 Block Diagram

The **Configuration** tab is the tab displayed by default when the software first opens. An overview of the AD7768-4 block diagram is shown, along with buttons that open pop-up menus for quick configuration of the device.

The **Waveform** tab displays captured waveform data. It also contains options to save the resulting data and shows the output header data from the conversion results.

The **FFT** and **Histogram** tabs show a more in depth analysis of the output data. This data can be saved to a file.

Use the **Registers** tab to change the configuration of the AD7768-4.

Sample Button

Click **Sample** to start ADC sampling; results are reported in the **Waveform**, **FFT**, and **Histogram** tabs. Set the mode of operation using the **Sampling Mode** drop-down box; the mode can be continuous sampling or a single run.

Number of Samples

The number of samples per channel is variable and can be changed using the **Samples** control.

MCLK

The **MCLK (Hz)** control in the **Configuration** tab must match the frequency of the ADC clock source.

V_{REF}

The **Ext. REF (V)** in the **Configuration** tab control must match the reference voltage of the ADC.

ADC Reset

Clicking **ADC Reset** in the **Configuration** tab sends a reset command to the ADC via the SPI, and resets the device to its default configuration.

Header Data

The **Header Data** area shows the header data output in the first eight bits of a conversion. It conveys status information and the channel number. Header data for each channel can be selected by changing the **Analysis Ch** option.

- **CRC Error** indicates that an error has occurred, and a reset is required.
- **Filter not settled** indicates that the filter did not settle before data was sampled.
- **Filter Type** indicates the type of filter that has been selected.
- **Filter saturated** indicates that filter saturation has occurred.

Note that the evaluation software has not been configured to output the CRC check code.
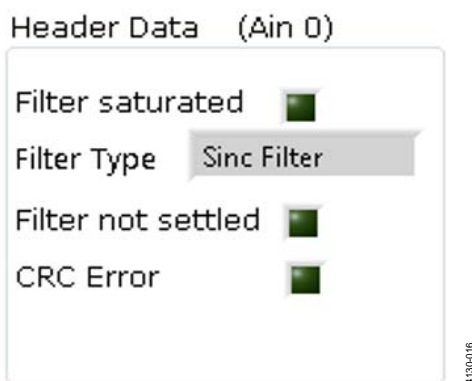
Figure 16. Example Header Data

Channel Enable/Disable Check Box

The channel enable and disable check boxes, as shown in Figure 17, individually enable channels for display and analysis.

Figure 17. Channel Enable/Disable Check Boxes

Help Button

Click the help button (the **?** icon) to show information about the AD7768-4 software. The help button is located in the top right corner of the **Configuration** tab (see Figure 15).

Status Indicator and Busy light

The status bar at the bottom of the screen indicates the current state of the AD7768-4 software. The **Busy** LED illuminates when the software is busy performing an action. Refrain from carrying out any more actions when this light is lit.

Waveform Tab

The **Waveform** tab displays a time-domain graph of the sampled data. Controls beneath the graph allow zooming and panning. Amplitude information is given beneath the graph for the analysis channel selected.
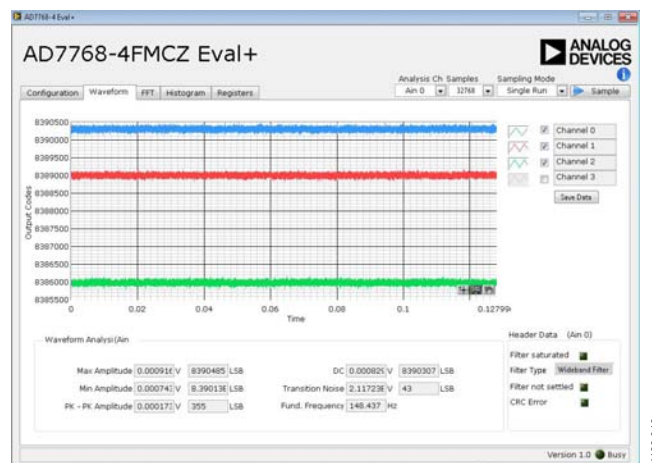
*Figure 18. **Waveform** Tab*

FFT Tab

The **FFT** tab shows a frequency domain graph of the sampled data. Controls beneath the graph allow zooming and panning, and control over amplitude and frequency scaling. Frequency and amplitude information is given beneath the graph for the selected analysis channel.
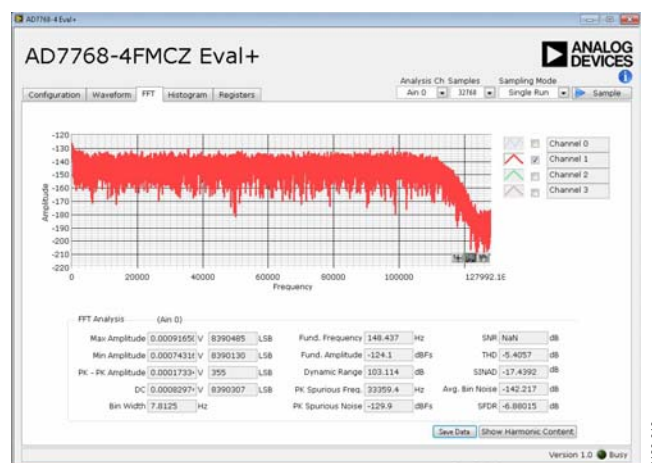
*Figure 19. **FFT** Tab*

Histogram Tab

The **Histogram** tab shows a histogram of the sampled data. Controls beneath the graph allow zooming and panning, and control over amplitude scaling. Amplitude information is given beneath the graph for the selected analysis channel.
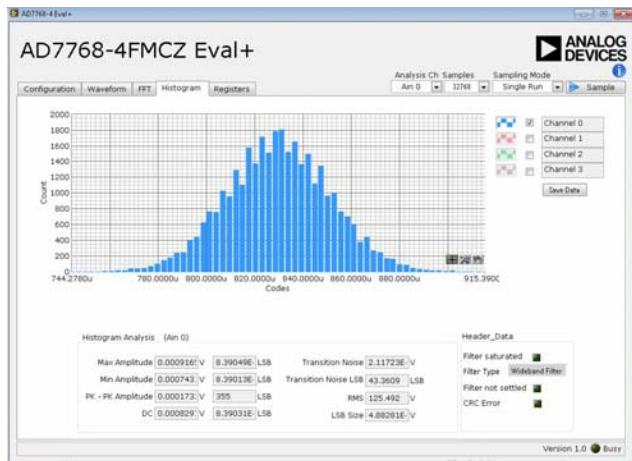
Figure 20. **Histogram** *Tab*

Registers Tab

The **Registers** tab allows precise control of the AD7768-4 registers, allowing them to be read back and written to. The registers are grouped together and can be altered in a number of ways, as shown in Figure 21. The register to be written to can be selected from the register map, located on the left hand side of the **Registers** tab. Individual register bits can be changed from the register section, or the entire register can also be written to by writing the required hexadecimal value. Drop-down options can be selected from the **Bitfields** section, or the entire bitfield can be written to with a hexadecimal value.

A particular register configuration can be saved to be loaded again at a later time.
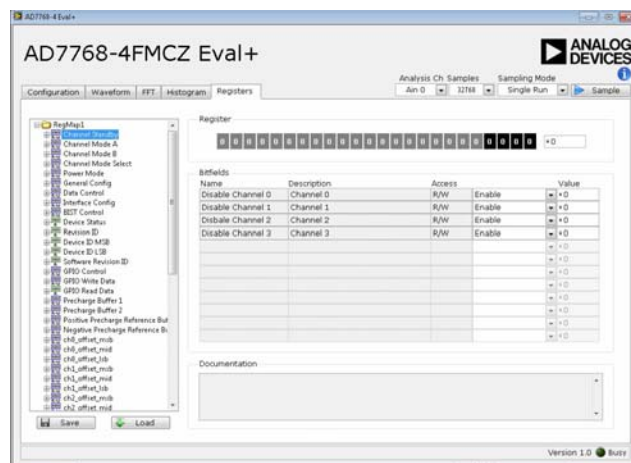
Figure 21. **Registers** *Tab*

Precharge Buffers: Register Operation

The precharge buffers operate differently then the other registers. To change these registers, it is recommended to navigate to the **Registers** tab, select **Precharge Buffer 1** or **Precharge Buffer 2** from the register map, and change the value of these registers using the hexadecimal value located on the right hand side of the **Register** section (see Figure 22). The software reads back the status of the registers correctly; however, to change a bit to 0, for example, a 1 must be written to the given bit in the register. See the AD7768-4 data sheet for more details.
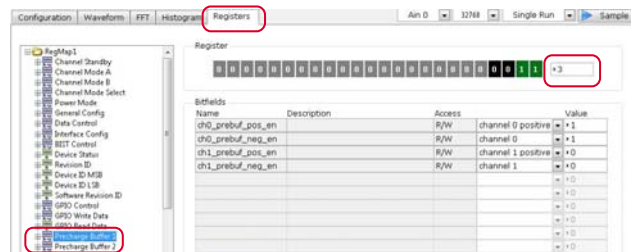
Figure 22. Enabling/Disabling the Precharge Buffers

Exiting the Software

To exit the software, click the red **X** at the top right hand corner of the main window. Be sure to press the reset button on the EVAL-SDP-CH1Z before the board is powered off.

Example

In this example, a sample is taken and analyzed with the help of the AD7768-4 software. The desired data is expected on Channel 2 of the ADC.

The following equipment is required:

- Audio Precision source (AP SYS-2722 or similar)
- A PC
- EVAL-AD7768-4FMCZ evaluation board
- EVAL-SDP-CH1Z SDP-H1 controller board
- 12 V power supply for the EVAL-SDP-CH1Z
- 9 V power supply for the EVAL-AD7768-4FMCZ

To sample and analyze the data, take the following steps:

1. Connect the evaluation board to the SDP-H1 board.
2. Set both LK1 and LK2 to Position B on the evaluation board.
3. Power up both boards, and then connect the SDP-H1 board to the PC via the USB cable supplied.
4. Start the AD7768-4 evaluation software. Wait for the **Busy** indicator to turn off.
5. Configure the Audio Precision source to the following settings, and connect the output to the Channel 2 input:
    - Select a sine wave output and **High Acc**
    - Set the output to balanced float
    - Set the frequency to 1 kHz
    - Set the amplitude to 7.734 V p-p
6. If not using the default configuration ensure that **MCLK (Hz)** and **Ext. REF (V)** on the software configuration tab are set to match the clock frequency and reference voltage supplied to the chip (by default, 32.768 MHz and 4.096 V).

7. Set the number of samples per channel to 32,768 (default).
8. Configure the registers as required using the pop-up menus under the **Configuration** tab. For this example, the settings are wideband filter, decimation by 32, fast power mode, and MCLK divide by four (all default).
9. Click **Sample** to take a reading. Wait for the **Busy** indicator to turn off.
10. The sampled data is now present in the data capture tabs (**Waveform**, **FFT**, and **Histogram** tabs). Change between each of these to view the results. In this case, select Channel 2 on the channel enable and disable check boxes to view the desired data on Channel 2.
11. Under the **FFT** tab, the FFT analysis shows results like the following:
    - **SNR** = 106.8 dB
    - **THD** = −120 dB
    - **SINAD** = 106.6 dB
    - **Fund. Frequency** = 1000 Hz
    - **Fund. Amplitude** = −0.5 dBFS
12. Change various settings and observe the output. For example, set the number of samples per channel to 16,384.
13. Click **Sample** to take a reading. Wait for the **Busy** indicator to turn off.
14. The sampled data is now present in the **Waveform**, **FFT**, and **Histogram** tabs.

For input amplitudes close to full scale (for the fundamental amplitude reading between 0 and −1 dBFS), the SNR and SINAD values displayed are adjusted to reflect a full-scale input.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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