# PCA9517A
## Level translating I²C-bus repeater

**Rev. 4.1 — 24 May 2016** **Product data sheet**

## 1. General description

The PCA9517A is a CMOS integrated circuit that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9517A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PCA9517A is unpowered.

The 2.7 V to 5.5 V bus port B drivers behave much like the drivers on the PCA9515A device, while the adjustable voltage bus port A drivers drive more current and eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0 V LOW on the port A which accommodates smaller voltage swings of lower voltage logic.

The static offset design of the port B PCA9517A I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515A, PCA9516A, PCA9517A (port B), or PCA9518. Port A of two or more PCA9517As can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9517As can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9517A drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the port B internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on port A drives a hard LOW and the input level is set at $0.3V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

**Table 1. PCA9517 and PCA9517A comparison**

| Parameter | PCA9517[1] | PCA9517A[2] |
|---|---|---|
| electrostatic discharge, HBM | > 2 kV | > 5.5 kV |

[1] PCA9517 will be discontinued in several years, so move to the PCA9517A for all new designs and system updates.

[2] The PCA9517A is an improved hot swap and ESD version of the PCA9517, but otherwise operates identically and should be used for all new designs and system updates.

## 2.    Features and benefits

- ■ 2 channel, bidirectional buffer isolates capacitance and allows 400 pF on either side of the device
- ■ Voltage level translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- ■ Footprint and functional replacement for PCA9515/15A
- ■ I$^2$C-bus and SMBus compatible
- ■ Active HIGH repeater enable input
- ■ Open-drain input/outputs
- ■ Lock-up free operation
- ■ Supports arbitration and clock stretching across the repeater
- ■ Accommodates Standard-mode and Fast-mode I$^2$C-bus devices and multiple masters
- ■ Powered-off high-impedance I$^2$C-bus pins
- ■ Port A operating supply voltage range of 0.9 V to 5.5 V
- ■ Port B operating supply voltage range of 2.7 V to 5.5 V
- ■ 5 V tolerant I$^2$C-bus and enable pins
- ■ 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ■ ESD protection exceeds 5500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- ■ Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- ■ Packages offered: SO8, TSSOP8 and HWSON8

## 3.    Ordering information
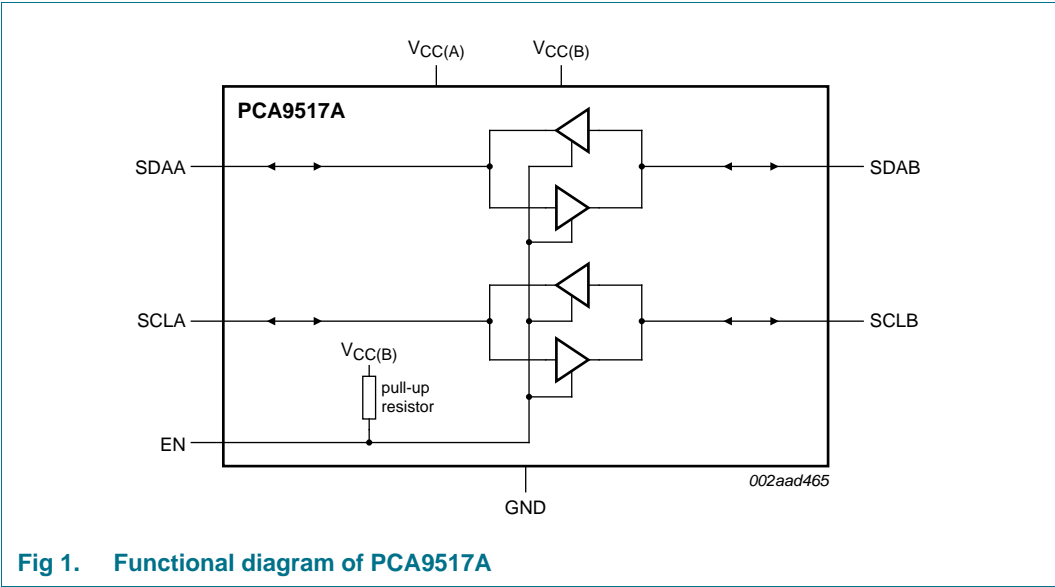
**Table 2.    Ordering information**
$T_{amb} = -40 \ ^\circ C \ to +85 \ ^\circ C.$

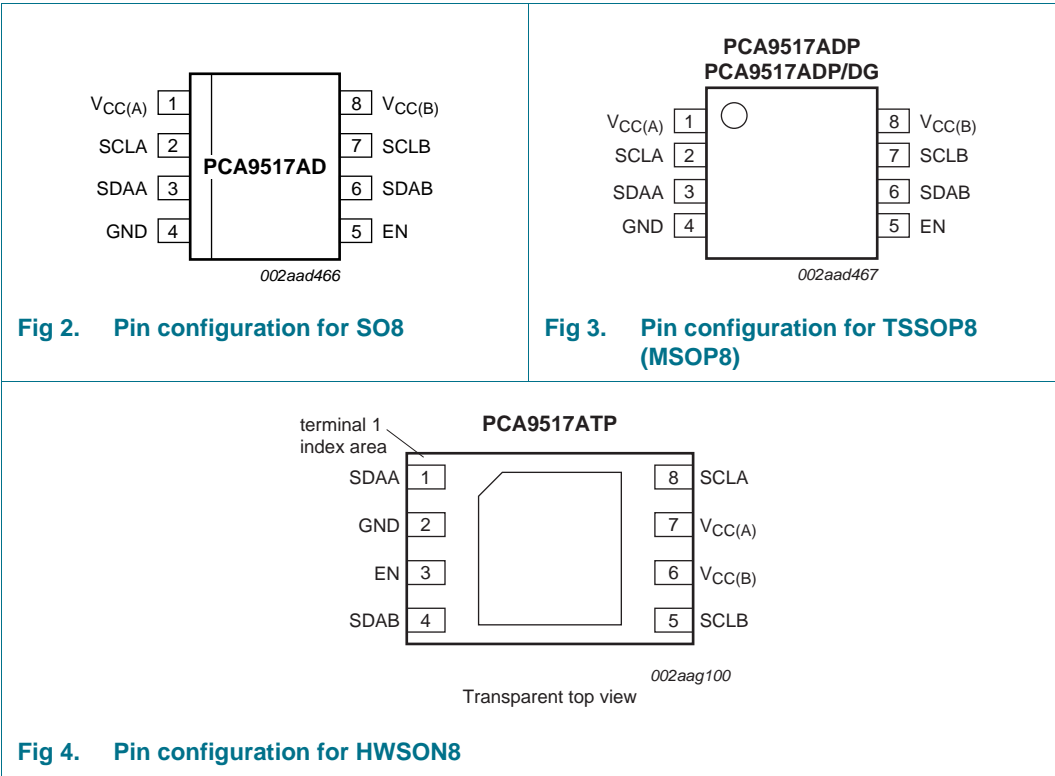| Type number | Topside mark | Package | | |
|---|---|---|---|---|
| | | **Name** | **Description** | **Version** |
| PCA9517AD | PA9517A | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| PCA9517ADP | 9517A | TSSOP8[1] | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| PCA9517ADP/DG | 9517A | TSSOP8[1][2] | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| PCA9517ATP | 17A | HWSON8 | plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm | SOT1069-2 |

[1] Also known as MSOP8.

[2] PCA9517ADP/DG is functionally the same (electrically and mechanically) as the PCA9517ADP, but was initially produced (e.g., "born") with Dark Green (lead-free and halogen/antimony-free) package material and is a temporary unique orderable part number for customers who desire to order and only receive Dark Green package material. The standard part PCA9517ADP will transition to Dark Green package material in 2Q'12 and then the PCA9517ADP and PCA9517ADP/DG devices will be identical. The PCA9517ADP/DG part number will be EOL after several years as customers who used this temporary part number update their BOM to the normal part number.

## 4.   Functional diagram



**Fig 1.    Functional diagram of PCA9517A**

## 5.   Pinning information

### 5.1   Pinning



**Fig 2.    Pin configuration for SO8**



**Fig 3.    Pin configuration for TSSOP8 (MSOP8)**



**Fig 4.    Pin configuration for HWSON8**

## 5.2 Pin description

**Table 3.** **Pin description**

| Symbol | Pin | | Description |
|--------|-----|---|-------------|
| | **SO8, TSSOP8** | **HWSON8** | |
| $V_{CC(A)}$ | 1 | 7 | port A supply voltage (0.9 V to 5.5 V) |
| SCLA | 2 | 8 | serial clock port A bus |
| SDAA | 3 | 1 | serial data port A bus |
| GND | 4 | 2[1] | supply ground (0 V) |
| EN | 5 | 3 | active HIGH repeater enable input |
| SDAB | 6 | 4 | serial data port B bus |
| SCLB | 7 | 5 | serial clock port B bus |
| $V_{CC(B)}$ | 8 | 6 | port B supply voltage (2.7 V to 5.5 V) |

[1] HWSON8 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper head conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

# 6. Functional description

Refer to Figure 1 "Functional diagram of PCA9517A".

The PCA9517A enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.9 V without degradation of system performance. The PCA9517A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.9 V) and a 3.3 V or 5 V I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0 V). The PCA9517A includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.5 V and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port A (below $0.3V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.5 V. When port A rises above $0.3V_{CC(A)}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V the port A driver is turned on and port A pulls down to 0 V. The port A pull-down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pull-down driver is enabled and port B will only be able to rise to 0.5 V until port A rises above $0.3V_{CC(A)}$, then port B will continue to rise being pulled up by the external pull-up resistor. The $V_{CC(A)}$ is only used to provide the $0.3V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PCA9517A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

## 6.1 Enable

The EN pin is active HIGH with an internal pull-up to $V_{CC(B)}$ and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

## 6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode and Fast mode I²C-bus devices in addition to SMBus devices. Standard mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

Please see Application Note *AN255, I²C/SMBus Repeaters, Hubs and Expanders* for additional information on sizing resistors and precautions when using more than one PCA9517A in a system or using the PCA9517A in conjunction with other bus buffers.

# 7. Application design-in information

A typical application is shown in Figure 5. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.
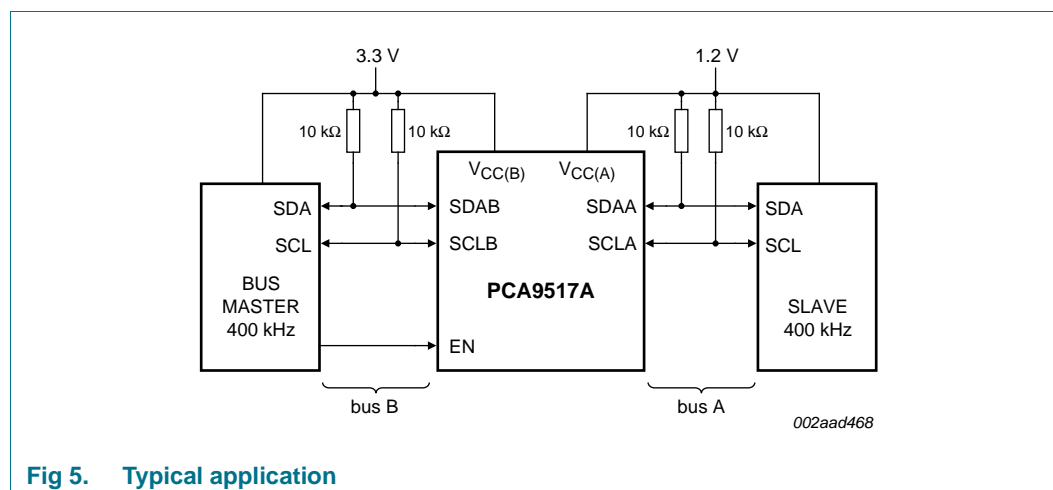


**Fig 5.    Typical application**

The PCA9517A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When port A of the PCA9517A is pulled LOW by a driver on the I$^2$C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9517A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 5 were to write to the slave through the PCA9517A, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I$^2$C-bus transmission except that the HIGH level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the PCA9517A, the clock and data lines would have a positive offset from ground equal to the $V_{OL}$ of the PCA9517A. After the eighth clock pulse, the data line will be pulled to the $V_{OL}$ of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9517A for a short delay while the A bus side rises above $0.3V_{CC(A)}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9517A ($V_{IL}$) be at or below 0.4 V to be recognized by the PCA9517A and then transmitted to the A bus side.

Multiple PCA9517A port A sides can be connected in a star configuration (Figure 6), allowing all nodes to communicate with each other.

Multiple PCA9517As can be connected in series (Figure 7) as long as port A is connected to port B. I$^2$C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

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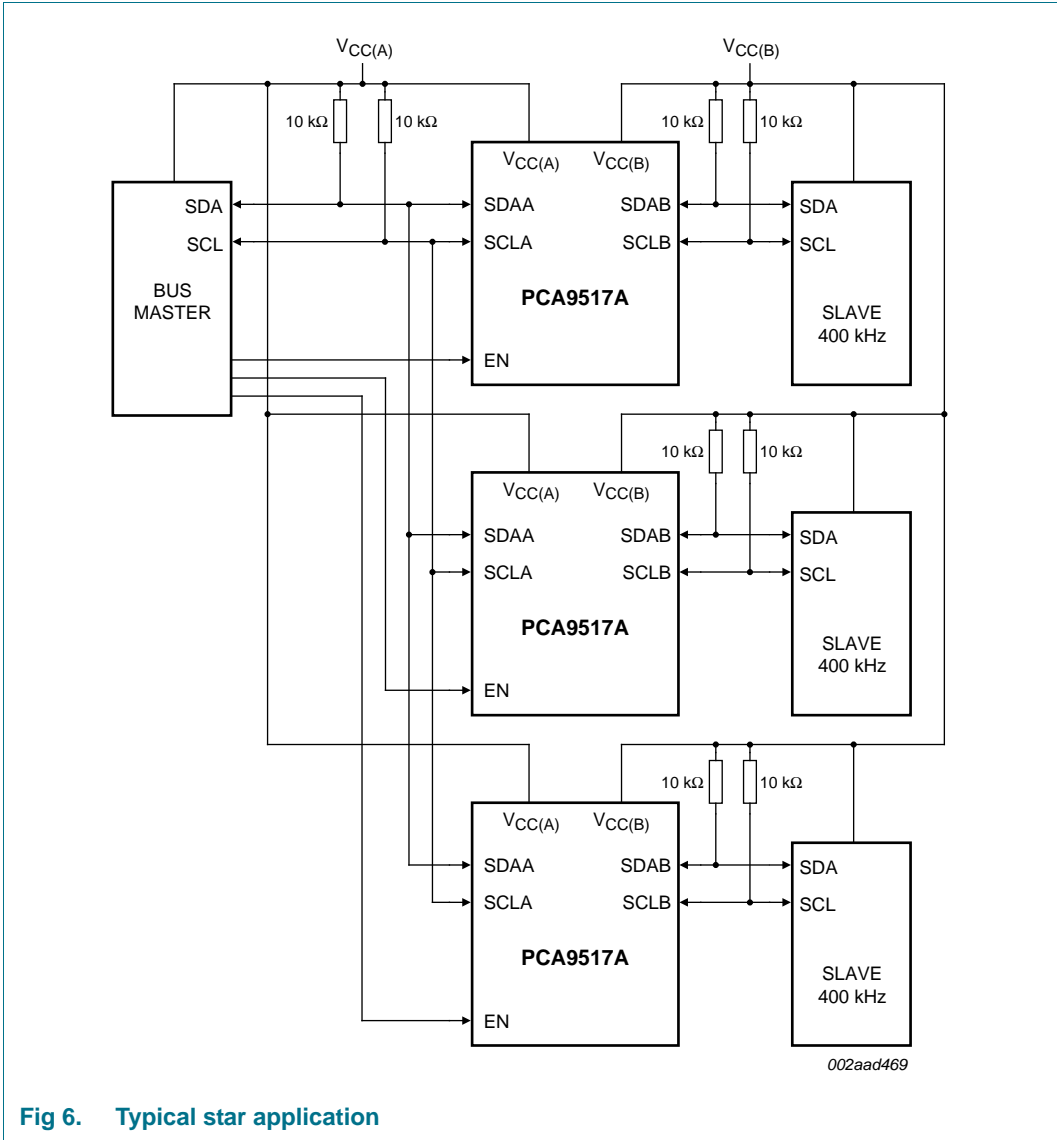**Product data sheet** Rev. 4.1 — 24 May 2016 6 of 22

Fig 6.    Typical star application
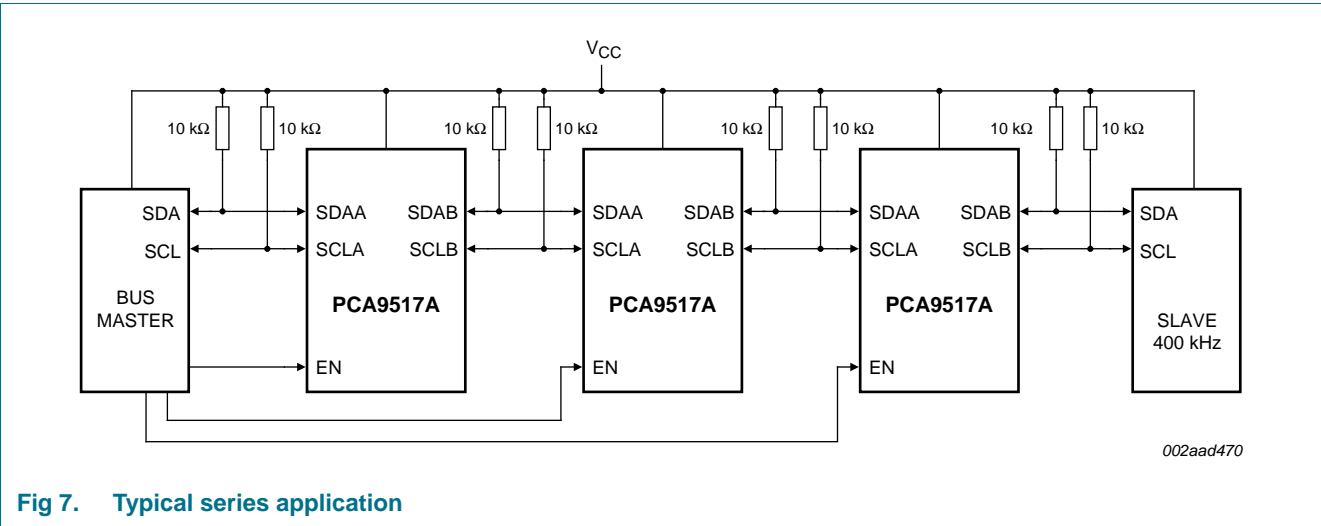


Fig 7.    Typical series application

**Remark:** Figure 9 and Figure 10 reference Figure 8 and assume master on Bus B side and slave on Bus A side.

**Fig 8.    Typical application of PCA9517A driving a short cable**



**Fig 9.    Bus A (0.9 V to 5.5 V bus) waveform**



**Fig 10.   Bus B (2.7 V to 5.5 V) waveform**
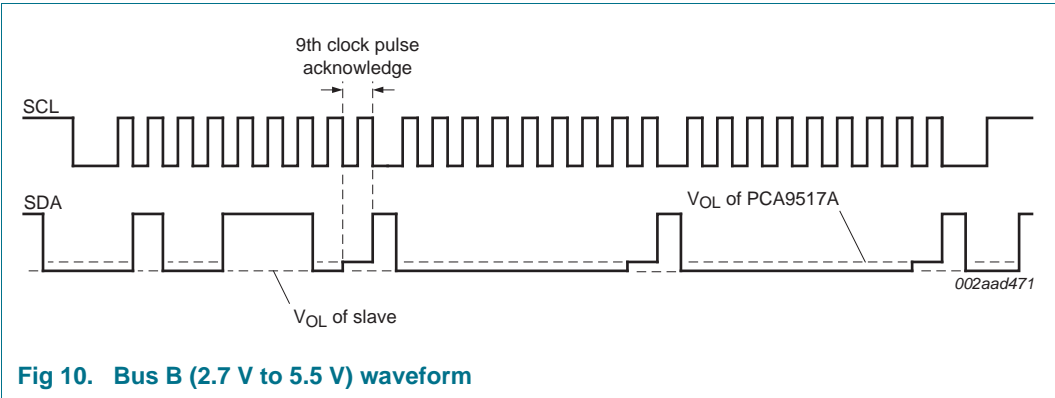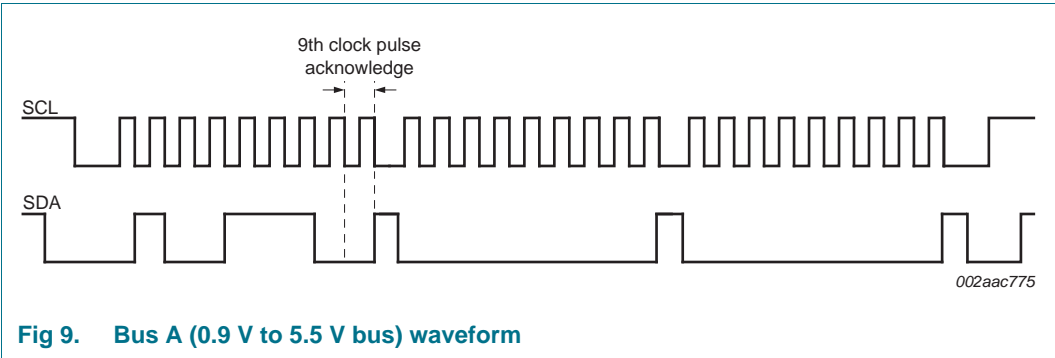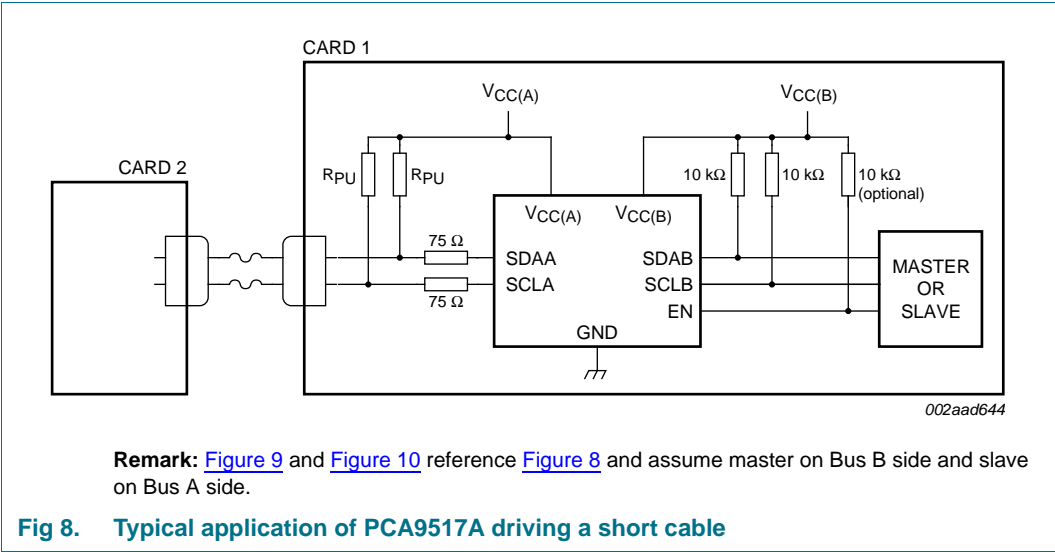
## 8. Limiting values

**Table 4.    Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(B)}$ | supply voltage port B | 2.7 V to 5.5 V | | −0.5 | +7 | V |
| $V_{CC(A)}$ | supply voltage port A | adjustable | | −0.5 | +7 | V |
| $V_{I/O}$ | voltage on an input/output pin | port A and port B; enable pin (EN) | | −0.5 | +7 | V |
| $I_{I/O}$ | input/output current | port A; port B | | - | 50 | mA |
| $I_I$ | input current | EN, $V_{CC(A)}$, $V_{CC(B)}$, GND | | - | 50 | mA |
| $P_{tot}$ | total power dissipation | | | - | 100 | mW |
| $T_{stg}$ | storage temperature | | | −55 | +125 | °C |
| $T_{amb}$ | ambient temperature | operating in free air | | −40 | +85 | °C |
| $T_j$ | junction temperature | | | - | +125 | °C |

## 9. Static characteristics

**Table 5.    Static characteristics**

$V_{CC}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{CC(B)}$ | supply voltage port B | | | 2.7 | - | 5.5 | V |
| $V_{CC(A)}$ | supply voltage port A | | [1] | 0.9 | - | 5.5 | V |
| $I_{CC(VCC(A))}$ | supply current on pin $V_{CC(A)}$ | | | - | - | 1 | mA |
| $I_{CCH}$ | HIGH-level supply current | both channels HIGH; $V_{CC}$ = 5.5 V; SDAn = SCLn = $V_{CC}$ | | - | 1.5 | 5 | mA |
| $I_{CCL}$ | LOW-level supply current | both channels LOW; $V_{CC}$ = 5.5 V; one SDA and one SCL = GND; other SDA and SCL open | | - | 1.5 | 5 | mA |
| $I_{CC(A)c}$ | contention port A supply current | $V_{CC}$ = 5.5 V; SDAn = SCLn = $V_{CC}$ | | - | 1.5 | 5 | mA |
| **Input and output SDAB and SCLB** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{CC(B)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | [2] | −0.5 | - | $+0.3V_{CC(B)}$ | V |
| $V_{ILc}$ | contention LOW-level input voltage | | | −0.5 | 0.4 | - | V |
| $V_{IK}$ | input clamping voltage | $I_I$ = −18 mA | | - | - | −1.2 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 3.6 V | | - | - | ±1 | μA |
| $I_{IL}$ | LOW-level input current | SDA, SCL; $V_I$ = 0.2 V | | - | - | 10 | μA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 100 μA or 6 mA | | 0.47 | 0.52 | 0.6 | V |
| $V_{OL}$–$V_{ILc}$ | difference between LOW-level output and LOW-level input voltage contention | guaranteed by design | | - | - | 70 | mV |
| $I_{LOH}$ | HIGH-level output leakage current | $V_O$ = 3.6 V | | - | - | 10 | μA |
| $C_{io}$ | input/output capacitance | $V_I$ = 3 V or 0 V; $V_{CC}$ = 3.3 V | | - | 6 | 7 | pF |
| | | $V_I$ = 3 V or 0 V; $V_{CC}$ = 0 V | | - | 6 | 7 | pF |
| **Input and output SDAA and SCLA** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{CC(A)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | [3] | −0.5 | - | $+0.3V_{CC(A)}$ | V |
| $V_{IK}$ | input clamping voltage | $I_I$ = −18 mA | | - | - | −1.2 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 3.6 V | | - | - | ±1 | μA |
| $I_{IL}$ | LOW-level input current | SDA, SCL; $V_I$ = 0.2 V | | - | - | 10 | μA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 6 mA | | - | 0.1 | 0.2 | V |
| $I_{LOH}$ | HIGH-level output leakage current | $V_O$ = 3.6 V | | - | - | 10 | μA |
| $C_{io}$ | input/output capacitance | $V_I$ = 3 V or 0 V; $V_{CC}$ = 3.3 V | | - | 6 | 7 | pF |
| | | $V_I$ = 3 V or 0 V; $V_{CC}$ = 0 V | | - | 6 | 7 | pF |

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**Table 5.     Static characteristics** *…continued*

*$V_{CC}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = −40 ℃ to +85 ℃; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Enable** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | −0.5 | - | +0.3$V_{CC(B)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{CC(B)}$ | - | 5.5 | V |
| $I_{IL(EN)}$ | LOW-level input current on pin EN | $V_I$ = 0.2 V, EN; $V_{CC}$ = 3.6 V | | - | −10 | −30 | µA |
| $I_{LI}$ | input leakage current | | | −1 | - | +1 | µA |
| $C_i$ | input capacitance | $V_I$ = 3.0 V or 0 V | | - | 6 | 7 | pF |

[1]   LOW-level supply voltage.

[2]   $V_{IL}$ specification is for the first LOW level seen by the SDAB/SCLB lines. $V_{ILc}$ is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.

[3]   $V_{IL}$ for port A with envelope noise must be below 0.3$V_{CC(A)}$ for stable performance.

# 10. Dynamic characteristics

**Table 6.     Dynamic characteristics**

*$V_{CC}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = −40 ℃ to +85 ℃; unless otherwise specified.[1][2]*

| Symbol | Parameter | Conditions | | Min | Typ[3] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW to HIGH propagation delay | port B to port A; Figure 13 | [4] | 100 | 170 | 250 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | port B to port A; Figure 11 | | | | | |
| | | $V_{CC(A)}$ ≤ 2.7 V | [5] | 30 | 80 | 110 | ns |
| | | $V_{CC(A)}$ ≥ 3 V | | 10 | 66 | 300 | ns |
| $t_{TLH}$ | LOW to HIGH output transition time | port A; Figure 11 | | 10 | 20 | 30 | ns |
| $t_{THL}$ | HIGH to LOW output transition time | port A; Figure 11 | | | | | |
| | | $V_{CC(A)}$ ≤ 2.7 V | [5] | 1 | 77 | 105 | ns |
| | | $V_{CC(A)}$ ≥ 3 V | | 20 | 70 | 175 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | port A to port B; Figure 12 | [6] | 25 | 53 | 110 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | port A to port B; Figure 12 | [6] | 60 | 79 | 230 | ns |
| $t_{TLH}$ | LOW to HIGH output transition time | port B; Figure 12 | | 120 | 140 | 170 | ns |
| $t_{THL}$ | HIGH to LOW output transition time | port B; Figure 12 | | 30 | 48 | 90 | ns |
| $t_{su}$ | set-up time | EN HIGH before START condition | [7] | 100 | - | - | ns |
| $t_h$ | hold time | EN HIGH after STOP condition | [7] | 100 | - | - | ns |

[1]   Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on port B, and 167 Ω pull-up resistance and 57 pF load capacitance on port A. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

[2]   Pull-up voltages are $V_{CC(A)}$ on port A and $V_{CC(B)}$ on port B.

[3]   Typical values were measured with $V_{CC(A)}$ = 3.3 V at $T_{amb}$ = 25 °C, unless otherwise noted.

[4]   The $t_{PLH}$ delay data from port B to port A is measured at 0.5 V on port B to 0.5$V_{CC(A)}$ on port A when $V_{CC(A)}$ is less than 2 V, and 1.5 V on port A if $V_{CC(A)}$ is greater than 2 V.

[5]   Typical value measured with $V_{CC(A)}$ = 2.7 V at $T_{amb}$ = 25 °C.

[6]   The proportional delay data from port A to port B is measured at 0.3$V_{CC(A)}$ on port A to 1.5 V on port B.

[7]   The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.
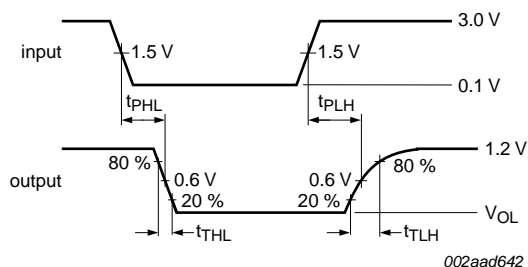
### 10.1 AC waveforms



**Fig 11.** Propagation delay and transition times; port B to port A
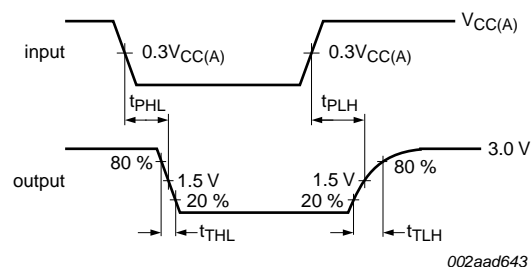


**Fig 12.** Propagation delay and transition times; port A to port B
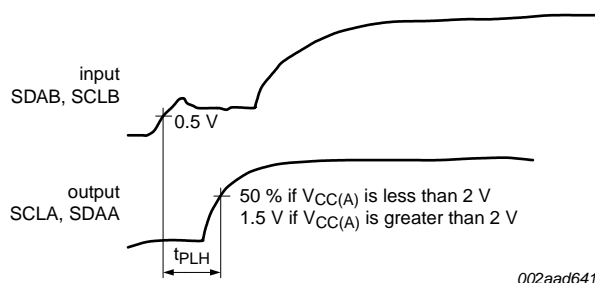


**Fig 13.** Propagation delay

## 11. Test information
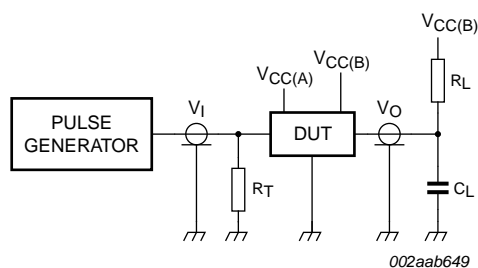


$R_L$ = load resistor; 1.35 kΩ on port B; 167 Ω on port A (0.9 V to 2.7 V) and 450 Ω on port A (3.0 V to 5.5 V).

$C_L$ = load capacitance includes jig and probe capacitance; 57 pF

$R_T$ = termination resistance should be equal to $Z_o$ of pulse generators

**Fig 14.** Test circuit for open-drain outputs

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## 12. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm**      **SOT96-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D[1] | E[2] | e | H_E | L | Lₚ | Q | v | w | y | Z[1] | θ |
|------|--------|-----|-----|-----|-----|-----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|
| mm | 1.75 | 0.25 / 0.10 | 1.45 / 1.25 | 0.25 | 0.49 / 0.36 | 0.25 / 0.19 | 5.0 / 4.8 | 4.0 / 3.8 | 1.27 | 6.2 / 5.8 | 1.05 | 1.0 / 0.4 | 0.7 / 0.6 | 0.25 | 0.25 | 0.1 | 0.7 / 0.3 | 8° / 0° |
| inches | 0.069 | 0.010 / 0.004 | 0.057 / 0.049 | 0.01 | 0.019 / 0.014 | 0.0100 / 0.0075 | 0.20 / 0.19 | 0.16 / 0.15 | 0.05 | 0.244 / 0.228 | 0.041 | 0.039 / 0.016 | 0.028 / 0.024 | 0.01 | 0.01 | 0.004 | 0.028 / 0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

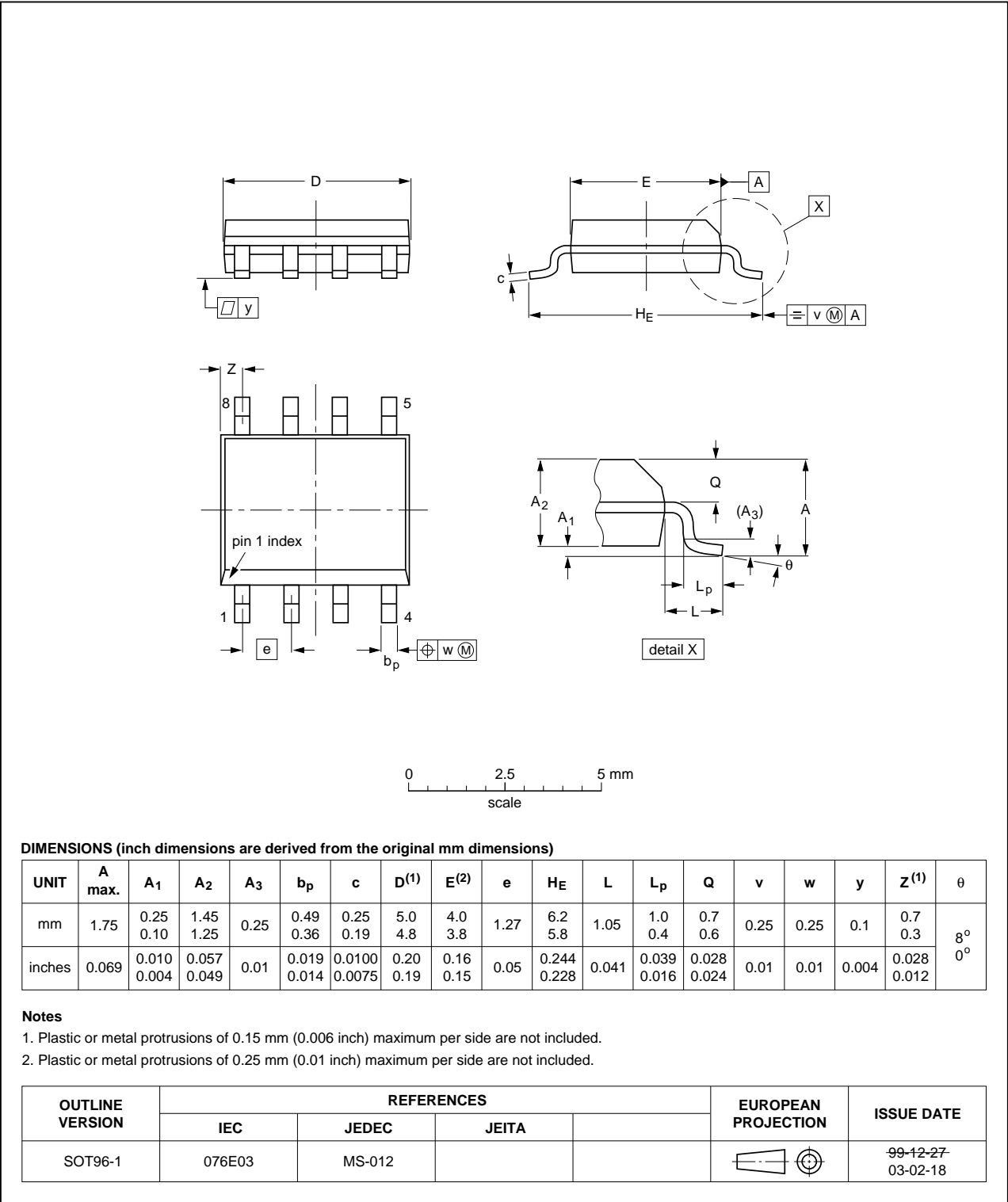| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|------|------|------|------|------|------|------|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~ 03-02-18 |

**Fig 15. Package outline SOT96-1 (SO8)**

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**



detail X

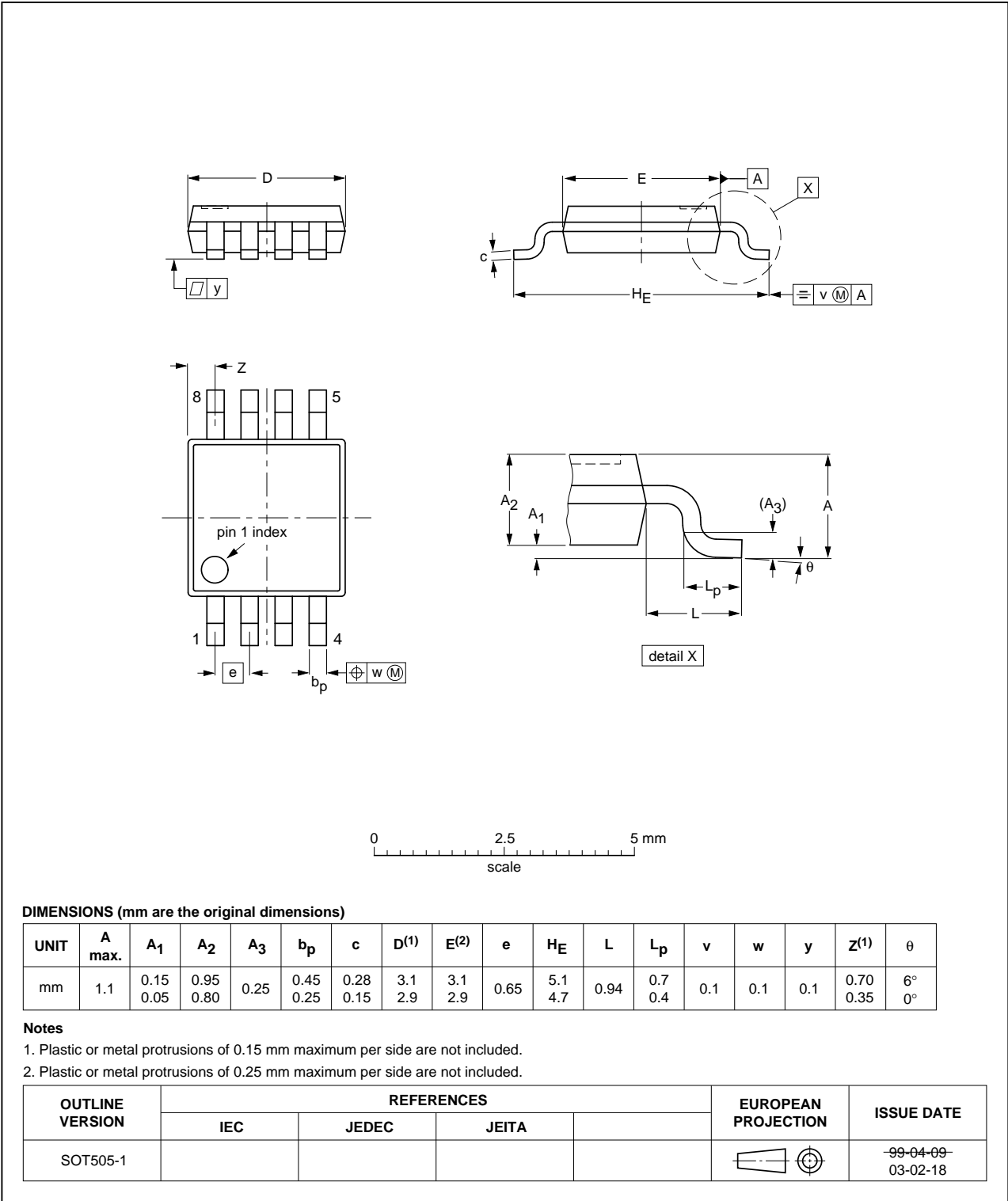0          2.5          5 mm

scale

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D(1) | E(2) | e | H_E | L | L_p | v | w | y | Z(1) | θ |
|------|--------|-----|-----|-----|-----|-----|------|------|-----|-----|-----|-----|-----|-----|-----|------|-----|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.45 0.25 | 0.28 0.15 | 3.1 2.9 | 3.1 2.9 | 0.65 | 5.1 4.7 | 0.94 | 0.7 0.4 | 0.1 | 0.1 | 0.1 | 0.70 0.35 | 6° 0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~ 03-02-18 |

**Fig 16.  Package outline SOT505-1 (TSSOP8)**

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HWSON8: plastic thermal enhanced very very thin small outline package; no leads;
8 terminals; body 2 x 3 x 0.75 mm

SOT1069-2



Dimensions

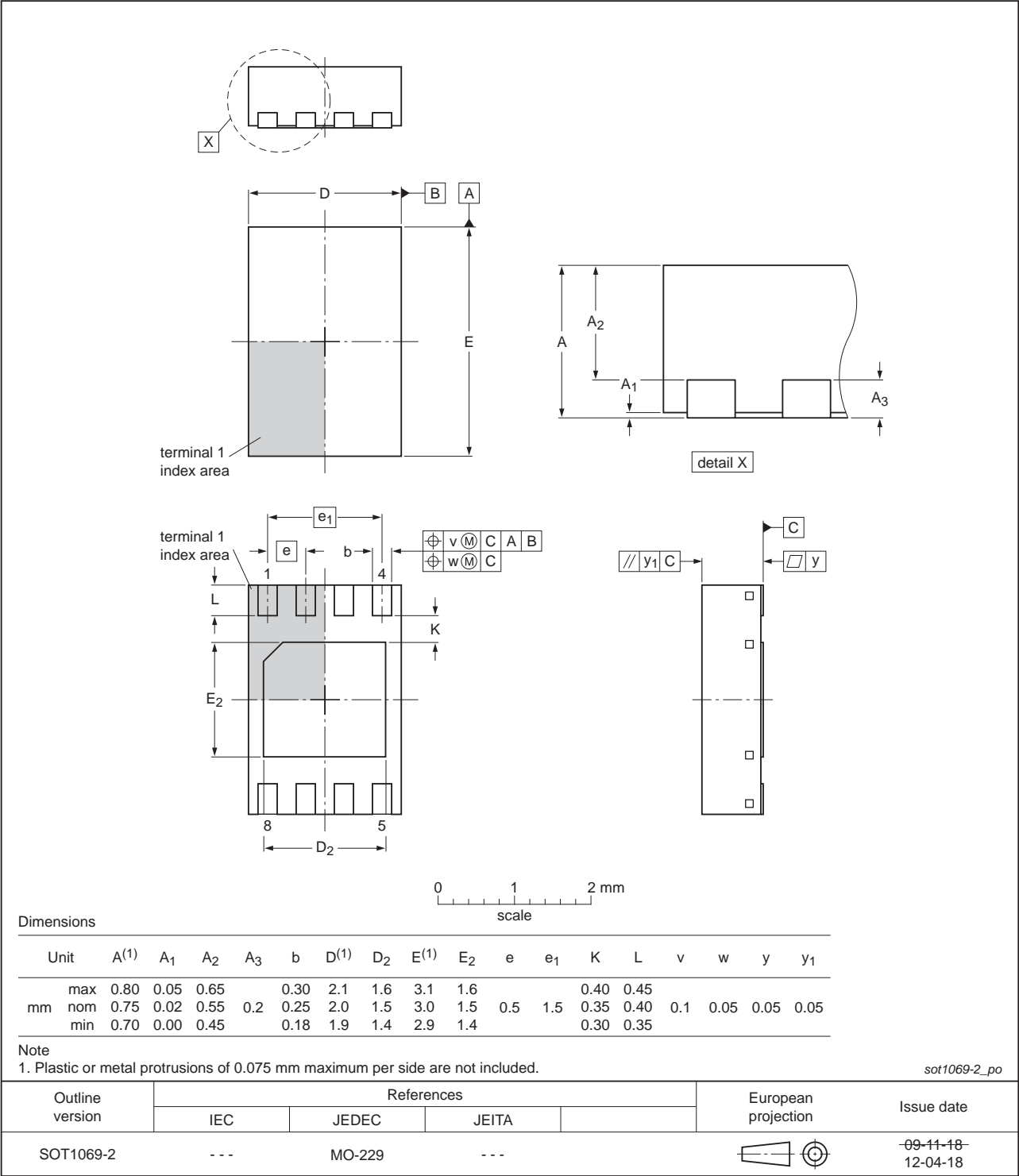| Unit | $A^{(1)}$ | $A_1$ | $A_2$ | $A_3$ | b | $D^{(1)}$ | $D_2$ | $E^{(1)}$ | $E_2$ | e | $e_1$ | K | L | v | w | y | $y_1$ |
|------|-----|-----|-----|-----|---|-----|-----|-----|-----|---|-----|---|---|---|---|---|----|
| | max 0.80 | 0.05 | 0.65 | | 0.30 | 2.1 | 1.6 | 3.1 | 1.6 | | | 0.40 | 0.45 | | | | |
| mm | nom 0.75 | 0.02 | 0.55 | 0.2 | 0.25 | 2.0 | 1.5 | 3.0 | 1.5 | 0.5 | 1.5 | 0.35 | 0.40 | 0.1 | 0.05 | 0.05 | 0.05 |
| | min 0.70 | 0.00 | 0.45 | | 0.18 | 1.9 | 1.4 | 2.9 | 1.4 | | | 0.30 | 0.35 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1069-2_po

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1069-2 | - - - | MO-229 | - - - | | | ~~09-11-18~~ 12-04-18 |

**Fig 17. Package outline SOT1069-2 (HWSON8)**

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## 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description".*

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

**Table 7.    SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
| --- | --- | --- |
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 8.    Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
| --- | --- | --- | --- |
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.

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MSL: Moisture Sensitivity Level

**Fig 18.   Temperature profiles for large and small components**
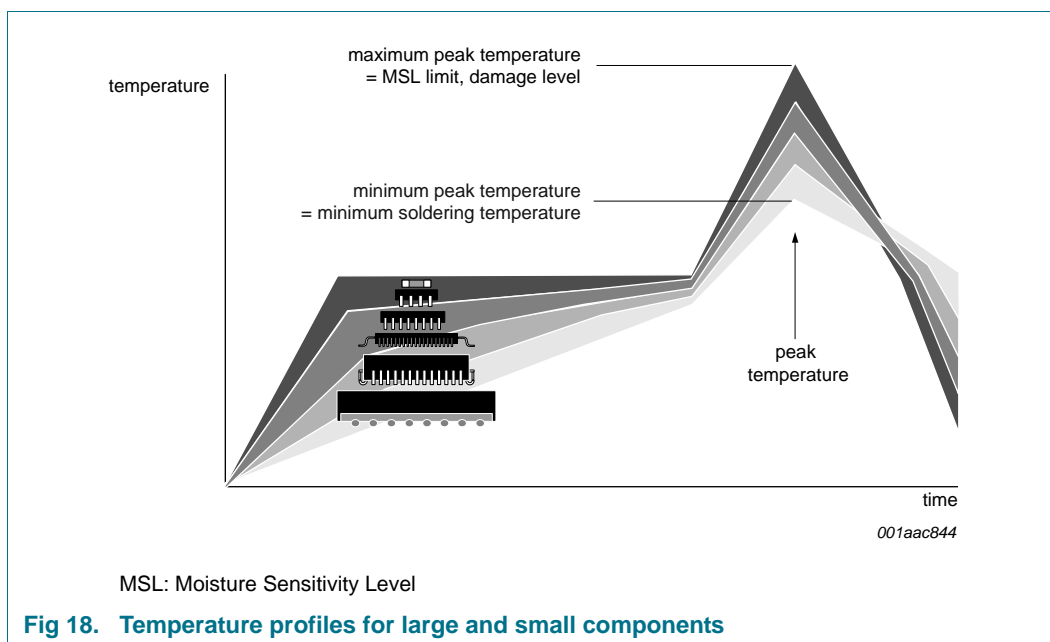
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

# 14. Abbreviations

**Table 9.      Abbreviations**

| Acronym | Description |
|---------|-------------|
| BOM | Bill Of Materials |
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| EOL | End Of Life |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I²C-bus | Inter Integrated Circuit bus |
| I/O | Input/Output |
| RC | Resistor-Capacitor network |
| SMBus | System Management Bus |

## 15. Revision history

**Table 10.    Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9517A v.4.1 | 20160524 | Product data sheet | - | PCA9517A v.4 |
| Modifications: | • Corrected the text in Section 6 "Functional description" on page 4: "When port B falls first and goes below $0.3V_{CC(B)}$" to "When port B falls first and goes below 0.4 V"; "The port B pull-down" to "The port A pull-down"; removed sentence "If the port B low voltage does not go below 0.5 V...." | | | |
| PCA9517A v.4 | 20120509 | Product data sheet | - | PCA9517A v.3 |
| Modifications: | • Table 1 "PCA9517 and PCA9517A comparison": <br> – Table note [1] is rewritten <br> – Table note [2] is rewritten <br> • Table 2 "Ordering information" <br> – Added type number PCA9517ADP/DG <br> – Added Table note [2] <br> • Figure 3 "Pin configuration for TSSOP8 (MSOP8)": added type number PCA9517ADP/DG | | | |
| PCA9517A v.3 | 20120229 | Product data sheet | - | PCA9517A v.2 |
| PCA9517A v.2 | 20080505 | Product data sheet | - | PCA9517A v.1 |
| PCA9517A v.1 | 20080222 | Product data sheet | - | - |

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# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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