CY3677

Evaluation Kit User Guide

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Safety Information

The CY3677 Evaluation Kit is intended for use as an evaluation platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure, so the board may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Also, this board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

	The CY3677 Evaluation Kit contains electrostatic discharge (ESD)-sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY3677 Evaluation Kit boards in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

The CY3677 Evaluation Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide the board over any surface.

Certification Disclaimer

This kit is intended for demonstration, evaluation, or development purposes only and is not considered by Cypress Semiconductor to be a finished end-product fit for general consumer use. It generates and can radiate radio frequency energy and has not been specifically tested for CE certification compliance. Operation of this equipment in other environments may cause interference with radio communications, in which case users at their own expense will be required to take whatever measures may be required to correct this interference.

1 Introduction

Thank you for your interest in the CY3677 Evaluation Kit (EVK). The CY3677 EVK is designed to enable you to evaluate the programmable clock device CY29430, the latest addition to the Cypress timing product portfolio. The clock device CY29430 is a high-performance programmable oscillator with one fractional PLL that generates any frequency up to 2.1 GHz with jitter as low as 110 fs. The device offers one differential output and one single-ended output. The device can be configured to generate either a single-ended output or a differential output but not both simultaneously. The device comes in a 16-pin QFN package for industrial applications. The differential I/O standards supported are LVDS, LVPECL, High-Speed Current Steering Logic (HCSL), and Current Mode Logic (CML). The single-ended signal supported is LVCMOS. The device also supports features such as a Voltage-Controlled Crystal Oscillator (VCXO), and provides the user with an I^2C programming interface. The device supports four frequency profiles, which can be switched dynamically using external Frequency Select (FS0 and FS1) signals. There are two jumpers provided on the EVK to perform frequency selection on the board.

The CY3677 EVK allows you to evaluate output clock signals by making required on-board termination settings.

The CY3677 EVK is available through the Cypress Online Store or through our distributors.

1.1 CY3677 EVK Contents

The CY3677 EVK includes the following:

- CY3677 Evaluation Board
- USB Standard-A to Mini-B cable
- Quick Start Guide

Figure 1-1. CY3677 Kit Contents

Inspect the contents of the kit. If you find any part missing, contact your nearest Cypress sales office for assistance: www.cypress.com/support.

1.2 Getting Started

To learn the solution quickly and apply it to your design, refer to the CY3677 Quick Start Guide inside the kit box or in the installation directory. The default location for the kit documents is:

```
<Install_Directory>\CY3677 Evaluation Kit\<version>\Documentation
```

This guide will help you get acquainted with the CY3677 EVK:

The Software Installation chapter describes the installation of the kit software.

The Kit Operation chapter describes the major features of the CY3677 Evaluation Kit.

The Hardware chapter describes the hardware content of the CY3677 Evaluation Kit and the hardware operation.

The Example Projects chapter describes the multiple projects that will help you understand how to evaluate different supported output standards on this kit.

The Appendix captures DC/AC Measurements of Clock Outputs, Schematics, Fab Drawing, and the bill of materials (BOM).

1.3 Additional Learning Resources

Visit www.cypress.com/CY3677 and www.cypress.com/HPO for additional learning resources including datasheets and application notes.

1.4 Technical Support

For assistance, go to www.cypress.com/support, or contact our customer support at +1(800) 541-4736 Ext. 2 (in the USA), or +1 (408) 943-2600 Ext. 2 (International).

1.5 Document Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ ...cd\icc\
Italics	Displays file names and reference documentation.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

1.6 Acronyms

Table 1-2. List of Acronyms used in this Document

Acronym	Definition
BOM	Bill of Materials
CML	Current Mode Logic
DNP, DNM	Do Not Populate, Do Not Mount
FS	Frequency Select
HCSL	High-Speed Current Steering Logic
I^2C	Inter-Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVPECL2	Low Voltage Positive Emitter Coupled Logic with zero Common-mode current
LVDS	Low Voltage Differential Signaling
OE	Output Enable
OT3	Third Overtone Crystal
SMA	Subminiature Version A
VCXO	Voltage-Controlled Crystal Oscillator
TCXO	Temperature Compensated Crystal Oscillator
OTP	One-Time Programmable

2 Software Installation

This chapter describes the steps to install the software tools and packages on a PC for using the CY3677 Evaluation Kit.

2.1 Before You Begin

All Cypress software installations require administrator privileges. Ensure that you have the required privileges on the system for successful installation. Before you install the kit software, close any other Cypress software that is currently running.

2.2 Install Software

Follow these steps to install the CY3677 Evaluation Kit software:

1. Download the CY3677 Evaluation Kit software from www.cypress.com/CY3677. The software is available in the following formats:
   a. **CY3677 Evaluation Kit Complete Setup:** This installation package contains the files related to the CY3677 Evaluation Kit. However, it does not include the Windows Installer or Microsoft .NET Framework packages. If these packages are not available on your computer, the installer directs you to download and install them from the Internet.
   b. **CY3677 Evaluation Kit Only:** This executable file installs only the CY3677 EVK contents, which include example projects, hardware files, and user documents. This package can be used if all the software prerequisites are installed on your PC.
   c. **CY3677 Evaluation Kit ISO:** This file is a complete package, stored in a CD/DVD-ROM image format that you can use to create a CD/DVD or extract using an ISO extraction program such as WinZip or WinRAR. The file can also be mounted similar to a virtual CD/DVD using virtual drive programs such as Virtual CloneDrive and MagicISO. This file includes all the required software, utilities, drivers, hardware files, and user documents.
2. If you have downloaded the ISO file, mount it on a virtual drive. If you do not have a virtual drive to mount, extract the ISO contents using the appropriate ISO extractor (such as MagicISO or PowerISO). Double-click *cyautorun.exe* in the root directory of the extracted content or the mounted ISO if the “Autorun from CD/DVD” option is not enabled on the PC. The installation window will appear automatically.

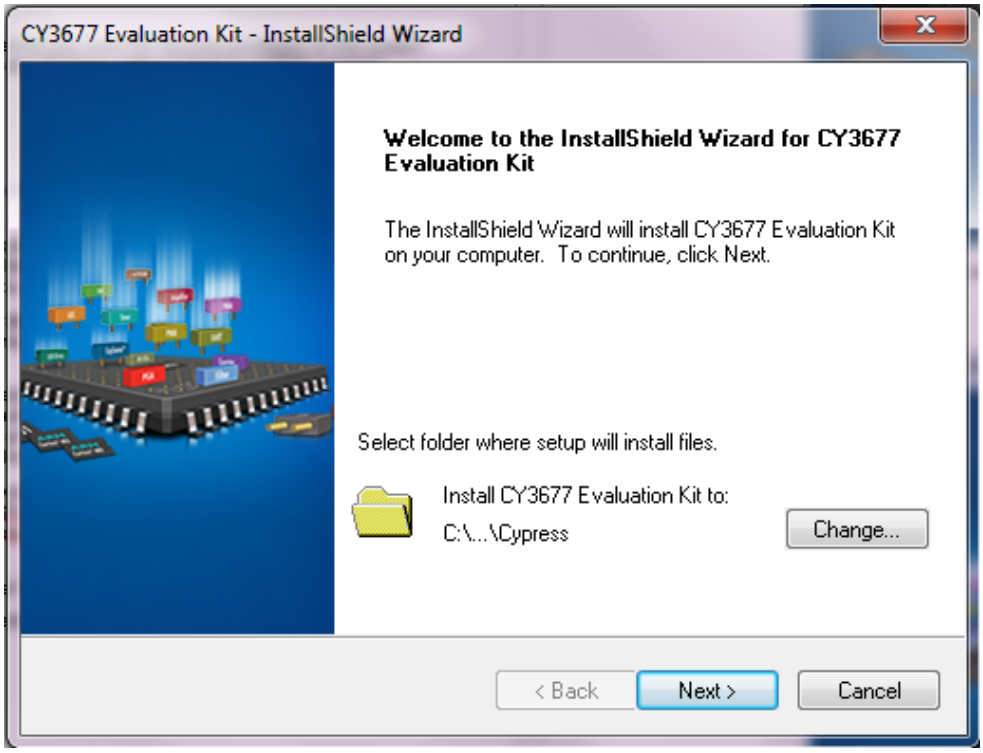
   Note: If you are using the “Kit Complete Setup” or “Kit Only” file, then go to step 4 for installation.
3. Click **Install CY3677 EVK** to start the installation as shown in Figure 2-1.

Figure 2-1. Installer Screen

4. Click **Change…** if you want to install the CY3677 EVK in a location other than the default, and then click **Next** as shown in Figure 2-2.

   Note: When you click **Next**, the CY3677 EVK installer automatically installs the required software, if it is not present on your computer. The pre-requisites are ClockWizard 2.1 and PSoC Programmer 3.25.0 or later.

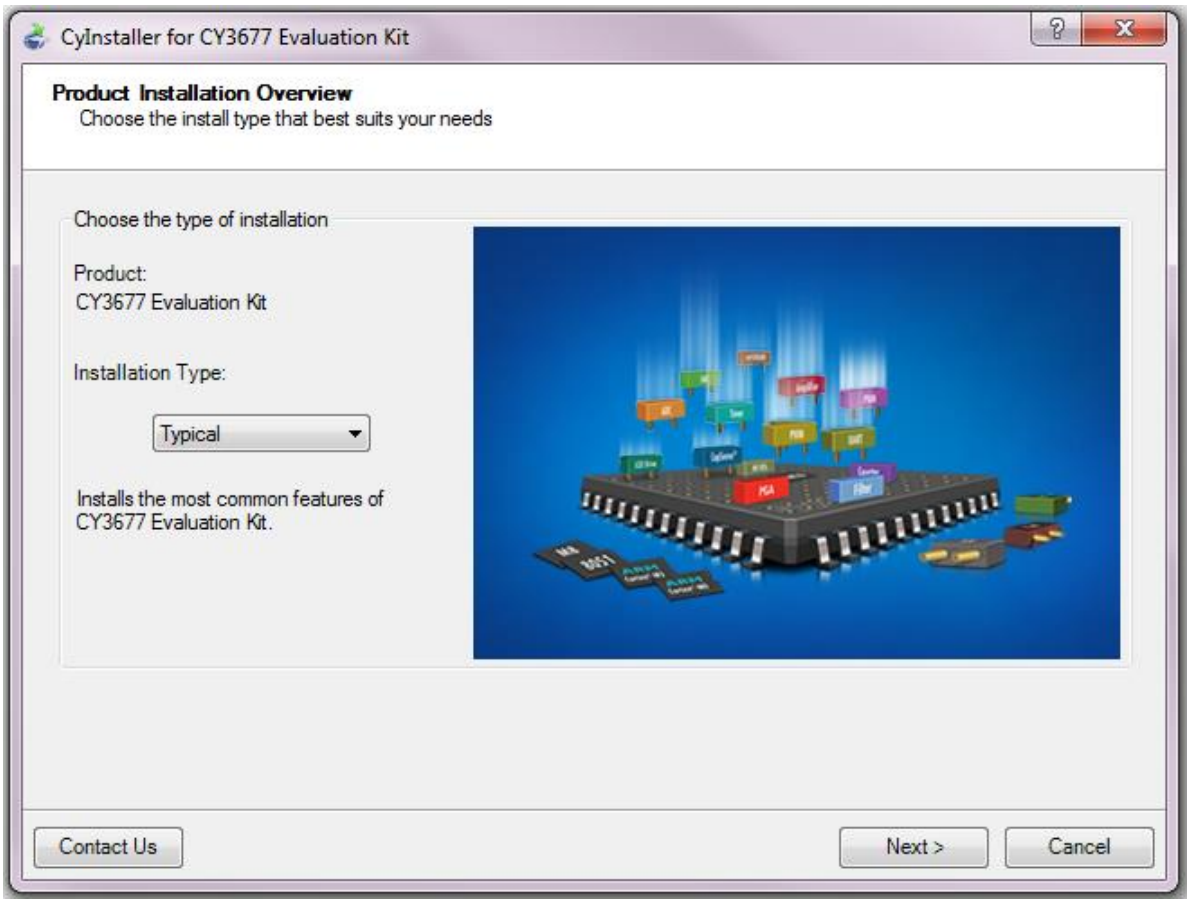
Figure 2-2. InstallShield Wizard



5. Select the **Installation Type** (see Figure 2-3). The drop-down menu contains three options: **Typical** (installs all the required features), **Custom** (lets you choose the features to be installed), and **Complete** (installs all the contents). Click **Next** after you select the Installation Type.

   Note: It is recommended that you choose the **Typical** Installation Type.

Figure 2-3. Product Installation Overview



6. Read and accept the End-User License Agreement, and then click **Next**.

   When the installation begins, a list of packages appears on the Installation page. A green check mark appears next to each package after successful installation.

7. Enter your contact information or select the **Continue Without Contact Information** check box.

8. Click **Finish** to complete the CY3677 Evaluation Kit installation.

   After the installation is complete, the kit contents are available at:

   `<Install_Directory>\CY3677 Evaluation Kit\<version>.`

   Default location:

   Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\CY3677 Evaluation Kit`

   Windows 7 (32-bit): `C:\Program Files\Cypress\CY3677 Evaluation Kit`

2.3 Install Hardware

No additional hardware installation is required for this kit.

2.4 Uninstall Software

You can uninstall the software using one of the following methods:

- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**, and select the specific software package. Click the **Uninstall** button.
- Go to **Start** > **Control Panel** > **Programs and Features**, and select the specific software package. Click the **Uninstall/Change** button.

3 Kit Operation

The CY3677 EVK can be used to evaluate the CY29430, a high performance programmable oscillator. Connect the CY3677 kit through USB to a PC running Cypress's ClockWizard 2.1 software. The clock device CY29430 can be configured and programmed to generate frequencies with best-in-class performance.

3.1 Theory of Operation

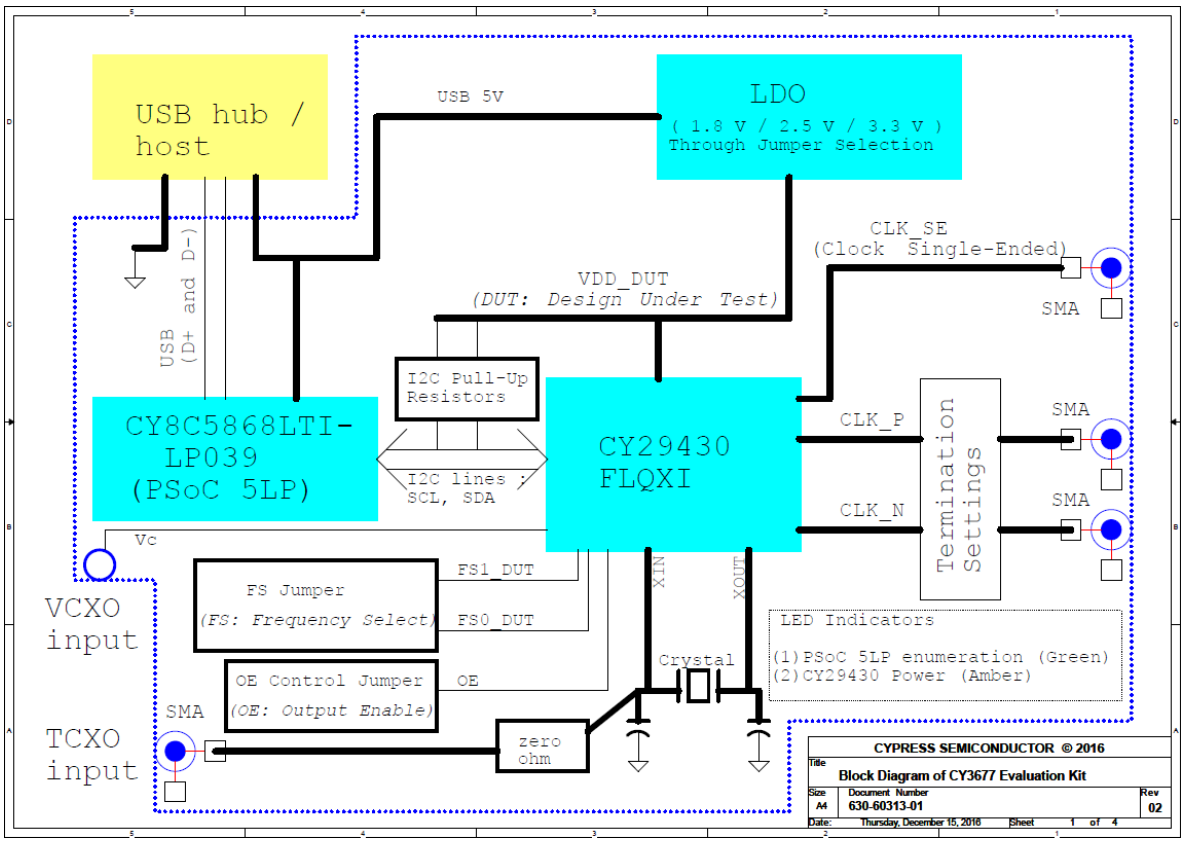
The CY3677 EVK offers one differential clock output and one single-ended clock output (only one operates at a time) for evaluation. The CY29430 device uses an on-board crystal or Temperature Compensated Crystal Oscillator (TCXO) reference input.

The kit is capable of generating fixed 3.3 V, 2.5 V, and 1.8 V voltages from a 5-V USB port. The on-board PSoC 5LP (U7) performs the USB-to-I^{2}C conversion. There is one power LED (LED2) driven from the on-board LDO supply and one status LED (LED1) controlled by PSoC 5LP. The output of LDO regulator (U8) is configurable (3.3 V, 2.5 V, or 1.8 V) through jumper J13.

Note: An additional on-board LDO (U9 – not shown in Figure 3-1) generates a fixed 3.3-V supply for the PSoC 5LP in the **CY3677 Rev **** EVK. This feature has been changed in **CY3677 Rev *A** EVK where the PSoC 5LP is directly powered by a 5-V USB supply. The CY3677 kit revision is printed on the label at the back of the kit box.

Figure 3-1 illustrates the block diagram of the CY3677 EVK.

Figure 3-1. CY3677 EVK Block Diagram

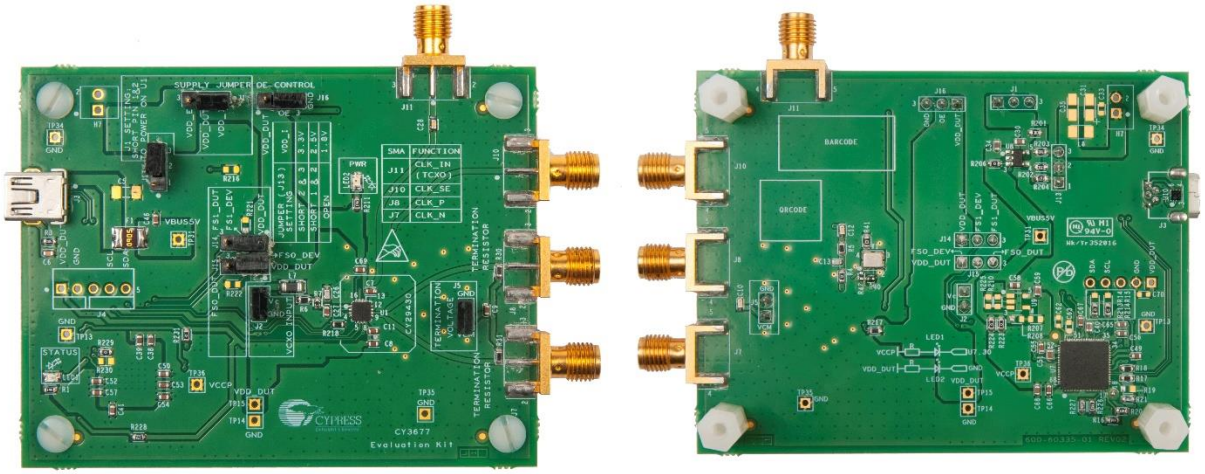


3.2 Functional Description

The differential clock outputs (J7, J8) and single-ended output (J10) are driven out on to SMA connectors. The EVK is populated with 50-Ω resistors (R30 and R31) for output termination. The termination options of the differential outputs on the evaluation board are listed in the Hardware chapter. These termination circuits are designed to terminate the output clocks in LVPECL, LVDS, HCSL, LVPECL2, and CML signal types by populating, or by not populating the J5 jumper shunt. The single-ended (LVCMOS) clock does not need any on-board termination settings.

Figure 3-2 illustrates the top view and bottom view of the CY3677 EVK.

Figure 3-2. CY3677 EVK (Top View, Bottom View)



CY3677 EVK Top View

CY3677 EVK Bottom View

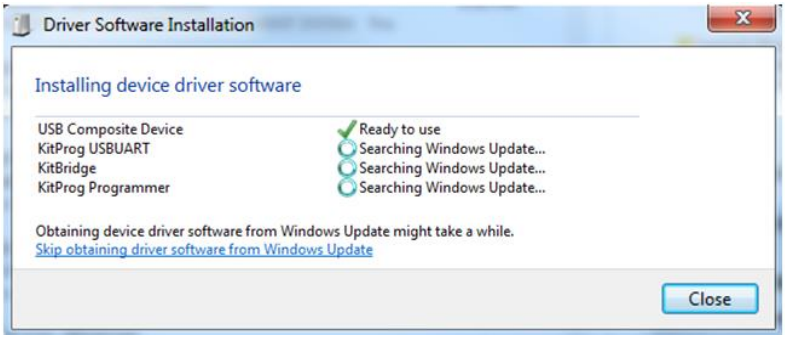
3.3 CY3677 EVK USB Connection

The CY29430 clock device on the kit is loaded with a default configuration. To view and evaluate other configurations on an oscilloscope (or other standard instruments), the clock device must be programmed with the desired configuration. The ClockWizard 2.1 application is required for programming any configuration. Therefore, the kit should be connected (see Figure 3-3) to a PC through a USB port for programming.

Figure 3-3. Kit Connected through USB

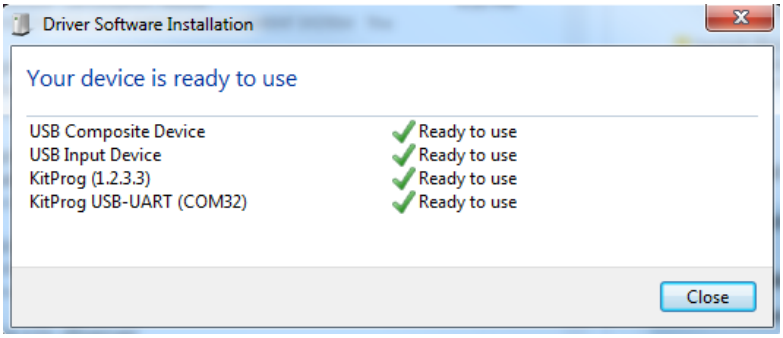
The kit enumerates as a USB Composite Device as part of the Driver Software installation on Windows.

Figure 3-4. USB Driver Installation



After the driver installation is complete, the device is ready to use.

Figure 3-5. USB Driver Installation Complete



3.4 Programming the CY29430

The CY29430 device has an internal one-time programmable (OTP) nonvolatile memory called eFuse. The device also contains volatile memory that stores an exact copy of the eFuse at the release of reset at power-up. The output frequency depends on the configurations in the volatile memory. Writing the entire device configuration in the volatile memory section of a blank device after power-up, is called Functional Programming. The CY3677 kit is shipped with a programmed CY29430 device. This program is written to a specific internal memory location of the device. This kit can be used to check both the Functional and eFuse Programming of the device using ClockWizard 2.1. See Functional Programming of the CY29430 and eFuse Programming of the CY29430 for details.

3.5 Functional Programming of the CY29430

ClockWizard 2.1 is used for functional programming of the CY29430. A configuration created in ClockWizard 2.1 can be downloaded to the volatile memory section of the device.

The example ClockWizard 2.1 projects can be found at the following location:

```
<Install_Directory>\CY3677 Evaluation Kit\<version>\Firmware\Example Projects
```

Configuration profiles generated from these projects can be used to evaluate the CY29430 device on the CY3677 EVK. Refer to Functional Programming for the kit's hardware settings prior to programming. It is recommended that you copy the example projects to another location if you want to make any modifications to the settings so that the default project is retained in the installation directory.

CAUTION	**Before programming the CY3677 EVK through ClockWizard 2.1, it is recommended to go through the Hardware section of this user guide. A mismatch between the hardware settings and the ClockWizard 2.1 configuration may cause potential damage of the EVK. Specifically, the voltage setting on the kit selected with J13 must match the voltage setting within the configuration to be programmed.**

3.5.1 Generating and Programming the Device Configuration Profile

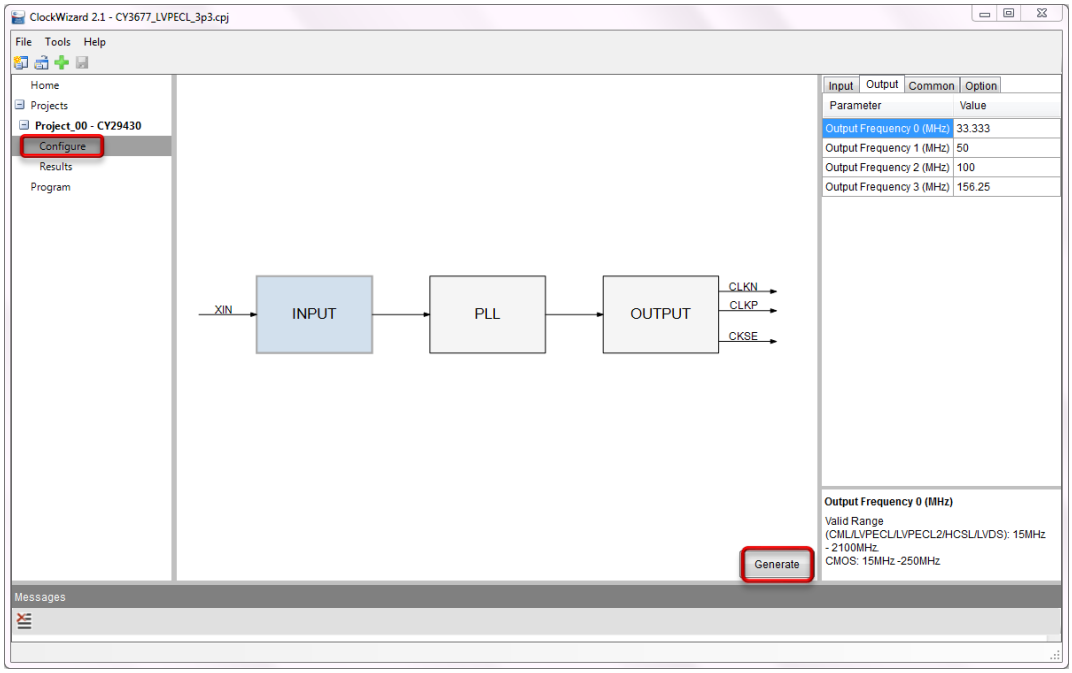
The ClockWizard 2.1 is used to generate profiles and to perform functional programming of the device.

1. Verify that the power supply voltage jumper (J13) is set for the voltage used in the project that you intend to program. See the Hardware section for details.
2. Connect the CY3677 EVK to your PC through the supplied USB cable.
3. To launch the ClockWizard 2.1 application, go to **Start** > **All Programs** > **Cypress** > **ClockWizard 2.1**.

   The workspace files are located in the Workspace folders. The four workspaces available are:

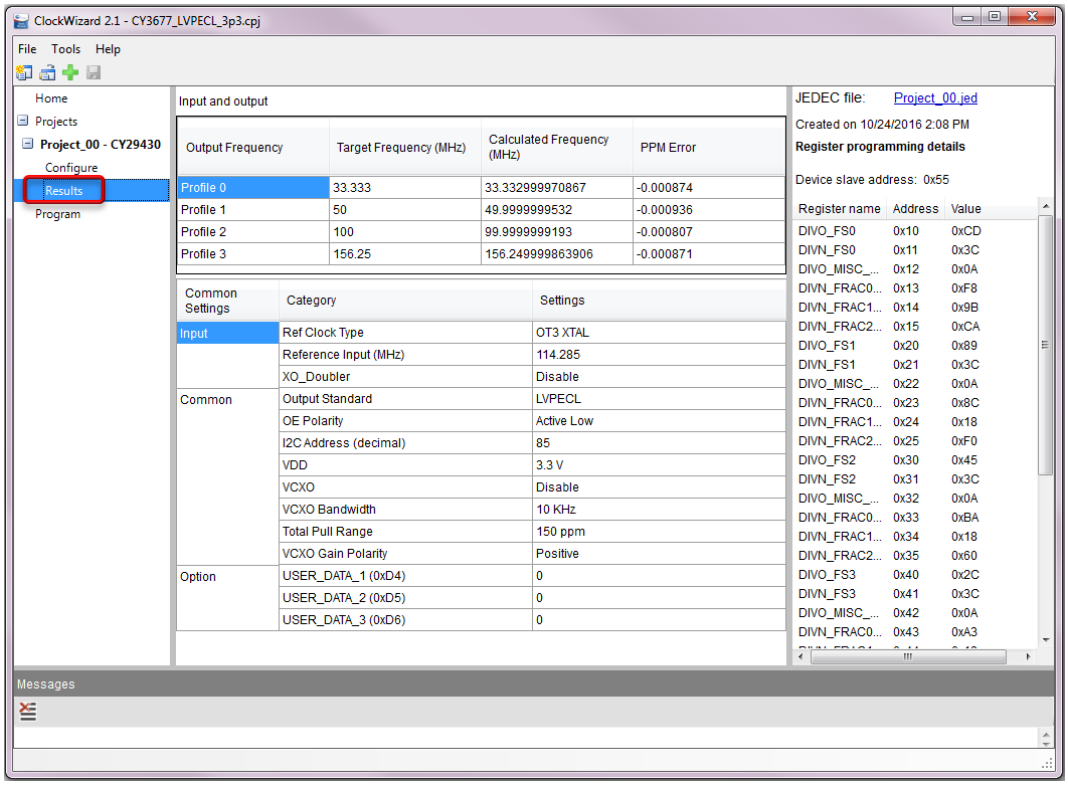
   - *CY3677_LVPECL_3p3.cpj*
   - *CY3677_LVDS_2p5.cpj*
   - *CY3677_HCSL_2p5.cpj*
   - *CY3677_LVCMOS_1p8.cpj*
4. Select the **File** menu in ClockWizard 2.1, select **Open workspace**, browse the required workspace file with a *.cpj* extension, and then click **Open**. Each Workspace file can contain multiple projects.
5. Click **Configure**, as shown in Figure 3-6. The various configuration parameters appear on the right panel of the block diagram in the tabbed interface. For more information on configuration parameters, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.
6. Click the **Generate** button (see Figure 3-6). This will generate the JEDEC file for the configuration selected. On completion of generation, the Results are displayed as shown in Figure 3-7.

Figure 3-6. Generating a Configuration Profile using ClockWizard 2.1



7. Click **Results** in the navigation pane to view the results at any time after a JEDEC file has been generated for a configuration, as shown in Figure 3-7.

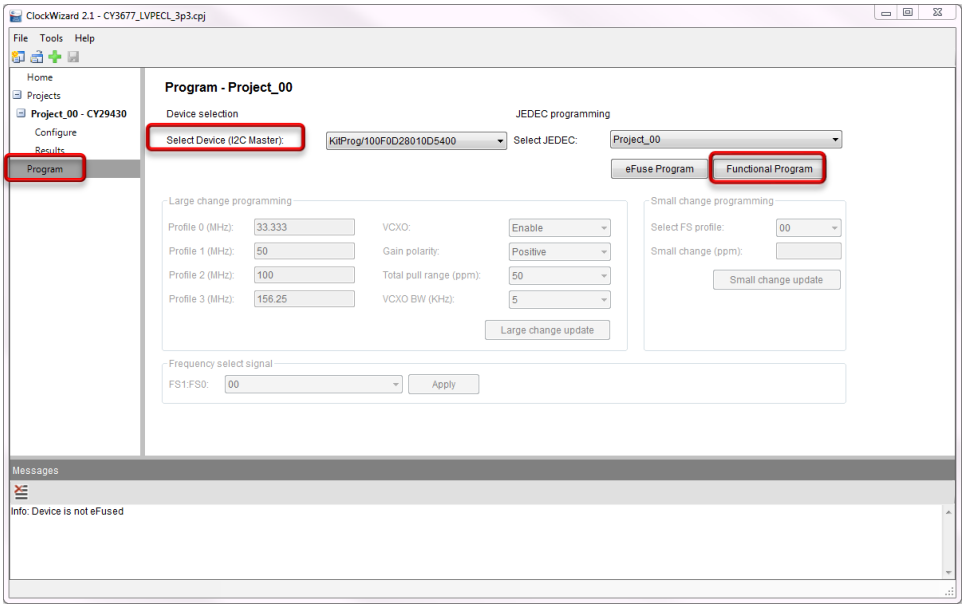
Figure 3-7. View Results Generated from the Configuration Profile using ClockWizard 2.1



8. To program the CY29430 device, select **Program** in the left navigation pane, as shown in Figure 3-8. Choose the appropriate device in the **Select Device (I2C Master)** drop-down list prior to programming, and then click the **Functional Program** button. This will program the device directly from ClockWizard. LED1 blinks to indicate that the device is being programmed. The required output will appear on the oscilloscope.

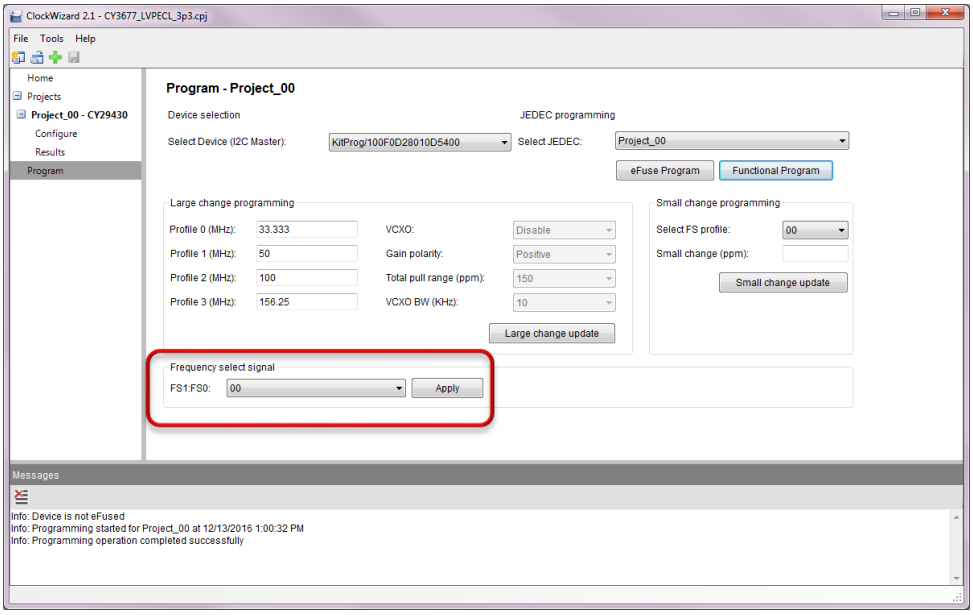
   For more information, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.

Figure 3-8. Programming Configuration Profile using ClockWizard 2.1



9. The CY29430 supports the selections of four frequency profiles for a single configuration. The Frequency Select inputs of the CY29430 device (FS0 and FS1) can either be controlled by ClockWizard 2.1 or they can be hard-coded using jumpers on the board. To allow selection of a frequency profile in ClockWizard 2.1, jumpers J14 and J15 must be set to positions 2 and 3. With the jumpers in those positions, you can select any of the four available profiles in ClockWizard 2.1 and click **Apply** (see Figure 3-9). Refer to the section Frequency Select (FS) for details on the hardware settings.

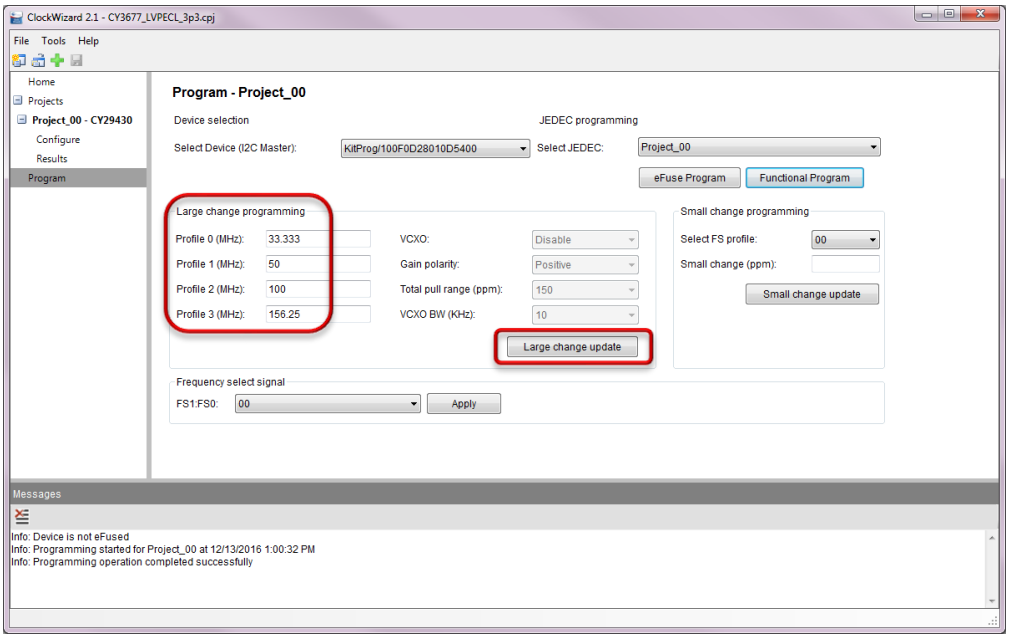
Figure 3-9. Frequency Select (FS) Operation of the CY29430 device through ClockWizard 2.1



10. After functional programming, the frequency values of the current *.cpj* are displayed in the following fields (see Figure 3-10): **Profile 0 (MHz)**, **Profile 1 (MHz)**, **Profile 2 (MHz)**, and **Profile 3 (MHz)**. You can change any of the frequencies in these fields. To make the changes effective, click **Large change update**. The expected output frequency will appear on the oscilloscope.

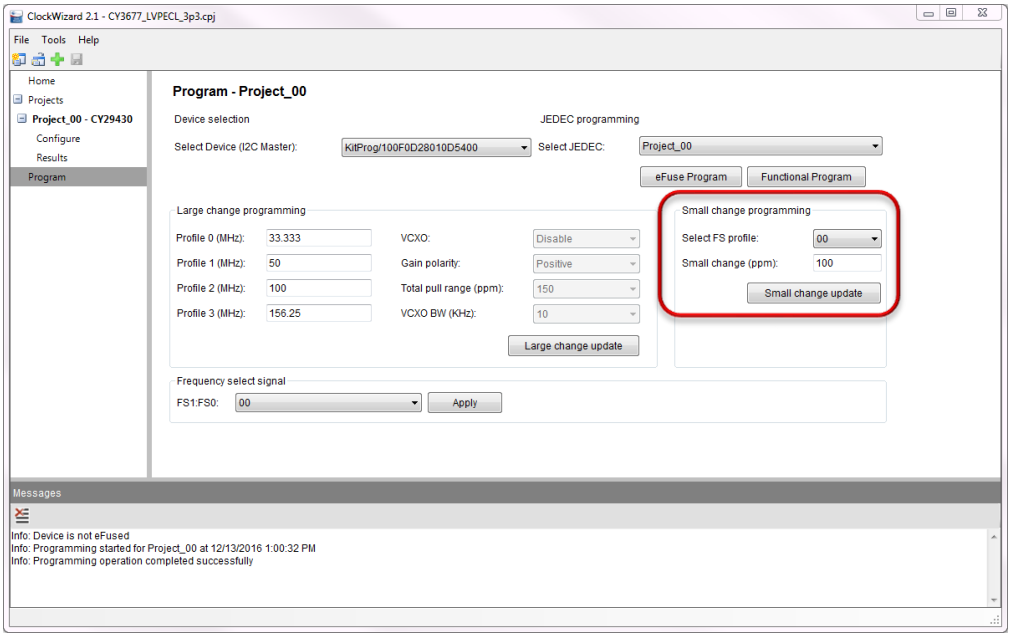
    Note: Large change programming refers to the case where the frequency is changing more than ± 500 ppm.

Figure 3-10. Evaluation of Other Frequencies through Large Change Update



11. If you want to change the frequency to less than ±500 ppm, fill in the desired ppm in the **Small change (ppm)** field, Select FS profile and click on **Small change update**. The settings are shown in Figure 3-11.

Figure 3-11. Evaluation of Other Frequencies through Small Change Update

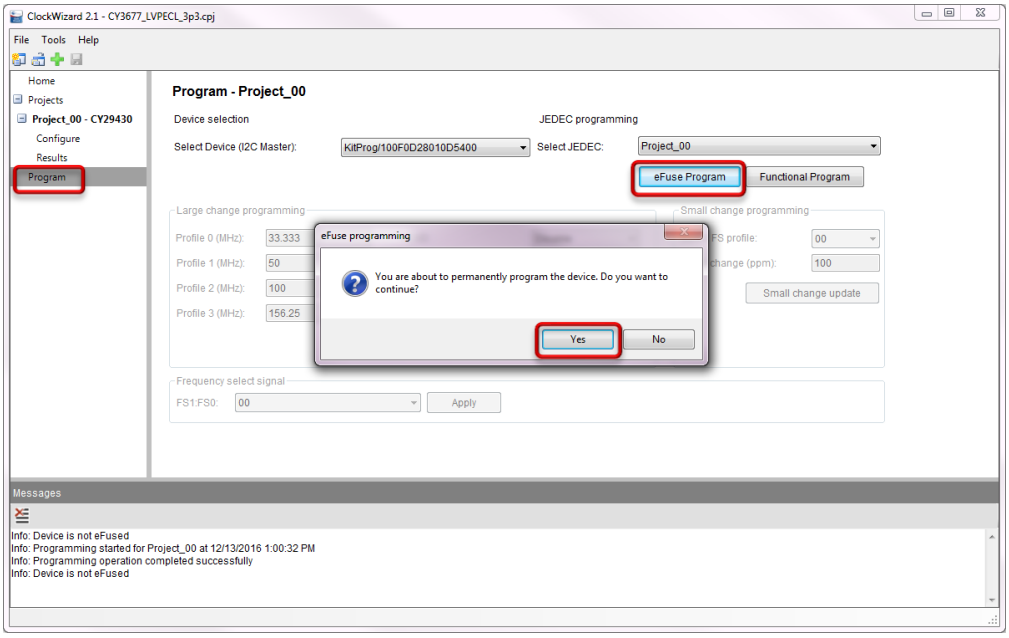


3.6 eFuse Programming of the CY29430

After functional programming and evaluation of different clock configurations, you may choose to write the configuration to the nonvolatile memory section of the device. The nonvolatile memory of the CY29430 is a one-time programmable (OTP) eFuse. Any configuration after functional evaluation can permanently be written to the eFuse of the device. See Figure 3-12 for the programming procedure.

Configure the device supply to 2.5 V before starting the eFuse programming. Table 4-2 provides the hardware configuration (J13 settings) of CY3677 for setting the device supply to 2.5 V.

Figure 3-12. eFuse Programming using ClockWizard 2.1



CAUTION

Evaluate the configuration via functional programming prior to writing a configuration to the eFuse. The configuration cannot be modified or erased once it is written to the eFuse.

The CY29430 supply must be set to 2.5 V for eFuse programming. Setting the CY29430 supply to any other voltage during eFuse programming will cause potential damage to the device.

After the device is eFuse-programmed, you can only change the output frequency through the following ways. Note that these changes will revert after a power cycle.

- Large change programming: This refers to the case where the frequency is changing more than ±500 ppm. Enter the desired frequencies in the **Profile 0 (MHz)**, **Profile 1 (MHz)**, **Profile 2 (MHz)**, and **Profile 3 (MHz)** fields, and click on **Large change update**. The device will recalibrate and reconfigure the internal circuit and the output will change to the desired frequencies.
- Small change programming: This refers to the case where the frequency is changing less than ±500 ppm. Select **FS profile**, enter the desired ppm in the **small change (ppm)**, and click on **Small change update**. The device will recalibrate and reconfigure the internal circuit and the output will change to the desired frequencies.

3.7 Custom Profile Generation

ClockWizard 2.1 should be used to generate custom configuration profiles. For details on how to create custom profiles, refer to the ClockWizard 2.1 User Guide located in **Help** > **User guide** of the ClockWizard 2.1 software.

To understand the output termination settings of different output standards (for example, LVPECL, HCSL, or LVDS), refer to the B.1. Termination Settings of Differential Clock Outputs section.

4 Hardware

4.1 Board Overview

The CY3677 EVK is used for evaluating the CY29430 device.

Following are the key features of the CY3677 EVK:

- Powered from a USB port
- Jumper to configure on-board LDO output
- Jumper to short or isolate external connection for termination settings

Figure 4-1 illustrates the CY3677 EVK board with a markup of the on-board components.

Figure 4-1. CY3677 EVK On-board Components

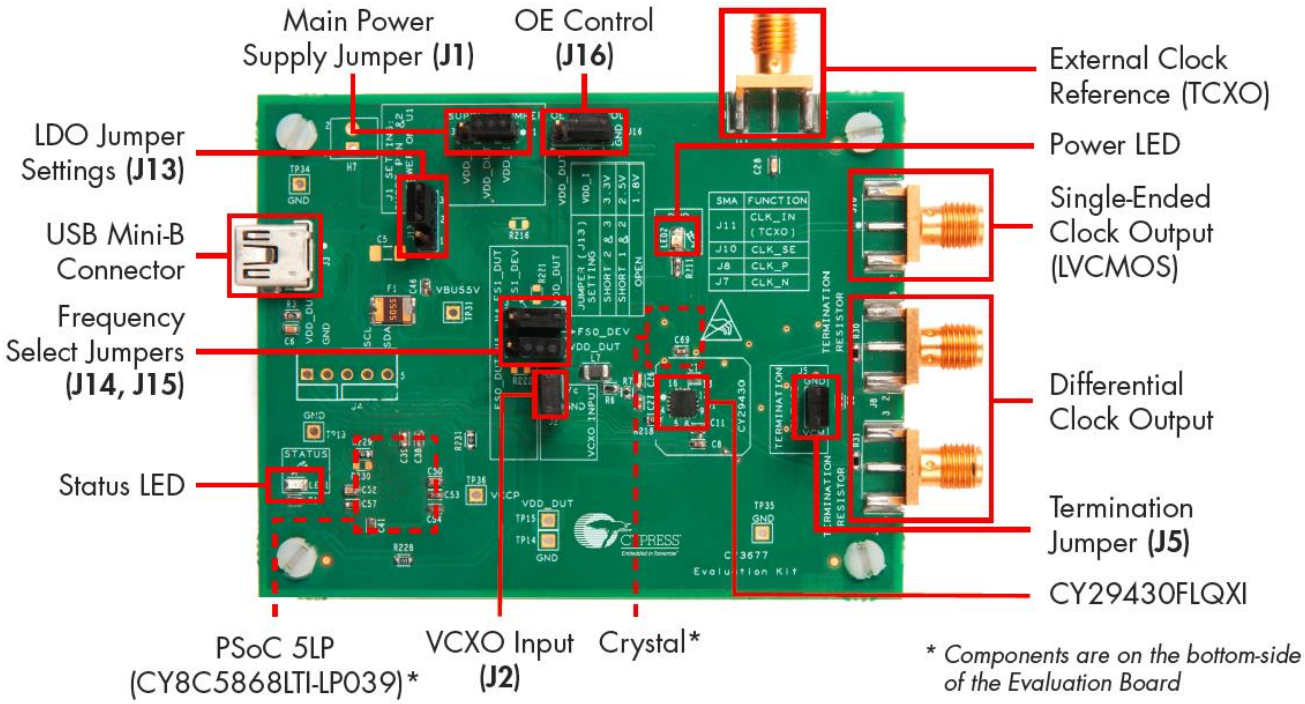


Table 4-1: CY3677 EVK Onboard Components Description

Label Name	Description
CY29430FLQXI	CY29430FLQXI is the Cypress clock chip that is evaluated with the CY3677 EVK.
Main Power Supply Jumper (J1)	Short pin 1 and 2 of jumper J1 to power up the CY29430. The core supply and I/O supply are shorted on the board, and hence are the same for the device.
LDO Settings Jumper (J13)	Set the J13 jumper per Table 4-2 to set the LDO output voltage. **Note:** The brightness of LED2 will vary depending on the voltage selection. It will be brightest at 3.3 V and dimmest at 1.8 V.
USB Mini-B Connector	Connect the kit to a PC using the USB Standard-A to Mini-B cable.
Differential Clock Output	Connect SMA cables to the SMA connectors (J7 and J8) on one end and to an oscilloscope on the other end.
Single-Ended Clock Output (LVCMOS)	Connect the SMA cable to the SMA connector (J10) on one end and to an oscilloscope on the other end.
External Clock Reference (TCXO)	Connect the SMA cable to the SMA connector (J11) on one end and to an external clock reference (TCXO) on the other end.
Termination Jumper (J5)	The board has an on-board jumper (J5) to connect and disconnect output termination.
Status LED	This LED (LED1) turns ON after the USB enumeration is completed. This LED blinks during programming of the CY29430 device from a PC.
Power LED	This LED (LED2) turns ON when the CY29430 device is powered.
OE Control (J16)	Jumper to set the OE input of the CY29430 to enable or disable the clock output.
Frequency Select Jumpers (J14, J15)	J14 and J15 are used to set the frequency select bits of CY29430.
Crystal	On-board 114.285 MHz OT3 crystal for the reference input of the CY29430 device. This crystal has frequency tolerance of ±20 ppm.
PSoC 5LP (CY8C5868LTI-LP039)	On-board PSoC 5LP device that converts the USB data-stream to I^2C format to program the CY29430 device.
VCXO Input (J2)	This jumper can be used to evaluate the VCXO operation of the CY29430 device. Vc (voltage at J2.1 pin) is by default set to 0 V via a jumper shunt. You can remove the shunt and instead apply an external power supply voltage (DC) to pin J2.1 to evaluate the VCXO operation. Cypress recommends that you contact our Technical Support team at www.cypress.com/support before connecting any external power supply to this jumper.

Table 4-2: J13 Jumper Settings

J13 Settings	LDO Output Voltage (Supply of CY29430)
Short pin 1 and 2	2.5 V
Short pin 2 and 3 (default)	3.3 V
Open	1.8 V

CAUTION	**The kit should strictly be operated from a USB supply by connecting to a PC.** **The PCB should not be powered by any external source. Application of an external power source to any of the jumper pins or test points may cause potential damage of the PCB.** **To configure the device to a clock standard other than those specified in the example projects, or to apply custom termination voltage, go to our support web page at www.cypress.com/support, or e-mail at: clocks@cypress.com.** **Incorrect application of supply or termination voltage will cause performance degradation of the clock output. Prolonged incorrect operation may permanently damage the kit.**

4.2 Board Details

4.2.1 Default Jumper Settings

The CY3677 EVK comes with default jumper settings that set the I/O and core supply voltages as 3.3 V. Table 4-3 lists the default jumper settings.

Table 4-3: Default Jumper Settings on the Kit

Jumper	Default Settings	Description
J1	Pin 1 and 2 are shorted	Power on CY29430.
J2	Pin 1 and 2 are shorted	VCXO input set to 0 V.
J5	Pin 1 and 2 are shorted	CY29430 output termination voltage set to 0 V through the 50-Ω termination resistors.
J13	Pin 2 and 3 are shorted	3.3 V selected for CY29430.
J14	Pin 1 and 2 are shorted	FS1 set to VDD_DUT (logic '1').
J15	Pin 1 and 2 are shorted	FS0 set to VDD_DUT (logic '1').
J16	Pin 2 and 3 are shorted	OE pin set to 0 V (logic '0').

4.2.2 Power Settings

The only power option of this EVK is 5 V that comes from a USB port. The device has the same core and I/O supply voltage. The supply voltage of the device can be selected from on-board generated supplies of 1.8 V, 2.5 V, or 3.3 V.

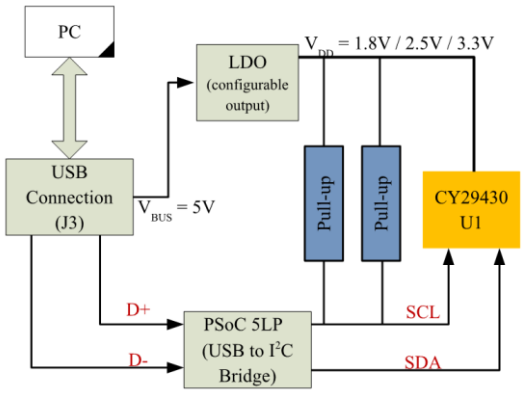
Table 4-2 lists the hardware settings required for power selection.

CAUTION	**The J13 selection must match with the software configuration of the supply voltage during functional programming and must be set to 2.5 V during eFuse programming. Mismatch between the J13 setting and ClockWizard 2.1 setting may cause incorrect output or reliability problems with the device.**

4.2.3 Functional Programming

The board should be connected to a PC through a USB connector to configure and program the device. Refer to the CY3677 EVK USB Connection section to learn how to connect the kit to a PC. Figure 4-2 illustrates the programming section of the kit.

Figure 4-2. Programming the CY29430 Device



The USB interface provides a 5-V power supply. The PSoC 5LP converts the JEDEC profiles into an I^2C-compatible format, which is then loaded into the CY29430 clock device.

Note: During functional programming, keep the power supply of the CY29430 device (hardware settings) the same as in the ClockWizard 2.1 configuration (software settings). Table 4-2 provides the supply settings for the CY29430. During eFuse programming, set the power supply of the CY29430 to 2.5 V.

The Example Projects section provides the example projects (*.cpj* files) created in ClockWizard 2.1.

4.2.4 LED Indicators

Table 4-4: LED Indicators

LED	Label	Indicator	Description
LED1	USB_PWR_LED	USB Power and Status	This LED turns ON when the kit is connected to the USB port on a PC using the cable provided. If this LED does not turn ON, it indicates that the USB enumeration of the kit did not happen with the host PC. This LED blinks continuously when the device is being programmed through the PSoC 5LP device. **Note:** This LED may glow with low intensity under the following condition: The CY29430 supply is disconnected through the jumper (J1). This low-intensity LED glow may be misleading to the user on the status of the USB connection to the board. It is, therefore, recommended to avoid this condition during use of the kit.
LED2	POWER_LED	Clock Device Power	This LED turns ON when the core of the CY29430 device is powered. Ensure that a jumper shunt is populated or not populated on J13 per Table 4-2 for proper supply of CY29430. The intensity of this LED for 1.8 V is lower compared to 2.5 V and 3.3 V.

4.2.5 On-Board Crystal

This EVK is populated with a Third Overtone Crystal (OT3) of 114.285 MHz. This crystal has a frequency tolerance of ±20 ppm. It serves as a clock source for the CY29430 device.

4.2.6 TCXO Input Reference

The CY29430 device can also be evaluated with external TCXO reference. The external reference clock source must be connected to the SMA connector J11. To activate the TCXO reference clock effective to the CY29430 device, desolder the resistor R40, and populate the 0-Ω resistor R42. R40 and R42 are located on the secondary side near the Y1 crystal.

4.2.7 Frequency Select (FS)

The volatile and the nonvolatile memory of the CY29430 device stores four frequency profiles. The Frequency Select inputs of the device (FS0 and FS1) can be controlled by the on-board jumpers J14 and J15. FS0 and FS1 can also be configured using ClockWizard 2.1. Refer to Table 4-5 for the Frequency Select operation.

Table 4-5: Jumper Settings for Frequency Select

Jumper Settings for Hardware Control of FS Bits		Jumper Settings for ClockWizard 2.1 Control of FS Bits				FS Input (logic) to CY29430		Frequency Profile Selected
J14 Settings	J15 Settings	J14 Settings	J15 Settings	ClockWizard 2.1 Settings		FS1_DUT	FS0_DUT	
Open	Open	Short pin 2 and 3	Short pin 2 and 3	Select FS1:FS0: as 00 and click **Apply**		0	0	0
Open	Short pin 1 and 2			Select FS1:FS0: as 01 and click **Apply**		0	1	1
Short pin 1 and 2	Open			Select FS1:FS0: as 10 and click **Apply**		1	0	2
Short pin 1 and 2	Short pin 1 and 2			Select FS1:FS0: as 11 and click **Apply**		1	1	3

Note: The Hardware and ClockWizard 2.1 control are mutually exclusive and only one works at a time

4.3 Evaluating Different I/O Standards Using the CY3677 EVK

The CY29430 device has one differential clock output pair (*CLK_P and CLK_N*) and one single-ended clock output (*CLK_SE*). The onboard components of the CY3677 can be configured to different settings for evaluating different clock standards.

Figure 4-3 and Table 4-6 illustrate the on-board components related to the CY29430 output clocks.

Figure 4-3. CY3677 Output Termination Settings

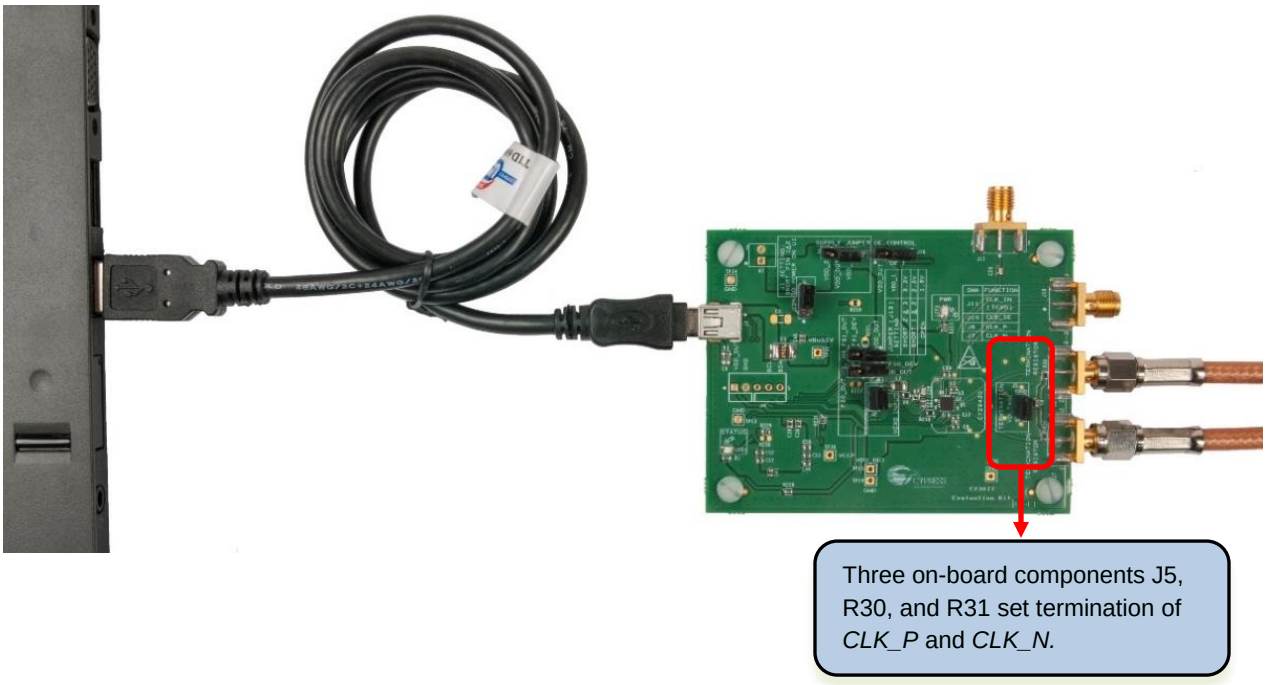


Table 4-6: CY29430 Clock Outputs

Clock Output	CY29430 Pin	SMA Connector on CY3677	Resistor to Set Termination (50 Ω)
CLK_P	10	J8	R30
CLK_N	9	J7	R31
CLK_SE	11	J10	NA

The CY29430 device supports LVPECL, LVDS, HCSL, LVPECL2, and CML differential output types. R30 and R31 are the on-board output termination resistors. The termination settings are controlled by the J5 jumper shunt. The typical laboratory setup for the evaluation of this kit is shown in Figure 4-4. See Table 4-7 to set correct on-board termination option of *CLK_P* and *CLK_N*.

Table 4-7: J5 Jumper Settings to Terminate Differential Clock Outputs

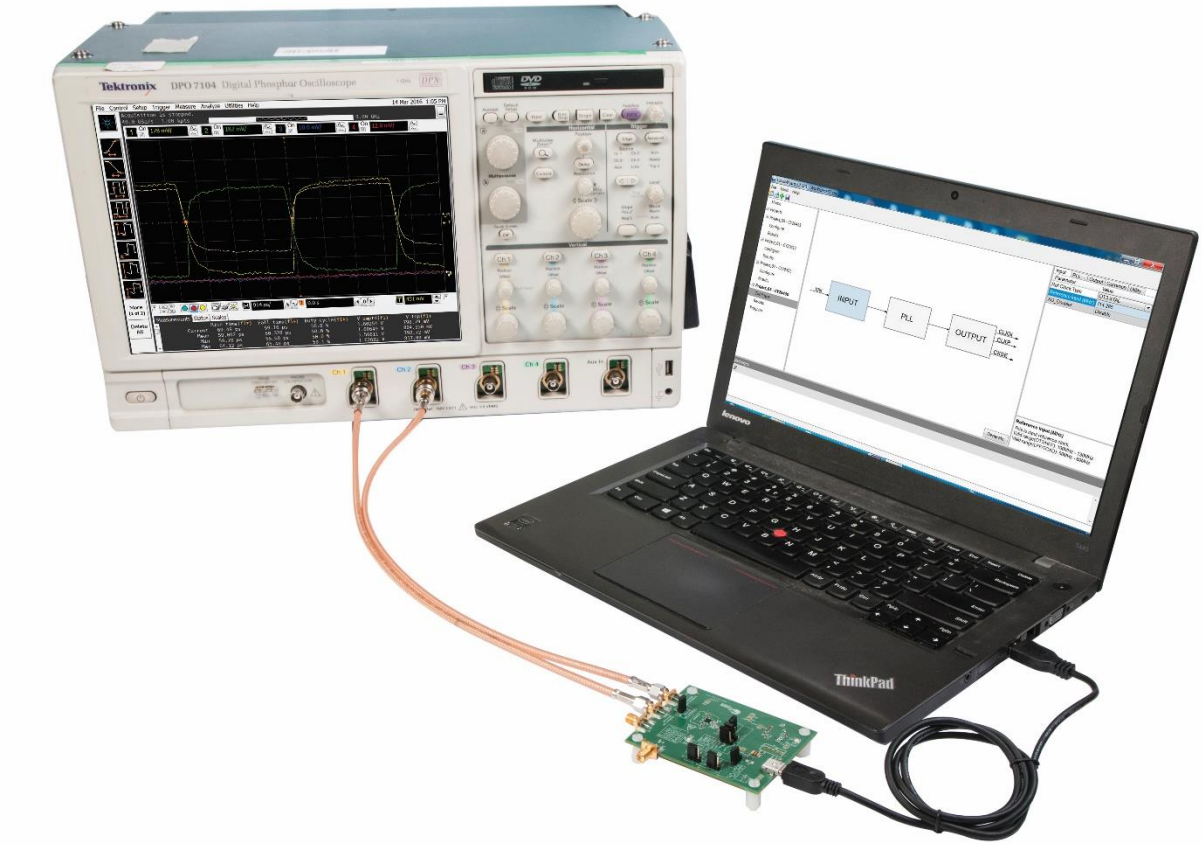
IO Standard	J5 Jumper Position	Description
LVPECL, HCSL	Short	*CLK_P* and *CLK_N* termination voltage set to 0 V through the 50-Ω termination resistors.
LVDS	Open	100 Ω differential impedance between the *CLK_P* and *CLK_N*.

CAUTION

If you want to configure this kit to any other mode, or any other termination setup, it is recommended to contact our support through the www.cypress.com/support web page, or e-mail at clocks@cypress.com.

J5 should not be powered by any external source. Connection of external power source may damage the EVK.

Figure 4-4. CY3677 EVK Connected to an Oscilloscope



5 Example Projects

5.1 Example Project Configuration Details

The CY3677 EVK can be evaluated with example projects that configure the device with different output types and frequency profiles. Each example project corresponds to a particular device configuration. This section provides the configuration details of each example project. The configuration generated from the example projects needs to be downloaded to the device and to be evaluated with on-board termination options. All the example projects are located at:

```
<Install_Directory>\CY3677 Evaluation Kit\<version>\Firmware\Example Projects
```

The device is loaded with the default configuration of 114.285 MHz LVDS output for 3.3-V VDD. To evaluate the example projects, follow the steps described in the Programming the CY29430 section and refer to the Hardware and Software settings provided in Table 5-1 for programming and evaluation.

Table 5-1: Example Project Details

Software Configurations			Hardware Settings					Evaluation in Oscilloscope	
Example Project	I/O Type	VDD	Set VDD_DUT J13 Jumper Position	Set VCM J5 Jumper Position	Set FS1 J14 Jumper Position	Set FS0 J15 Jumper Position	Setup	Output Frequency (MHz)	Expected Peak-to-Peak Voltage (mV)
CY3677_LVPECL_3p3.cpj	LVPECL	3.3V	2 and 3	Short	Open	Open	Connect SMA cables to J7 and J8, and connect the other ends to an oscilloscope.	33.333	375 to 450
					Open	1 and 2		50	
					1 and 2	Open		100	
					1 and 2	1 and 2		156.25	
CY3677_HCSL_2p5.cpj	HCSL	2.5V	1 and 2	Short	Open	Open		33.333	375 to 430
					Open	1 and 2		50	
					1 and 2	Open		125	
					1 and 2	1 and 2		100	
CY3677_LVDS_2p5.cpj	LVDS	2.5V	1 and 2	Open	Open	Open		133.33	38.5 to 50
					Open	1 and 2		100	
					1 and 2	Open		156.25	
					1 and 2	1 and 2		50	
CY3677_LVCMOS_1p8.cpj	LVCMOS	1.8V	Open	NA	Open	Open	1. Connect an SMA cable between J11 and 52-MHz TCXO reference source. 2. Connect an SMA cable between J10 and the oscilloscope. 3. Desolder the resistor, R40. 4. Populate 0 Ω resistor, R42.	19.2	155 to 175
					Open	1 and 2		38.4	
					1 and 2	Open		52	
					1 and 2	1 and 2		26	

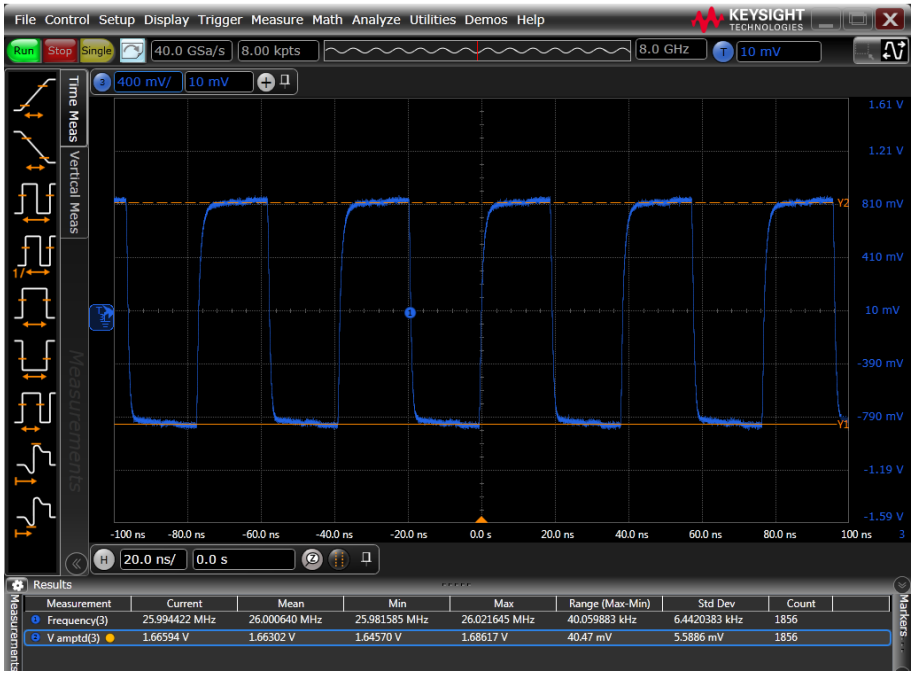
The peak-to-peak voltage provided in Table 5-1 will vary with different types of oscilloscope probes, scope-termination, and type of coupling used during measurement. These measurements are done using an 8-GHz oscilloscope, SMA cables, 50-Ω scope termination, and DC coupling. Sample example project outputs are shown in Figure 5-1 through Figure 5-4.

Figure 5-1. LVPECL 3.3 V, 156.25 MHz Clock Measured with DC Coupling, 50-Ω Scope Termination

Figure 5-2. HCSL 2.5 V, 100 MHz Clock Measured with DC Coupling, 50-Ω Scope Termination

Figure 5-3. LVDS 2.5 V, 50 MHz Clock Measured with DC Coupling, 50-Ω Scope Termination

Figure 5-4. LVCMOS 1.8 V, 26 MHz Clock Measured with DC Coupling, 10X Settings, 50-Ω Scope Termination

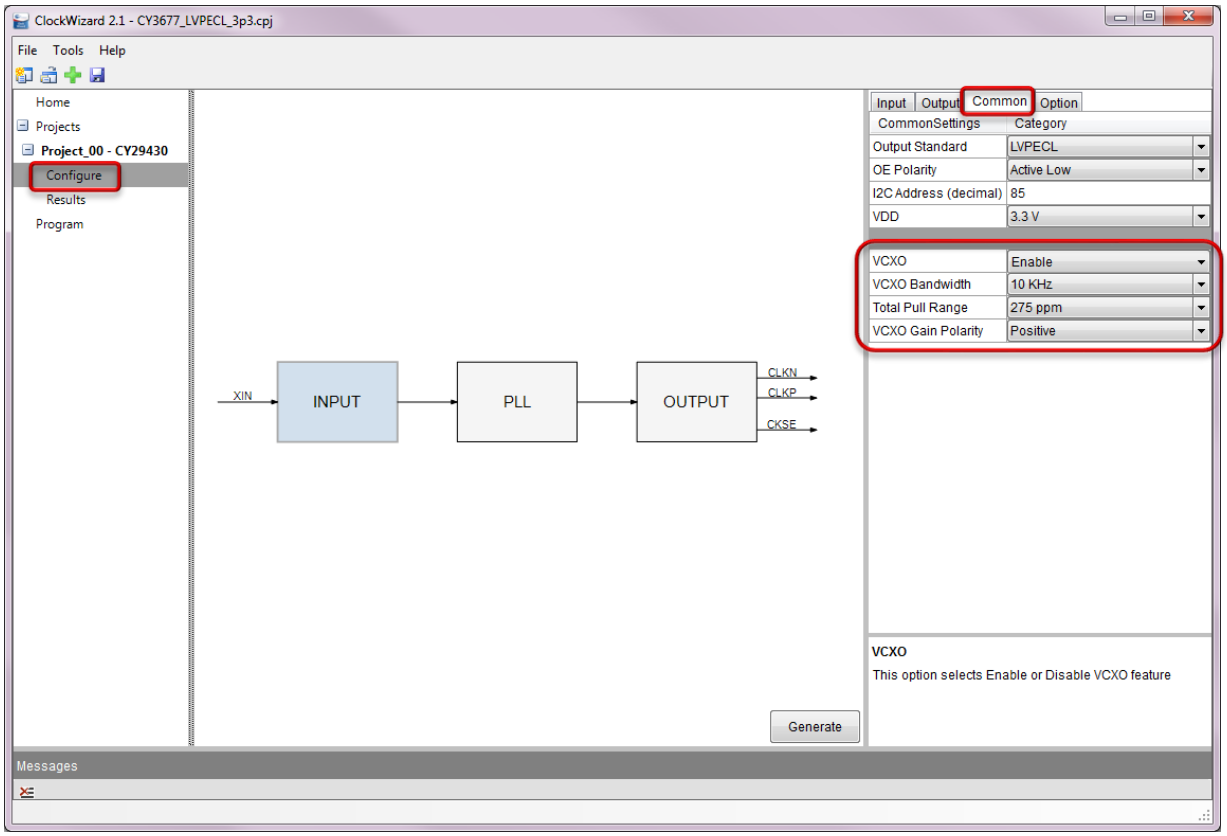


5.2 Evaluation of VCXO Functionality

You can edit any of the four example projects described in Section 5.1 to evaluate the VCXO functionality of the CY29430 device. Following is an example to evaluate the VCXO functionality:

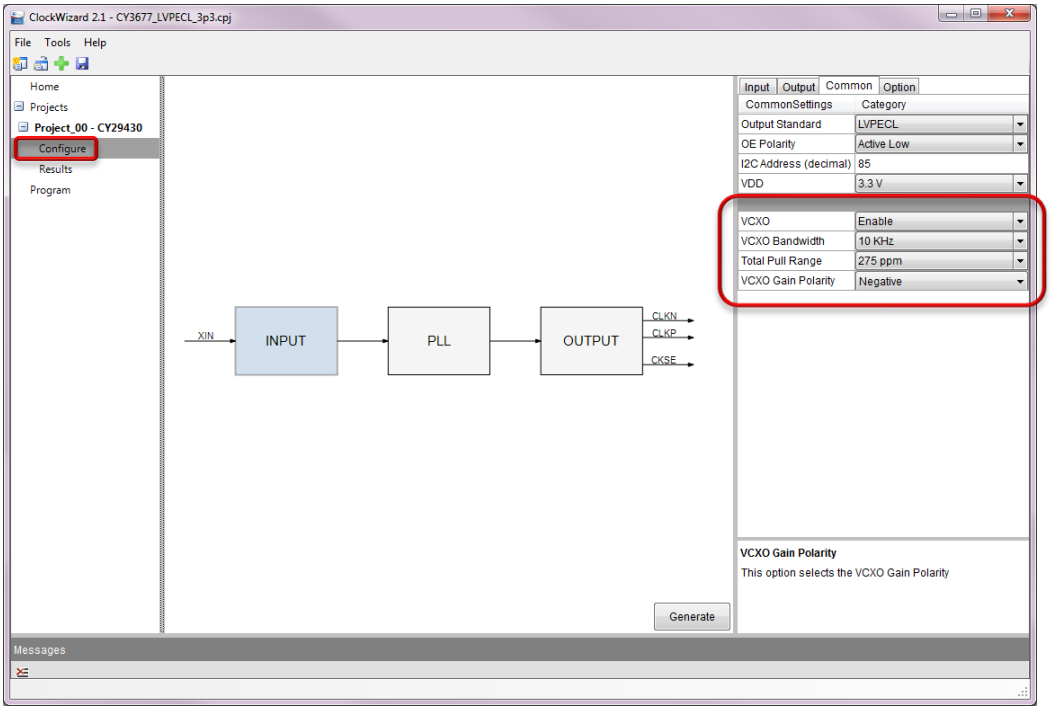
1. Open the example project *CY3677_LVPECL_3p3.cpj* using ClockWizard 2.1. Refer Table 5-1 for the required jumper settings of this project.
2. Select **Configure** in the left navigation pane. Click the **Common** tab.
3. Change VCXO settings from **Disable** to **Enable**. Select **Total Pull Range** to **275 ppm**, and **VCXO Gain Polarity** to **Positive**. Click the **Generate** button. The settings is shown in Figure 5-5.

Figure 5-5. VCXO Settings of Total Pull Range 275 ppm, and VCXO Gain Polarity Positive



4. Select **Program** in the left navigation pane, and click the **Functional Program** button.
5. Click on **Large change update**.
6. Measure frequency using a standard instrument (for example: an oscilloscope of bandwidth 8 GHz, frequency counter, or Signal source analyzer). The frequency changes from 156.25 MHz to 156.20 MHz.
7. Repeat Step 2.
8. Select **VCXO Gain Polarity** to **Negative**. Click the **Generate** button. The settings is shown in Figure 5-6.

Figure 5-6. VCXO Settings of Total Pull Range 275 ppm and VCXO Gain Polarity Negative



9. Repeat Step 4 and 5.
10. Measure frequency using a standard instrument (for example: an oscilloscope of bandwidth 8 GHz, frequency counter, or signal source analyzer). You will see the frequency has changed from 156.25 MHz to 156.30 MHz.

    The measured frequencies 156.20 MHz and 156.30 MHz are the minimum and maximum frequencies that can be controlled through VCXO operation.

CAUTION	**If you want to evaluate the Phase Noise plot of the CY29430 device in CY3677 EVK for any project with the VCXO parameter set as Enable through Functional Program, it is required to do Large change update prior to taking Phase Noise plot.** **User can directly take Phase Noise plot of the CY29430 without doing Large change update if the device is eFuse programmed.** **VCXO input jumper J2 should not be powered by any external source. Incorrect connection of external power source may damage the EVK. If user wants to apply any external source for VCXO evaluation, it is recommended to contact our support through the www.cypress.com/support web page, or e-mail at clocks@cypress.com.**

Note [1]: The default 114.285-MHz LVDS profile programmed into the device does not have the OE functionality enabled. Hence you cannot control it through the J16 jumper.

Note [2]: If you want to evaluate the OE functionality of the device through the functional programming by setting OE as Active High in the ClockWizard project, it is recommended to populate the J16 jumper between pin 2 and 3 to disable the clock, and to remove jumper J16 to enable the output clock.

The example projects provide instruction guidelines for four I/O standards (HCSL, LVPECL, LVDS, and LVCMOS). Other than these four I/O standards, the CY29430 supports other standards such as CML and LVPECL2. Evaluation of these two configurations needs additional laboratory setup and oscilloscope adjustments. Cypress recommends that you contact Cypress Technical support through the www.cypress.com/support web page, or e-mail at clocks@cypress.com if you are evaluating the CML or LVPECL2 I/O standard or want to use different coupling, or any other termination voltage that is not part of these example projects.

Any of the four example projects provided in this document, or a project you created can be permanently programmed to the nonvolatile memory. Refer to the eFuse Programming of the CY29430 section for the required guidelines on using this feature.

A. Appendix

A.1. BCP Script to Disable the Default Power-up Profile of CY29430

The CY3677 EVK is shipped with a programmed CY29430 device. This program is loaded in a particular memory location of the CY29430 device so that the on-board crystal frequency (114.285 MHz) comes out at CLK_P and CLK_N. This is the default power-up profile of the CY3677 EVK. But this power-up profile disables the OE functionality of the CY29430 device. This profile also has impact on the VCXO performance of the CY29430 device. Hence the output clock will show higher RMS Phase Jitter if VCXO is set **Enable** through ClockWizard 2.1.

To disable the default power-up profile of the CY29430 device, execute the following script in the Bridge Control Panel tool:

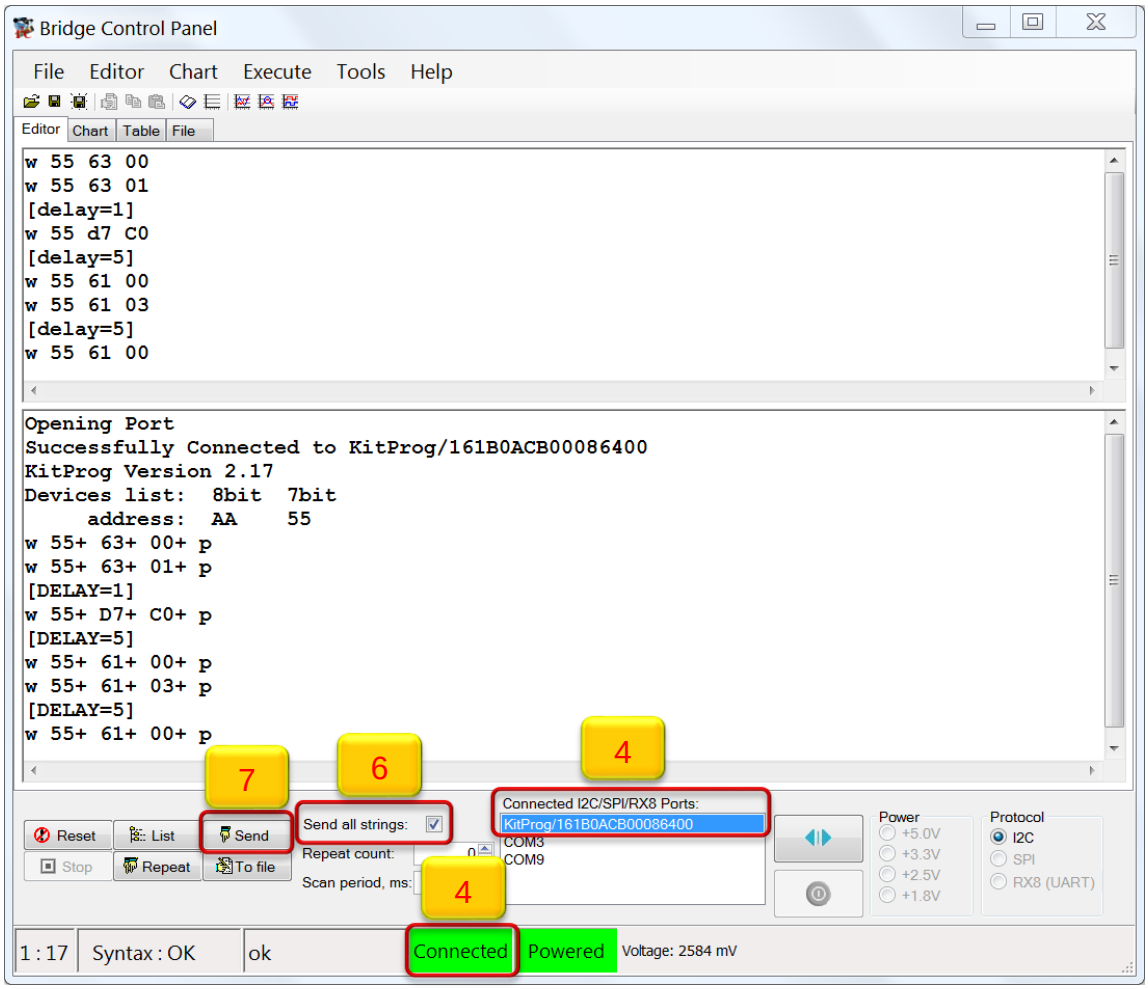
1. Create a file with a name of your choice and the extension *.iic* (for example, "*myfile.iic*").
2. Write the following set of commands in your *.iic* file:

```
w 55 63 00
w 55 63 01
[delay=1]
w 55 d7 C0
[delay=5]
w 55 61 00
w 55 61 03
[delay=5]
w 55 61 00
```

3. Open the Bridge Control Panel utility from **All Programs** > **Cypress** > **Bridge Control Panel** > **Bridge Control Panel**.
4. Click on the specific **KitProg/…** device in the connected I2C/SPI/RX8 Ports. The connected indicator is displayed in green color indicating the device is connected successfully (see Figure A-1).
5. Go to **File** > **Open File** > ***.iic***. The sequence of commands will appear in the editor, as shown in Figure A-1.
6. Check the **Send all strings** box, as shown in Figure A-1.
7. Click the **Send** button, as shown in Figure A-1.
8. Close the Bridge Control Panel.
9. Power cycle the CY29430 device.

Note: The device will permanently switch back to the unprogrammed state and will not show any default clock output during power-up. But you can perform all possible programming using the ClockWizard 2.1 tool, and evaluate the CY29430 device in the CY3677 EVK.

Figure A-1. BCP Script to Disable the Default Power-up Profile of CY29430



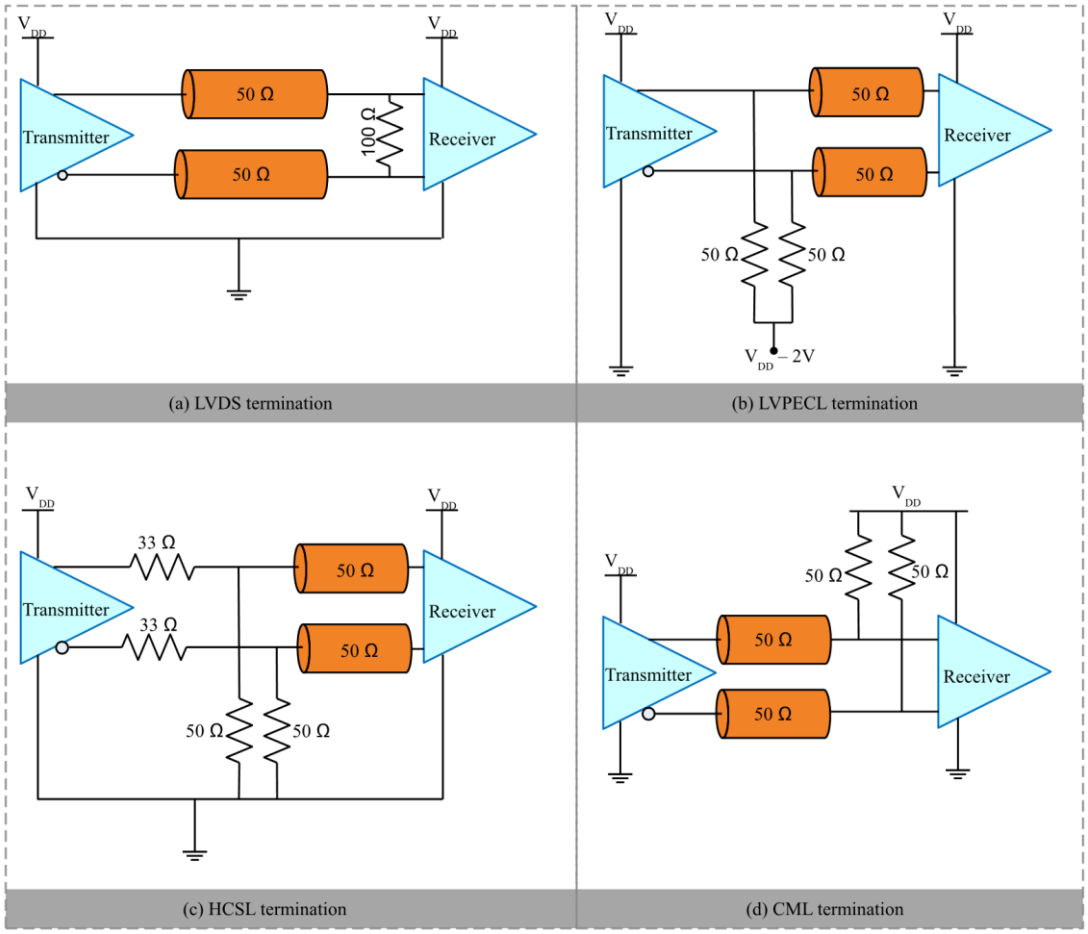
B. Appendix

B.1. Termination Settings of Differential Clock Outputs

The CY29430 device supports four high-speed differential I/O standards.

Figure B-1 illustrates industry standard differential termination techniques for reference.

Figure B-1. Recommended Differential Termination Scheme for DC/AC Measurements

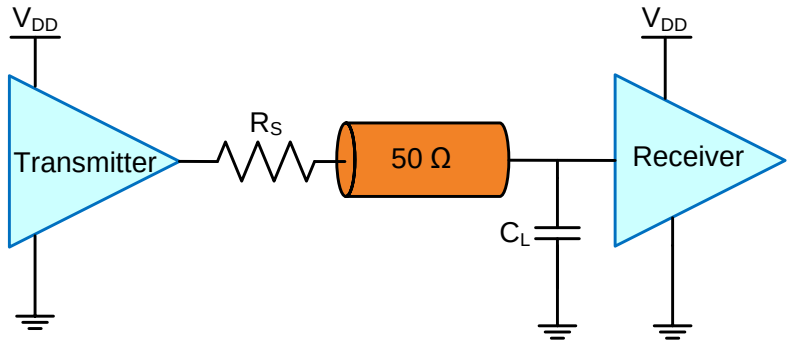


B.2. Termination Settings of LVCMOS Clock Output

Figure B-2 illustrates an industry-standard LVCMOS application circuit for quick reference. The LVCMOS output drives capacitive load only (C_L), and needs only one series termination resistor (R_S).

R_S is chosen based on the signal integrity requirement of the connection between the transmitter and the receiver.

Figure B-2. Recommended LVCMOS Termination Scheme for DC/AC Measurements



The desired output measurement can be done using an SMA cable connected to an oscilloscope. SMA offers an extra 50 Ω to the oscilloscope ground, which should be taken into account while doing measurements. This kit does not have any on-board series termination or AC coupling options. Cypress recommends contacting Cypress Technical Support through www.cypress.com/support or e-mail at clocks@cypress.com, if you want to evaluate any output with series termination or with AC coupling.

B.3. Schematics

Figure B-3. Block Diagram

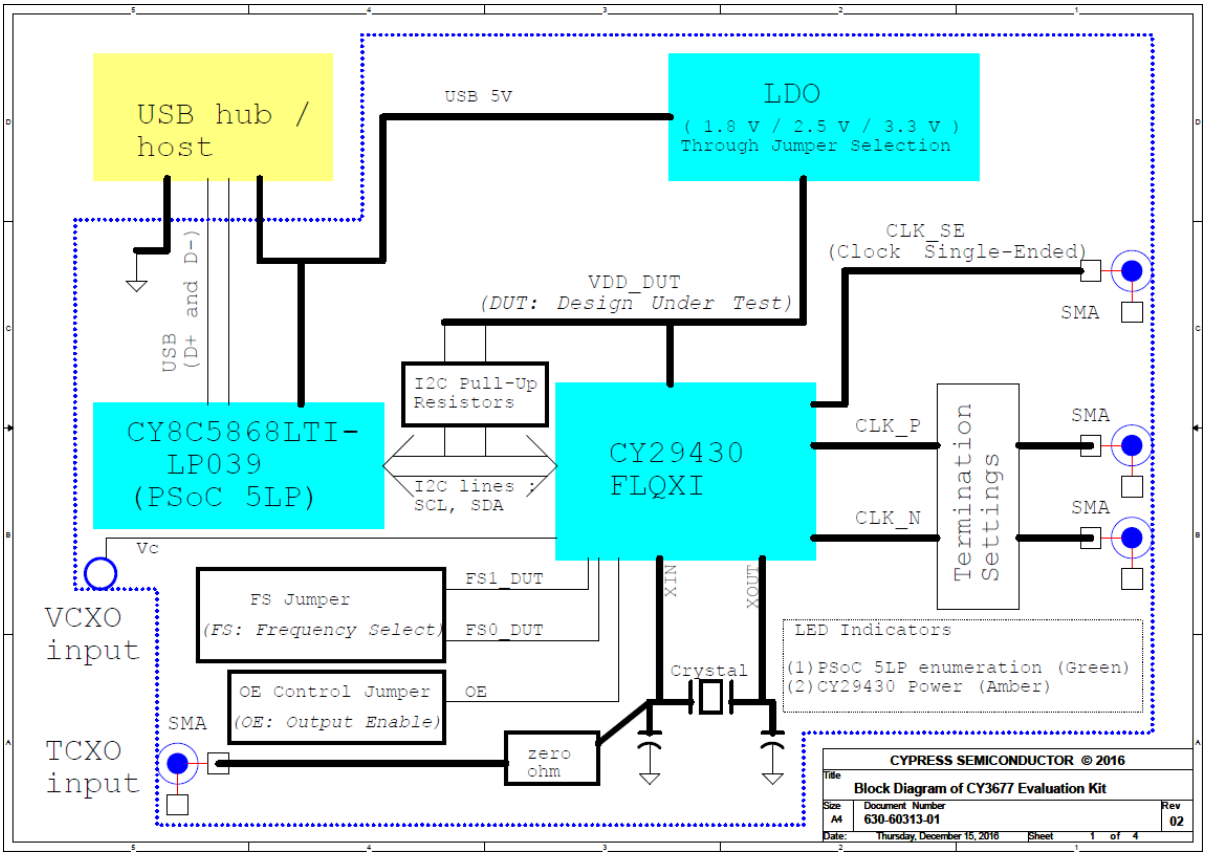


Figure B-4. Power Supply Design and LED Indicators

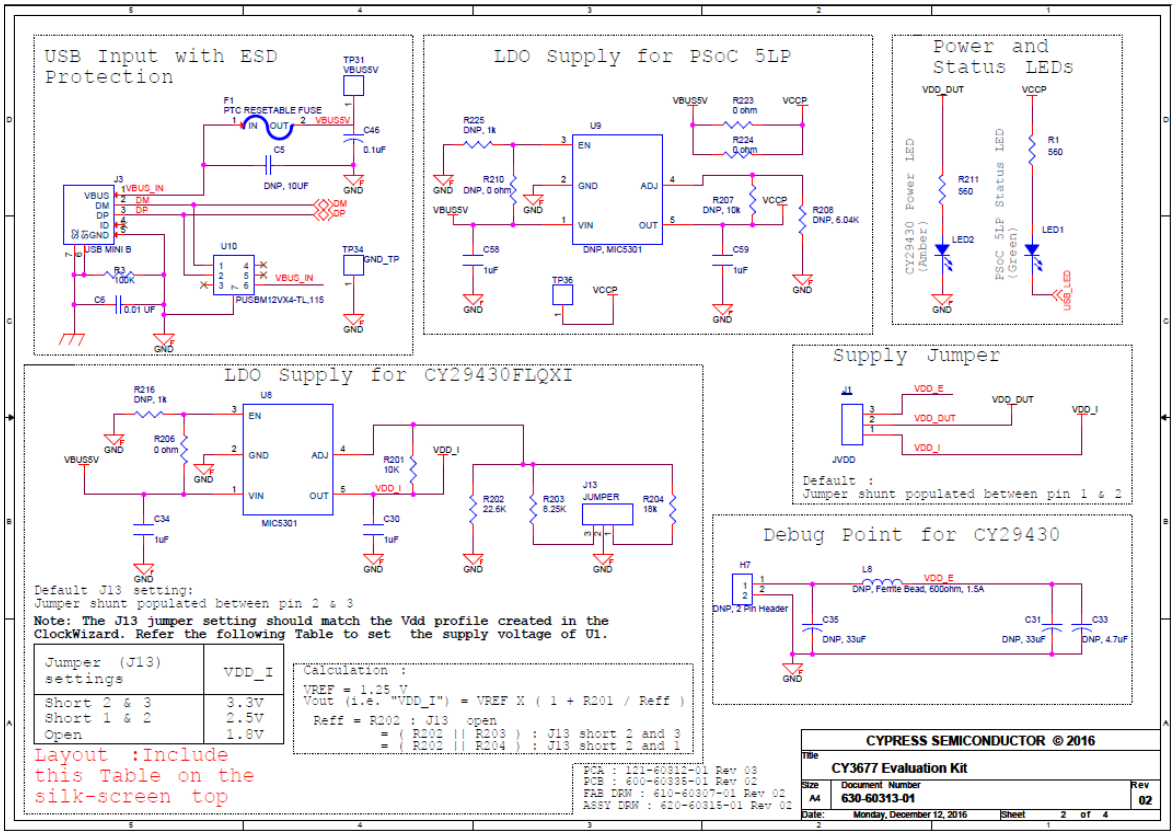


Figure B-5. Controller Schematics

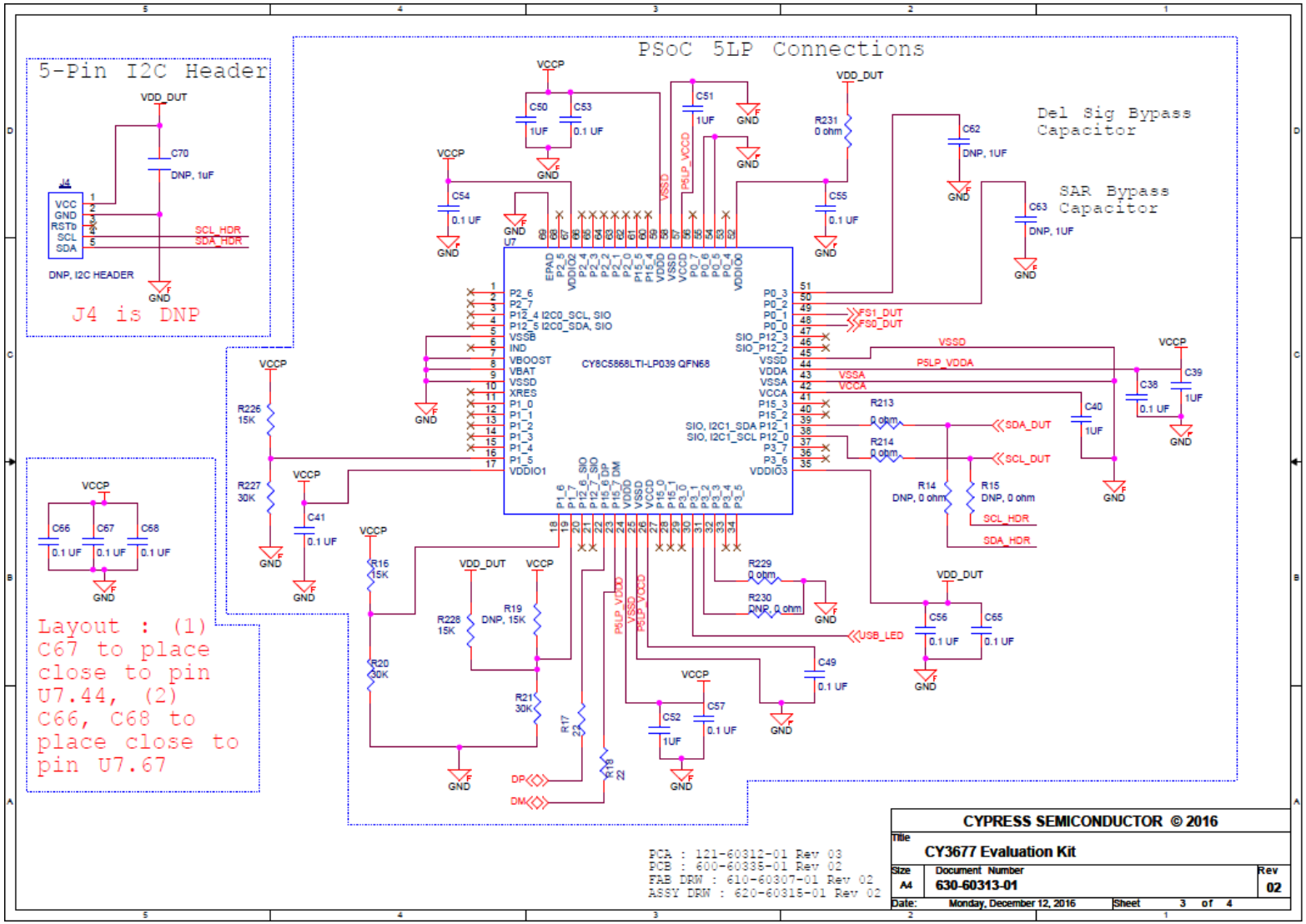
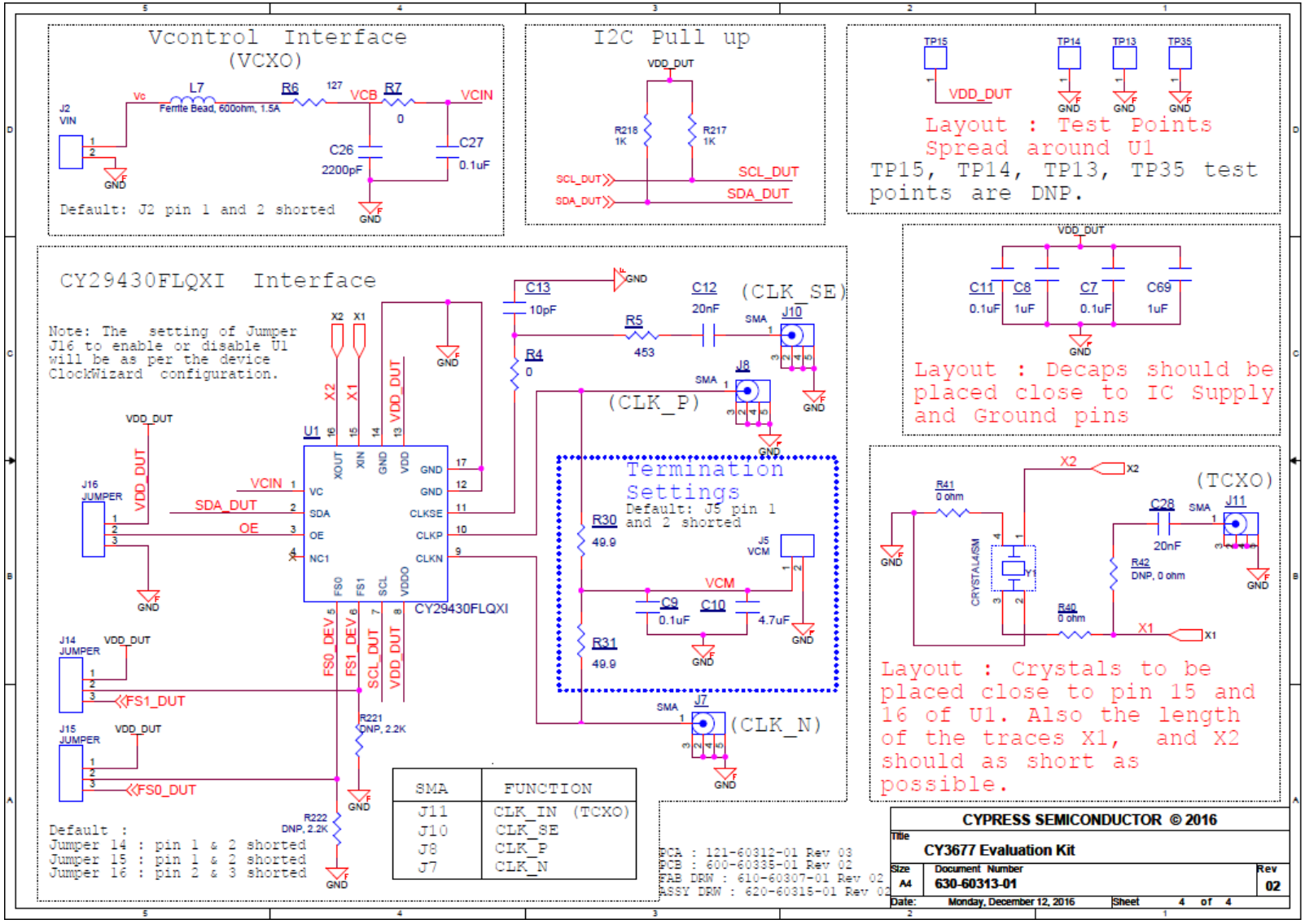
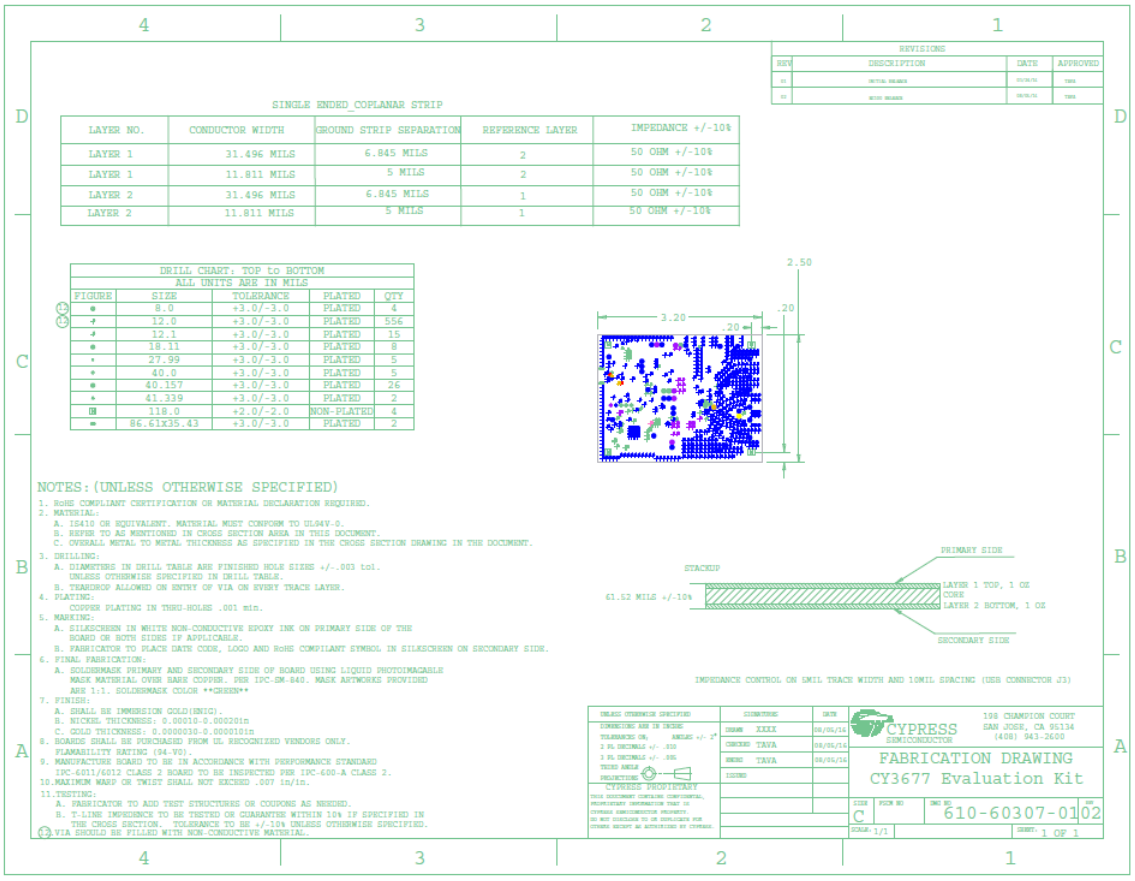


Figure B-6. CY29430 Schematics



B.4. Fabrication Drawing

Figure B-7. Fabrication Drawing



B.5. Bill of Materials

Table B-1. Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Manufacturing Part Number
1	1	C6	0.01 UF	CAP CER 10000PF 50V 10% X7R 0603	Murata Electronics	GRM188R71H103KA01D
2	17	C7,C9,C11,C27, C38,C41,C46,C 49,C53,C54,C5 5,C56,C57,C65, C66,C67,C68	0.1uF	CAP CER 0.1UF 50V Y5V 0603	Yageo	CC0603ZRY5V9BB104
3	1	C10	4.7uF	CAP CER 4.7UF 6.3V X5R 0603	Murata Electronics	GRM188R60J475KE19D
4	2	C12,C28	20nF	CAP CER 0.02UF 50V X7R 0603	Samsung Electro-Mechanics America, Inc.	CL10B203KB8NNNC
5	1	C13	10pF	CAP CER 10PF 50V C0G 0603	TDK Corporation	C1608C0G1H100C080AA
6	1	C26	2200pF	CAP CER 2200PF 50V NP0 0603	Murata Electronics	GRM1885C1H222JA01D
7	11	C8,C30,C34,C3 9,C40,C50,C51, C52,C58,C59,C 69	1UF	CAP CER 1UF 25V 10% X5R 0603	Taiyo Yuden	TMK107BJ105KA-T
8	1	F1	PTC RESETABLE FUSE	PTC RESETTABLE .50A 15V 1812	Bourns Inc.	MF-MSMF050-2
9	1	J2	VIN	CONN HEADR BRKWAY .100 02POS STR	TE Connectivity AMP Connectors	9-146280-0-02
10	1	J5	VCM	CONN HEADR BRKWAY .100 02POS STR	TE Connectivity AMP Connectors	9-146280-0-02
11	1	J3	USB MINI B	MINI USB RCPT R/A DIP	TE Connectivity AMP Connectors	1734510-1
12	4	J7,J8,J10,J11	SMA	CONN SMA JACK 50 OHM EDGE MNT	Cinch Connectivity Solutions Johnson	142-0701-801
13	5	J1,J13,J14,J15, J16	JUMPER	CONN HEADR BRKWAY .100 03POS STR	TE Connectivity AMP Connectors	9-146280-0-03
14	1	LED1	LED Green	LED GREEN CLEAR 0805 SMD	Visual Communications Company - VCC	CMD17-21VGC/TR8
15	1	LED2	LED Amber	LED AMBER CLEAR 0805 SMD	Bivar Inc.	SM0805AC
16	1	L7	FERRITE CHIP 600 OHM 1.5A	FERRITE CHIP 600 OHM 1500MA 1206	Murata Electronics	BLM31PG601SN1L
17	2	R30,R31	49.9	RES SMD 49.9 OHM 0.1% 1/10W 0603	Panasonic Electronic Components	ERA-3AEB49R9V
18	2	R7, R40	0 ohm	RES SMD 0.0 OHM JUMPER 1/10W (0402pkg)	Panasonic Electronic Components	ERJ-2GE0R00X
19	2	R1,R211	560	RES SMD 560 OHM 5% 1/10W 0603	Panasonic Electronic Components	ERJ-3GEYJ561V
20	1	R3	100K	RES SMD 100K OHM 5% 1/10W 0603	Panasonic Electronic Components	ERJ-3GEYJ104V
21	1	R5	453	RES SMD 453 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF4530V
22	1	R6	127	RES SMD 127 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF1270V

Table B-1. Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Manufacturing Part Number
23	3	R16,R226, R228	15K	RES SMD 15K OHM 5% 1/10W 0603	Panasonic Electronic Components	ERJ-3GEYJ153V
24	2	R17,R18	22	RES SMD 22 OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF22R0V
25	3	R20,R21,R227	30K	RES SMD 30K OHM 5% 1/10W 0603	Panasonic Electronic Components	ERJ-3GEYJ303V
26	1	R201	10k	RES SMD 10K OHM 1% 1/10W 0603	Yageo	RC0603FR-0710KL
27	1	R202	22.6K	RES SMD 22.6K OHM 1% 1/10W 0603	Yageo	RC0603FR-0722K6L
28	1	R203	8.25K	RES SMD 8.25K OHM 1% 1/10W 0603	Yageo	RC0603FR-078K25L
29	1	R204	18k	RES SMD 18K OHM 1% 1/10W 0603	Yageo	RC0603FR-0718KL
30	9	R4, R41, R206, R213, R214, R223, R224, R229, R231	0 ohm	RES SMD 0.0 OHM JUMPER 1/10W	Panasonic Electronic Components	ERJ-3GEY0R00V
31	2	R217,R218	1K	RES SMD 1K OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF1001V
32	1	U1	CY29430FLQXI	Clock generator, QFN package	Cypress	CY29430FLQXI
33	1	U7	CY8C5868LTI-LP039 QFN68	CY8C5868LTI-LP039 QFN68	Cypress	CY8C5868LTI-LP039
34	1	U8	MIC5301	IC REG LDO ADJ 0.15A TSOT23-5	Microchip Technology	MIC5301YD5-TR
35	1	U10	PUSBM12VX4-TL,115	TVS DIODE 5.5VWM 12VC 6HXSON	NXP Semiconductors	PUSBM12VX4-TL,115
36	1	Y1	CRYSTAL4/SM	CRYSTAL 114.2850MHZ 18PF SMD	NDK	NX3225SA-114.285MHZ-EXS00A-CS06528
Special Jumper Installation Instructions						
37	1	J1	Install jumper across pins 1 and 2	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
38	1	J2	Install jumper across pins 1 and 2	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
39	1	J5	Install jumper across pins 1 and 2	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
40	1	J13	Install jumper across pins 2 and 3	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
41	1	J14	Install jumper across pins 1 and 2	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
42	1	J15	Install jumper across pins 1 and 2	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
43	1	J16	Install jumper across pins 2 and 3	HW, CONN, Rectangular, MINI JUMPER, 6.5mm, CLOSE TYPE, BLACK, NICKEL	Sullins Connector Solutions	STC02SYAN
Label						
44	1	N/A	N/A	LBL, PCA Label, Vendor Code, Datecode, Serial Number 121-	Cypress Semiconductor	

Table B-1. Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Manufacturing Part Number
				60312-01 Rev 03 (YYWWVVXXXXX)		
No Load Components						
45	1	C5	10UF	CAP TANT 10UF 16V 10% 1206	AVX Corporation	TAJA106K016R
46	2	C31,C35	33uF	CAP TANT 33UF 6.3V 20% 1206	Rohm Semiconductor	TCA0J336M8R
47	3	C62,C63,C70	1UF	CAP CER 1UF 25V 10% X5R 0603	Taiyo Yuden	TMK107BJ105KA-T
48	1	C33	4.7uF	CAP CER 4.7UF 6.3V X5R 0603	Murata Electronics	GRM188R60J475KE19D
49	5	R14,R15,R210, R223,R224,R230	0 ohm	RES SMD 0.0 OHM JUMPER 1/10W	Panasonic Electronic Components	ERJ-3GEY0R00V
50	2	R216,R225	1k	RES SMD 1K OHM 1% 1/10W 0603	Panasonic Electronic Components	ERJ-3EKF1001V
51	2	R221,R222	2.2K	RES SMD 2.2K OHM 5% 1/10W 0603	Yageo	RC0603JR-072K2L
52	1	R42	0 ohm	RES SMD 0.0 OHM JUMPER 1/10W (0402pkg)	Panasonic Electronic Components	ERJ-2GE0R00X
53	1	R19	15K	RES SMD 15K OHM 5% 1/10W 0603	Panasonic Electronic Components	ERJ-3GEYJ153V
54	1	R208	6.04K	RES SMD 6.04K OHM 1% 1/10W 0603	Yageo	RC0603FR-076K04L
55	1	R207	10k	RES SMD 10K OHM 1% 1/10W 0603	Yageo	RC0603FR-0710KL
56	1	J4	I2C HEADER	CONN HEADER 5POS .100 VERT TIN	Molex, LLC	22-23-2051
57	1	L8	FERRITE CHIP 600 OHM 1.5A	FERRITE CHIP 600 OHM 1500MA 1206	Murata Electronics	BLM31PG601SN1L
58	1	H7	2 Pin Header	TE_640456-2 (2-pin Header)	TE Connectivity AMP Connectors	640456-2
59	1	U9	MIC5301	IC REG LDO ADJ 0.15A TSOT23-5	Microchip Technology	MIC5301YD5-TR

Revision History

Document Revision History

Document Title: CY3677 Evaluation Kit User Guide Document Number: 002-12185			
Revision	**Issue Date**	**Origin of Change**	**Description of Change**
**	06/23/2016	TAVA	Initial version of the kit guide.
*A	07/08/2016	TAVA	Updated Figure 2-3 and Table 5-1. Updated Acronyms, Functional Description, On-Board Crystal, and Example Projects. Updated Step 8 in Generating and Programming the Device Configuration Profile. Updated table title for Table 4-4 and Table 4-7.
*B	08/16/2016	TAVA	Updated Introduction, Programming the CY29430, and Generating and Programming the Device Configuration Profile. Updated Table 4-1 and Table 4-7. Added Figure 5-1 through Figure 5-4, and Figure B-2. Updated Copyrights.
*C	12/23/2016	TAVA	Added TCXO Input Reference and A. Appendix. Updated Programming the CY29430, Example Projects, B. Appendix, and Bill of Materials. Updated Figure 1-1, Figure 3-6, and Figure 4-1. Added Figure 3-8, Figure 3-9, Figure 3-10, Figure 3-11, Figure 3-12, Figure 5-5, and Figure 5-6. Updated Copyright.
*D	01/27/2017	TAVA	Updated Figure 1-1. Added a Note in Section 5.2. Minor change in Bill of Materials.