MachXO™ Starter Evaluation Board

User's Guide

April 2007
Revision: ebug14_01.4

Introduction

The Lattice MachXO Starter Evaluation Board provides a convenient platform to evaluate, test and debug user designs. The board features a Lattice MachXO256 cross-over programmable logic device in a 100-pin TQFP package, power input jacks, a 33MHz clock oscillator and I/O connections. The Lattice MachXO I/Os are connected to a rich variety of interfaces, including switches (momentary and ON/OFF), LEDs, 0.10" headers and PCB test points.

Features

- Lattice MachXO device
- Prototyping area
- Access to 81 user I/Os
- Independent voltage control for core and I/O
- 33MHz on-board oscillator
- Status LEDs
- Input switches
- Pads for optional board expansion.
- AC adapter
- Lattice ispDOWNLOAD® cable, to download programming files to the MachXO device.

Software Support

- Lattice ispLEVER® design tools (release 5.0 SP1 or later) for HDL design targeting the MachXO device. The MachXO device is supported in the ispLEVER-Starter software, available from www.latticesemi.com/starter.
- ispVM® System, for device programming. Available for download from www.latticesemi.com/software.

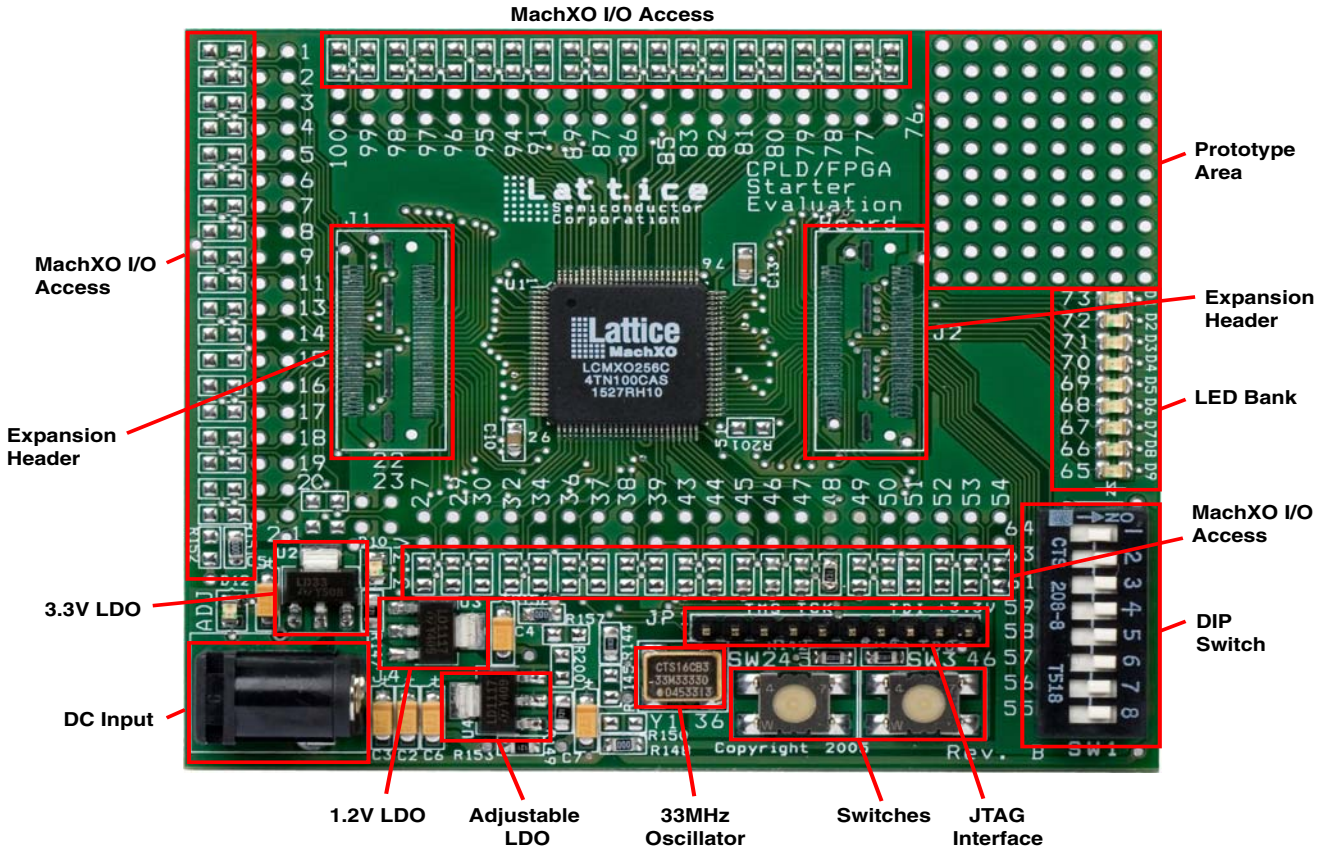
Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 2.875 inches by 3.375 inches. The environmental specifications are as follows:

- Operating temperature: 0ºC to 55ºC
- Storage temperature: -40ºC to 75ºC
- Humidity: < 95% without condensation
- VDC input (+/- 10%) up to 4A

Figure 1 shows the board outline.

Figure 1. MachXO Starter Outline



Resources relating to the Lattice MachXO Starter Evaluation Board, including user documentation updates and sample programs, can be found at www.latticesemi.com/boards. Click on the appropriate link for the Lattice MachXO Starter Evaluation Board.

Lattice MachXO Device

The MachXO Starter Evaluation Board features a Lattice MachXO device with a 3.3V DC core. The board is populated with a MachXO256 device in a plastic 100-pin TQFP package. The MachXO Starter Evaluation Board allows for density migration to other Lattice MachXO densities in the 100 TQFP package, with either 3.3V or 1.2V cores. A complete description of this device can be found in the Lattice MachXO Family Data Sheet on the Lattice web site at www.latticesemi.com.

Device Core and I/O Voltage

Core Voltage

The MachXO is available with either 3.3V or 1.2V core voltage devices. Boards populated with a 3.3V DC core device will allow operation of the core between 1.8V and 3.3V DC. The core voltage is fixed at 3.3V during manufacturing. The core voltage may be changed from the fixed 3.3V rail to the adjustable voltage rail by changing the 0 ohm resistor at R157 to R158.

Boards populated with a 1.2V core device operate at 1.2V only, with the core voltage supply fixed at 1.2V during manufacturing. Refer to the board silkscreen outline in the appendix for component location.

I/O Voltage

The Lattice MachXO device has two sysIO™ banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), which allows each I/O bank to be completely independent. Refer to the Lattice MachXO Family Data Sheet for additional information about supported I/O standards. This data sheet can be downloaded from www.latticesemi.com.

The MachXO Starter Evaluation Board allows individual control of each I/O bank capable of supporting V_{CCIO} between 1.2V and 3.3V. The board includes 0 ohm resistors which allow the user to select 3.3V or an adjustable voltage between 1.25V and 3.3V. During manufacturing, the V_{CCIO} banks are set to 3.3V. The adjustable voltage rail (ADJ) is fixed at 2.5V during manufacturing. Table 1 shows the required resistor population to set the appropriate core and I/O voltages.

Table 1. Voltage Jumpers/Settings for V_{CCIO} and VCC_CORE

	3.3V	ADJ	1.2V
VCC_CORE	R157 (default[1])	R158	R156(default*)
V_{CCIO0}	R148 (default)	R150	N/A
V_{CCIO1}	R151 (default)	R152	N/A

1. Default resistor is based on device core I/O voltage, 3.3V for "C" devices, and 1.2V for "E" devices.

Device Clocks

The MachXO Starter Evaluation Board provides a variety of ways to supply clock signals to the MachXO device. These include a 33MHz on-board crystal oscillator, expansion connectors and 0.1" header pins. The on-board oscillator is connected to MachXO pin 36, which is a dedicated clock input. The oscillator can be enabled/disabled via pull up (R144) /down (R145), or through pin 44 of the MachXO. Dedicated clock inputs are also available on the following pins: 38, 85 and 86. These pins are brought out to test points on the PCB, and to the expansion headers.

Device I/O Banks

MachXO I/O banks 0 and 1 are general purpose I/O banks connected to a combination of test pads, switches, LEDs and two board expansion headers. The switches consist of two user defined push-button switches and an 8-position DIP switch. Both types of switches are pulled up to the associated V_{CCIO} voltage with 10K Ω resistors (when in the up position) and connected to GND when activated (in the down position). LEDs are active (lit) when the device I/O is low. Table 2 details the I/O banks 0 and 1 connections.

I/Os listed as GPIO (General Purpose I/O) are connected to 0.1" centered plated through hole, with an associated GND hole and pads for a pull-up or pull-down resistor. The pull-up pads are located on the component side of the PCB, and the pull-down pads on the solder side. These pads are sized for 0805 components. Each device I/O is connected to a test point on the PCB. The PCB silkscreen is marked with the corresponding MachXO 100-TQFP I/O pin.

Table 2. Device I/O Connections

Pin #	Pin Name	Expansion Connect	Function/PCB Connect
1	PL2A	J1-5	GPIO
2	PL2B	J1-6	GPIO
3	PL3A	J1-7	GPIO
4	PL3B	J1-8	GPIO
5	PL3C	J1-9	GPIO
6	PL3D	J1-10	GPIO
7	PL4A	J1-11	GPIO
8	PL4B	J1-12	GPIO
9	PL5A	J1-13	GPIO

Table 2. Device I/O Connections (Continued)

Pin #	Pin Name	Expansion Connect	Function/PCB Connect
11	PL5B	J1-14	GPIO
13	PL5C	J1-15	GPIO
14	PL5D/GSR_N	J1-16	GPIO
15	PL6A	J1-17	GPIO
16	PL6B/TSALL	J1-18	GPIO
17	PL7A	J1-19	GPIO
18	PL7B	J1-20	GPIO
19	PL7C	J1-21	GPIO
20	PL7D	J1-22	GPIO
21	PL8A	J1-23	GPIO
22	PL8B	J1-24	GPIO
23	PL9A	J1-25	GPIO
27	PL9B	J1-36	GPIO
29	PB2A	J1-37	GPIO
30	PB2B	J1-38	GPIO
32	PB2C	J1-39	GPIO
34	PB2D	J1-40	GPIO
36	PCLKT1_1/PB3A	J1-41	Y1
37	PB3B	J1-42	GPIO
38	PCLKT1_0/PB3C	J1-43	GPIO
39	PB3D	J1-44	GPIO
43	PB5A	J2-21	GPIO
44	PB4B	J2-22	OSC_EN
45	PB4C	J2-37	SW2
46	PB4D	J2-23	SW3
47	PB5A	J2-24	GPIO
48	SLEEPN	J2-25	GPIO/SW[1]
49	PB5C	J2-26	GPIO
50	PB5D	J2-20	GPIO
51	PR9B	J2-19	GPIO
52	PR9A	J2-18	GPIO
53	PR8B	J2-17	GPIO
54	PR8A	J2-16	GPIO
55	PR7D	J2-38	SW1-8
56	PR7C	J2-39	SW1-7
57	PR7B	J2-40	SW1-6
58	PR7A	J2-41	SW1-5
59	PR6B	J2-42	SW1-4
61	PR6A	J2-43	SW1-3
63	PR5D	J2-44	SW1-2
64	PR5C	J2-45	SW1-1
65	PR5B	J2-46	LED D9
66	PR5A	J2-47	LED D8
67	PR4B	J2-48	LED D7

Table 2. Device I/O Connections (Continued)

Pin #	Pin Name	Expansion Connect	Function/PCB Connect
68	PR4A	J2-49	LED D6
69	PR3D	J2-50	LED D5
70	PR3C	J2-51	LED D4
71	PR3B	J2-52	LED D3
72	PR3A	J2-53	LED D2
73	PR2B	J2-54	LED D1
76	PR2A	J2-15	GPIO
77	PT5C	J2-14	GPIO
78	PT5B	J2-13	GPIO
79	PT5A	J2-12	GPIO
80	PT4F	J2-11	GPIO
81	PT4E	J2-10	GPIO
82	PT4D	J2-9	GPIO
83	PT4C	J2-8	GPIO
85	PCLKT0_1/PT4B	J2-7	GPIO
86	PCLKT0_0/PT4A	J2-6	GPIO
87	PT3D	J2-5	GPIO
89	PT3C	J1-45	GPIO
91	PT3B	J1-46	GPIO
94	PT3A	J1-47	GPIO
95	PT2F	J1-48	GPIO
96	PT2E	J1-49	GPIO
97	PT2D	J1-50	GPIO
98	PT2C	J1-51	GPIO
99	PT2B	J1-52	GPIO
100	PT2A	J1-53	GPIO

1. By shorting R201 with a 0 ohm resistor.

Expansion Header

The MachXO Starter board includes two Samtec board-to-board connector footprints (connectors not included) for expansion purposes. All MachXO I/O pins, JTAG signals and board voltages are connected to these pads. Refer to Table 3 for MachXO connections to the expansion headers. Programming pins can be referenced in the Programming Headers sections of this guide. Power connections are listed in Table 3.

Table 3. Expansion Connector Power Connections

Power Supply	Expansion Connector Pin
3.3V	J2-1,J2-2,J2-3,J2-4, J2-55,J2-56,J2-57, J2-58,J2-59,J2-60
ADJ	J1-1,J1-2,J1-3,J1-4
1.2V	J1-26,J1-27,J1-28, J1-29,J1-30
GND	J1-31,J1-54,J1-55, J1-56,J1-57,J1-58, J1-59,J1-60, J2-27, J2-28,J2-29,J2-30, J2-31,J2-32,J2-33, J2-34,J2-35,J2-36, J1 and J2 Center

The connectors are Samtec part number QTH-030-01-F-D-A. Mating connectors are Samtec part number QSH-030-01. A mechanical drawing with placement dimensions is available from Lattice.

Prototype Area

The MachXO Starter Evaluation Board contains a 0.8" x 1.0" plated through hole prototype area. The holes are spaced on 0.1" centers and are not connected to any MachXO device pins.

Programming Headers

A 1x10 programming header is provided on the MachXO Starter Evaluation Board, providing access to the MachXO JTAG port. The header is compatible with all Lattice ispDOWNLOAD cables. The pinout for the header is provided in Table 4.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the MachXO device and render the board inoperable.*

An ispDOWNLOAD cable is included with purchase of the ispLEVER design tools. Cables may also be purchased separately from Lattice. Visit the Lattice web store to learn more at: www.latticesemi.com/store.

Table 4. JTAG Programming Header Connections

JTAG Programming Function	JP1 Pin Number (1x10)	Mach XO Device Pin	Expansion Connector Pin
+3.3V	1	N/A	N/A
TDO	2	31	J1-34
TDI	3	33	J1-35
N/C	4	N/A	N/A
N/C	5	N/A	N/A
TMS[1]	6	26	J1-33
GND	7	N/A	N/A
TCK[1]	8	28	J1-32
N/C	9	N/A	N/A
N/C	10	N/A	N/A

1. Please note that some versions of the MachXO Starter Evaluation Board may have an incorrect silkscreen marking for these pins on the printed circuit board. Please follow the connections guidelines in Table 4, and not the silkscreen markings on the board.

Power Setup

Power is supplied to the PCB via the supplied 5V AC/DC transformer. The DC input jack is a 2.5mm, positive tip size connector. Input voltage should not exceed 9V DC. 800mA low dropout regulators provide V_{CC} core and V_{CCIO} voltages. The adjustable voltage regulator output can be modified by changing the value of resistor R153. The equation for calculating V_{ADJ} is as follows:

$$V_{ADJ} = 1.25 * (1 + R2/120)$$

Table 5 shows some common voltages, and the appropriate resistor value for setting each voltage. Resistance given is for the closest standard value. Resistor pads are 0805 component size.

Table 5. Adjustable Voltage Resistor Values

ADJ Voltage	R153 Resistor Value
3.3V	200 Ω
2.8V	150 Ω
2.5V	120 Ω
1.8V	51 Ω
1.5V	24 Ω

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO 256C Evaluation Board - Starter	LCMXO256C-S-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
March 2007	01.3	Added Ordering Information section.
April 2007	01.4	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.

Appendix A. PCB Schematics

Figure 2. MachXO Starter Evaluation Board Expansion Port

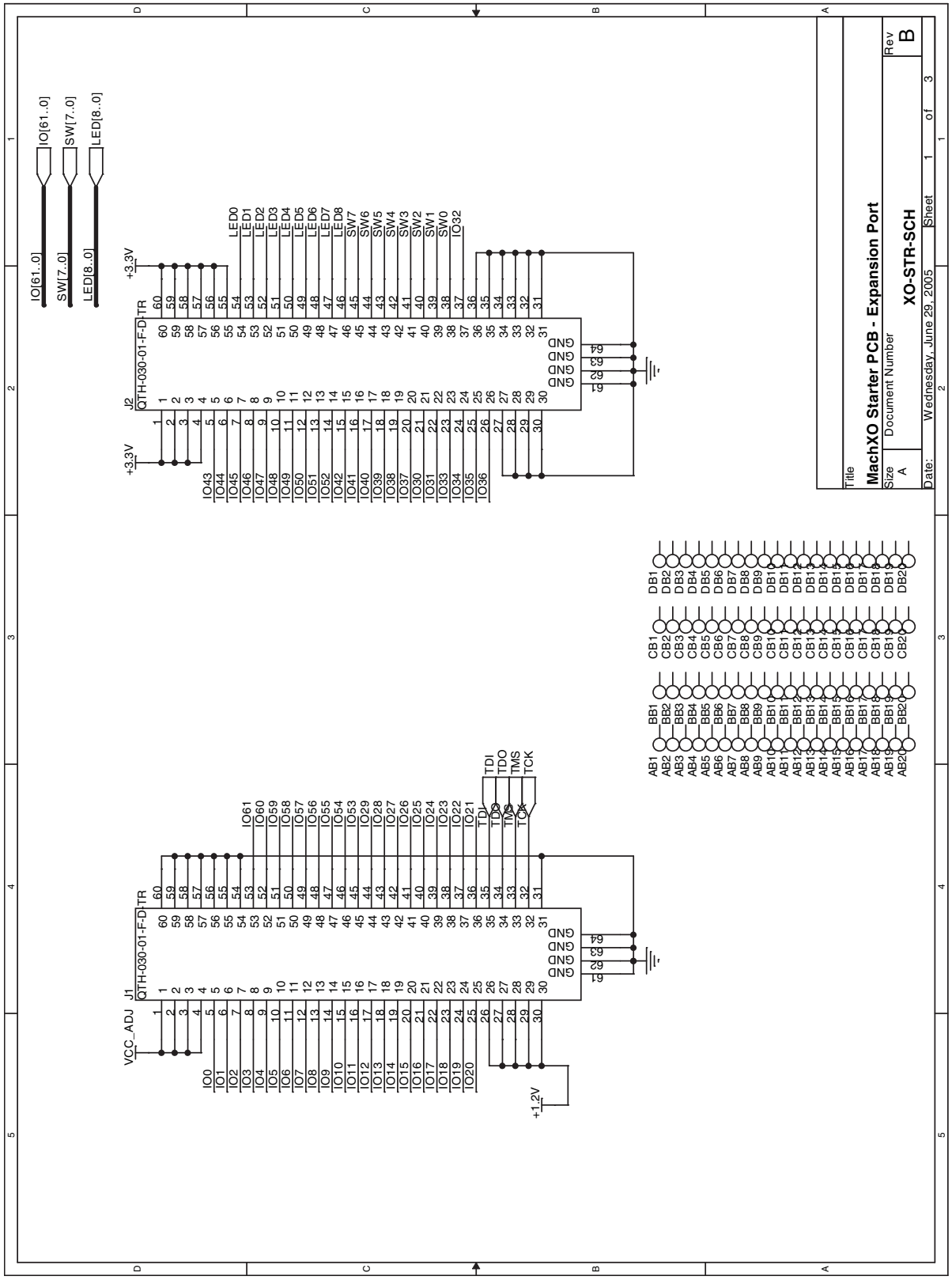


Figure 3. MachXO Starter Evaluation Board

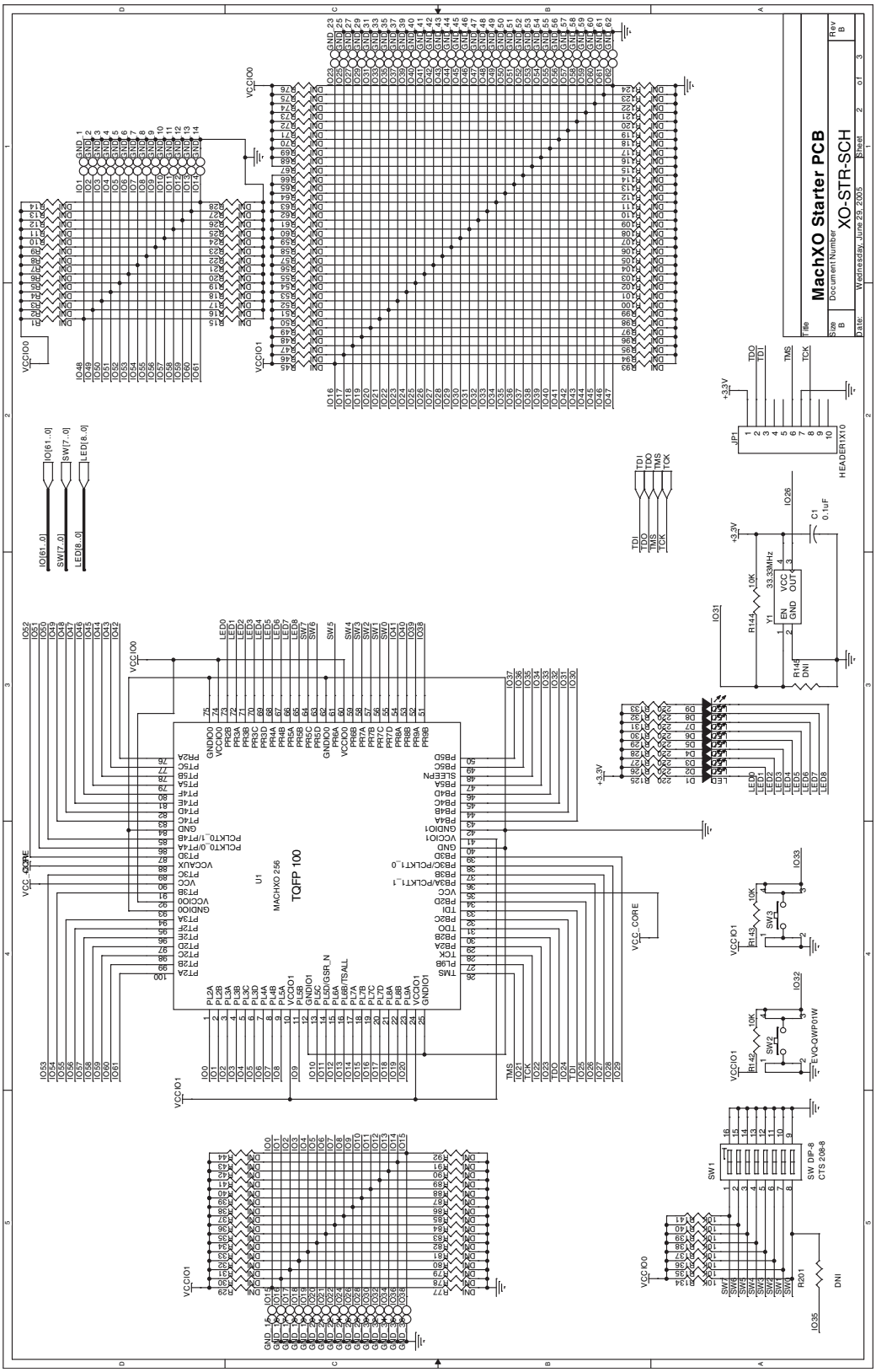
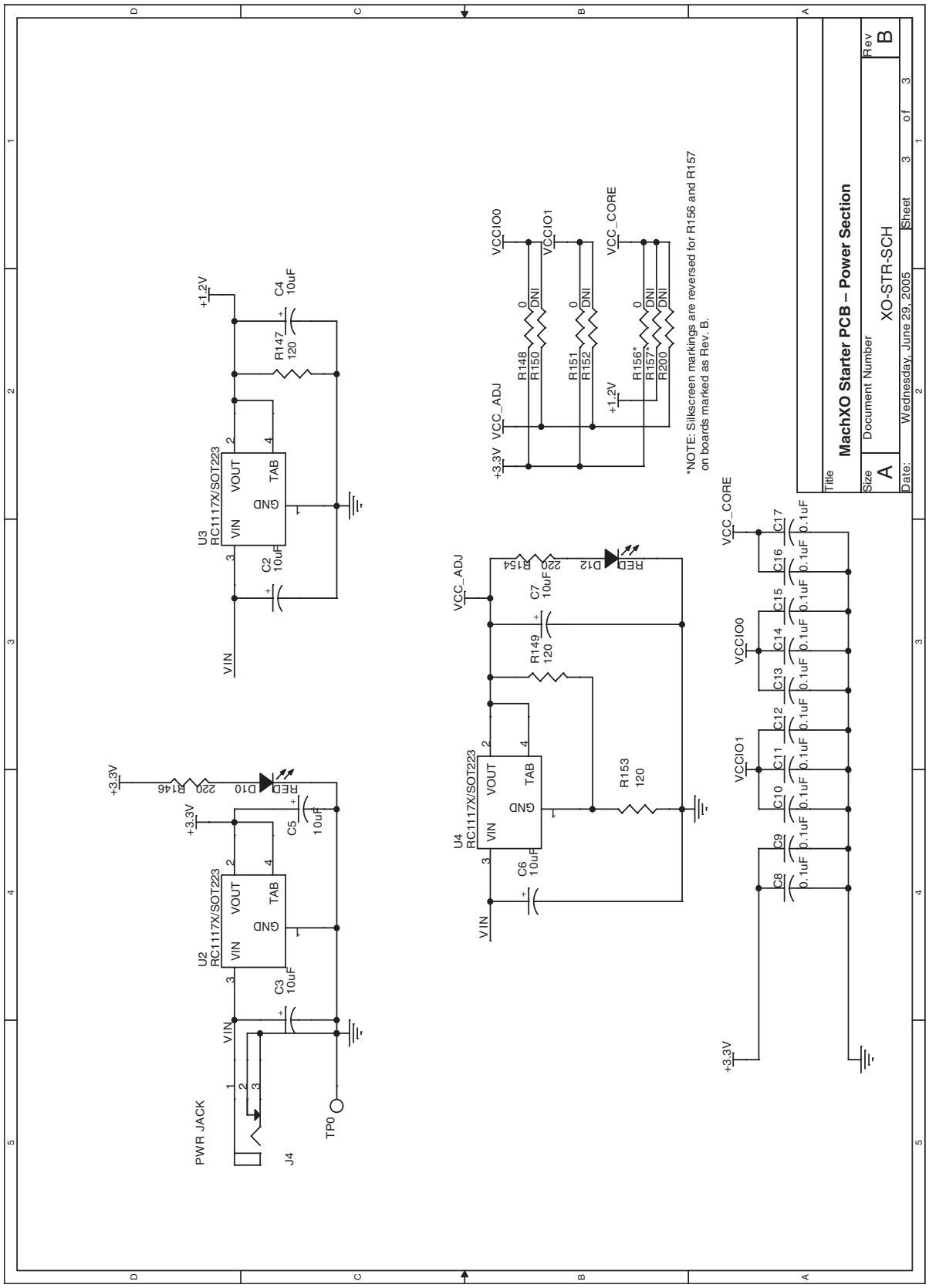


Figure 4. MachXO Starter Evaluation Board – Power Section



Appendix B. PCB Layout Diagrams

Figure 5. MachXO Starter Evaluation Board Layout Diagrams

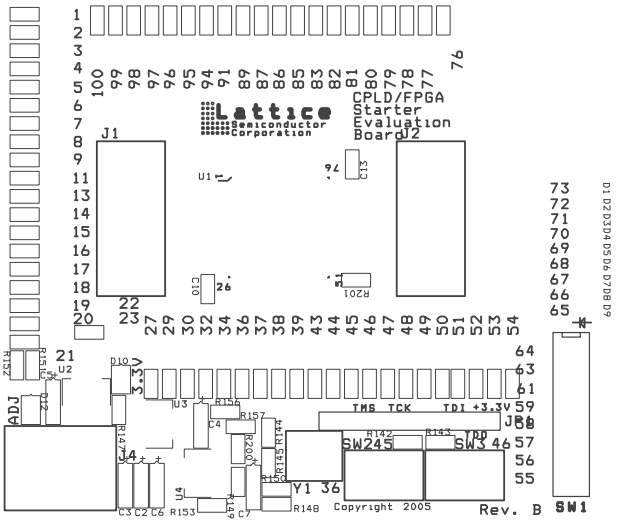


Figure 1. Top Silkscreen

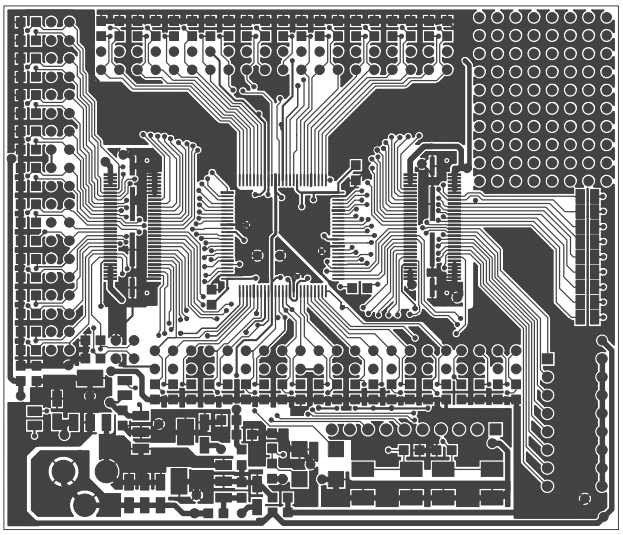


Figure 2. Component Side Layout

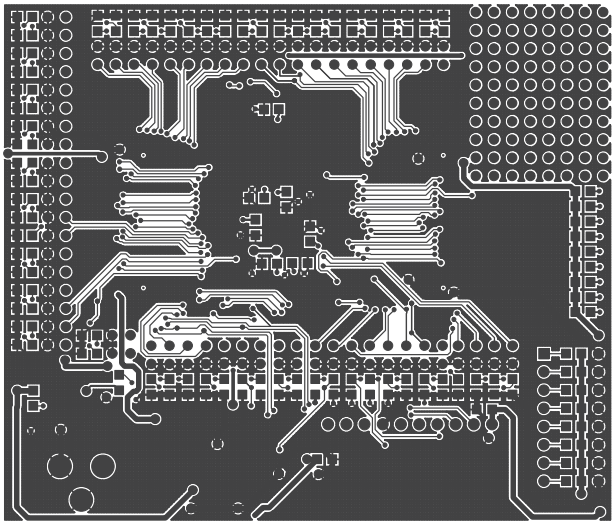


Figure 3. Solder Side Layout

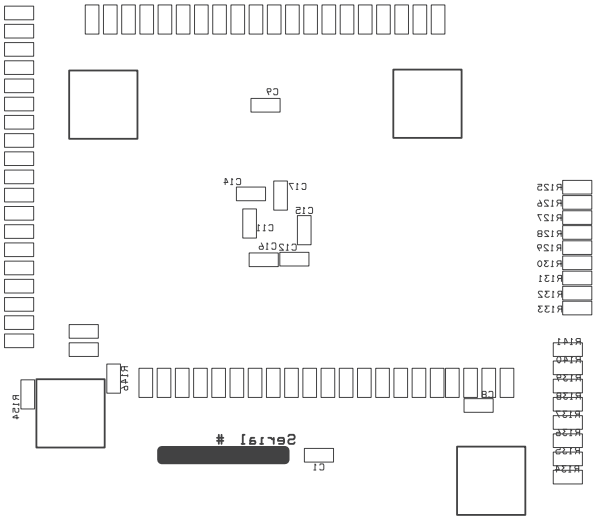


Figure 4. Bottom Silkscreen

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Lattice:

LCMXO256C-S-EV LCMXO256C-S-EVN