

SL2S1402_SL2S1502_SL2S1602

ICODE ILT

Rev. 3.3 — 15 October 2019

234333

Product data sheet
COMPANY PUBLIC

1 General description

The ISO 18000-3 mode 3/EPC Class-1 HF standard allows the commercialized provision of mass adoption of HF RFID technology for passive smart tags and labels. Main fields of applications are supply chain management and logistics for worldwide use.

The ICODE ILT is a dedicated chip for passive, intelligent tags and labels supporting the ISO 18000-3 mode 3 RFID standard. It is especially suited for applications where reliable identification and high anti-collision rates are required.

The ICODE ILT is a product out of the NXP Semiconductors ICODE product family. The entire ICODE product family offers anti-collision functionality. This allows a reader to simultaneously operate multiple labels/tags within its antenna field. A ICODE ILT based label/tag requires no external power supply.

Its contactless interface generates the power supply via the antenna circuit by inductive energy transmission from the interrogator (reader), while the system clock is extracted from the magnetic field. Data transmitted from interrogator to label/tag is demodulated by the interface, and it also modulates the interrogator's magnetic field for data transmission from label/tag to interrogator. A label/tag can be operated without the need for line of sight or battery, as long as it is connected to a dedicated antenna for the targeted frequency range. When the label/tag is within the interrogator's operating range, the high-speed wireless interface allows data transmission in both directions.



2 Features and benefits

2.1 Key features

- Up to 240-bit of EPC memory
- 96-bit tag identifier (TID) including 48-bit unique serial number
- EAS (Electronic Article Surveillance) functionality
- Recommissioning feature (privacy) with 32-bit kill password
- 32-bit access password to allow a transition into the secured state
- Long read/write ranges due to extremely low-power design
- Reliable operation of multiple tags due to advanced anti-collision (up to 800 tags/s)
- Fast initialization (write EPC)
- Forward link: 25 kbit/s to 100 kbit/s
- Return link: 53 kbit/s to 848 kbit/s

2.2 Key benefits

- High sensitivity provides long read range
- Highly advanced anti-collision resulting in highest identification speed
- Reliable and robust RFID technology suitable noisy environments and dense label populations

2.3 Custom features

- EAS
Enables the HF RFID tag to be used as EAS tag without the need for a backend data base.

3 Applications

- Healthcare and pharmaceutical supply chain
- Medical lab automation
- Document tracking
- Casino chips
- Laundry automation

4 Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|---|---------|
| | Name | Description | Version |
| SL2S1402FUD | Wafer | sawn, bumped wafer, 120 μm , on film frame carrier, C_i between LA and LB = 0 pF (typical) | - |
| SL2S1402FUF | Wafer | sawn, bumped wafer, 75 μm , on film frame carrier, C_i between LA and LB = 0 pF (typical) | - |
| SL2S1502FUD | Wafer | sawn, bumped wafer, 120 μm , on film frame carrier, C_i between LA and LB = 23.5 pF (typical) | - |
| SL2S1502FUF | Wafer | sawn, bumped wafer, 75 μm , on film frame carrier, C_i between LA and LB = 23.5 pF (typical) | - |
| SL2S1602FUD | Wafer | sawn, bumped wafer, 120 μm , on film frame carrier, C_i between LA and LB = 97 pF (typical) | - |
| SL2S1502FTB | XSON3 | plastic extremely thin small outline package; no leads; 3 terminals; body 1 x 1.45 x 0.5 mm; C_i between LA and LB = 23.5 pF (typical) | SOT1122 |

5 Block diagram

The SL2S1402; SL2S1502; SL2S1602 IC consists of three major blocks:

- Analog RF Interface
- Digital Controller
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader for being processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

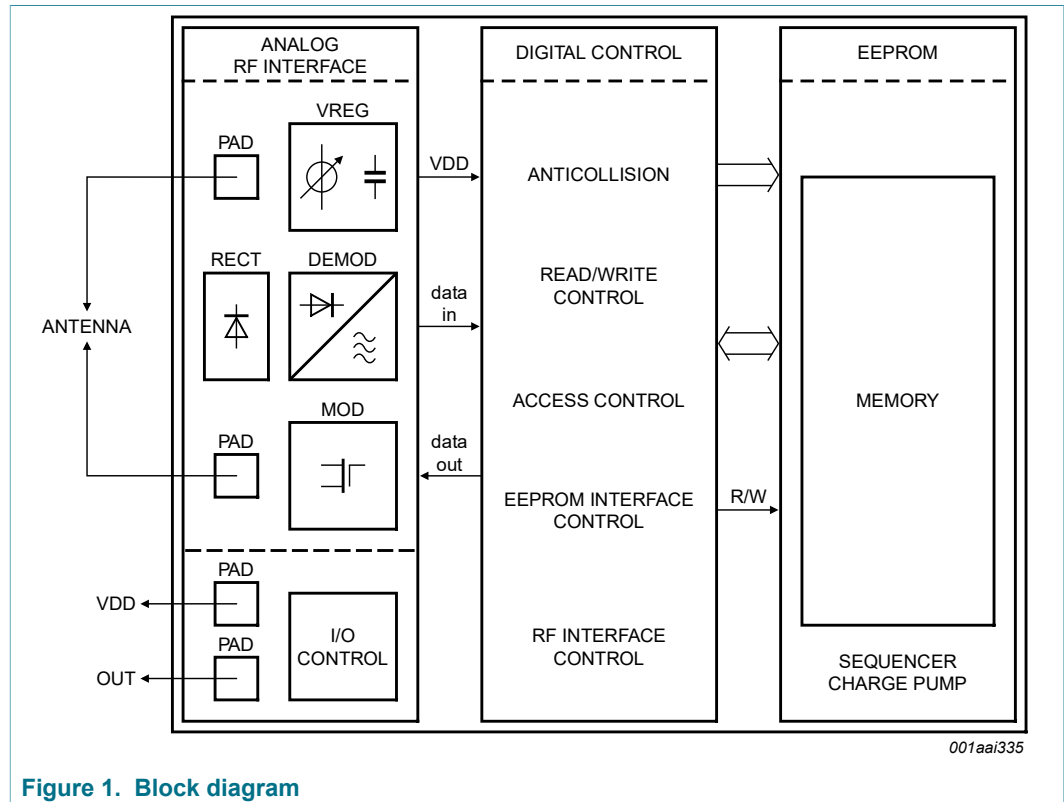


Figure 1. Block diagram

6 Pinning information

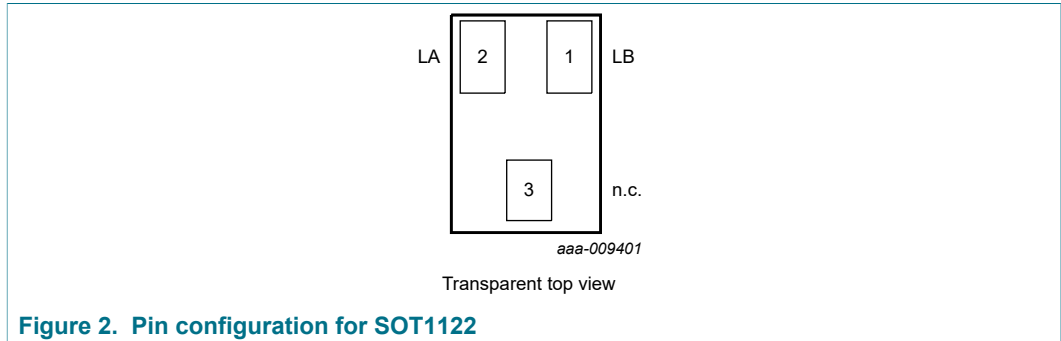
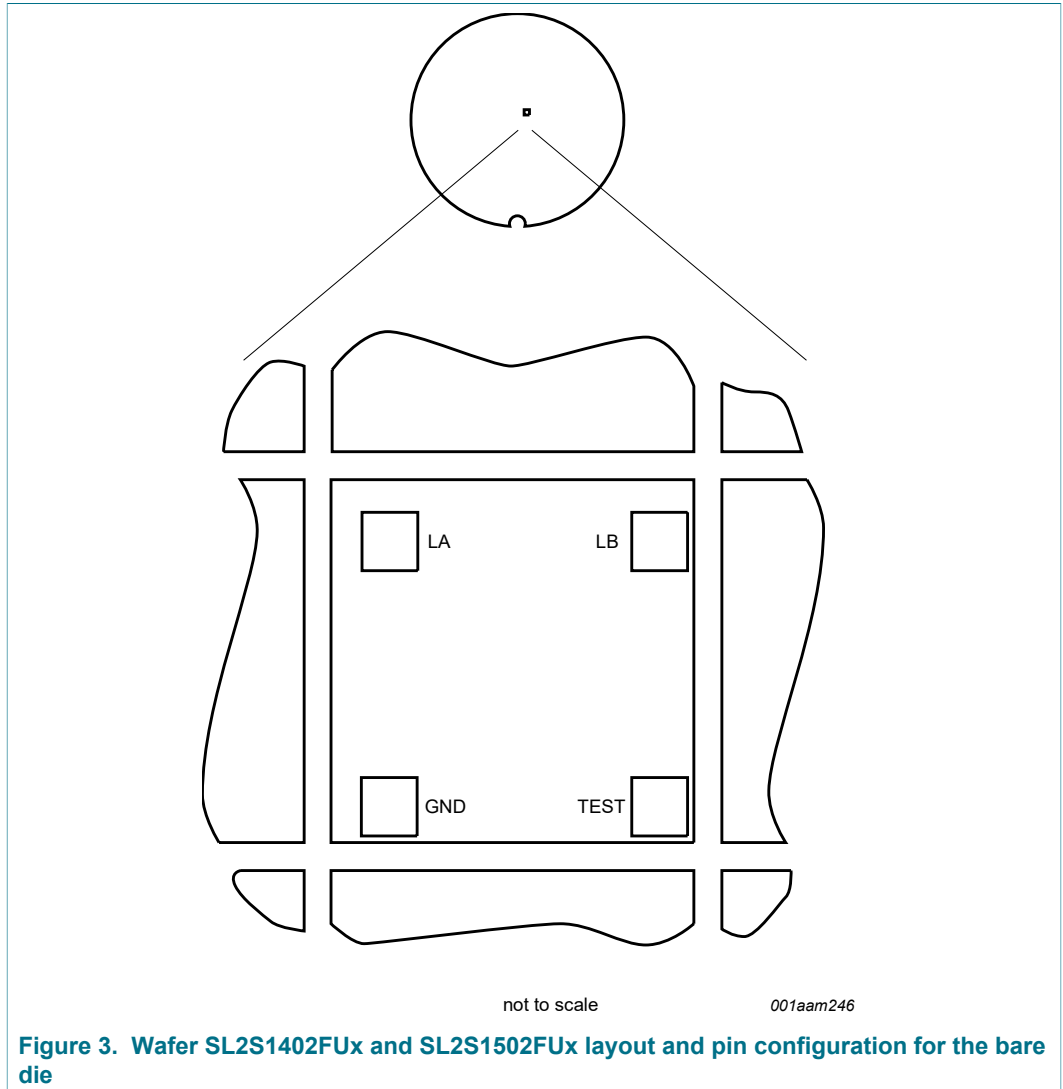


Table 2. Pin description SOT1122

| Pin | Symbol | Description |
|-----|--------|------------------|
| 1 | LB | antenna RF input |
| 2 | LA | antenna RF input |
| 3 | n.c. | not connected |

7 Wafer layout



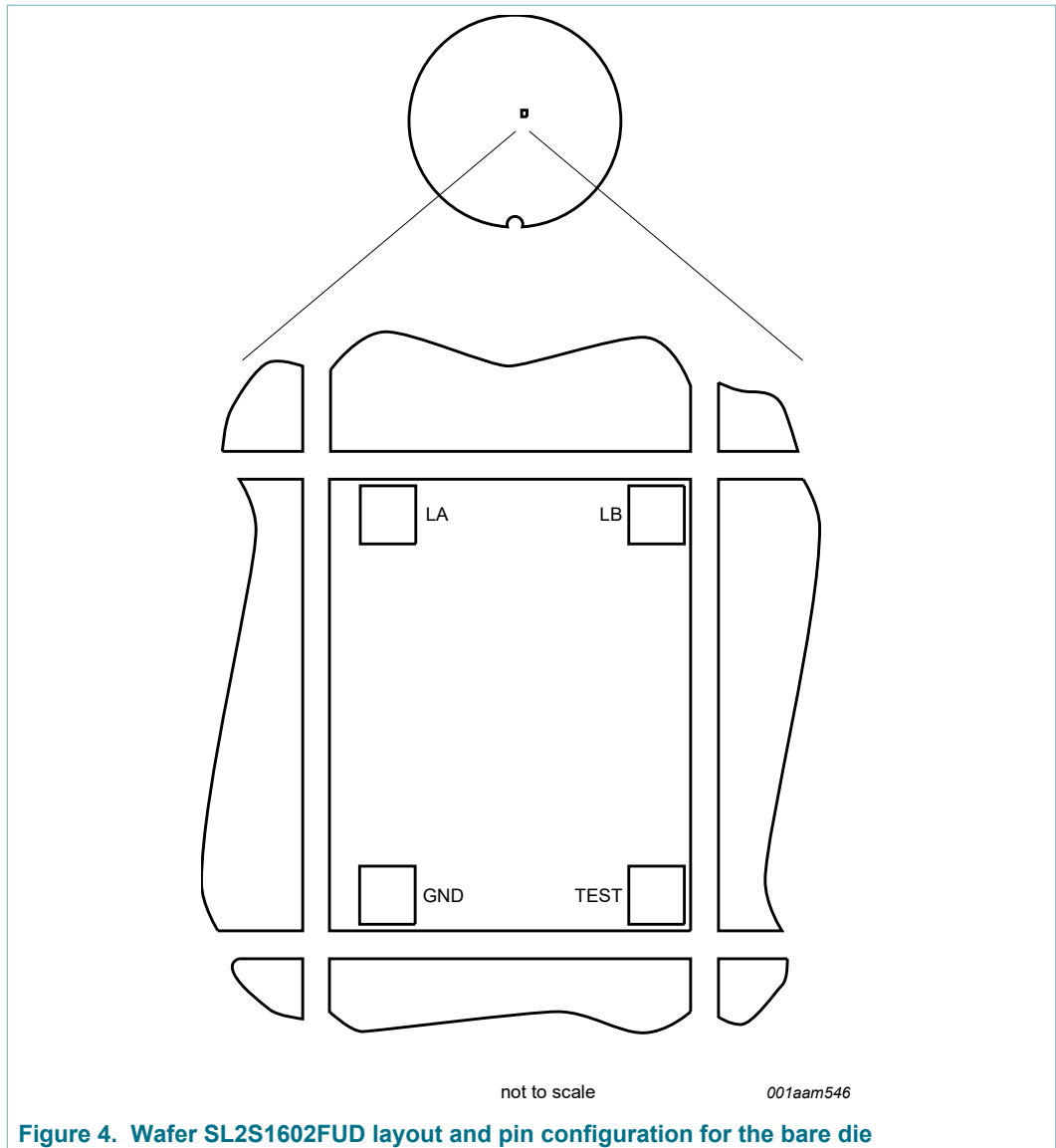


Figure 4. Wafer SL2S1602FUD layout and pin configuration for the bare die

Table 3. Bond pad description

| Symbol | Description |
|--------|------------------|
| LA | antenna RF input |
| LB | antenna RF input |
| GND | ground |
| TEST | test input |

8 Mechanical specification

8.1 Wafer specification

See [Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking"](#).

Table 4. Wafer specification

| Wafer | |
|---|---|
| Designation | each wafer is inscribed with batch number and wafer number |
| Diameter | 200 mm (8 inches) |
| Thickness | |
| SL2S1402FUD/ SL2S1502FUD/ SL2S1602FUD | 120 $\mu\text{m} \pm 15 \mu\text{m}$ |
| SL2S1402FUF/SL2S1502FUF | 75 $\mu\text{m} \pm 15 \mu\text{m}$ |
| Process | CMOS 0.14 μm |
| Batch size | 25 wafers |
| Dies per wafer | |
| SL2S1402FUx/SL2S1502FUx | 110050 |
| SL2S1602FUD | 88225 |
| Wafer backside | |
| Material | Si |
| Treatment | ground and stress release |
| Roughness | R_a minimum = 0.5 μm |
| | R_t maximum = 5 μm |
| Chip dimensions | |
| Die size without scribe | |
| SL2S1402FUx/SL2S1502FUx | 520 $\mu\text{m} \times 484 \mu\text{m} = 251680 \mu\text{m}^2$ |
| SL2S1602FUD | 520 $\mu\text{m} \times 607 \mu\text{m} = 315640 \mu\text{m}^2$ |
| Scribe line width | |
| X-dimension | 15 μm (scribe line width measured between nitride edges) |
| Y-dimension | 15 μm (scribe line width measured between nitride edges) |
| Number of pads | 4 |
| Pad location | non-diagonal/placed in chip corners |
| Distance pad to pad LA to LB | 400 μm |
| Distance pad to pad LB to TEST | |
| SL2S1402FUx/SL2S1502FUx | 360 μm |
| SL2S1602FUD | 517 μm |
| Passivation on front | |

| | |
|--------------------------|---|
| Type | sandwich structure |
| Material | PE-nitride (on top) |
| Thickness | 1.75 μm total thickness of passivation |
| Au bump | |
| Material | >99.9 % pure Au |
| Hardness | 35 HV to 80 HV 0.005 |
| Shear strength | >70 MPa |
| Height | 18 μm |
| Height uniformity | |
| within a die | $\pm 2 \mu\text{m}$ |
| within a wafer | $\pm 3 \mu\text{m}$ |
| wafer to wafer | $\pm 4 \mu\text{m}$ |
| Bump flatness | $\pm 1.5 \mu\text{m}$ |
| Bump size | |
| LA, LB | 60 μm \times 60 μm |
| TEST, GND | 60 μm \times 60 μm |
| variation | $\pm 5 \mu\text{m}$ |
| Under bump metallization | sputtered TiW |

8.1.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking"](#).

8.1.2 Map file distribution

See [Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking"](#).

9 Functional description

9.1 Power transfer

Whenever connected to a very simple and cheap type of antenna (as a result of the 13.56 MHz carrier frequency) made out of a few windings printed, wound, etched or punched coil the ICODE ILT IC can be operated without line of sight up to a distance of 1.5 m (gate width). No battery is needed.

9.2 Data transfer

9.2.1 Reader to tag Link

An interrogator transmits information to the ICODE ILT by modulating an RF signal in the 13.56 MHz frequency. The ICODE ILT receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least an inventory round. It communicates to the ICODE ILT by modulating an RF carrier using DSB-ASK with PIE encoding.

For further details refer to [Section 18](#), [Ref. 2](#). Interrogator-to-tag (R=>T) communications.

9.2.2 Tag to reader Link

An interrogator receives information from the ICODE ILT by transmitting a continuous-wave RF signal to the tag; the ICODE ILT responds by load modulation of the 13.56 MHz carrier frequency, thereby generating modulated sidebands used to transmit an information signal to the interrogator. The system is a reader talks first (RTF) system, meaning that a ICODE ILT only responds with an information signal after being directed by the interrogator.

ICODE ILT transmits information using ASK modulation. The returned data are either coded with FM0 baseband, Miller with sub carrier or Manchester with sub carrier. The interrogator can select if the ICODE ILT shall respond with a sub carrier frequency of 424 kHz or 848 kHz.

For further details refer to [Section 18](#), [Ref. 2](#). tag-to-interrogator (T=>R) communications.

9.3 Air interface standards

The ICODE ILT fully supports all parts of the ISO 18000-3 Mode 3 (refer to [Section 18](#), [Ref. 1](#)) and the "EPC™ Radio-Frequency Identity Protocols EPC Class-1 HF RFID Air Interface Protocol for Communications at 13.56 MHz, Version 2.0.3" (refer to [Section 18](#), [Ref. 2](#)).

10 Memory configuration

This section contains all information including commands by which a reader selects, inventories, and accesses a ICODE ILT population

An interrogator manages ICODE ILT equipped tag populations using three basic operations. Each of these operations comprises one or more commands. The operations are defined as follows:

Table 5. Tag populations

| Operation | Description |
|------------|--|
| Select: | The process by which an interrogator selects a tag population for inventory and access. Interrogators may use one or more Select commands to select a particular tag population prior to inventory. |
| Inventory: | The process by which an interrogator identifies ICODE ILT equipped tags. An interrogator begins an inventory round by transmitting a BeginRound command in one of two sessions. One or more tags may reply. The interrogator detects a single tag reply and requests the PC, EPC, and CRC-16 from the chip. An inventory round operates in one and only one session at a time. For an example of an interrogator inventorying and accessing a single tag refer to Section 18, Ref. 2 . |
| Access: | The process by which an interrogator transacts with (reads from or writes to) individual tags. An individual tag must be uniquely identified prior to access. Access comprises multiple commands, some of which employ one-time-pad based cover-coding of the R=>T link. |

10.1 Memory

For the general memory layout according to the standard [Section 18, Ref. 2](#). The tag memory is logically subdivided into four distinct banks.

In accordance to the standard [Section 18, Ref. 2](#). The tag memory of the ICODE ILT is organized in following 4 memory sections:

Table 6. Memory sections

| Name | Size | Bank |
|--|---------|------|
| Reserved memory (32-bit ACCESS and 32-bit KILL password) | 64 bit | 00b |
| EPC (excluding 16 bit CRC-16 and 16-bit PC) | 240 bit | 01b |
| TID (including unique 48 bit serial number) | 96 bit | 10b |

The logical address of all memory banks begin at zero (00h).

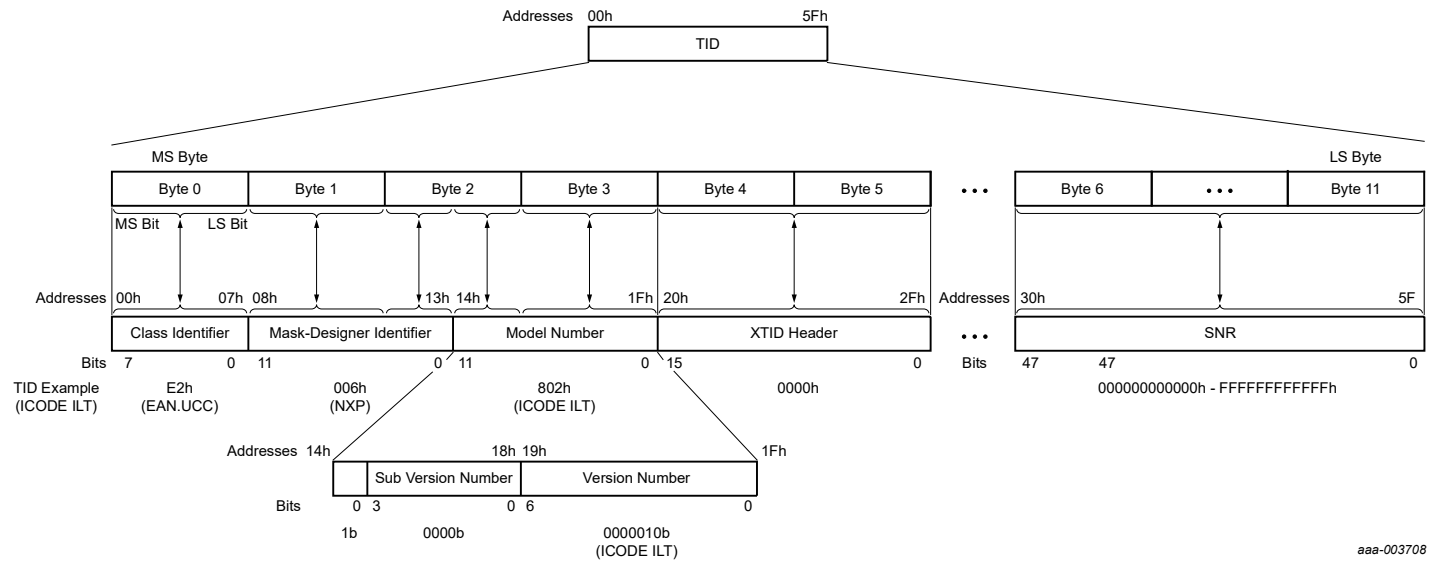


Figure 5. TID for ICODE ILT

Table 7. Model number

| | SI (Status Indicator Bit) | Sub Version No. | Version (Silicon) No. |
|-----------|---------------------------|-----------------|-----------------------|
| ICODE ILT | 1 | 0000b | 0000010b |

10.1.1 Memory map

Table 8. Memory map

| Bank address | Memory address | Type | Content | Initial ^[1] | Remark |
|--------------|----------------|----------|--|------------------------|---------------------------------|
| Bank 00 | 00h – 1Fh | Reserved | kill password: refer to Section 18, Ref. 2 | all 00h | unlocked memory |
| | 20h – 3Fh | Reserved | access password: refer to Section 18, Ref. 2 | all 00h | unlocked memory |
| Bank 01 | 00h – 0Fh | EPC | CRC-16: refer to Section 18, Ref. 2 | | memory mapped calculated CRC |
| | 10h – 14h | EPC | Backscatter length: refer to Section 18, Ref. 2 | 00110b | unlocked memory |
| | 15h | EPC | UMI refer to Section 18, Ref. 2 | 0b | unlocked memory |
| | 16h | EPC | XI: refer to Section 18, Ref. 2 | 0b | calculated |
| | 17h – 1Fh | EPC | Numbering system indicator: refer to Section 18, Ref. 2 | 00h | unlocked memory |
| | 20h - 10Fh | EPC | EPC: refer to Section 18, Ref. 2 | | unlocked memory |
| | 110h - 1FFh | EPC | RFU | 0000h | factory locked memory |
| | 200h - 20Fh | EPC | ConfigWord | 0000h | unlocked memory |
| | 210h - 21Fh | EPC | XPC_W1 | 0000h | factory locked memory |
| Bank 10 | 00h – 07h | TID | allocation class identifier: refer to Section 18, Ref. 2 | 1110 0010b | factory locked memory |
| | 08h – 13h | TID | tag mask designer identifier: refer to Section 18, Ref. 2 | 0000 0000 0110b | factory locked memory |
| | 14h – 1Fh | TID | tag model number: refer to Section 18, Ref. 2 | TMNR | factory locked memory |
| | 20h – 2Fh | TID | Extended TID header refer to Section 18, Ref. 3 | XTID Header | locked memory |
| | 30h – 5Fh | TID | serial number: refer to Section 18, Ref. 2 | SNR | locked memory |

[1] This is the initial memory content when delivered by NXP Semiconductors

10.1.1.1 Supported EPC types

The EPC types are defined in the EPC Tag Standards document from EPCglobal.

These standards define completely that portion of EPC tag data that is standardized, including how that data is encoded on the EPC tag itself (i.e. the EPC Tag Encodings),

as well as how it is encoded for use in the information systems layers of the EPC Systems Network (i.e. the EPC URI or Uniform Resource Identifier Encodings).

The EPC Tag Encodings include a Header field followed by one or more Value Fields. The Header field indicates the length of the Values Fields and contains a numbering system identifier (NSI). The Value Fields contain a unique EPC Identifier and optional Filter Value when the latter is judged to be important to encode on the tag itself.

11 Interrogator commands and tag replies

For a detailed description refer to [Section 18, Ref. 2](#).

11.1 Commands

An overview of interrogator to tag commands is located in [Section 18, Ref. 2](#).

Note that all mandatory commands are implemented on the ICODE ILT according to the standard. Additionally the optional command Access is supported by the ICODE ILT IC (for details refer to [Section 11.5 "Optional Access Command"](#)). Besides also custom commands are implemented on the ICODE ILT IC (for details refer to [Section 11.7 "Custom Commands"](#)).

11.2 Mandatory Select Commands

Select commands select a particular ICODE ILT tag population based on user-defined criteria.

11.2.1 Select

For a detailed description of the mandatory Select command refer to [Section 18, Ref. 2](#).

11.3 Mandatory Inventory Commands

Inventory commands are used to run the collision arbitration protocol.

11.3.1 BeginRound

For a detailed description of the mandatory BeginRound command refer to [Section 18, Ref. 2](#).

11.3.2 AdjustRound

For a detailed description of the mandatory AdjustRound command refer to [Section 18, Ref. 2](#).

11.3.3 NextSlot

For a detailed description of the mandatory NextSlot command refer to [Section 18, Ref. 2](#).

11.3.4 ACK

For a detailed description of the mandatory ACK command refer to [Section 18, Ref. 2](#).

11.3.5 NAK

For a detailed description of the mandatory NAK command refer to [Section 18, Ref. 2](#).

11.4 Mandatory Access Commands

Access commands are used to read or write data from or to the ICODE ILT memory. For a detailed description of the mandatory Access command refer to [Section 18, Ref. 2](#).

11.4.1 REQ_RN

Access commands are used to read or write data from or to the ICODE ILT memory. For a detailed description of the mandatory Access command refer to [Section 18, Ref. 2](#).

11.4.2 READ

For a detailed description of the mandatory Req_RN command refer to [Section 18, Ref. 2](#).

11.4.3 WRITE

For a detailed description of the mandatory Write command refer to [Section 18, Ref. 2](#).

11.4.4 KILL (RECOMMISSIONING)

Only mandatory asserted Recom bit 3SB is supported.

For a detailed description of the mandatory Kill command refer to [Section 18, Ref. 2](#).

11.4.5 LOCK

For a detailed description of the mandatory Lock command refer to [Section 18, Ref. 2](#).

11.5 Optional Access Command

11.5.1 Access

For a detailed description of the optional Access command refer to [Section 18, Ref. 2](#), section 6.3.2.10.

11.5.2 BlockWrite

The BlockWrite command supports the writing of up to two data words at once (WordCount = 00h to 02h). For a detailed description of the optional BlockWrite command refer to [Section 18, Ref. 2](#).

11.6 Optional Features

11.6.1 UMI

The UMI (User Memory Indicator bit 15h) of the Protocol-control (PC) word is supported using Method 2 (written by the reader). For a detailed description of the optional UMI bit refer to [Section 18, Ref. 2](#).

11.7 Custom Commands

11.7.1 ChangeConfigWord

The ConfigWord is located in the EPC Memory Bank at the memory address 200h - 20Fh. Dedicated bits in this word control the custom-specific feature EAS. Memory is accessible with Select and Read sequence.

The ChangeConfigWord command allows to read the dedicated bits in open and secured state. Changing these dedicated bits is only possible if the access password is not equal zero and the IC is in the secured state.

Table 9. ConfigWord

| Bank address | Memory address | Type | Initial | Remark |
|---------------|----------------|---------------|---------|--------|
| Bank 01 (EPC) | 200h - 20Eh | RFU | 0b | |
| | 20Fh | EAS Alarm bit | 0b | |

Table 10. ConfigWord details

| MSB | | | | | | | | | | | | | | | LSB |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------------|
| 200 hex | 201 hex | 202 hex | 203 hex | 204 hex | 205 hex | 206 hex | 207 hex | 208 hex | 209 hex | 20A hex | 20B hex | 20C hex | 20D hex | 20E hex | 20F hex |
| RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | EAS alarm bit |

Table 11. Command coding

| | Command | RFU | Data | RN | CRC-16 |
|-------------|-------------------|-----------|------------------------------------|--------|--------|
| No. of bits | 16 | 8 | 16 | 16 | 16 |
| Description | 11100000 00000111 | 0000 0000 | Toggle EAS Bit optionally XOR RN16 | handle | |

After completing a successful ChangeConfigWord command the ICODE ILT backscatters the reply within 20 ms shown below comprising a header (a 0-bit), the ConfigWord, the handle, and a CRC-16 calculated over the 0-bit, ConfigWord and handle.

Table 12. ChangeConfigWord command response

| | Header | Status bits | RN | CRC-16 |
|-------------|--------|-------------|--------|--------|
| No. of bits | 1 | 16 | 16 | 16 |
| Description | 0 | ConfigWord | handle | |

If the toggle bits are transmitted with a value of 00h the ICODE ILT responds with a successful Change ConfigWord reply (i.e. the ConfigWord) which allows to read the actual ConfigWord content.

If the ICODE ILT encounters an error during execution of ChangeConfigWord it backscatters an error code (see [Section 18](#), [Ref. 2](#) for error-code definitions and for the reply format).

Table 13. Command response table

| Starting state | Condition | Response | Next state |
|--------------------------------|--|--|------------|
| ready | all | - | ready |
| arbitrate, reply, acknowledged | all | - | arbitrate |
| open | valid handle, ConfigWord needs to change | Backscatter unchanged ConfigWord immediately | open |
| | valid handle, ConfigWord does not need to change | Backscatter ConfigWord immediately | open |
| secured | valid handle, ConfigWord needs to change | Backscatter modified ConfigWord, when done | secured |
| | valid handle, ConfigWord does not need to change | Backscatter ConfigWord immediately | secured |
| | invalid handle | - | secured |
| killed | all | - | killed |

11.8 Custom features

11.8.1 EAS

The ICODE ILT offers an EAS feature which can be enabled or disabled with the ChangeConfigWord command by toggling the EAS Alarm bit.

Only tags with the EAS Alarm bit set to 1 will respond to the following command sequence (inventory round) with their EPC:

1. Select command to the EAS Alarm bit with the parameters
 MemBank: 01h (EPC)
 Action: 010b (deassert SL if not matching)
 Pointer: 20Fh
 Mask length: 01h
 Mask: 1b
2. BeginRound
3. ACK

11.8.2 FastInitialWrite

If the memory content where data shall be written is completely 00h the write command will be executed within shorter time. The FastInitialWrite is internally executed for all commands where the memory content is changed (e.g. Write, Lock, BlockWrite, BlockPermalock,...).

12 Limiting values

Table 14. Limiting values (Wafer)^{[1][2]}

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---------------------|---------------------------------|------------------|------------|-----|------|------|
| T _{stg} | storage temperature | | | -55 | +125 | °C |
| P _{tot} | total power dissipation | | | - | 125 | mW |
| T _j | junction temperature | | | -40 | +85 | °C |
| I _{i(max)} | maximum input current | LA to LB; peak | [3] | - | ±60 | mA |
| I _I | input current | LA to LB; RMS | | - | 30 | mA |
| V _{ESD} | electrostatic discharge voltage | Human body model | [4] [5] | - | ±2 | kV |

- [1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the operating conditions and electrical characteristics sections of this specification is not implied.
- [2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- [3] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_I).
- [4] For ESD measurement, the IC was mounted in a CDIP8 package.
- [5] HBM: ANSI/ESDA/JEDEC JS-001

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13 Characteristics

13.1 Memory characteristics

Table 15. EEPROM characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-----------------|---|--------|-----|-----|-------|
| t_{ret} | retention time | $T_{\text{amb}} \leq 55 \text{ }^\circ\text{C}$ | 50 | - | - | year |
| $N_{\text{endu(W)}}$ | write endurance | | 100000 | - | - | cycle |

13.2 Interface characteristics

Table 16. Interface characteristics

Typical ratings are not guaranteed. The values listed are at room temperature.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-------------------------------|---------------------------|----------------------|-----|--------|-------|--------|---------------|
| f_i | input frequency | | [1] | 13.553 | 13.56 | 13.567 | MHz |
| $V_{i(\text{RMS})\text{min}}$ | minimum RMS input voltage | operating read/write | | 1.5 | - | 1.7 | V |
| $P_{i(\text{min})}$ | minimum input power | operating | [2] | - | 40 | - | μW |
| C_i | input capacitance | between LA and LB | [3] | | | | |
| | | SL2S1402FUx | | - | - | - | pF |
| | | SL2S1502FUx | | 22.3 | 23.5 | 24.7 | pF |
| | | SL2S1602FUD | | 92 | 97 | 102 | pF |

[1] Bandwidth limitation (± 7 kHz) according to ISM band regulations.

[2] Including losses in the resonant capacitor and rectifier.

[3] Measured with an HP4285A LCR meter at 13.56 MHz and 2 V RMS.

14 Marking

14.1 Marking SOT1122

Table 17. Marking SOT1122

| Type number | Marking code |
|-------------|--------------|
| SL2S1502FTB | S0 |

15 Package outline

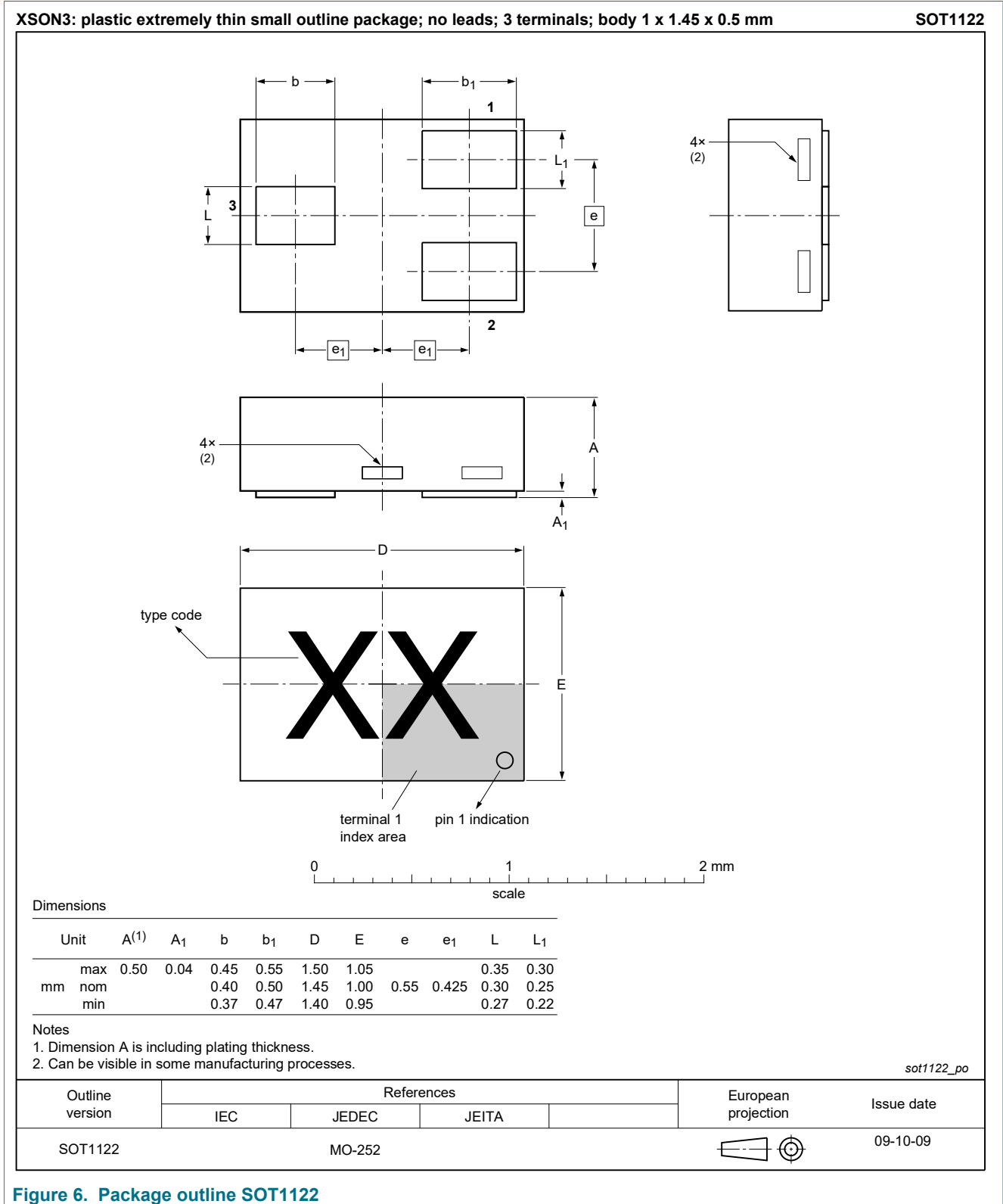
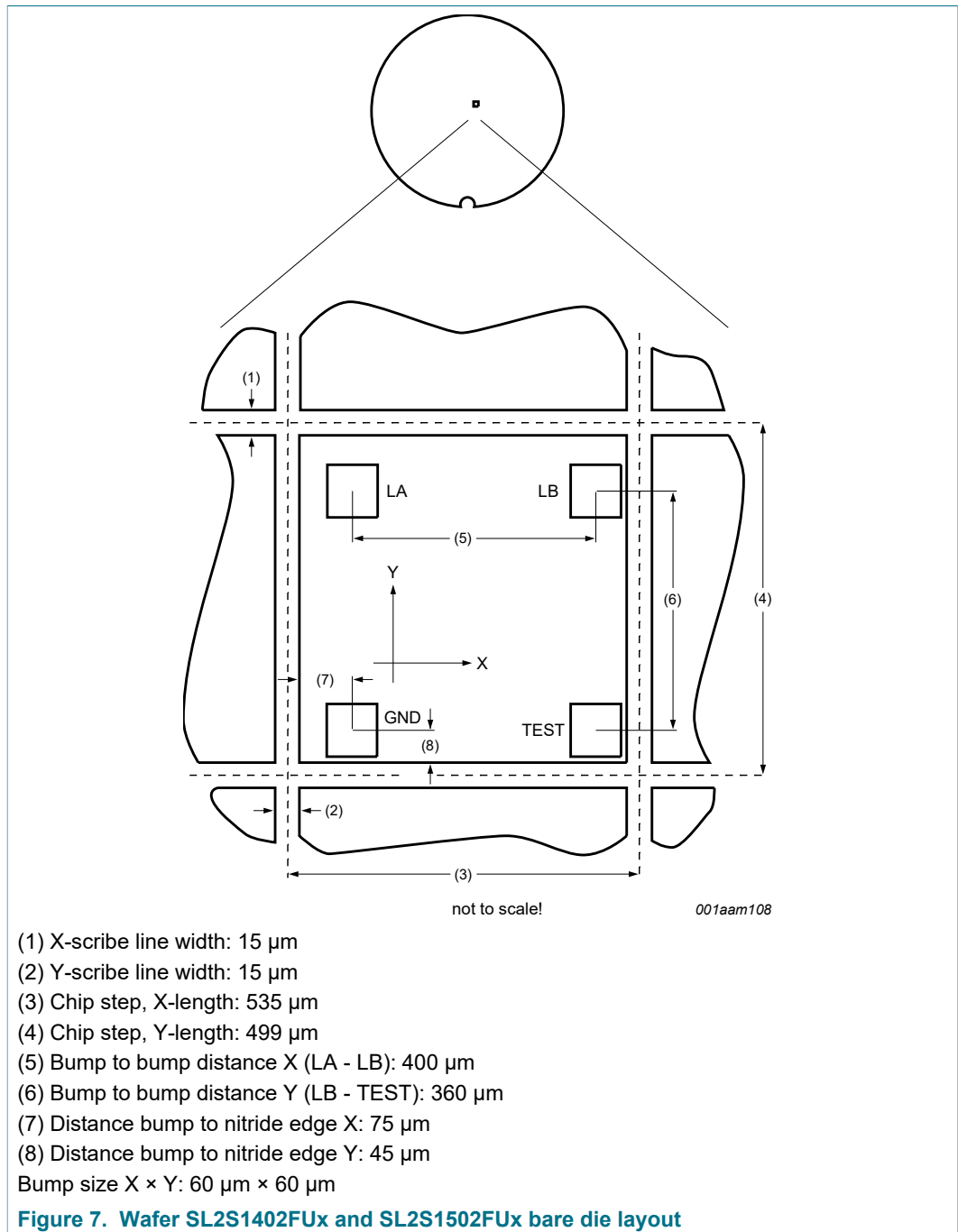
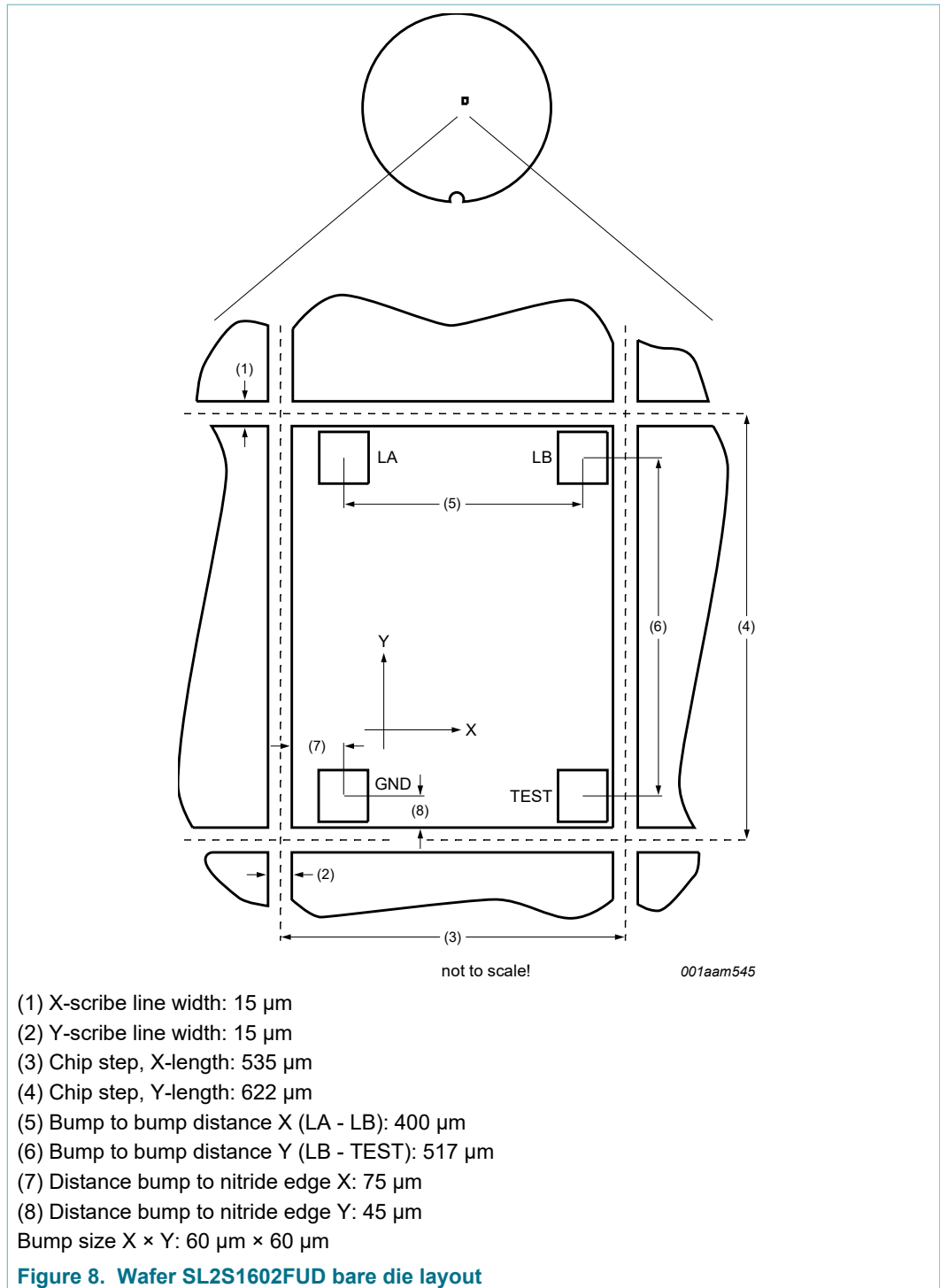


Figure 6. Package outline SOT1122

16 Bare die outline





17 Abbreviations

Table 18. Abbreviations

| Acronym | Description |
|-------------------|---|
| CRC | Cyclic redundancy check |
| CW | Continuous wave |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EPC | Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number) |
| FM0 | Bi phase space modulation |
| IC | Integrated Circuit |
| LSB | Least Significant Byte/Bit |
| MSB | Most Significant Byte/Bit |
| NRZ | Non-Return to Zero coding |
| RF | Radio Frequency |
| RTF | Reader Talks First |
| Tari | Type A Reference Interval (ISO 18000-3 mode 3/EPC Class-1 HF) |
| HF | High Frequency |
| XX _b | Value in binary notation |
| XX _{hex} | Value in hexadecimal notation |

18 References

1. ISO 18000-3M3
2. EPC™ Radio-Frequency Identity Protocols EPC Class-1 HF RFID Air Interface Protocol for Communications at 13.56 MHz, Version 2.0.3
3. EPCglobal: EPC Tag Data Standards 1.5
4. ECC ERC Recommendation 70-03 Annex 9
5. ISO/IEC Directives, Part 2: Rules for the structure and drafting of International Standards
6. ISO/IEC 3309: Information technology – Telecommunications and information exchange between systems – High-level data link control (HDLC) procedures – Frame structure
7. ISO/IEC 15961: Information technology, Automatic identification and data capture – Radio frequency identification (RFID) for item management – Data protocol: application interface
8. ISO/IEC 15962: Information technology, Automatic identification and data capture techniques – Radio frequency identification (RFID) for item management – Data protocol: data encoding rules and logical memory functions
9. ISO/IEC 15963: Information technology — Radio frequency identification for item management — Unique identification for RF tags
10. ISO/IEC 18000-1: Information technology — Radio frequency identification for item management — Part 1: Reference architecture and definition of parameters to be standardized
11. ISO/IEC 19762: Information technology AIDC techniques – Harmonized vocabulary – Part 3: radio-frequency identification (RFID)
12. U.S. Code of Federal Regulations (CFR), Title 47, Chapter I, Part 15: Radio-frequency devices, U.S. Federal Communications Commission

[13]

General specification for 8" wafer on UV-tape with electronic fail die marking, Delivery type description – BU-ID document number: 1093**¹.

1 ** ... document version number

19 Revision history

Table 19. Revision history

| Document ID | Release date | Data sheet status | Supersedes |
|--------------------------------------|--|--------------------|--------------------------------------|
| SL2S1402_SL2S1502_SL2S1602 v. 3.3 | 20191015 | Product data sheet | SL2S1402_SL2S1502_SL2S1602 v. 3.2 |
| Modifications: | <ul style="list-style-type: none"> 75 μ wafer thickness delivery types SL2S1402FUF and SL2S1502FUF in Section 4 "Ordering Information" and Section 8.1 "Wafer specification" added | | |
| SL2S1402_SL2S1502_SL2S1602 v. 3.2 | 20131008 | Product data sheet | SL2S1402_SL2S1502_SL2S1602 v. 3.1 |
| Modifications: | <ul style="list-style-type: none"> Type SL2S1502FTB added Section 14 "Marking" and Section 15 "Package outline": added | | |
| SL2S1402_SL2S1502_SL2S1602 v. 3.1 | 20130923 | Product data sheet | SL2S1402_SL2S1502_SL2S1602 v. 3.0 |
| Modifications: | <ul style="list-style-type: none"> Security status changed into COMPANY PUBLIC | | |
| SL2S1402_SL2S1502_SL2S1602 v. 3.0 | 20120522 | Product data sheet | - |

20 Legal information

20.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own

risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — While NXP Semiconductors has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP Semiconductors accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

ICODE and I-CODE — are trademarks of NXP B.V.

Tables

| | | | | | |
|----------|-------------------------------|----|----------|---|----|
| Tab. 1. | Ordering information | 4 | Tab. 11. | Command coding | 18 |
| Tab. 2. | Pin description SOT1122 | 6 | Tab. 12. | ChangeConfigWord command response | 18 |
| Tab. 3. | Bond pad description | 8 | Tab. 13. | Command response table | 19 |
| Tab. 4. | Wafer specification | 9 | Tab. 14. | Limiting values (Wafer) | 20 |
| Tab. 5. | Tag populations | 12 | Tab. 15. | EEPROM characteristics | 21 |
| Tab. 6. | Memory sections | 12 | Tab. 16. | Interface characteristics | 21 |
| Tab. 7. | Model number | 14 | Tab. 17. | Marking SOT1122 | 22 |
| Tab. 8. | Memory map | 14 | Tab. 18. | Abbreviations | 26 |
| Tab. 9. | ConfigWord | 18 | Tab. 19. | Revision history | 28 |
| Tab. 10. | ConfigWord details | 18 | | | |

Figures

| | | | | | |
|---------|--|---|---------|--|----|
| Fig. 1. | Block diagram | 5 | Fig. 5. | TID for ICODE ILT | 13 |
| Fig. 2. | Pin configuration for SOT1122 | 6 | Fig. 6. | Package outline SOT1122 | 23 |
| Fig. 3. | Wafer SL2S1402FUx and SL2S1502FUx layout and pin configuration for the bare die | 7 | Fig. 7. | Wafer SL2S1402FUx and SL2S1502FUx bare die layout | 24 |
| Fig. 4. | Wafer SL2S1602FUD layout and pin configuration for the bare die | 8 | Fig. 8. | Wafer SL2S1602FUD bare die layout | 25 |

Contents

| | | | | | |
|-----------|--|-----------|-----------|---------------------------|-----------|
| 1 | General description | 1 | 13.2 | Interface characteristics | 21 |
| 2 | Features and benefits | 2 | 14 | Marking | 22 |
| 2.1 | Key features | 2 | 14.1 | Marking SOT1122 | 22 |
| 2.2 | Key benefits | 2 | 15 | Package outline | 23 |
| 2.3 | Custom features | 2 | 16 | Bare die outline | 24 |
| 3 | Applications | 3 | 17 | Abbreviations | 26 |
| 4 | Ordering information | 4 | 18 | References | 27 |
| 5 | Block diagram | 5 | 19 | Revision history | 28 |
| 6 | Pinning information | 6 | 20 | Legal information | 29 |
| 7 | Wafer layout | 7 | | | |
| 8 | Mechanical specification | 9 | | | |
| 8.1 | Wafer specification | 9 | | | |
| 8.1.1 | Fail die identification | 10 | | | |
| 8.1.2 | Map file distribution | 10 | | | |
| 9 | Functional description | 11 | | | |
| 9.1 | Power transfer | 11 | | | |
| 9.2 | Data transfer | 11 | | | |
| 9.2.1 | Reader to tag Link | 11 | | | |
| 9.2.2 | Tag to reader Link | 11 | | | |
| 9.3 | Air interface standards | 11 | | | |
| 10 | Memory configuration | 12 | | | |
| 10.1 | Memory | 12 | | | |
| 10.1.1 | Memory map | 14 | | | |
| 10.1.1.1 | Supported EPC types | 14 | | | |
| 11 | Interrogator commands and tag replies | 16 | | | |
| 11.1 | Commands | 16 | | | |
| 11.2 | Mandatory Select Commands | 16 | | | |
| 11.2.1 | Select | 16 | | | |
| 11.3 | Mandatory Inventory Commands | 16 | | | |
| 11.3.1 | BeginRound | 16 | | | |
| 11.3.2 | AdjustRound | 16 | | | |
| 11.3.3 | NextSlot | 16 | | | |
| 11.3.4 | ACK | 16 | | | |
| 11.3.5 | NAK | 16 | | | |
| 11.4 | Mandatory Access Commands | 17 | | | |
| 11.4.1 | REQ_RN | 17 | | | |
| 11.4.2 | READ | 17 | | | |
| 11.4.3 | WRITE | 17 | | | |
| 11.4.4 | KILL (RECOMMISSIONING) | 17 | | | |
| 11.4.5 | LOCK | 17 | | | |
| 11.5 | Optional Access Command | 17 | | | |
| 11.5.1 | Access | 17 | | | |
| 11.5.2 | BlockWrite | 17 | | | |
| 11.6 | Optional Features | 17 | | | |
| 11.6.1 | UMI | 17 | | | |
| 11.7 | Custom Commands | 17 | | | |
| 11.7.1 | ChangeConfigWord | 18 | | | |
| 11.8 | Custom features | 19 | | | |
| 11.8.1 | EAS | 19 | | | |
| 11.8.2 | FastInitialWrite | 19 | | | |
| 12 | Limiting values | 20 | | | |
| 13 | Characteristics | 21 | | | |
| 13.1 | Memory characteristics | 21 | | | |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 October 2019

Document identifier: SL2S1402_SL2S1502_SL2S1602

Document number: 234333