

NOIV1SN016KA, NOIV1SN012KA

VITA 16/12 MegaPixels Single Foot Print CMOS Image Sensor



ON Semiconductor®

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Features

- Active Pixel Array:
 - ◆ 16K = 4096 × 4096 Active Pixels
 - ◆ 12K = 4096 × 3072 Active Pixels
- Optical Format:
 - ◆ 16K = APS-C Optical Format
 - ◆ 12K = 4/3 inch Optical Format
- 4.5 μm × 4.5 μm Square Pixels
- 32/16 Low-Voltage Differential Signaling (LVDS) High-speed Serial Outputs
- VITA 16K Frame Rate at Full Resolution, 32 LVDS Outputs
 - ◆ 80 Frames per Second normal ROT
 - ◆ 125 Frames per Second Zero ROT
- VITA 12K Frame Rate at Full Resolution, 32 LVDS Outputs
 - ◆ 110 Frames per Second normal ROT
 - ◆ 160 Frames per Second Zero ROT
- Monochrome (SN), Color (SE)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 8-bit or 10-bit Output Mode
- 32 Random Programmable Region of Interest (ROI) readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- Serial Peripheral Interface (SPI)
- Operational Temperature Range: -40°C to +85°C
- Single 355-pin μPGA package across resolutions
- Power Dissipation: 4.1 W @ 2 Gpix/s
- These Devices are Pb-Free and are RoHS Compliant

Description

The high-resolution VITA CMOS image sensor family features global and rolling shutter mode. The on-chip programmable state machine controls the sensor array and enables high flexibility with changes in operation modes and 32 frame-to-frame configurable Regions-of-Interest (ROI). The 5T pixel on a 4.5 μm pitch enables pipelining of integration and read-out in both triggered and un-triggered global shutter mode.

A second pipeline stage provides a maximum frame rate increase by allowing the sensor to run in Zero-ROT mode. The roller shutter mode supports correlated double sampling, reducing temporal noise by approximately 3 dB. The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The image's black level has an automatic calibration with adjustable user programmable offset. The image data interface consists of 32 or 16 LVDS channels with additional clock and synchronization channels in parallel, each running at 680 Mbps.

The high-resolution VITA family is packaged in a ceramic 355-pin PGA package and is available in a monochrome and color version.

Contact your local ON Semiconductor office for more information.

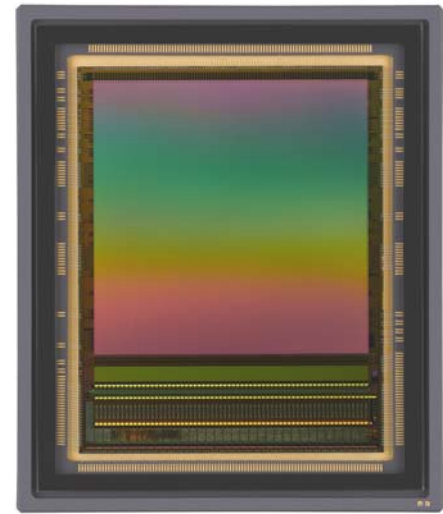


Figure 1. VITA 16K/12K Photograph

Applications

- Machine Vision
- Motion Monitoring
- Intelligent Traffic Systems (ITS)
- Pick and Place Machines
- Inspection
- Metrology

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ORDERING INFORMATION

| Part Number | Family | Description | Package | Product Status | | |
|------------------|----------|--|-------------------|----------------|-------------------|------------|
| NOIV1SN016KA-GDI | VITA 16K | 16 MegaPixel, Monochrome, no Protective Tape | 355-pin μ PGA | Production | | |
| NOIV1SE016KA-GDI | | 16 MegaPixel, Color, no Protective Tape | | | | |
| NOIV1SN016KA-GTI | | 16 MegaPixel, Monochrome, Protective Tape | | | | |
| NOIV1SE016KA-GTI | | 16 MegaPixel, Color, Protective Tape | | | | |
| NOIV1SN012KA-GDI | VITA 12K | 12 MegaPixel, Monochrome, no Protective Tape | | | 355-pin μ PGA | Production |
| NOIV1SE012KA-GDI | | 12 MegaPixel, Color, no Protective Tape | | | | |
| NOIV1SN012KA-GTI | | 12 MegaPixel, Monochrome, Protective Tape | | | | |
| NOIV1SE012KA-GTI | | 12 MegaPixel, Color, Protective Tape | | | | |

The V1 – SN/SE base part is used to reference the mono and color enhanced versions of the LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310-D.PDF

Package Mark

Side 1 near Pin 1: **NOIV1xx0RRKA-GDI**, where xx denotes mono micro lens (SN) or color micro lens (SE), RR is the resolution of the sensor in MP (16 or 12)

Side 2: **AWLYYWW**, where AWL is Production lot traceability, and YYWW is the 4-digit date code

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SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

| Parameter | Specification |
|------------------------|--|
| Active pixels | 4096 (H) x 4096 (V) |
| Pixel size | 4.5 μm x 4.5 μm |
| Shutter type | Pipelined and triggered global shutter, rolling shutter |
| Master clock | 340 MHz (10-bit default) 272 MHz (8-bit) |
| Windowing features | 32 Randomly programmable windows. Normal, sub-sampled and binned readout modes |
| ADC resolution | 10-bit, 8-bit |
| Number of LVDS outputs | 32/16 data + 1 sync + 1 clock |
| Data rate | 32/16 x 680 Mbps (10-bit default) 32/16 x 544 Mbps (8-bit) |
| Power dissipation | 4.1 W @ ~2 Gpix/s (32 LVDS) |
| Package type | 355 μPGA |
| Color | RGB color, mono |

Table 2. ELECTRO-OPTICAL SPECIFICATIONS [1]

| Parameter | Specification |
|-----------------------------------|---|
| Frame rate at full resolution | Refer to Table 6 |
| Optical format | APS-C |
| Conversion gain | 0.064 LSB $_{10}$ /e $^{-}$, 79.4 $\mu\text{V}/\text{e}^{-}$ |
| Dark noise | 34e $^{-}$ in global shutter 23e $^{-}$ in rolling shutter |
| Responsivity at 550 nm | 3.1 V/lux.s |
| Parasitic Light Sensitivity (PLS) | <1/800 at 550 nm |
| Full well charge | 19000 e $^{-}$ |
| Quantum efficiency (QE) x FF | 52% at 550 nm |
| Pixel FPN | rolling shutter: 0.7 LSB $_{10}$ global shutter: 4.2 LSB $_{10}$ |
| Row FPN | rolling shutter: 0.4 LSB $_{10}$ global shutter: 0.7 LSB $_{10}$ |
| Column FPN | rolling shutter: 0.4 LSB $_{10}$ global shutter: 0.5 LSB $_{10}$ |
| Dynamic range | 53 dB in global shutter mode 56 dB in rolling shutter mode |
| Signal-to-Noise Ratio (SNR) | 43 dB |
| Dark signal | 22 e $^{-}$ /s, 1.3 LSB $_{10}$ /s at +40°C |

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

| Symbol | Description | Min | Max | Units |
|--------|-----------------------------|-----|-----|-------|
| T $_J$ | Operating temperature range | -40 | +85 | °C |

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 3)

| Symbol | Parameter | Min | Max | Units |
|---|---|------|-----|-------|
| ABS (1.0 V supply) | ABS rating for 1.0 V supply | -0.5 | 1.2 | V |
| ABS (1.8 V supply group) | ABS rating for 1.8 V supply group | -0.5 | 2.2 | V |
| ABS (3.3 V supply group) | ABS rating for 3.3 V supply group | -0.5 | 4.3 | V |
| ABS (4.2 V supply) | ABS rating for 4.2 V supply | -0.5 | 4.6 | V |
| ABS (4.5 V supply) | ABS rating for 4.5 V supply | -0.5 | 5.0 | V |
| T $_S$ (Notes 3 and 4) | ABS storage temperature range | 0 | 150 | °C |
| | ABS storage humidity range at 85°C | | 85 | %RH |
| Electrostatic discharge (ESD) (Notes 2 and 3) | Human Body Model (HBM): JS-001-2010 | 2000 | | V |
| | Charged Device Model (CDM): JESD22-C101 | 500 | | |
| LU | Latch-up: JESD-78 | 140 | | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- While the ADC is 11-bit, the data is converted to 10-bit in two digital gain stages. The first digital gain stage has a fixed gain of 2/3. This may be bypassed by asserting register bit 129[11]. The second digital gain stage can be tuned by changing the value in register 205.
- Operating ratings are conditions in which operation of the device is intended to be functional.
- ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
- Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

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Electrical Specifications

Power Supply Ratings

Table 5. POWER SUPPLY RATINGS

Limits in bold apply for for $T_J = T_{MIN}$ to T_{MAX} , all other limits $T_J = +30^{\circ}C$ [5], [6], [7], [8]

| Parameter | Description | Min | Typ | Max | Units |
|---|--|--------------|------|------------|-------|
| Power Supply Parameters | | | | | |
| vdda_33 | Analog supply - 3.3 V domain. gnda_33 is connected to substrate | 3 | 3.3 | 3.6 | V |
| ldda_33 | Current consumption from analog supply | | 915 | | mA |
| vddd_33 | Digital supply - 3.3 V domain. gndd_33 is connected to substrate | 3 | 3.3 | 3.6 | V |
| lddd_33 | Current consumption from 3.3 V digital supply | | 90 | | mA |
| vdd_18 | Digital supply - 1.8 V domain. gndd_18 is connected to substrate | 1.6 | 1.8 | 2 | V |
| lidd_18 | Current consumption 1.8 V digital supply | | 370 | | mA |
| vdd_pix | Pixel array supply | 3 | 3.3 | 3.6 | V |
| lidd_pix | Current consumption from pixel supply | | 35 | | mA |
| vdd_resfd | Floating diffusion reset supply | 3.3 | 4.5 | 4.6 | V |
| gnd_resfd | Floating diffusion reset ground. Not connected to substrate | 0 | 0 | 1.0 | V |
| vdd_respd | Photo diode reset supply | 3.3 | 4.2 | 4.6 | V |
| gnd_respd | Photo diode reset ground. Not connected to substrate. Note This is a sinking power supply with 200 mA range. | 0 | 0 | 1.0 | V |
| vdd_trans | Pixel transfer supply | 3.3 | 4.2 | 4.6 | V |
| gnd_trans | Pixel transfer ground. Not connected to substrate | 0 | 0 | 1.0 | V |
| vdd_sel | Pixel select supply | 3.0 | 3.3 | 3.6 | V |
| gnd_sel | Pixel select ground. Not connected to substrate. | 0 | 0 | 0 | V |
| vdd_casc | Cascode supply | 0.9 | 1.0 | 1.1 | V |
| vref_colmux [8] | Column multiplexer reference supply | – | 1.0 | – | V |
| gnd_colbias | Column biasing ground. Dedicated ground signal for pixel biasing. Connected to substrate | – | 0 | – | V |
| gnd_colpc | Column precharge ground. Dedicated ground signal for pixel biasing. Not connected to substrate | – | 0 | – | V |
| Ptot | Total power consumption | | 4100 | | mW |
| Pstby1 | Power consumption in standby mode, reset_n = high, clock running | – | 300 | – | mW |
| Pstby2 | Power consumption in standby mode, reset_n = low, clock running | – | 200 | – | mW |
| Pstby3 | Power consumption in standby mode, reset_n = low, no clock | – | 30 | – | mW |
| Popt | Power consumption at lower pixel rates | Configurable | | | |
| I/O - LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed | | | | | |
| fserdata | Data rate on data channels in 10-bit mode DDR signaling | | | 680 | Mbps |
| fserdata | Data rate on data channels in 8-bit mode DDR signaling | | | 544 | Mbps |
| fserclock | Clock rate of output clock in 10-bit mode Clock output for mesochronous signaling | | | 340 | MHz |
| fserclock | Clock rate of output clock in 8-bit mode Clock output for mesochronous signaling | | | 272 | MHz |
| Vicm | LVDS input common mode level | 0.3 | 1.25 | 2.2 | V |
| Tcck | Channel to channel skew (training pattern allows per-channel skew correction) | | | 50 | ps |

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Table 5. POWER SUPPLY RATINGS

Limits in bold apply for for $T_J = T_{MIN}$ to T_{MAX} , all other limits $T_J = +30^{\circ}C$ [5], [6], [7], [8]

| Parameter | Description | Min | Typ | Max | Units |
|----------------------------------|----------------------------------|-----|-----|-----|-------|
| LVDS Electrical/Interface | | | | | |
| fin | Input clock rate for 10-bit mode | | | 340 | MHz |
| fin | Input clock rate for 8-bit mode | | | 272 | MHz |
| tfdc | Input clock duty cycle | 45 | 50 | 55 | % |
| tj | Input clock jitter | | 20 | | ps |
| fspi | SPI clock rate | | | 10 | MHz |
| ratspi | 10-bit: ratio: Fin/fspi | 30 | | | |
| | 8-bit: ratio: Fin/fspi | 24 | | | |

5. All parameters are characterized for DC conditions after thermal equilibrium is established.

6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.

7. Minimum and maximum limits are guaranteed through test and design.

8. Vref_colmux supply should be able to source and sink current

Disclaimer: Image sensor products and specifications are subject to change without notice. Products are warranted to meet the production data sheet and acceptance criteria specifications only.

Table 6. FRAME RATE

| Parameter | Description | 32 LVDS Channels | | Units |
|-----------|---|------------------|---------|-------|
| | | Zero ROT | | |
| | | Disabled | Enabled | |
| fps_roi1 | $X_{res} \times Y_{res} = 4096 \times 4096$ | 80 | 125 | fps |
| fps_roi2 | $X_{res} \times Y_{res} = 4096 \times 3072$ | 110 | 160 | fps |
| fps_roi3 | $X_{res} \times Y_{res} = 3072 \times 3072$ | 130 | 215 | fps |
| fps_roi4 | $X_{res} \times Y_{res} = 2048 \times 2048$ | 245 | 470 | fps |
| fps_roi5 | $X_{res} \times Y_{res} = 1920 \times 1080$ | 470 | 880 | fps |
| fps_roi6 | $X_{res} \times Y_{res} = 1024 \times 1024$ | 640 | 920 | fps |
| fps_roi7 | $X_{res} \times Y_{res} = 640 \times 480$ | 1475 | 1860 | fps |
| fps_roi8 | $X_{res} \times Y_{res} = 512 \times 512$ | 1450 | 1760 | fps |
| fps_roi9 | $X_{res} \times Y_{res} = 256 \times 256$ | 2925 | 3210 | fps |

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Power Distribution Network

A power distribution network (PDN) is designed to ensure proper power management to the VITA sensor. Table 7 provides the recommended power supplies for the VITA

power management. Please refer to the AN65466 for recommended linear regulator selection, decoupling capacitor network and BOM for the power distribution network.

Table 7. RECOMMENDED POWER SUPPLIES

| Category | Power Supply | Source/Sink Stage | Min Rating (V) | Typ Rating (V) | Max Rating (V) | Max DC Current (mA) | Peak Currents at Allowable pk-pk Ripples |
|----------|--------------|--------------------|----------------|----------------|----------------|------------------------|--|
| Digital | VDDD_18 | Sourcing | 1.6 | 1.8 | 2 | 440 | 2 A at 200 mV |
| | VDDD_33 | Sourcing | 3 | 3.3 | 3.6 | 110 | 0.6 A at 200 mV |
| | VDD_sel | Sourcing | 3 | 3.3 | 3.6 | 0 | 1 mA at 20 mV |
| Analog | VDDA_33 | Sourcing | 3 | 3.3 | 3.6 | 965 | 1.5 A at 50 mV |
| | VDD_pix | Sourcing | 3 | 3.3 | 3.6 | 45 | 700 mA at 100 mV |
| | VDD_respd | Sourcing | 3.3 | 4.2 | 4.6 | 7 | 300 mA at 20 mV |
| | VDD_trans | Sourcing | 3.3 | 4.2 | 4.6 | 7 | |
| | VDD_resfd | Sourcing | 3.3 | 4.5 | 4.6 | 7 | |
| | VDD_casc | Sourcing | 0.9 | 1 | 1.1 | 0 | 6 mA at 300 mV |
| | Vref_colmux | Sourcing & Sinking | | 1 | | 0 | 0.35 A at 0.5 mV |
| | gnd_respd | Sinking | 0 | 0 | 1 | 30 mA sinking at 0.4 V | 200 mA at 20 mV |

9. Combining power supplies:

- VDD_sel can be combined with either VDDD_33 or VDDA_33
- VDD_respd and VDD_trans can be grouped together as VDD_42
- gnd_respd is designed to be a 7 mA sinking supply, but can be tied to ground with no impact to image quality

Color Filter Array

The VITA color sensor is processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left. Green1 and green2 have a slightly different spectral response due to (optical) cross talk from neighboring pixels. Green1 pixels are located on a green-red row, green2 pixels are located on a blue-green row.

Figure 3 depicts the spectral response for the mono and color devices. Figure 4 shows the photovoltaic response for the VITA.

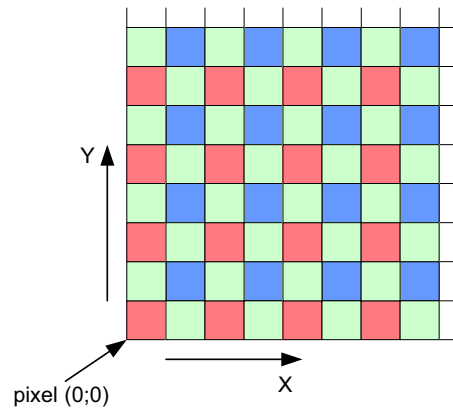


Figure 2. Color Filter Array for the Pixel Array

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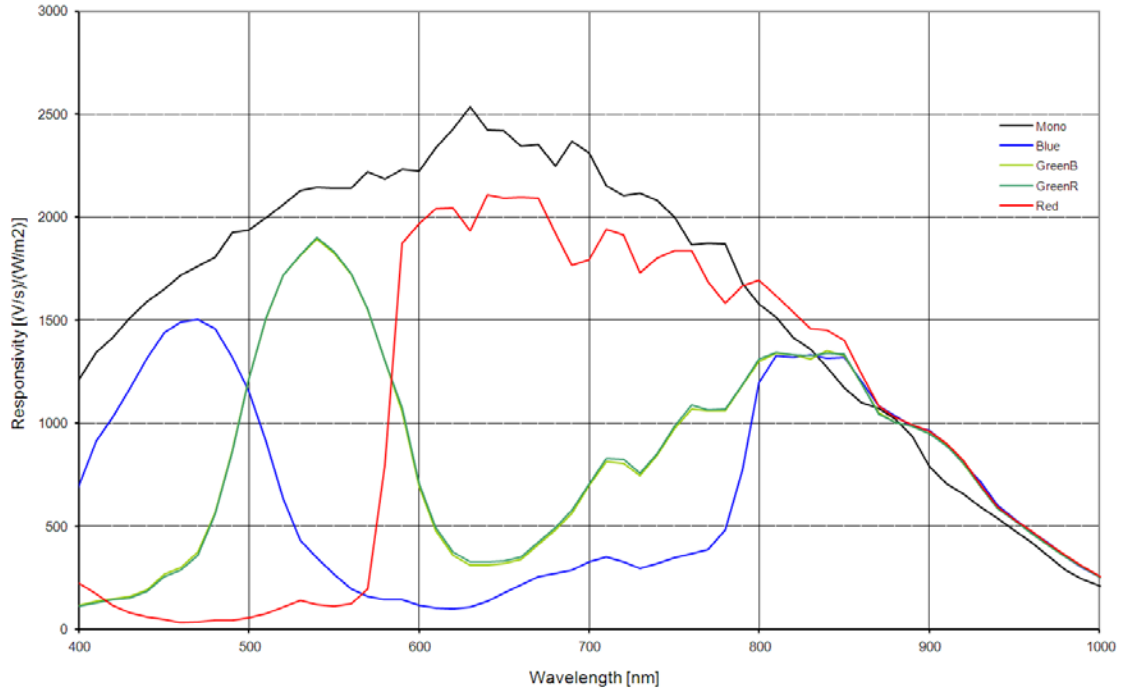


Figure 3. Mono and Color Spectral Response with Micro Lens

Note that green pixels on a Green-Red (Green 1) and Green-Blue (Green 2) row have similar responsivity to wavelength trend as is depicted by the legend “Green”.

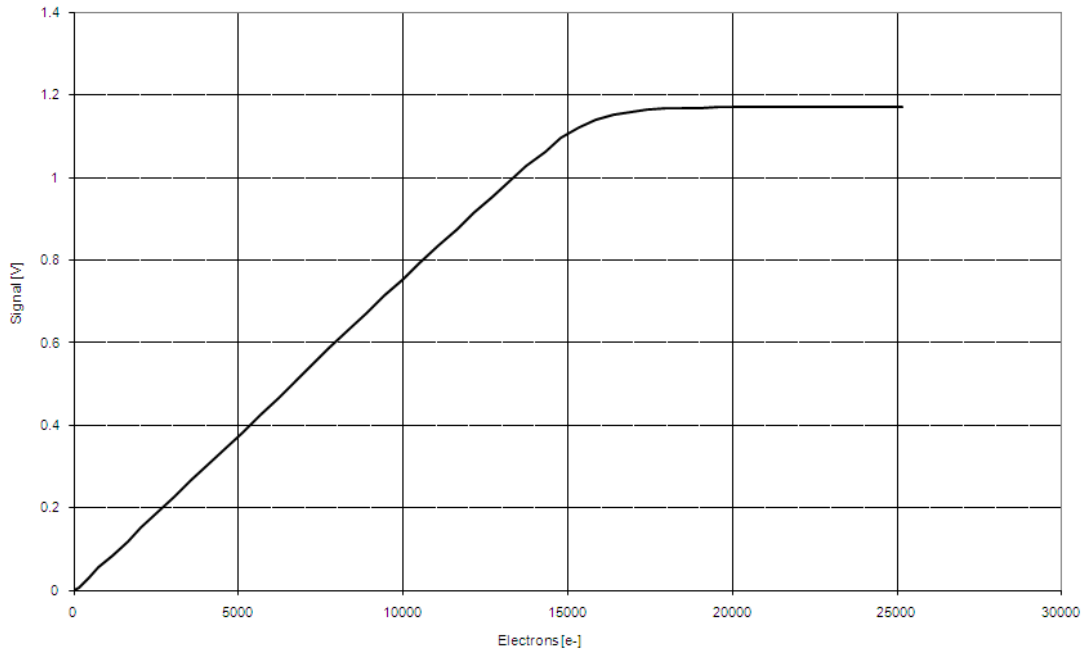


Figure 4. Typical Photovoltaic Response

OVERVIEW

Figure 5 gives an overview of all functional blocks in the image sensor. The system clock is received by the LVDS clock receiver block and distributed to other blocks. The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS) or double sampling (DS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10-bit data stream.

Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. The data then goes to the low voltage serial (LVDS) interface block that sends the data out through the I/O ring.

On-chip programmability is controlled through the Serial Peripheral Interface (SPI). See Register Map on page 45 for register details. A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

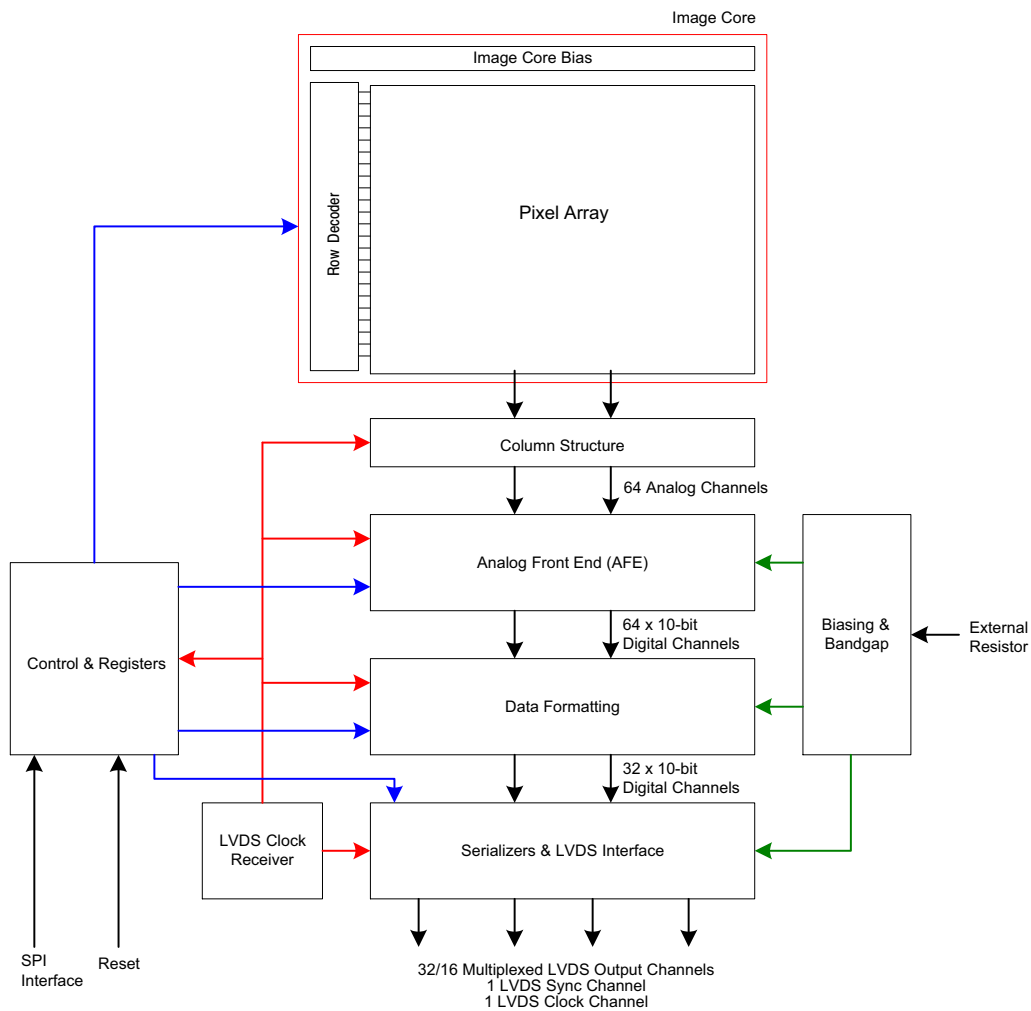


Figure 5. Block Diagram

Image Core

The image core consists of:

- Pixel array
- Address decoders and row drivers
- Pixel biasing

The VITA16K pixel array contains 4352 (H) x 4104 (V) readable pixels with a pixel pitch of 4.5 μm , inclusive of 4 pixel rows and 128 pixel columns at every side to allow for reprocessing or color reconstruction.

The VITA12K pixel array contains 4352 (H) x 3080 (V) readable pixels with a pixel pitch of 4.5 μm , inclusive of 4 pixel rows and 128 pixel columns at every side to allow for reprocessing or color reconstruction. The sensor uses a 5T pixel architecture, which makes it possible to read out the pixel array in global shutter mode with DS, or rolling shutter mode with CDS.

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in global and rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 340 MHz in 10-bit mode and 272 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

The 4096 pixels of one image row are stored in 4096 column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 64 parallel differential outputs operating at a frequency of 34 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal at this stage. The column multiplexer also supports a subsampled readout mode (read-1-skip-1 for mono and read-2-skip-2 for color version). Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 k Ω , connected between the pins *ibias_master* and *ibias_out* is required for the bias generator to operate properly.

Analog Front End

The AFE contains 64 channels, each containing a PGA and a 10-bit ADC. The PGA can be programmed to apply a gain of 1x, 1.39x, 1.94x, and 2.72x to the image signal. Together with the gain applied in the column multiplexer, a total signal gain of 10x can be achieved.

For each of the 64 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one LVDS block. A cyclic redundancy check (CRC) code is calculated on the passing data. For each LVDS output channel, one data block is instantiated. An extra data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data bit rate is 680 Mbps per channel. In 8-bit mode, the maximum output data bit rate is 544 Mbps per channel.

In addition to the 32 LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

It is possible to use only 16 channels to grab the frame. It does reduce the maximum frame rate by 2.

Sequencer

The sequencer is responsible for the following tasks:

- Controls the image core. Starts and stops integration in rolling and global shutter modes and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

OPERATING MODES

This sensor supports multiple operation modes. The following list provides an overview.

- Global Shutter mode
 - ◆ Pipelined global shutter mode
 - Master mode
 - Slave mode
 - ◆ Triggered global shutter
 - Master mode
 - Slave mode
- Rolling shutter mode
- Normal and Zero ROT mode
- Multiple windowing readout
 - ◆ Flexible window configuration
 - ◆ Processing multiple windows in Global Shutter mode
- Subsampling and binning
 - ◆ Pixel binning
 - ◆ Subsampling

Global Shutter Mode

In a global shutter mode, light integration takes place on all pixels in sync, although subsequent readout is sequential, as shown in Figure 6. Figure 7 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same time. The whole pixel core is reset simultaneously and, after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. The integration and readout can occur in parallel or sequentially.

The integration starts at a certain period, relative to the frame start.

Pipelined Global Shutter Mode

In pipelined shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with

a frame overhead time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the row overhead time (ROT).

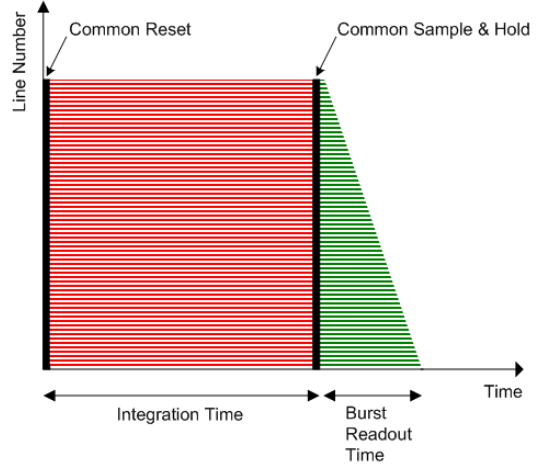


Figure 6. Global Shutter Operation

Master Mode

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins.

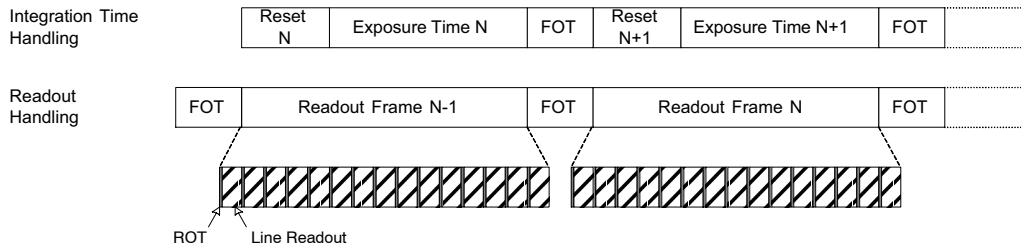


Figure 7. Integration and Readout for Pipelined Shutter

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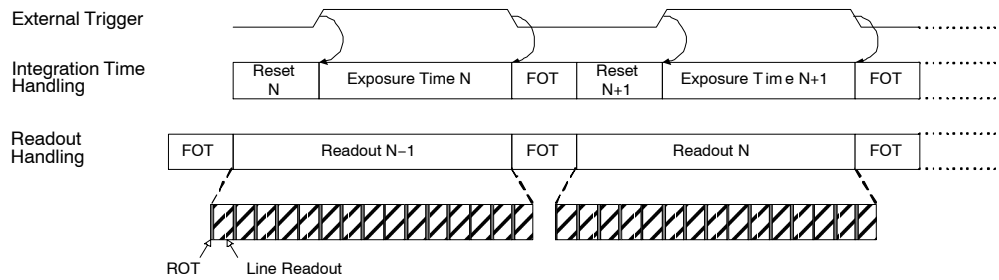


Figure 8. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter master mode are:

- Upon user action, a single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is user-controlled through an external pin.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

As shown in Figure 9, in the master mode a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is read out sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode, in which both integration time and readout requests are controlled by an external trigger. An external synchronization pin controls the start of integration. The moment it is deasserted, the FOT starts. At this time, the analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

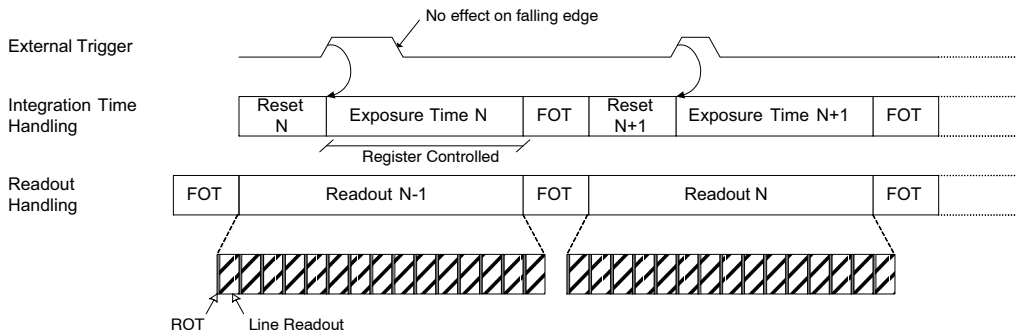


Figure 9. Triggered Shutter Operated in Master Mode

Rolling Shutter Mode

The sensor also supports the rolling shutter mode. The shutter mechanism is an electronic rolling shutter and the sensor operates in streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers, as indicated in Figure 10. One of them points to the row that is to be reset for rolling shutter operation and the other points to the row to be read out. Functionally, a row is reset first and selected for readout later. The time elapsed between these two operations is the exposure time.

Figure 10 schematically indicates the relative shift of the integration times of different lines during rolling shutter operation. Each row is read and reset sequentially, as described in the previous paragraph. Each row in a particular frame is integrated for the same time, but all lines in a frame ‘see’ a different stare time. Therefore, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, a second pointer indicates the rows that need to be reset for the rolling shutter mechanism.

The distance between the reset pointer and the readout pointer determines the integration time.

The VITA 16K/12K supports dynamic exposure time updates without artifacts or interrupting the image data stream.

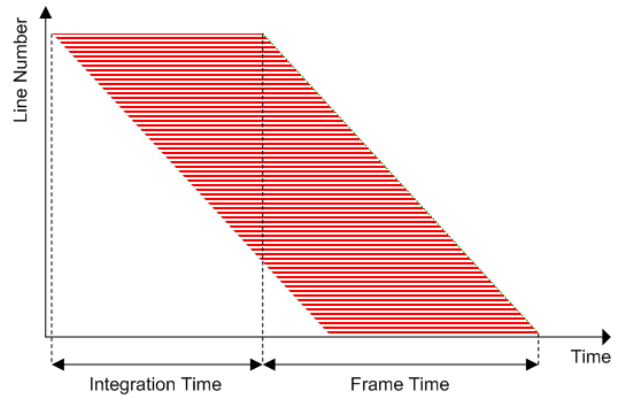


Figure 10. Rolling Shutter Operation

Normal and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 11.

In Reduced/Zero ROT operation mode (refer to Figure 12), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter ('overhead' spent per line is reduced).

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock-rate.

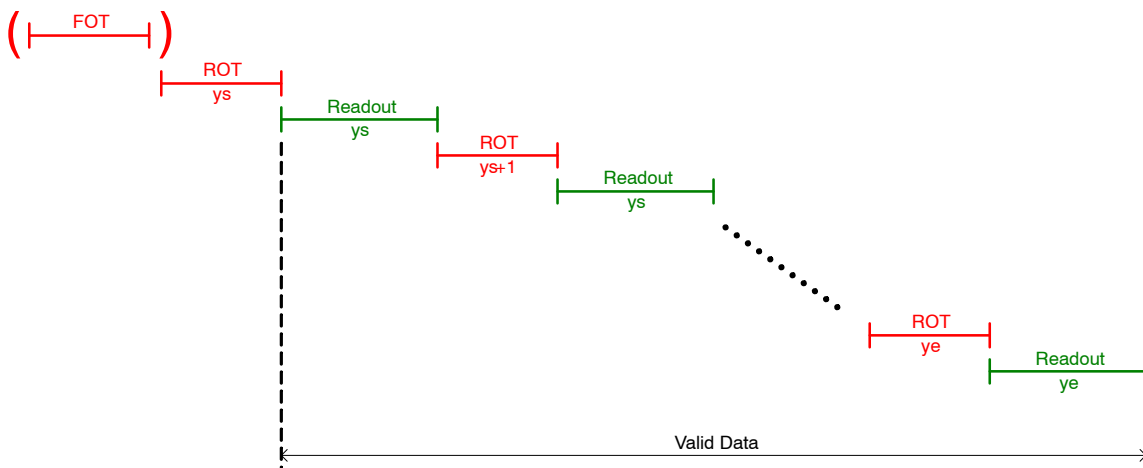


Figure 11. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Normal ROT Readout.

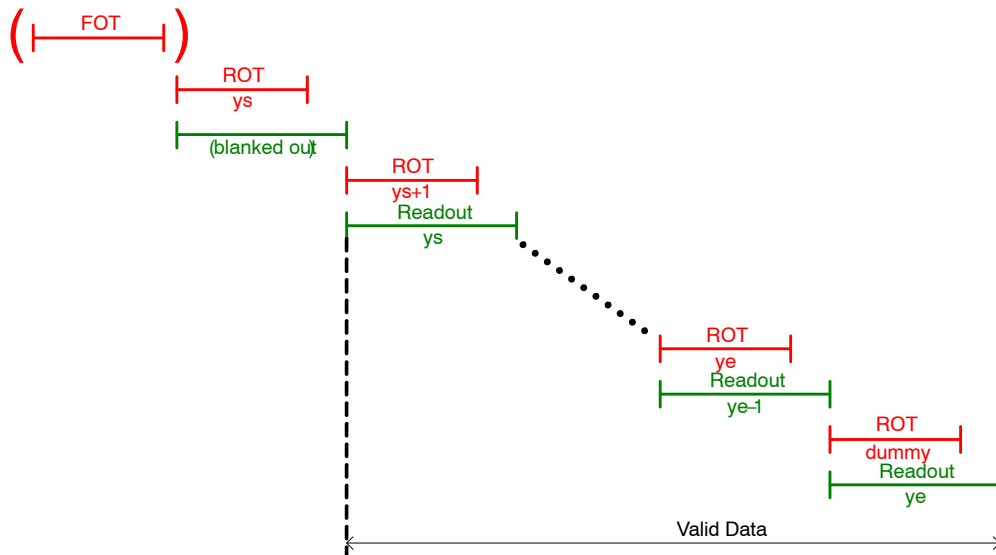


Figure 12. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.

SENSOR OPERATION

Operation Flowchart

Figure 13 shows the flow chart diagram of the sensor operation. The sensor can be in five different ‘states’. Every state is indicated with the oval circle. These states are:

- Power-Off
- Standby (1)
- Standby (2)
- Idle
- Running

The states above are ordered by power dissipation. Clearly, in ‘power-off’ state the power dissipation will be minimal; in ‘running’ state the power dissipation will be maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grabbing images.

This flowchart provides the trade-offs between power saving and enabling time of the sensor.

Next to the ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flow chart diagram. These user actions make it possible to move from one state to another.

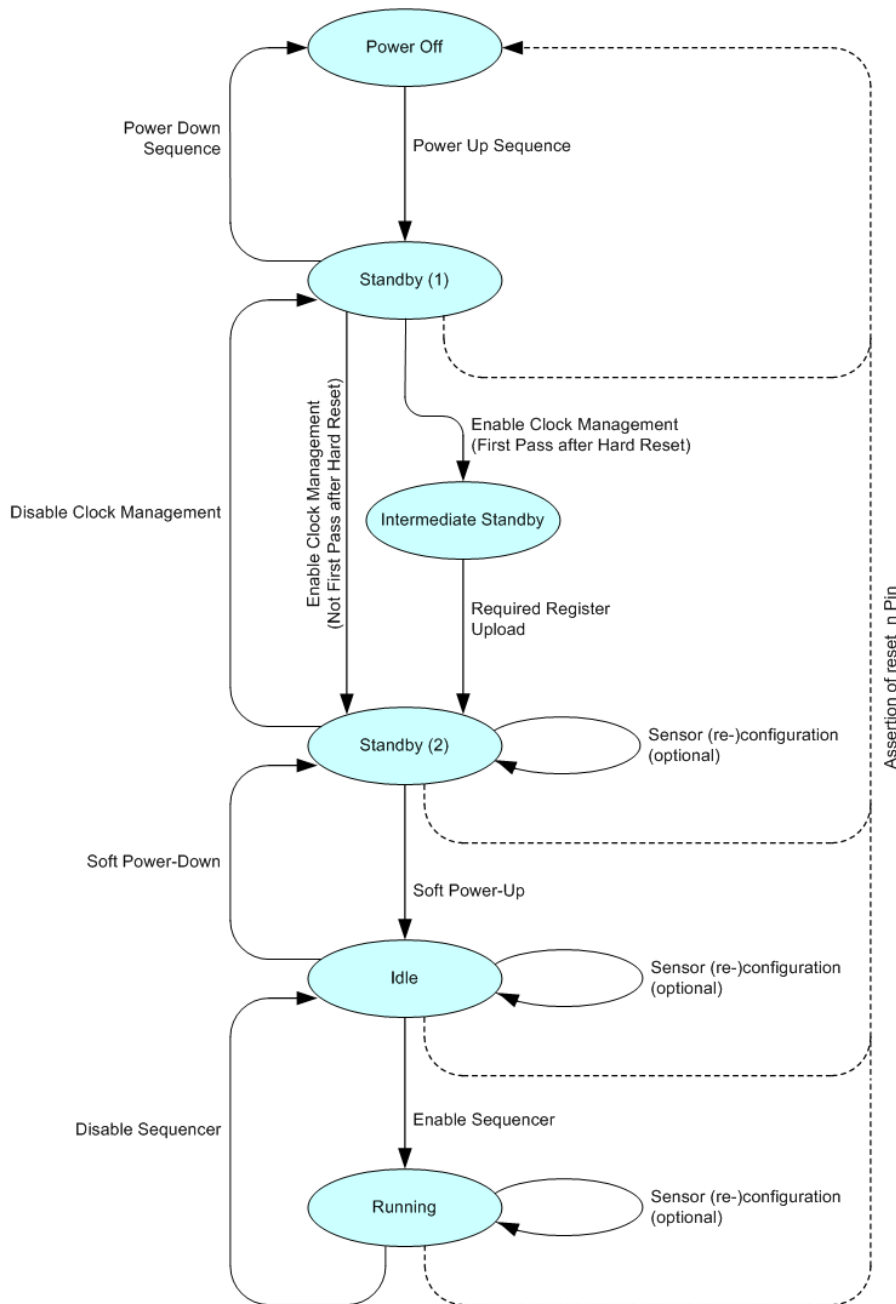


Figure 13. Sensor Operation Flow

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The sensor can be in five different states:

Power-off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Standby (1)

The registers below address 40 can be configured.

Standby (2)

In this standby state all SPI registers are active, meaning that all SPI registers can be accessed for read and write operations. All other blocks are disabled.

Note: An Intermediate Standby state is traversed after a hard reset. In this state the sensor contains the default configurations. Uploads of reserved registers are required to traverse to the Standby (2) state

Idle

In the idle state, all sensor clocks are running and all blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different rolling/global master/slave modes.

User Actions: Functional Mode to Power Up Sequences

To ‘travel’ between the five possible states, a set of actions is defined. Except for the power-up and power-down sequences, all actions consist of a set of SPI uploads.

The “Sensor reconfiguration actions” indicated in Figure 13 are used to reconfigure the operation modes of the sensor. The sensor state itself is not altered.

Power-up Sequence

Figure 13 shows the power-up timing of the sensor. Apply all power supplies in the order shown in the figure. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up

When all the supplies are stable, enable the sensor clock signal; then deassert the reset_n signal. After leaving the hard-reset mode, the sensor enters the standby (1) state. To go to the standby (2) mode, the sensor requires the reconfiguration of some registers. This reconfiguration can be applied 10 μs after the hard reset is released.

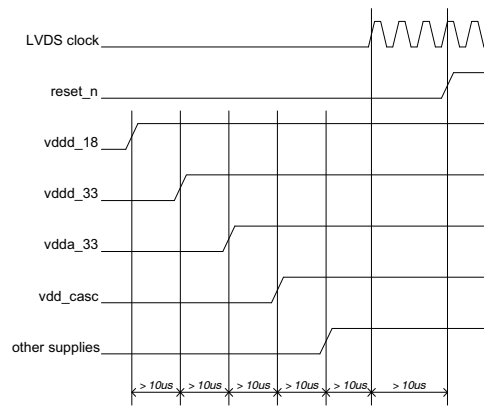


Figure 14. Power-up Procedure

NOTE: vdd_casc should come up prior to vdd_respd, vdd_resfd, and vdd_trans.

The required input clock frequency depends on the word depth mode of the sensor. This is possible in the following mode:

- 8-bit
- 10-bit

The input clock frequencies to achieve a frame rate of 58 frames/s are listed in Table 8.

Table 8. CLOCK FREQUENCY OVERVIEW

| Parameter | 8-bit Mode | 10-bit Mode |
|-----------------------|------------|-------------|
| Input Clock Frequency | 272 MHz | 340 MHz |

Enable Clock Management

The next step consists of SPI uploads which configures the internal clock distribution. The required uploads are listed in Table 9. It is important to follow the upload sequence as listed.

Table 9. ENABLE CLOCK MANAGEMENT UPLOAD

| No. | Address | Data | Description |
|-----|---------|--------|----------------------------|
| 1 | 2 | 0x0000 | NOIV1SN016KA |
| | | 0x0001 | NOIV1SE016KA |
| 2 | 32 | 0x2002 | Configure Clock Management |
| 3 | 34 | 0x0001 | Enable Logic Blocks |

Required Register Uploads

In this phase the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 10.

Table 10. REQUIRED REGISTER UPLOADS

| No. | Address | Data | Description |
|-----|---------|--------|--|
| 1 | 65 | 0x008B | General Biasing |
| 2 | 66 | 0x53C8 | AFE Biasing |
| 3 | 67 | 0x8848 | Mux Biasing |
| 4 | 68 | 0x0086 | LVDS Biasing |
| 5 | 128 | 0x4520 | Set desired output level to code 32 for 10-bit mode, code 8 for 8-bit mode. Set number of samples for black calibration to 2 ⁵ . |
| 6 | 204 | 0x09E5 | Configure unity gain (Normal ROT) |
| | | 0x09E6 | Configure unity gain (Zero ROT) |
| 7 | 224 | 0x3E04 | Dummy rows upon integration start |
| 8 | 225 | 0x6733 | Configure internal latency |
| 9 | 129[13] | 0x0 | 10-bit Mode |
| | | 0x1 | 8-bit Mode |
| 10 | 447 | 0x0BF1 | Configure sequencer |
| 11 | 448 | 0x0BC3 | Configure sequencer |
| 12 | 256 | 0x4708 | Configure ROI (x) |
| 13 | 257 | 0x0200 | Configure ROI (y) – 16K res. |
| | | 0x0400 | Configure ROI (y) – 12K res. |
| 14 | 258 | 0x11FF | Configure ROI (y) – 16K res. |
| | | 0x0FFF | Configure ROI (y) – 12K res. |

Soft Power Up

During the soft power-up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power-up uploads are listed in Table 11.

Table 11. SOFT POWER UP REGISTER UPLOADS

| No. | Address | Data | Description |
|-----|---------|--------|----------------------------------|
| 1 | 32 | 0x2003 | Enable Analog Clock Distribution |
| 2 | 64 | 0x0001 | Enable Biasing Block |
| 3 | 40 | 0x0003 | Enable Column Multiplexer |
| 4 | 48 | 0x0001 | Enable Analog Front-End (AFE) |
| 5 | 112 | 0x0007 | Enable LVDS Transmitters |

Enable Sequencer

During the 'Enable Sequencer'-action, the frame grabbing sequencer is enabled. The sensor will start grabbing images in the configured operation mode. Refer to Operating Modes on page 10 for an overview of the possible operation modes.

The 'Enable Sequencer' action consists of a set of register uploads. The required uploads are listed in Table 12.

Table 12. ENABLE SEQUENCER REGISTER UPLOADS

| No. | Address | Data (Normal ROT) | Data (Zero ROT) |
|-----|---------|-------------------|-----------------|
| 1 | 192 | 0x0001 | 0x000D |

User Actions: Functional Mode to Power Down Sequences

Disable Sequencer

During the 'Disable Sequencer'-action, the frame grabbing sequencer is stopped. The sensor will stop grabbing images and returns to the idle mode.

The 'Disable Sequencer' action consists of a set of register uploads. The required uploads are listed in Table 13.

Table 13. DISABLE SEQUENCER REGISTER UPLOADS

| No. | Address | Data | Description |
|-----|---------|------|---|
| 1 | 192[0] | 0x0 | Disable of Sequencer. NOTE: This address contains other configuration bits to select the operation mode. |

Soft Power Down

During the soft power-down action, the internal blocks are disabled and the sensor is put in standby state in order to reduce the current dissipation. This action exists of a set of register uploads. The soft power-down uploads are listed in Table 14.

Table 14. SOFT POWER DOWN REGISTER UPLOADS

| No. | Address | Data | Description |
|-----|---------|--------|-----------------------------------|
| 1 | 112 | 0x0000 | Disable LVDS Transmitters |
| 2 | 48 | 0x0000 | Disable Analog Front-End (AFE) |
| 3 | 40 | 0x0000 | Disable Column Multiplexer |
| 4 | 64 | 0x0000 | Disable Biasing Block |
| 5 | 32 | 0x2002 | Disable Analog Clock Distribution |

Disable Clock Management

The ‘Disable Clock Management’-action stops the internal clocking in order to further decrease the power dissipation. This action exists of a set of register uploads as listed in Table 15.

Table 15. DISABLE CLOCK MANAGEMENT UPLOADS

| No. | Address | Data | Description |
|-----|---------|--------|----------------------|
| 1 | 34 | 0x0000 | Disable Logic Blocks |

Power-down Sequence

The timing diagram of the advised power-down sequence is given in Figure 15. Any other sequence might cause high peak currents.

NOTE: vdd_casc should be powered down after vdd_respd, vdd_resfd, and vdd_trans.

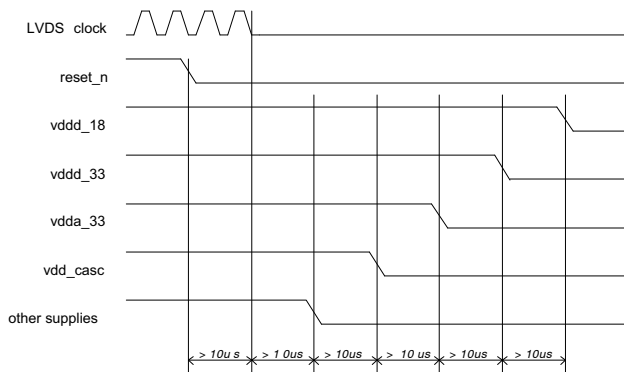


Figure 15. Power-down Sequence

Shutter and Operation Mode Reconfiguration

The VITA sensor operates in two shutter modes: global shutter and rolling shutter. The global shutter mode can be combined with a set of operation modes, as described Operation Modes on page 10.

These modes can be combined with subsampling and binning modes.

The shutter and operation modes are controlled by register 192, when the sensor is in standby or idle mode. Table 16 gives an overview of the available register settings to control

the shutter and operation modes. During this action, only the fields listed in Table 16 are affected. All other settings encapsulated in register 192 must remain unchanged.

Table 16. SHUTTER/OPERATION MODE CONFIGURATION REGISTERS

| Address | Default Value | Description |
|-----------|---------------|---|
| 192 [1] | 0x0 | Shutter type selection 0: Global shutter 1: Rolling shutter |
| 192 [3:2] | 0x0 | Normal/Zero ROT mode selection 0: Normal ROT mode 3: Zero ROT mode |
| 192 [4] | 0x0 | Triggered mode selection (global shutter only) 0: Normal mode 1: Triggered mode |
| 192 [5] | 0x0 | Master/Slave selection (global shutter only) 0: Master mode 1: Slave mode |
| 192 [7] | 0x0 | Subsampling mode selection 0: Subsampling disabled 1: Subsampling enabled |
| 192 [8] | 0x0 | Binning mode selection 0: Binning disabled 1: Binning enabled |

Windowing Reconfiguration

The windowing settings can be configured during standby, idle, and running mode.

The required regions of interest (ROI) can be programmed in the roi_configuration registers (addresses 256 up to 351). Registers roi_active0 and roi_active1 are used to activate the desired ROIs.

Default window configuration (after sensor reset) is one window, full frame (window #0).

Exposure/Gain Reconfiguration

The exposure time and gain settings can be configured during standby, idle, and running mode. Refer to Signal Gain Path on page 29 for more information.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 17. Table 17 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 17. STATIC READOUT PARAMETERS

| Group | Addresses | Description |
|--------------------------|-----------|--|
| Clock generator | 32 | Configure according to recommendation |
| Image core | 40 | Configure according to recommendation |
| AFE | 48 | Configure according to recommendation |
| Bias | 64–71 | Configure according to recommendation |
| LVDS | 112 | Configure according to recommendation |
| Sequencer mode selection | 192 | <ul style="list-style-type: none"> Rolling shutter enable triggered_mode slave_mode nzrot_xsm_delay_enable |
| All reserved registers | | Keep reserved registers to their default state, unless otherwise described in the recommendation |

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 18 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images

during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 18. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

| Group | Addresses | Description |
|-------------------------------|--------------------|---|
| Black level configuration | 128–129 197[8] | Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation. |
| Sync codes | 129[13] 130–135 | Incorrect sync codes may be generated during the frame in which these registers are modified. |
| Datablock test configurations | 144–150 | Modification of these registers may generate incorrect test patterns during a transient frame. |

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 19.

Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 19. DYNAMIC READOUT PARAMETERS

| Group | Addresses | Description |
|--------------------------|--------------------|---|
| Subsampling/binning | 192[7] 192[8] | Subsampling or binning is synchronized to a new frame start. |
| Black lines | 197 | Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode |
| Dummy lines | 198 | Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. N/A for global shutter mode. |
| ROI configuration | 195-196 256-351 | Optionally, it is possible to blank out one frame after reconfiguration of the active ROIs in rolling shutter mode. Therefore, register 206[8] must be asserted (blank_roi_switch configuration). An ROI switch is only detected when a new window is selected as the active window (re-configuration of registers 195, 196, or both). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image. |
| Exposure reconfiguration | 199-201 | Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master). |
| Gain reconfiguration | 204 | Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] - gain_lat_comp). |

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor’s sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 16 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = ‘1’. Configurations are synchronized to the frame boundaries (The registers exposure, fr_length, and mult_timer are not used in this mode)

Figure 17 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is deasserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

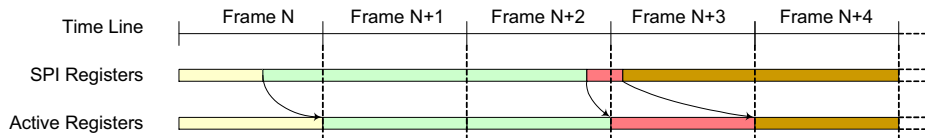


Figure 16. Frame Synchronization of Configurations (no freezing)

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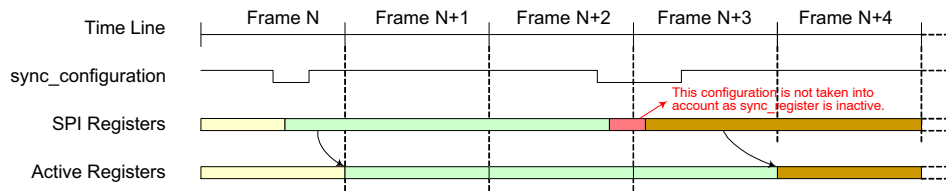


Figure 17. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 20 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 20. ALTERNATE SYNC CONFIGURATIONS

| Group | Affected Registers | Description |
|------------------|--|--|
| sync_rs_x_length | rs_x_length | Update of x-length configuration (rolling shutter only) is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_black_lines | black_lines | Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_dummy_lines | dummy_lines | Update of dummy line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_exposure | mult_timer fr_length exposure | Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_gain | mux_gainsw afe_gain | Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_roi | roi_active0[15:0] roi_active1[15:0] subsampling binning | Update of active ROI configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. Note: The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting. |

Window Configuration

Global Shutter Mode

Up to 32 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 351. Each window can be activated or deactivated separately using registers 195 and 196. It is possible to reconfigure the inactive windows while acquiring images. Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one (if the total number of windows is smaller than 17) or two (if more than 16 windows are defined) registers.

Rolling Shutter Mode

In rolling shutter mode it is not possible to read multiple windows. Do not activate more than one window (registers 205–206). However, it is possible to configure more than one window and dynamically switch between the different window configurations. Note that switching between two

different windows might result in a corrupted frame. This is inherent in the rolling shutter mechanism, where each line must be reset sequentially before being read out. This corrupted window can be blanked out by setting register 206[8]. In this case, a dead time is noted on the LVDS interface when the window-switch occurs in the sensor. During this blank out, training patterns are sent out on the data and sync channels for the duration of one frame.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to '0'. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to '0' when setting the black level target to '0'.

The black level is calibrated for the 64 columns contained in one kernel. This implies 64 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 21.

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Table 21. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

| Group | Addresses | Description |
|---|--|--|
| Black Line Generation | | |
| 197[7:0] | black_lines | This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 127. Note: When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Global Shutter - Each black line contains 80 kernels. Rolling Shutter - As the line length is fundamental for rolling shutter operation, the length of a black line is defined by the active window. |
| 197[8] | gate_first_line | When asserting this configuration, the first black line of the frame is blanked out and is not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm. |
| Black Value Filtering | | |
| 129[0] | auto_blackcal_enable | Internal black-level calibration functionality is enabled when set to '1'. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to '0', the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. Note: Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations. |
| 129[9:1] | blackcal_offset | Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to '0'. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). Note: All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all-'1') in auto calibration mode. Any value different from 0x1FF re-enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes. |
| 129[10] | blackcal_offset_dec | Sign of blackcal_offset. If set to '0', the black calibration offset is added to each pixel. If set to '1', the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to '1'. |
| 128[10:8] | black_samples | The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is $2^{\text{black_samples}}$. Note: An error is reported by the device if more samples than available are requested (refer to registers 136 to 139). |
| Black Level Filtering Monitoring | | |
| 136 137 138 139 | blackcal_error0 blackcal_error1 blackcal_error2 blackcal_error3 | An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: <ul style="list-style-type: none"> • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift. |

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

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Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 18 shows the communication protocol for read and write accesses of the SPI registers. The VITA 16K/12K sensor uses 9-bit addresses and 16-bit data words

Data driven by the system is colored blue in Figure 18, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle (100 ns) after selecting the sensor, the 9-bit address is transferred, most

3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
 - For write commands, the master continues sending the 16-bit data, most significant bit first.
 - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI is $1/30^{\text{th}}$ (in 10-bit mode) and $1/24^{\text{th}}$ (in 8-bit mode) of the LVDS input clock frequency. For nominal input frequency (340 MHz / 272 MHz), this is 10 MHz.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

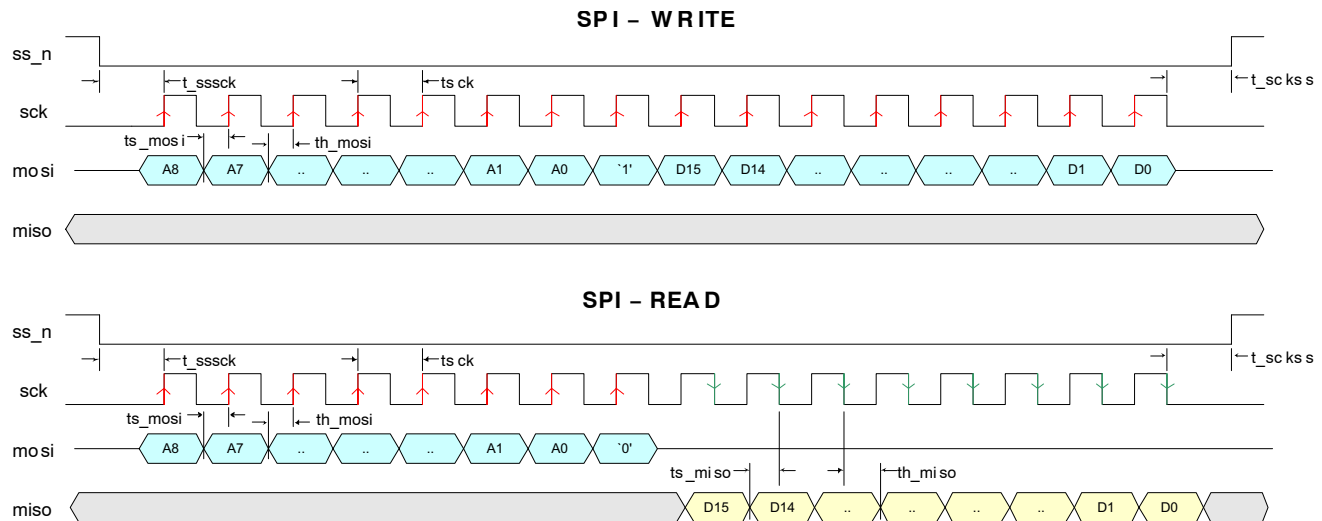


Figure 18. SPI Read and Write Timing Diagram

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Table 22. SPI TIMING REQUIREMENTS

| Group | Addresses | Description | Units |
|---------|---|-------------|-------|
| tsck | sck clock period | 100 (*) | ns |
| tsssck | ss_n low to sck rising edge | tsck | ns |
| tsckss | sck falling edge to ss_n high | tsck | ns |
| ts_mosi | Required setup time for mosi | 20 | ns |
| th_mosi | Required hold time for mosi | 20 | ns |
| ts_miso | Setup time for miso | tsck/2-10 | ns |
| th_miso | Hold time for miso | tsck/2-20 | ns |
| tspi | Minimal time between two consecutive SPI accesses (not shown in figure) | 2 x tsck | ns |

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

Global Shutter Mode*Pipelined Global Mode (Master)*

The sensor timing in master global shutter mode is controlled by the user by means of configuration registers. One can distinguish three parameters for the frame timing in global shutter mode:

- Image Array Reset Length
- Integration Time
- Frame Length

The relation between these parameters is:

$$\text{Frame Length} = \text{Reset Length} + \text{Integration Time}$$

The FOT time needs to be added to the frame length parameter to determine the total frame Time

$$\text{Total Frame Time} = \text{FOT Time} + \text{Frame Length}$$

Frame and integration time configuration can be controlled in two ways:

1. $\text{fr_mode} = 0x0$
The reset length and integration time is configured by the user. The sensor shall calculate the frame length as the sum of both parameters.
2. $\text{fr_mode} = 0x1$
The frame length and integration time is configured by the user. The reset time during which the pixels are reset, is calculated by the sensor as being the difference between the frame length and the desired integration time.

The configuration registers are $\text{exposure}[15:0]$ and $\text{fr_length}[15:0]$. The latter configuration registers is either used as Reset Length configuration ($\text{fr_mode} = 0x0$) or as Frame Length ($\text{fr_mode} = 0x1$). The granularity of both registers is defined by the $\text{mult_timer}[15:0]$ register and is expressed in number of 68 MHz cycles (14.706 ns nominal).

Reset Length and Integration Time as Parameters

The reset time for the pixel array is controlled by the registers $\text{fr_length}[15:0]$ and $\text{exposure}[15:0]$. The mult_timer configuration defines the granularity of the registers fr_length and exposure and is to be read as the number of 68 MHz cycles (14.706 ns nominal).

The exposure control for pipelined global master mode is depicted in Figure 19.

The pixel values are transferred to the storage node during the FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the fr_length and mult_timer registers, as shown in the figure. Meanwhile, the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or

exposure time. The length of the exposure time is defined by the registers exposure and mult_timer .

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
- Make sure that the sum of the reset time and exposure time exceeds the time required to read out all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.

Frame Length and Integration Time as Parameters

When fr_mode is configured to $0x1$, one configures the frame time and exposure. The reset_length is determined by the sequencer. This configuration mode is depicted in Figure 2.

The frame length is configured in register fr_length , while the integration time is configured in register exposure . The mult_timer register defines granularity of both settings. Note that the FOT needs to be added to the configured fr_length to calculate the total frame time.

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger pin. The exposure or integration time is defined by the registers exposure and mult_timer , similar to the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 21.

NOTES:

- The falling edge on the trigger pin does not have any impact. However, the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in reset state is extended to the start of a new line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0 , indicating the very first line when $\text{monitor_select} = 0x5$ – a new trigger can be initiated after a rising edge on monitor0).

If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.

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Figure 19. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x0)



Figure 20. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x1)

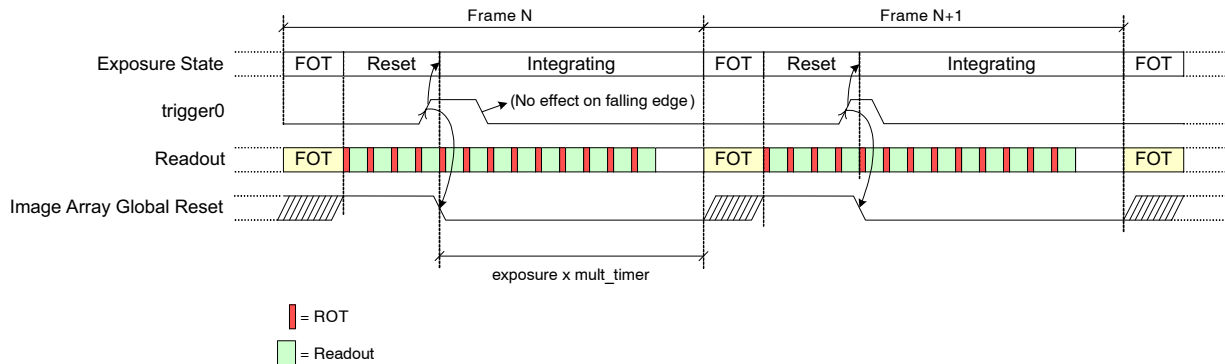


Figure 21. Exposure Time Control in Triggered Global Mode (Master)

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The register's fr_length, exposure, and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 22.

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period

starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.

- If the trigger is deasserted before the end of readout, the exposure time is extended until the end of the last active line. Consequently the FOT and start of frame readout is postponed accordingly.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).

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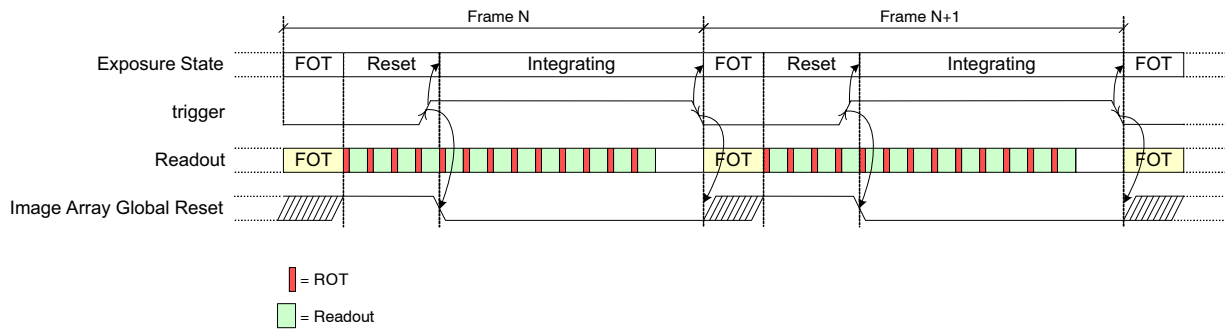


Figure 22. Exposure Time Control in Global-Slave Mode

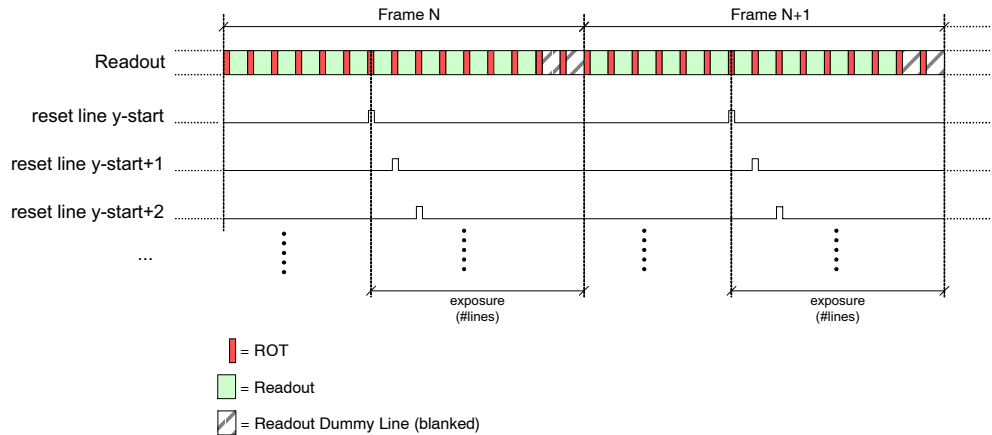
Rolling Shutter Mode

The exposure time during rolling shutter mode is always an integer multiple of line-times. The exposure time is defined by the register exposure and expressed in number of lines. The register fr_length and mult_timer are not used in this mode.

The maximum exposure time is limited by the frame time. It is possible to increase the exposure time at the cost of the frame rate by adding so called dummy lines. A dummy line lasts for the same time as a regular line, but no pixel data is transferred to the system. The number of dummy lines is controlled by the register dummy_lines.

The rolling shutter exposure mechanism is graphically shown in Figure 23.

The duration of one line is the sum of ROT and the time required to read out one line (depending on the number of active kernels in the window). Optionally, this readout time can be extended by the configuration rs_x_length. This register, expressed in number of periods of the logic clock (16.129 ns nominal), determines the length of the x-readout. However, the minimum length is governed by the window size (x-size).



NOTE: This figure illustrates a short frame with a few dummy lines.

Figure 23. Integration Control in Rolling Shutter Mode

ADDITIONAL FEATURES

Multiple Window Readout

The sequencer supports multiple window readout. This means that small ROIs, which are read out sequentially, can be defined in the full image array. Therefore, the sequencer scans all requested kernels line by line.

Window Configuration

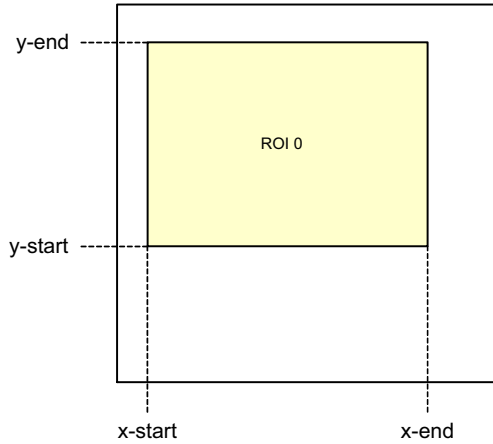


Figure 24. Region of Interest Configuration

Figure 24 shows the four parameters defining a region of interest (ROI). These parameters are explained here.

- **x-start[6:0]**
x-start defines the x-starting point of the desired window. The sensor reads out 64 pixels in a single clock cycle. Therefore, the granularity for configuring the x-start position is also 64 pixels. To find the corresponding column in the pixel array, multiply the value in the x-start register by 64.
- **x-end[6:0]**
This register defines the window end point on the x-axis. As for x-start, the granularity for this configuration is one kernel. x-end must be larger than x-start. The minimal window width is two kernels.
- **y-start[12:0]**
This is the start line of the readout window. The granularity of this setting is one line.
- **y-end[12:0]**
This is the end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.

The configuration width of the required settings is mentioned between brackets. Seven bits are required for the x boundaries, 13 bits for the y boundaries.

Up to 32 windows can be defined, possibly (partially) overlapping. Figure 25 illustrates the use of overlapping windows. Note that pixel (0,0) is located in the left bottom corner.

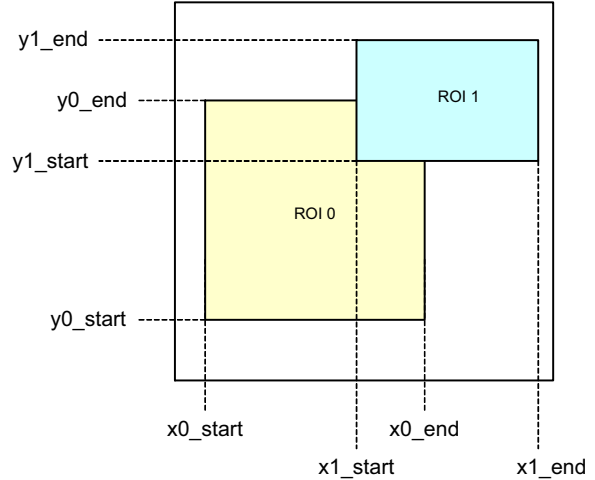


Figure 25. Overlapping Multiple Window Configuration

For each line to be scanned, the sequencer control block analyzes which windows must be read out, from left to right. The following restrictions apply to the window configurations (they must be valid for each line):

- For each line, the windows are ordered from left to right, based on their x-start address:
 $x_start_roi(i) \ \& \ x_start_roi(j)$ where $j > i$
- Overlapping in the x-direction is restricted to simple window overlapping schemes. When a new window is started, it needs to continue at least until the end of the previous window. In other words, it is not possible to start a window M, overlap with a window M+1, and at the end of window M+1, re-enter window M. The end of window M+1 must coincide or be larger than the end of window M:
 $x_end_roi(i) \ \& \ x_end_roi(j)$ where $j > i$
- For subsampling and binning modes, the start addresses are restricted to even addresses; the end addresses are restricted to even addresses for subsampling and odd addresses for binning. Erroneous start and end addresses are corrected by the sensor logic.
- The x-start, x-end, y-start and y-end addresses should be limited to the following ranges:

Table 23. WINDOW OFFSETS

| | Data | |
|---------|--------------|--------------|
| | NOIV1Sx016KA | NOIV1Sx012KA |
| x-start | 0x06 | 0x06 |
| x-end | 0x49 | 0x49 |
| y-start | 0x01FC | 0x03FC |
| y-end | 0x1203 | 0x1003 |

Processing Multiple Windows

Global Shutter

The multiple windowing mechanism described in this section is only valid for the global shutter operation mode.

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y-counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, the y-counter is initialized to the y-start address of the first window. It runs until the y-end address of the last window to be read out. Note that the last window is configured by the configuration registers and is not necessarily window #31.

The x-counter starts counting from the x-start address of the window with the lowest ID that is active on the addressed line. Only windows in which the current y-address is enclosed are taken into account for scanning. Other windows are skipped.

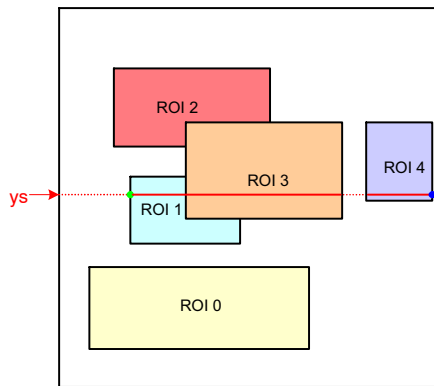


Figure 26. Scanning the Image Array with Five Subwindows

Figure 26 illustrates a practical example of a configuration with five windows. The current position of the read pointer (*ys*) is indicated by a red line crossing the image array. For this position, three windows need to be read out. The initial start position for the x-kernel pointer is the x-start configuration of ROI1. Kernels are scanned up to the ROI3 x-end position. From there, the x-pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4's x-end position, the read pointer is incremented to the next line and *xs* is reinitialized to the starting position of ROI1.

NOTES:

- The initial starting point for the readout pointer at the start of a frame is the y-start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in

y-direction. For Figure 26, this is the case when reaching the end of ROI0 where the read pointer jumps to the y-start position of ROI1.

- The x-pointer starting position is equal to the x-start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x-pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.

Rolling Shutter

Multiple windowing is not supported in rolling shutter mode. Only single-window readout is possible. The active window can be selected among the 32 windows in the configuration. Dynamic window reconfiguration (or dynamic selection of a different window configuration) is supported. Eventual corrupted images due to transients are blanked out in the sensor.

Subsampling and Binning

Pixel binning and subsampling methods are used as way of decimating the image. The number of pixel samples is reduced by a factor of four, while the optical area is maintained.

Pixel Binning

Pixel binning is a technique in which different pixels belonging to a rectangular bin are averaged in the analog domain. Two-by-two pixel binning is implemented such that two adjacent pixels are averaged both in column and row. Binning is configurable using a register setting. Pixel binning is not supported on the color option.

Note: register 194[9] needs to be configured to 0x1 for 2x2 pixel binning. When configuring to 0x0, 2x1 binning is obtained (binning in x only).

Subsampling

Subsampling is obtained by adapting the readout sequence. In subsampling mode, both lines and pixels are read in a read-N-skip-N mode. This reduces the number of lines in a frame and the number of pixels in a line. Overall frame time is reduced by a factor 4.

The monochrome sensor is read out in a read-one-skip-one pattern for both the rows and the columns, while the color version supports a read-two-skip-two subsampling scheme. This mode is selectable through register configuration. Figure 27 shows which pixels are read and which ones are skipped for monochrome and color sensors respectively. Readout direction is indicated as an x and y arrow.

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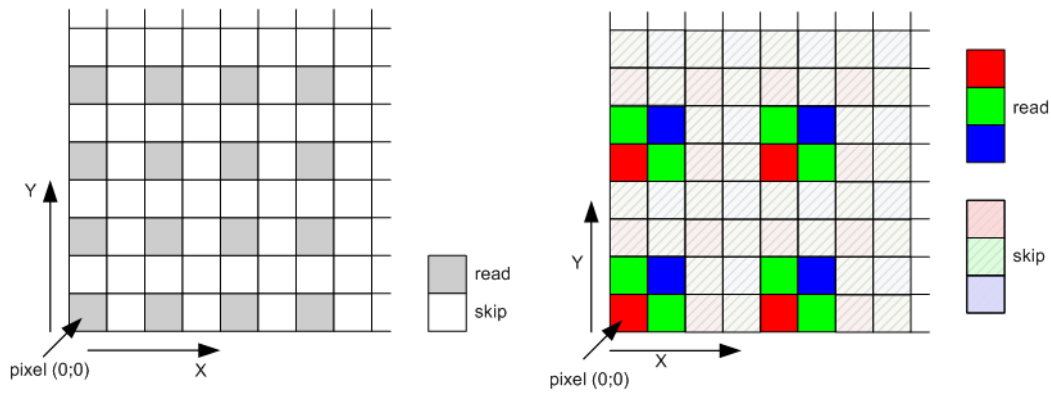


Figure 27. Subsampling Scheme

Signal Gain Path

Table 24 and Table 25 show the available registers (fields) to program the desired exposure time and gain settings. Settings 199[1:0] and 199[15:14] should remain unchanged.

Table 24. EXPOSURE TIME CONFIGURATION REGISTERS

| Address | Default Value | Description |
|---------|---------------|--|
| 201 | 0x0000 | Exposure time Rolling shutter: granularity = lines Global shutter: granularity defined by 'Mult Timer' (register 199). |
| 199 | 0x0001 | Mult Timer (global shutter only) Defines granularity of exposure and reset length. unit = 1/68 MHz for normal ROT mode |
| 200 | 0x0000 | Reset length or Frame Length (global shutter only) Granularity defined by 'Mult Timer' (register 199) |

Table 25. GAIN CONFIGURATION REGISTERS

| Address | Unity Gain Configuration | Description |
|------------|--------------------------|---|
| 204 [4:0] | 0x05 | Column gain setting (Normal ROT) 0x07: column gain = 2/3x 0x05: column gain = 1x 0x09: column gain = 2x 0x13: column gain = 4x Other settings are not supported. |
| | 0x06 | Column gain setting (Zero ROT) 0x06: column gain = 1x 0x10: column gain = 2x 0x14: column gain = 4x Other settings are not supported. |
| 204 [12:5] | 0x4F | AFE gain setting 0x4F: AFE gain = 1.00x 0x33: AFE gain = 1.39x 0x36: AFE gain = 1.94x 0x66: AFE gain = 2.72x Other settings are not supported. |
| 204 [13] | | Postpone gain update by one frame when '1' to compensate for exposure time updates latency. |
| 205[11:0] | 0x080 | Digital Gain, 5.7 unsigned representation (5 bits before decimal point, 7 bits for fractional part). Maximum gain is 31.992 |

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Mode Changes and Frame Blanking

Dynamically reconfiguring the sensor may lead to corrupted or non-uniformly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is

summarized in the following table for the sensor's image related modes.

NOTE: Major mode switching (i.e. switching between rolling and global shutter modes, master, triggered, slave modes) must be performed while the sequencer is disabled (`reg_seq_enable = 0x0`).

Table 26. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

| Configuration | Global Shutter | | Rolling Shutter | | Notes |
|-----------------------------------|---|-------------------|-----------------|-------------------|---|
| | Corrupted Frame | Blanked Out Frame | Corrupted Frame | Blanked Out Frame | |
| Shutter Mode and Operation | | | | | |
| rolling_shutter_enable | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting <code>reg_seq_enable = 0x0</code> . | | | | |
| triggered_mode | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting <code>reg_seq_enable = 0x0</code> . | | | | |
| slave_mode | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting <code>reg_seq_enable = 0x0</code> . | | | | |
| zero_rot_enable | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting <code>reg_seq_enable = 0x0</code> . | | | | |
| subsampling | Enabling: No Disabling: Yes | Configurable | No | Yes | For global shutter mode: configurable with <code>blank_subsampling_ss</code> register. For rolling shutter mode: frame is always blanked out. |
| binning | No | Configurable | No | Yes | For global shutter mode: configurable with <code>blank_subsampling_ss</code> register For rolling shutter mode: frame is always blanked out. |
| Frame Timing | | | | | |
| rs_x_length | No | No | No | No | |
| black_lines | No | No | No | No | |
| dummy_lines | N/A | N/A | No | No | |
| Exposure Control | | | | | |
| mult_timer | No | No | N/A | N/A | Latency is 1 frame |
| fr_length | No | No | N/A | N/A | Latency is 1 frame |
| exposure | No | No | No | No | Latency is 1 frame |
| Gain | | | | | |
| mux_gainsw | No | No | No | No | Latency configurable by means of <code>gain_lat_comp</code> register |
| afe_gain | No | No | No | No | Latency configurable by means of <code>gain_lat_comp</code> register. |
| db_gain | No | No | No | No | Latency configurable by means of <code>gain_lat_comp</code> register. |
| Window/ROI | | | | | |
| roi_active | See Note | No | No | Configurable | For Global shutter mode: Windows containing lines previously not read out may lead to corrupted frames. For Rolling shutter mode: Frame blanking when <code>blank_roi_switch</code> is asserted (recommended). |

Table 26. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

| Configuration | Global Shutter | | Rolling Shutter | | Notes |
|--------------------------|-----------------|-------------------|-----------------|-------------------|---|
| | Corrupted Frame | Blanked Out Frame | Corrupted Frame | Blanked Out Frame | |
| roi_configuration | See Note | No | Yes | No | Reconfiguring the windows by means of roi*_configuration* may lead to corrupted frames when configured close to frame boundaries. It is recommended to (re)configure an inactive window and switch the roi_active register. See Notes on roi_active. |
| Black Calibration | | | | | |
| black_samples | No | No | No | No | If configured within range of configured black lines |
| auto_blackal_enable | See Note | No | See Note | No | Manual correction factors become instantly active when auto_blackal_enable is deasserted during operation. |
| blackcal_offset | See Note | No | See Note | No | Manual blackcal_offset updates are instantly active. |
| CRC Calculation | | | | | |
| crc_seed | No | No | No | No | Impacts the transmitted CRC |
| Sync Channel | | | | | |
| bl | No | No | No | No | Impacts the Sync channel information, not the Data channels. |
| img | No | No | No | No | Impacts the Sync channel information, not the Data channels. |
| crc | No | No | No | No | Impacts the Sync channel information, not the Data channels. |
| tr | No | No | No | No | Impacts the Sync channel information, not the Data channels. |

Sensor Status

The currently used exposure and gain parameters are reported by the sensor in registers 208 to 214. These status registers are updated at the start of the frame in which these parameters become active.

Temperature Diode

The temperature diode allows the monitoring of the sensor die temperature during operation. The diode can be connected through the pins td_anode and td_cathode.

The die temperature (T_{die}), as a function of the measured forward threshold voltage of the diode, with a known bias current (V_{diode} at bias 40 μA), is determined according to the following formula:

$$T_{die} = (0.77 - V_{diode \text{ at bias } 40 \mu A}) / 0.00158^{\circ}C$$

Monitor Pins

The sensor features three logic monitor output pins. These pins can provide internal state and synchronization information to the outside system. These status pins can be used during system setup or for system frame synchronization.

The pins are named monitor0, monitor1, and monitor2. The information provided on these pins is configured with the register monitor_select (register 192[13:11]).

NOTE: Monitor indications are generated in the sequencer. These signals lead the image and synchronization data on the LVDS channels.

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Table 27. MONITOR SELECT

| Monitor Select | Monitor Output | Description |
|----------------|--|--|
| 0x0 | monitor0: '0' | No information is provided on the output pins. All outputs are driven to logic '0' |
| | monitor1: '0' | |
| | monitor2: '0' | |
| 0x1 | monitor0: Integration time indication | High during integration |
| | monitor1: ROT indication | High when ROT is active, low outside ROT |
| | monitor2: Dummy line indication | High during dummy lines, low during all other lines |
| 0x2 | monitor0: Integration time indication | High during integration |
| | monitor1: N/A | N/A |
| | monitor2: N/A | N/A |
| 0x3 | monitor0: Start of X-readout | Pulse indicating the start of x-readout |
| | monitor1: Black line indication | High during black lines, low during all other lines |
| | monitor2: Dummy line indication | High during dummy lines, low during all other lines |
| 0x4 | monitor0: Frame start | Pulse indicating the start of a new frame |
| | monitor1: Start of ROT | Pulse indicating the start of ROT |
| | monitor2: Start of X-readout | Pulse indicating the start of x-readout |
| 0x5 | monitor0: First line indication | High during the first line of each frame, low for all others |
| | monitor1: Start of ROT indication | Pulse indicating the start of ROT |
| | monitor2: ROT inactive indication | Low during ROT, high outside ROT |
| 0x6 | monitor0: ROT indication | High when ROT is active, low outside ROT |
| | monitor1: Start of X-readout | Pulse indicating the start of X-readout |
| | monitor2: X-readout inactive indication | Low during X-readout, high outside X-readout |
| 0x7 | monitor0: Start of X-readout for black lines | Pulse indicating the start of X-readout for black lines |
| | monitor1: Start of X-readout for image lines | Pulse indicating the start of X-readout for image lines |
| | monitor2: Start of X-readout for dummy lines | Pulse indicating the start of X-readout for dummy lines |

DATA OUTPUT FORMAT

LVDS Output Channels

The image data output occurs through 32 or 16 LVDS data channels, operating at 680 Mbps in 10-bit mode and 544 Mbps in 8-bit mode. A synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The data channels are used to output the image data only. The sync channel transmits information about data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC).

To perform word synchronization on the output data stream, a predefined training pattern is sent after startup of the sensor and during idle times (during FOT, ROT, and in between frames and lines). This data is used to perform word alignment on the receiving side.

To decrease the data bit rate at the outputs (and reduce the power consumption), the sensor can operate in 8-bit mode.

In 10-bit mode, the words on data and sync channels have a 10-bit length. The words are serialized most significant bit first. The output data rate is 680 Mbps max.

In 8-bit mode, the words on data and sync channels have an 8-bit length. The words are serialized most significant bit first. The output data rate is 544 Mbps max.

This decreases the data bit rate on the LVDS data channels. Power consumption is reduced by reconfiguring the internal bias currents. LVDS channels run at 272 MHz (DDR) in 8-bit mode.

Table 28. LVDS OUTPUT CHANNELS CONFIGURATION

| Configuration | | | Description | Output Data Rate Channel [Mbps] | Number of data channels |
|--------------------|--------------------|-------------------------------|---------------|---------------------------------|-------------------------|
| MUX mode (pin F25) | ADC mode (pin H22) | 8-bit_mode (register 129[13]) | | | |
| 0 | 0 | 0 | 10-bit mode | 680 | 32 |
| 1 | 0 | 0 | 10-bit mode | 680 | 16 |
| 0 | 1 | 1 | 8-bit mode | 544 | 32 |
| 1 | 1 | 1 | 8-bit mode | 544 | 16 |
| X | 0 | 1 | Not supported | N/A | N/A |
| X | 1 | 0 | Not supported | N/A | N/A |

The 8-bit mode is selected using the `adc_mode` pin. The datablock sync channel is configured accordingly (8-bit_mode configuration). In 8-bit mode, the eight most significant bits of the ADC data words are transmitted over the data channels.

Sync channel encoding is similar to the 10-bit mode. The two least significant bits of the (configured) sync codes are omitted and the window ID is transmitted after each frame synchronization word (the two LSBs are to be ignored).

NOTE: The 8-bit mode can only be used to reduce the data rate at the cost of image data resolution. Operating the sensor in 8-bit mode at a higher clock frequency to achieve higher frame rates is not supported.

LVDS Channel Multiplexing with the MUX Mode Pin

The MUX mode pin (F25) enables the reduction of the number of used data channels at the expense of maximum frame rate. When asserted, the sensor will multiplex down the 32 data channels to use only the 16 even-numbered data channels. The image data from even and odd channels will be interleaved on the even-numbered channels, while the synchronization channel will show two repeated synchronization codes. The unused data channels are powered down and will not send any data. Note that the sensor needs to be reset after change of multiplexing mode.

Serial Link Interface Operation

This sensor's serial link interface is based on a mesochronous clocking system. This means that all data and control links operate at the same frequency, but their phase may be different due to skew. The host provides an LVDS clock as input to the sensor. To compensate for possible large on-chip delays, the sensor retransmits this clock with the same delay as that seen by the data channels and synchronization channel. The receiver end (generally an FPGA-based system) performs per-interface skew compensation.

The data on high-speed serial links can drift due to various reasons such as skew, jitter, PCB trace delays, process, voltage, and temperature variations. The receiver performs per-LVDS interface skew compensation using bit and word alignment techniques.

To support per-interface skew compensation, the sensor provides a training mode that allows the system to perform bit and word alignment on all interfaces.

During idle moments (when the sensor is not capturing images or during frame and line overhead), the image sensor transmits training patterns. These patterns are configurable by means of a register upload and should be chosen such that these can easily be detected by reducing the risk of mimicking in the regular data stream.

Bit Alignment

Bit alignment procedures position the sampling edge of the clock at the center of the data eye window by adding delay to the data path (using delay taps).

Word Alignment

Word alignment procedures ensure that the reconstructed parallel data bits are in correct order at the output of the deserializer. Word alignment is done by looking for well known training patterns.

All major FPGA vendors provide bit and word alignment methods for their FPGAs. Refer to the FPGA vendor's application for more information on the use of these functionalities.

When the host succeeds in a lock for bit and word alignment procedures, the system enables the sensor for image acquisition. Specific frame alignment patterns are transmitted for image frame synchronization purposes.

Frame Format

The frame format is explained by example of the readout of two (overlapping) windows, as shown in Figure 28 (a).

The readout of a frame occurs on a line-by-line basis. In this representation, the read pointer goes from left to right, bottom to top.

Figure 28 indicates that, after the FOT is complete, a number of lines which only include information of 'ROI 0' are sent out, starting at position $y0_start$. When the line at position $y1_start$ is reached, a number of lines containing

data of 'ROI 0' and 'ROI 1' are sent out, until the line position of $y0_end$ is reached. From there on, only data of 'ROI 1' appears on the data output channels until line position $y1_end$ is reached.

NOTE: Only frame start and frame end sync words are indicated in (b). CRC codes are also omitted from Figure 28.

During readout of image data over the data channels, the sync channel sends out frame synchronization codes, which provide information related to the image data being sent over the data channels.

Each line of a window starts with a line start (LS) indication and ends with a line end (LE) indication. The line start of the first line is replaced by a frame start; the line end of the last line is replaced with a frame end indication. Each such frame synchronization code is followed by a window ID (range 0 to 31).

The data channels contain valid pixel data during FS/FE/LS/LE and window ID synchronization codes.

NOTE: For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out. As shown in the illustration, no LE is transmitted for the overlapping part of window 0.

Black lines are read out at the start of a frame. These lines are enclosed by LS and LE indications (no frame start/end). The window ID for the black lines must be ignored.

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Figure 28. Frame Sync Codes

Figure 29 and Figure 30 show the details of the readout of a number of lines for single window readout, at the beginning of the frame.

Figure 31 shows the details of the readout of a number of lines for two overlapping windows.



Figure 29. Timeline Showing Readout of Black Line for Global Shutter

NOTE: For rolling shutter, the number of black pixels on one line is reduced to the selected window's length. The sequence shown is repeated if more than one black line is generated.

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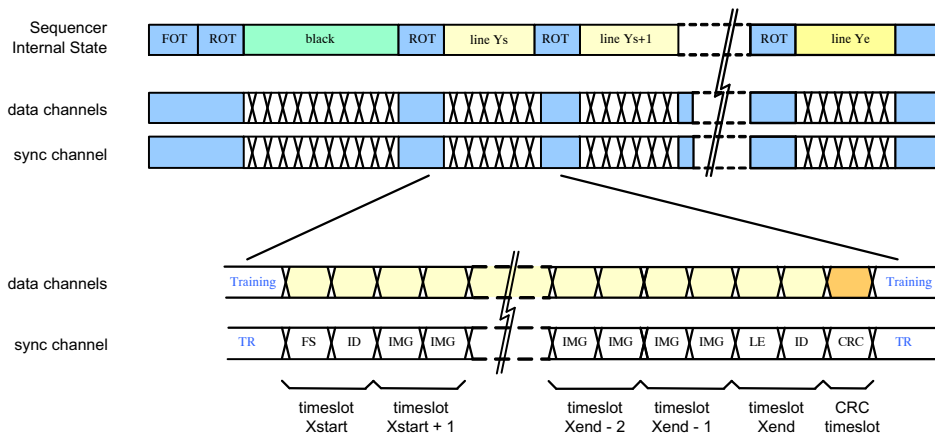


Figure 30. Timeline for Single Window Readout

NOTE: In the figure, the second image line is shown in more detail. The LS code is replaced by FS for the first line and the LE code is replaced by FE for the last line in the window.

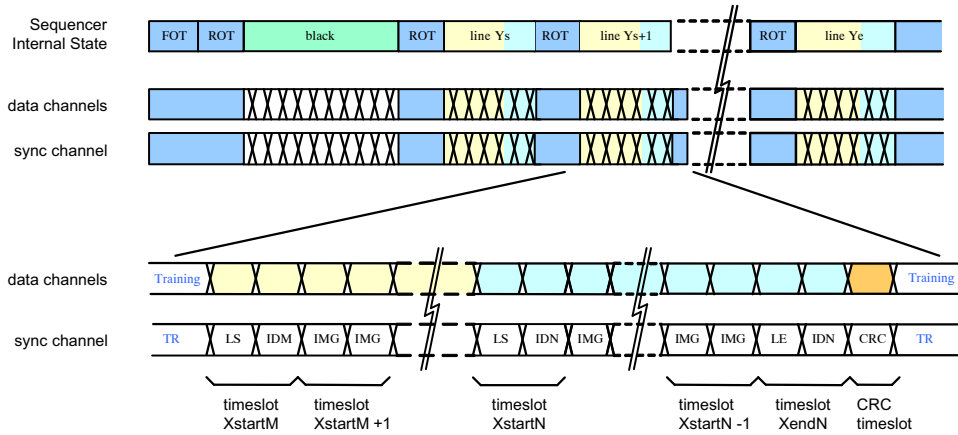


Figure 31. Timeline Showing Readout of Two Overlapping Windows

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Frame Format in 8-bit Mode

The frame format is identical to the 10-bit mode. Sync and data word depth is reduced to eight bits. Synchronization Words

Frame Synchronization for 10-Bit Mode

Table 29 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable) for 10-bit mode. If more than one window is active at the same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 29. FRAME SYNCHRONIZATION CODE DETAILS FOR 10-BIT MODE

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|--|
| 9:7 | N/A | 0x5 | Frame start indication |
| 9:7 | N/A | 0x6 | Frame end indication |
| 9:7 | N/A | 0x1 | Line start indication |
| 9:7 | N/A | 0x2 | Line end indication |
| 6:0 | 131[6:0] | 0x2A | These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting |

Window Identification

Frame synchronization codes are always followed by a 5-bit window identification (bits 4:0). This is an integer number, ranging from 0 to 31, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 30.

Table 30. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10-BIT MODE

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|--|
| 9:0 | 132 [9:0] | 0x015 | Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets. |
| 9:0 | 133 [9:0] | 0x035 | Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image). |
| 9:0 | 134 [9:0] | 0x059 | CRC value. The data on the data output channels is the CRC code of the finished image data line. |
| 9:0 | 135 [9:0] | 0x3A6 | Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting. |

Frame Synchronization in 8-bit Mode

The frame synchronization words are configured using the same registers as in 10-bit mode. The two least significant bits of these configuration registers are ignored

and not sent out. Table 31 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8-bit mode.

Table 31. FRAME SYNCHRONIZATION CODE DETAILS FOR 8-BIT MODE

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|---|
| 7:5 | N/A | 0x5 | Frame start (FS) indication |
| 7:5 | N/A | 0x6 | Frame end (FE) indication |
| 7:5 | N/A | 0x1 | Line start (LS) indication |
| 7:5 | N/A | 0x2 | Line end (LE) indication |
| 4:0 | [6:2] | 0x0A | These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting. |

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Window Identification

Similar to 10-bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 6:2 (all other bit positions are '0'). The same restriction for overlapping windows applies in 8-bit mode.

Data Classification Codes

BL, IMG, CRC, and TR codes are defined by the same registers as in 10-bit mode. Bits 9:2 of the respective configuration registers are used as classification code. The default values are listed in Table 32.

Table 32. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 8-BIT MODE

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|--|
| 7:0 | 132 [9:2] | 0x05 | Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets. |
| 7:0 | 133 [9:2] | 0x0D | Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image). |
| 7:0 | 134 [9:2] | 0x16 | CRC value. The data on the data output channels is the CRC code of the finished image data line. |
| 7:0 | 135 [9:2] | 0xE9 | Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting. |

Training Patterns on Data Channels

In 10-bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable

independent of the training code on the sync channel as shown in Table 33. In 8-bit mode, the training pattern for the data channels is defined by the same register as in 8-bit mode, where the lower two bits are omitted; see Table 34.

Table 33. TRAINING CODE ON SYNC CHANNEL IN 10-BIT MODE

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|---|
| [9:0] | 130 [9:0] | 0x3A6 | Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel. |

Table 34. TRAINING PATTERN ON DATA CHANNEL IN 8-BIT MODE

| Data Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|---|
| [7:0] | 130 [9:2] | 0xE9 | Data Channel Training Pattern (Training pattern). |

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10-bit operation mode is $x^{10}+x^9+x^6+x^3+x^2+x+1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the `crc_seed` register. When '0', the CRC is seeded by all-'0'; when '1' it is seeded with all-'1'.

In 8-bit mode, the polynomial is $x^8+x^6+x^3+x^2+1$. The CRC seed is configured by means of the `crc_seed` register.

NOTE: Note The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is at a minimum, equal to 1. The length of the black lines depends on the operation mode. For rolling shutter mode, it is equal to the line length configured in the active window. For global shutter mode, the sensor always reads out the entire line (80 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual LVDS channels, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, without frame start and ends (only line start and ends). The window ID is to be ignored and data is indicated by a BL code. In 8-bit mode, the configuration of the black level calibration block automatically scales to 8-bit mode. No reconfiguration is required.

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Example Using Multiple Windowing

Figure 32 shows an example of the synchronization codes sent when reading out multiple windows.

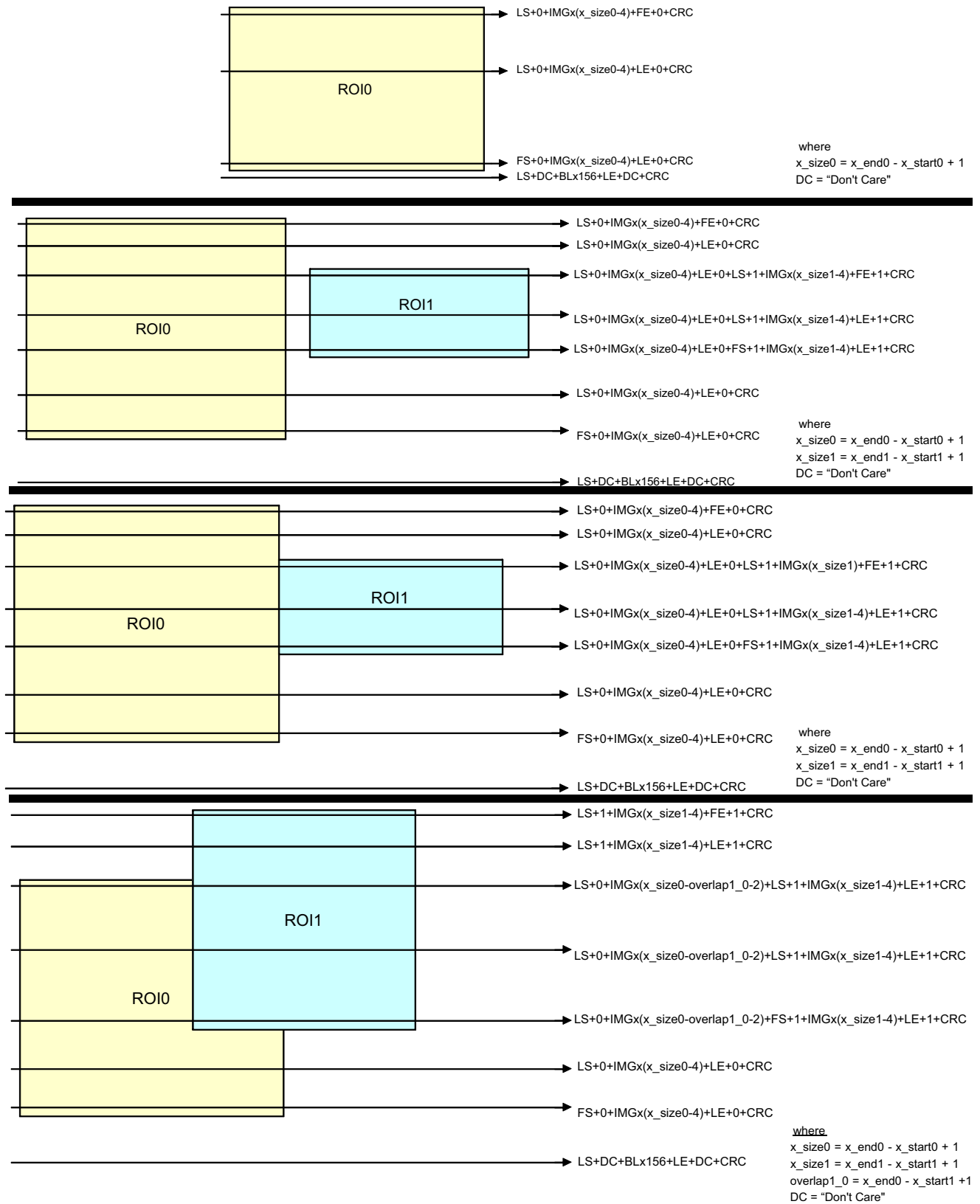


Figure 32. Synchronization Codes for Multiple Windows (applicable for Global Shutter only)

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Data Order

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is 64 pixels in x-direction by one pixel in y-direction.

The data order in 8-bit mode is identical to the 10-bit mode. Figure 33 indicates how the kernels are organized. The data order of this image data on the data output channels depends on the subsampling mode.

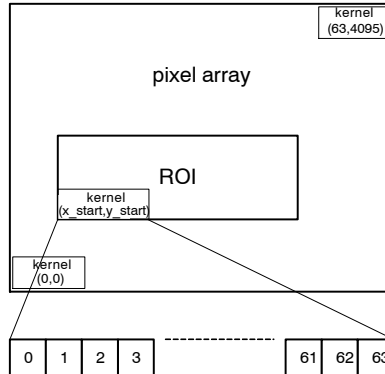


Figure 33. Kernel Organization in Pixel Array

- P1-SE/SN: Subsampling Disabled
 - ◆ 32 LVDS Output Channels

The image data is read out in kernels of 64 pixels in x-direction by one pixel in y-direction. One data channel delivers two pixel values of one kernel sequentially.

Figure 34 shows how a kernel is read out over the 32 output channels. For even positioned kernels, the kernels are read out ascending, and for odd positioned kernels the data order is reversed (descending).

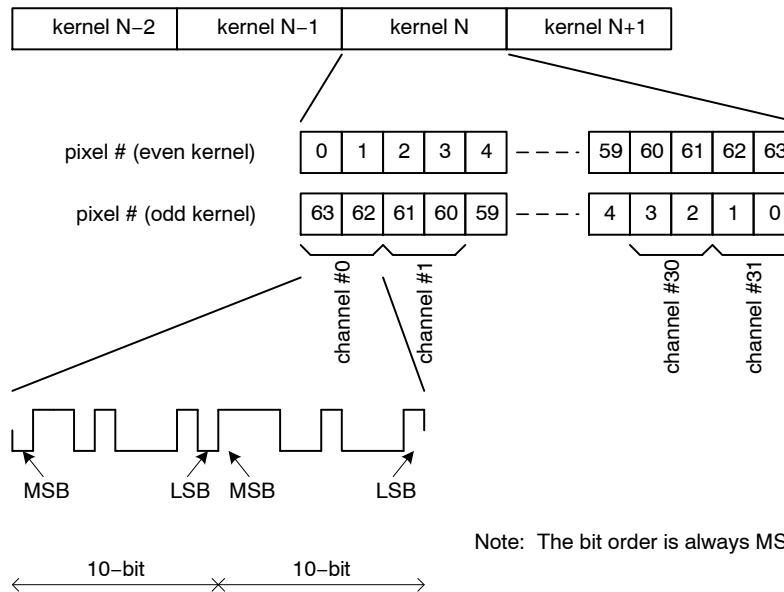


Figure 34. 32 LVDS Data Output Order when Subsampling is Disabled

- ◆ 16 LVDS Output Channels

Figure 35 shows how a kernel is read out over the 16 output channels. Each pair of adjacent channels is multiplexed into one channel. For even positioned kernels,

the kernels are read out ascending but in pair of even and odd pixels, while for odd positioned kernels the data order is reversed (descending) but in pair of even and odd pixels.

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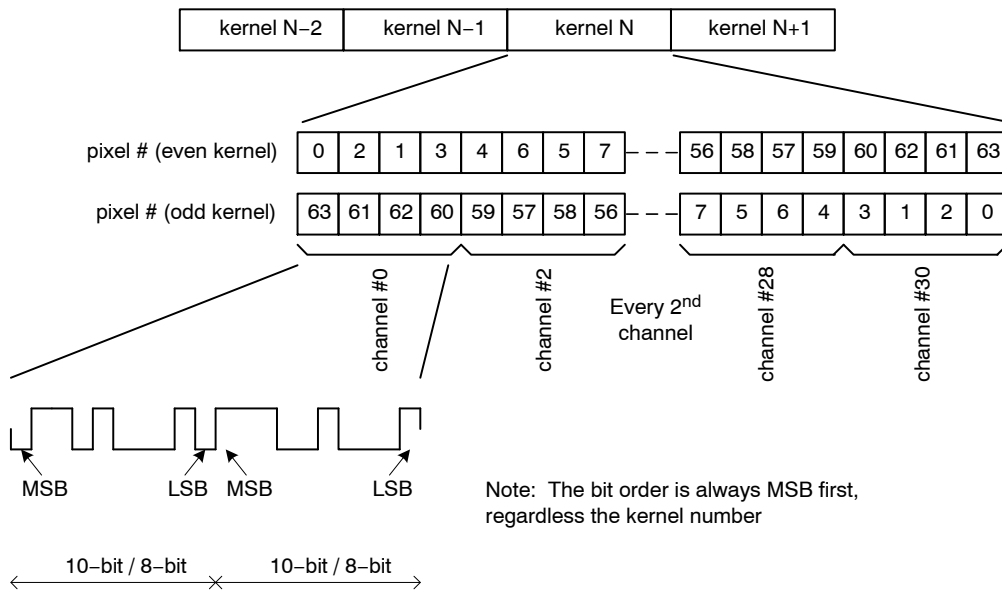


Figure 35. Data Output Order for 16 LVDS Outputs when Subsampling is Disabled

- **Subsampling on Monochrome Sensors**

During subsampling, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and one pixel in the y-direction.

Note that there is no difference in data order for even and odd kernel numbers. This is opposed to the 'no-subsampling' readout described earlier.

- ♦ **32 LVDS Output Channels**

Figure 36 shows the data order for 32 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

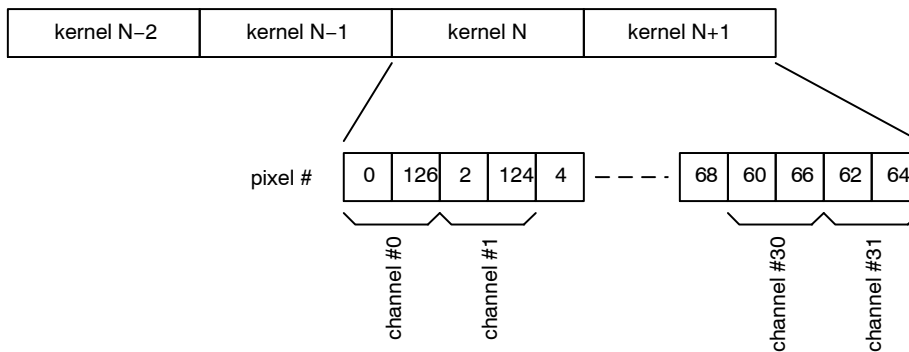


Figure 36. Data Output Order for 32 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

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◆ 16 LVDS Output Channels

Figure 37 shows the data order for 16 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

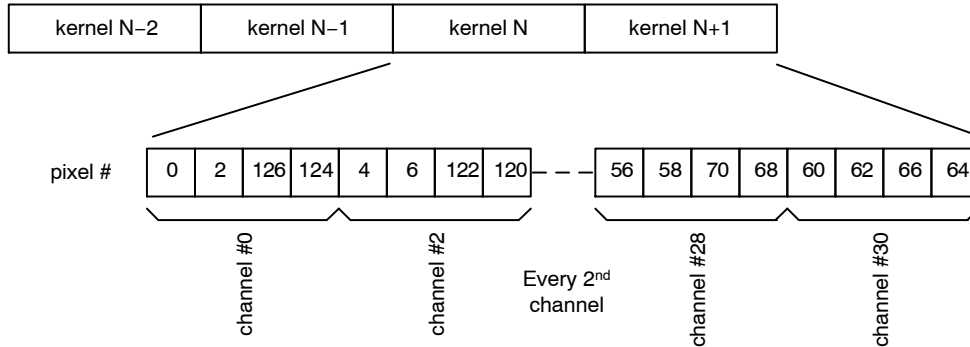


Figure 37. Data Output Order for 16 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

● Binning Mode

The output order in binning mode is identical to the subsampled mode.

● Subsampling on Color Sensor

To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and 1 pixel in

the y-direction. Only the pixels 0, 1, 4, 5, 8, 9, 12, 13 to 124, and 125 are read out. There is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section.

◆ 32 LVDS Output Channels

Figure 38 shows the data order for 32 LVDS output channels.

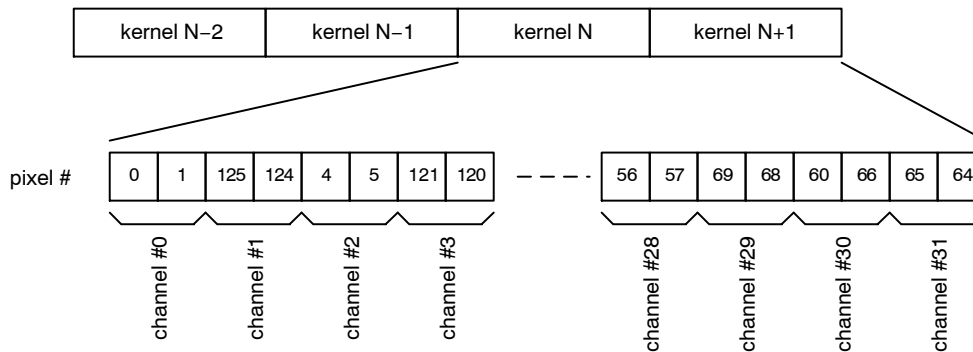


Figure 38. Data Output Order for 32 LVDS Output Channels in Subsampling Mode on a Color Sensor

◆ 16 LVDS Output Channels

Figure 39 shows the data order for 16 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

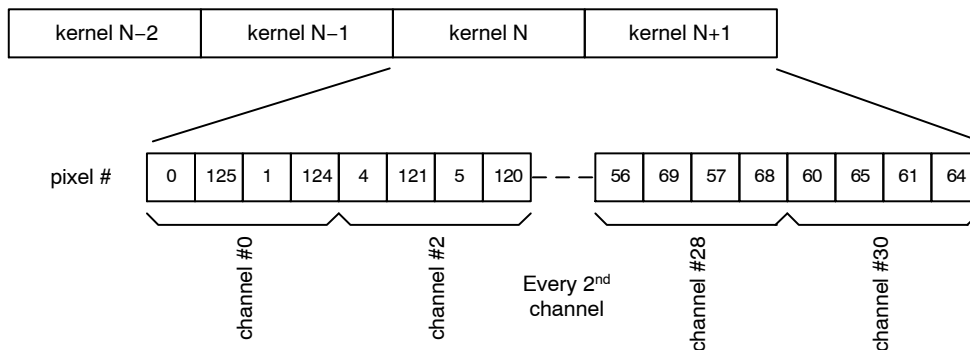


Figure 39. Data Output Order for 16 LVDS Output Channels in Subsampling Mode on a Color Sensor

Frame Rate

Frame rate for subsampling and binning mode is compared to the normal mode. Assume the y-resolution is the programmed number of lines to read out.

Normal Readout

The frame time in normal readout mode is shown by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (\text{y-resolution}) \times (t_{\text{ROT}} + t_{\text{readout}})$$

The frame rate is equal to 1/FrameTime. Nominal frame rate for full frame readout is 80 fps.

Subsampling Mode

The frame time for subsampled readout is shown by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (\text{y-resolution} / 2) \times (t_{\text{ROT}} + t_{\text{readout}} / 2),$$

where t_{ROT} represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.

Binning Mode

The frame time for subsampled readout is given by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (\text{y-resolution} / 2) \times (t_{\text{ROT}} \times 2 + t_{\text{readout}} / 2),$$

where t_{ROT} represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.

Test Pattern Generation

The data block provides several test pattern generation capabilities. Figure 40 shows the functional diagram for the data channels. It is possible to inject synthesized test patterns at various points. Refer to the Register Map on page 45 for the test mode configuration registers (registers 144 to 150).

In 8-bit mode, test patterns are generated as in 10-bit mode, however the two least significant bits of the resulting data are not transmitted.

The test pattern modes are summarized in Table 35. Note that these modes only exist for the data channel. The sync and clock channels do not provide this functionality.

For each test mode, the user can select whether the generated data is framed. When the register `frame_testpattern` is asserted, the test data simply replaces the ADC data. This means that the test data is only sent between frame/line start and frame/line end indications. Outside these windows, regular training patterns are sent, as during normal operation. CRC is calculated and inserted as for normal data for the fixed and incrementing test pattern generation.

Table 35. TEST MODE SUMMARY

| Register Configuration | | | Description |
|------------------------|----------------|-------------|--|
| prbs_en | testpattern_en | testpattern | |
| 0 | 0 | X | Normal operation mode |
| 0 | 1 | 0 | Fixed pattern generation. Pattern is defined by testpattern register |
| 0 | 1 | 1 | Incrementing pattern generation. Initial value is determined by testpattern. |
| 1 | X | X | PRBS data generation. The testpattern register determines the seed for the PRBS generator. |

When `frame_testpattern` is deasserted, the output is constantly replaced by the generated test data. No training patterns are generated.

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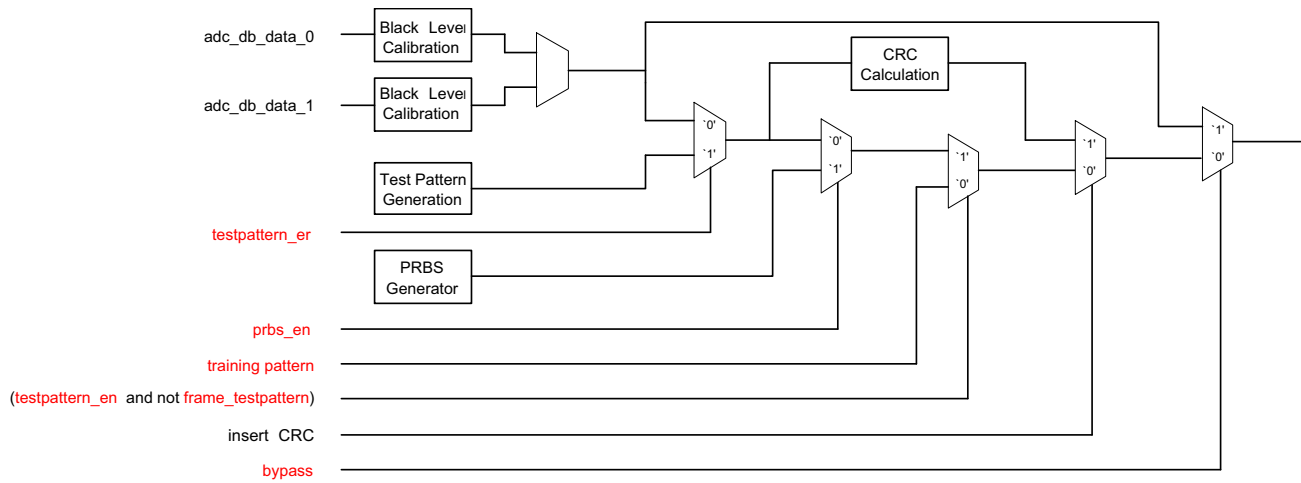


Figure 40. Functional Block Diagrams for the Data Channels

NOTE: In the figure, register configurations are indicated in red.

The sync channel continues to send regular frame timing information when the sequencer is enabled (independently of the test pattern configurations).

The synthesized test patterns are injected directly into the data channels. Therefore, no data demultiplexing is required at the receiving end (as opposed to regular image data capture).

Fixed Pattern

A configured word can be continuously repeated on the output. This word is configurable for each data channel separately (testpattern). The testpattern is inserted when testpattern_en is asserted.

Incrementing Test Pattern

In each cycle, the test pattern word is incremented by one, when inc_testpattern is asserted. After reaching the maximum value, the incrementer is reset to its start value (testpattern). When the testdata is framed, the incrementer is also reset to the testpattern value at each line start.

To enable this mode, enable the digital testpattern mode (assert testpattern_en) and assert inc_testpattern.

Pseudo Random Bit Sequence Generation

In this test mode, the output channels are sourced with pseudo random bit sequence (PRBS) pattern. The PRBS seed can be configured for each data channel using the testpattern register. For the other test pattern generation mode, the datastream is not interrupted when frame_testpattern is deasserted.

NOTES:

- The CRC generator is not functional in this mode, and no real CRC can be calculated. Instead, the CRC slot is used to send one more PRBS word.
- A PRBS generator does not generate random data when the seed is all zero. Therefore, it is advisable to configure the testpattern registers to a value different

from '0'. Using different seeds for each channel results in different sequences for each data channel.

E-grey and E-black Settings for Automatically Provided Correction Data

The uploads in Table 36 and Table 37 may be used to generate e-grey and e-black images for collecting image data to be used in correction algorithms without obscuring or illuminating the sensor.

Table 36. UPLOADS FOR E-BLACK IMAGE

| Register | Value |
|----------|--------|
| 219 | 0x3E3E |
| 220 | 0x6767 |

Table 37. UPLOADS FOR E-GREY IMAGE

| Register | Value |
|----------|--------|
| 219 | 0x3E2D |
| 220 | 0x674F |
| 429 | 0x0100 |
| 430 | 0x0BF1 |
| 431 | 0x0BC3 |
| 432 | 0x0BC2 |
| 435 | 0x2143 |
| 436 | 0x2142 |
| 463 | 0x0100 |
| 464 | 0x0FE4 |
| 465 | 0x0BC2 |
| 472 | 0x0B46 |
| 475 | 0x2143 |
| 476 | 0x2142 |

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REGISTER MAP

Each functional entity has a dedicated address space, starting at a block offset. The register address is obtained by adding the address offset to the block offset. This address

must be used to perform SPI uploads and is shown in the Address column of the register map table.

Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|------------------------------------|---------|-----------|--------------------|-------------|---------|--|--------|
| Chip ID [Block Offset: 0] | | | | | | | |
| 0 | 0 | | chip_id | 0x56FA | 22266 | | RO |
| | | [15:0] | id | 0x56FA | 22266 | ON Semiconductor Chip ID | |
| 1 | 1 | | revision | 0x0002 | 2 | | RO |
| | | [3:0] | rev | 0x2 | 2 | Chip Revision Numbering | |
| 2 | 2 | | chip_configuration | 0x0000 | 0 | | RW |
| | | [0] | color | 0x0 | 0 | Configure according to part number: Mono: 0x0 Color: 0x1 | |
| Clock Generator [Block Offset: 32] | | | | | | | |
| 0 | 32 | | config | 0x0004 | 4 | | RW |
| | | [0] | enable | 0x0 | 0 | Enable analogue clocks '0' = disabled, '1' = enabled | |
| | | [14:1] | reserved | 0x0002 | 2 | Reserved | |
| General Logic [Block Offset: 34] | | | | | | | |
| 0 | 34 | | config | 0x0000 | 0 | | RW |
| | | [0] | enable | 0x0 | 0 | Logic General Enable Configuration '0' = Disable '1' = Enable | |
| Image Core [Block Offset: 40] | | | | | | | |
| 0 | 40 | | image_core_config | 0x0000 | 0 | | RW |
| | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | [1] | mux_pwd_n | 0x0 | 0 | Column Multiplexer Power Down '0' = powered down, '1' = powered up | |
| | | [2] | reserved | 0x0 | 0 | Reserved | |
| 1 | 41 | | image_core_config | 0x0B5A | 2906 | | RW |
| | | [12:0] | reserved | 0xB5A | 2906 | Reserved | |
| | | [13] | testpattern | 0x0 | 0 | Testpattern generation in the columns | |
| | | [14] | injectlevel | 0x0 | 0 | Inject level for testpattern generation | |
| | | [15] | reserved | 0x0 | 0 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|-----------------------------------|---------|-----------|-------------------|-------------|---------|--|--------|
| AFE [Block Offset: 48] | | | | | | | |
| 0 | 48 | | power_down | 0x0000 | 0 | | RW |
| | | [0] | pwd_n | 0x0 | 0 | Power down for AFE's (64 columns) '0' = powered down, '1' = powered up | |
| Bias Generator [Block Offset: 64] | | | | | | | |
| 0 | 64 | | power_down | 0x0000 | 0 | | RW |
| | | [0] | pwd_n | 0x0 | 0 | Power down bandgap '0' = powered down, '1' = powered up | |
| 1 | 65 | | configuration | 0x888B | 34955 | | RW |
| | | [0] | extres | 0x1 | 1 | External Resistor Selection '0' = internal resistor, '1' = external resistor | |
| | | [3:1] | bgrtrim | 0x5 | 5 | Bandgap Trim | |
| | | [7:4] | imc_colpc_ibias | 0x8 | 8 | Column Precharge ibias Configuration | |
| | | [11:8] | imc_colbias_ibias | 0x8 | 8 | Column Bias ibias Configuration | |
| | | [15:12] | reserved | 0x8 | 8 | Reserved | |
| 2 | 66 | | afe_bias | 0x53C8 | 21448 | | RW |
| | | [3:0] | afe_ibias | 0x8 | 8 | AFE ibias Configuration | |
| | | [7:4] | afe_adc_iref | 0xC | 12 | ADC iref Configuration | |
| | | [14:8] | afe_pga_iref | 0x53 | 83 | PGA iref Configuration | |
| 3 | 67 | | mux_bias | 0x8888 | 34952 | | RW |
| | | [3:0] | mux_25u_stage1 | 0x8 | 8 | Column Multiplexer Stage 1 Bias Configuration | |
| | | [7:4] | mux_25u_stage2 | 0x8 | 8 | Column Multiplexer Stage 2 Bias Configuration | |
| | | [11:8] | mux_25u_delay | 0x8 | 8 | Column Multiplexer Delay Bias Configuration | |
| | | [15:12] | mux_25u_vcmbuff | 0x8 | 8 | Column Multiplexer Vcm Bias Configuration | |
| 4 | 68 | | lvds_bias | 0x0088 | 136 | | RW |
| | | [3:0] | lvds_ibias | 0x8 | 8 | LVDS Ibias | |
| | | [7:4] | lvds_iref | 0x8 | 8 | LVDS Iref | |
| 6 | 70 | | reserved | 0x8888 | 34952 | | RW |
| | | [15:0] | reserved | 0x8888 | 34952 | Reserved | |
| Test [Block Offset: 80] | | | | | | | |
| 0 | 80 | | reserved | 0x0000 | 0 | | RW |
| | | [9:0] | reserved | 0x0 | 0 | Reserved | |
| 1 | 81 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|---------------------------------|---------|-----------|-----------------------|-------------|---------|---|--------|
| 16 | 96 | | reserved | 0x0000 | 0 | | RW |
| | | [5:0] | reserved | 0x0 | 0 | Reserved | |
| 17 | 97 | | reserved | 0x0000 | 0 | | RO |
| | | [7:0] | reserved | 0x00 | 0 | Reserved | |
| Ser/lvds/io [Block Offset: 112] | | | | | | | |
| 0 | 112 | | power_down | 0x0000 | 0 | | RW |
| | | [0] | clock_out_pwd_n | 0x0 | 0 | Power down for Clock Output. '0' = powered down, '1' = powered up | |
| | | [1] | sync_pwd_n | 0x0 | 0 | Power down for Sync channel '0' = powered down, '1' = powered up | |
| | | [2] | data_pwd_n | 0x0 | 0 | Power down for data channels (4 channels) '0' = powered down, '1' = powered up | |
| Data Block [Block Offset: 128] | | | | | | | |
| 0 | 128 | | blackcal | 0x4008 | 16392 | | RW |
| | | [7:0] | black_offset | 0x08 | 8 | Desired black level at output | |
| | | [10:8] | black_samples | 0x0 | 0 | Black pixels taken into account for black calibration. Total samples = 2**black_samples | |
| | | [14:11] | reserved | 0x8 | 8 | Reserved | |
| | | [15] | crc_seed | 0x0 | 0 | CRC Seed '0' = All-0 '1' = All-1 | |
| 1 | 129 | | general_configuration | 0xC001 | 49153 | | RW |
| | | [0] | auto_blackcal_enable | 0x1 | 1 | Automatic blackcalibration is enabled when 1, bypassed when 0 | |
| | | [9:1] | blackcal_offset | 0x00 | 0 | Black Calibration offset used when auto_black_cal_en = '0'. | |
| | | [10] | blackcal_offset_dec | 0x0 | 0 | blackcal_offset is added when 0, subtracted when 1 | |
| | | [11] | reserved | 0x0 | 0 | Reserved | |
| | | [12] | reserved | 0x0 | 0 | Reserved | |
| | | [13] | 8bit_mode | 0x0 | 0 | Shifts window ID indications by 4 cycles. '0' = 10-bit mode, '1' = 8-bit mode | |
| | | [15:14] | reserved | 0x3 | 3 | Reserved | |
| 2 | 130 | | trainingpattern | 0x03A6 | 934 | | RW |
| | | [9:0] | trainingpattern | 0x3A6 | 934 | Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels. | |
| | | [10] | reserved | 0x0 | 0 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|-----------------------|-------------|---------|---|--------|
| 3 | 131 | | sync_code0 | 0x002A | 42 | | RW |
| | | [6:0] | frame_sync | 0x02A | 42 | Frame Sync LSBs Note: The three MSBs of the resulting 10-bit Frame sync word is not configurable. The tenth bit indicates frame/line sync code, ninth bit indicates start, eighth bit indicates end. | |
| 4 | 132 | | sync_code1 | 0x0015 | 21 | | RW |
| | | [9:0] | bl | 0x015 | 21 | Black Pixel Identification Sync Code | |
| 5 | 133 | | sync_code2 | 0x0035 | 53 | | RW |
| | | [9:0] | img | 0x035 | 53 | Valid Pixel Identification Sync Code | |
| 6 | 134 | | sync_code3 | 0x0059 | 89 | | RW |
| | | [9:0] | crc | 0x059 | 89 | CRC Value Identification Sync Code | |
| 7 | 135 | | sync_code4 | 0x03A6 | 934 | | RW |
| | | [9:0] | tr | 0x3A6 | 934 | Training Value Identification Sync Code | |
| 8 | 136 | | blackcal_error0 | 0x0000 | 0 | | RO |
| | | [15:0] | blackcal_error[15:0] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0-15 | |
| 9 | 137 | | blackcal_error1 | 0x0000 | 0 | | RO |
| | | [15:0] | blackcal_error[31:16] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 16-31 | |
| 10 | 138 | | blackcal_error2 | 0x0000 | 0 | | RO |
| | | [15:0] | blackcal_error[47:32] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 32-47 | |
| 11 | 139 | | blackcal_error3 | 0x0000 | 0 | | RO |
| | | [15:0] | blackcal_error[63:48] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 48-63 | |
| 12 | 140 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 13 | 141 | | reserved | 0xFFFF | 65535 | | RW |
| | | [15:0] | reserved | 0xFFFF | 65535 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|--------------------|---------|-----------|---------------------|-------------|---------|--|--------|
| (Datablock - Test) | | | | | | | |
| 16 | 144 | | test_configuration | 0x0000 | 0 | | RW |
| | | [0] | testpattern_en | 0x0 | 0 | Insert synthesized testpattern when '1', normal operation when '0'. | |
| | | [1] | inc_testpattern | 0x0 | 0 | Incrementing testpattern when '1', constant testpattern when '0' | |
| | | [2] | prbs_en | 0x0 | 0 | Incrementing tstpattern when '1'. constant testpattern when '0'. Lower bound is defined by testpattern*, upper bound is 1023. After reaching 1023, the counter is reloaded with configured start data. | |
| | | [3] | frame_testpattern | 0x0 | 0 | Frame test patterns when '1', unframed testpatterns when '0' | |
| | | [4] | reserved | 0x0 | 0 | Reserved | |
| 17 | 145 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | | 0 | Reserved | |
| 18 | 146 | | test_configuration0 | 0x0100 | 256 | | RW |
| | | [7:0] | testpattern0_lsb | 0x00 | 0 | Testpattern (LSBs) used on datapath #0, #8, #16, #24 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | [15:8] | testpattern1_lsb | 0x01 | 1 | Testpattern (LSBs) used on datapath #1, #9, #17, # 25 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| 19 | 147 | | test_configuration1 | 0x0302 | 770 | | RW |
| | | [7:0] | testpattern2_lsb | 0x02 | 2 | Testpattern (LSBs) used on datapath #2, #10, #18, #26 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | [15:8] | testpattern3_lsb | 0x03 | 3 | Testpattern (LSBs) used on datapath #3, #11, #19, #27 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| 20 | 148 | | test_configuration2 | 0x0504 | 1284 | | RW |
| | | [7:0] | testpattern4_lsb | 0x04 | 4 | Testpattern (LSBs) used on datapath #4, #12, #20, #28 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | [15:8] | testpattern5_lsb | 0x05 | 5 | Testpattern (LSBs) used on datapath #5, #13, #21, #29 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------|-------------|---------|--|--------|
| 21 | 149 | | test_configuration3 | 0x0706 | 1798 | | RW |
| | | [7:0] | testpattern6_lsb | 0x06 | 6 | Testpattern (LSBs) used on datapath #6, #14, #22, #30 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | [15:8] | testpattern7_lsb | 0x07 | 7 | Testpattern (LSBs) used on datapath #7, #15, #23, #31 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| 22 | 150 | | test_configuration16 | 0x0000 | 0 | | RW |
| | | [1:0] | testpattern0_msb | 0x0 | 0 | Testpattern (LSBs) used on datapath #0, #8, #16, #24 when testpattern_en = '1'. Note: Least significant bits are configured in register 146. | |
| | | [3:2] | testpattern1_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #1, #9, #17, #25 when testpattern_en = '1'. Note: Least significant bits are configured in register 146. | |
| | | [5:4] | testpattern2_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #2, #10, #18, #26 when testpattern_en = '1'. Note: Least significant bits are configured in register 147. | |
| | | [7:6] | testpattern3_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #3, #11, #19, #27 when testpattern_en = '1'. Note: Least significant bits are configured in register 147. | |
| | | [9:8] | testpattern4_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #4, #12, #20, #28 when testpattern_en = '1'. Note: Least significant bits are configured in register 148. | |
| | | [11:10] | testpattern5_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #5, #13, #21, #29 when testpattern_en = '1'. Note: Least significant bits are configured in register 148. | |
| | | [13:12] | testpattern6_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #6, #14, #22, #30 when testpattern_en = '1'. Note: Least significant bits are configured in register 149. | |
| | | [15:14] | testpattern7_msb | 0x0 | 0 | Testpattern (MSBs) used on datapath #7, #15, #23, #31 when testpattern_en = '1'. Note: Least significant bits are configured in register 149. | |
| 26 | 154 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 27 | 155 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|-------------------------------|---------|-----------|------------------------|-------------|---------|---|--------|
| 0 | 160 | | reserved | | | | RW |
| | | [15:0] | reserved | | | Reserved | |
| ... | ... | ... | ... | | | ... | |
| 31 | 191 | | reserved | | | | RW |
| | | [15:0] | reserved | | | Reserved | |
| Sequencer [Block Offset: 192] | | | | | | | |
| 0 | 192 | | general_configuration | 0x0000 | 0 | | RW |
| | | [0] | enable | 0x0 | 0 | Enable sequencer '0' = Idle, '1' = enabled | |
| | | [1] | rolling_shutter_enable | 0x0 | 0 | Operation Selection '0' = Global Shutter, '1' = Rolling Shutter | |
| | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | [4] | triggered_mode | 0x0 | 0 | Triggered Mode Selection (Global Shutter only) '0' = Normal Mode, '1' = Triggered Mode | |
| | | [5] | slave_mode | 0x0 | 0 | Master/Slave Selection (Global Shutter only) '0' = master, '1' = slave | |
| | | [6] | reserved | 0x0 | 0 | Reserved | |
| | | [7] | subsampling | 0x0 | 0 | Subsampling mode selection '0' = no subsampling, '1' = subsampling | |
| | | [8] | binning | 0x0 | 0 | Binning mode selection '0' = no binning, '1' = binning | |
| | | [9] | reserved | 0x0 | 0 | Reserved | |
| | | [10] | reserved | 0x0 | 0 | Reserved | |
| | | [13:11] | monitor_select | 0x0 | 0 | Control of the monitor pins | |
| | | [14] | reserved | 0x0 | 0 | Reserved | |
| 1 | 193 | | delay_configuration | 0x0000 | 0 | | RW |
| | | [7:0] | rs_x_length | 0x00 | 0 | X-Readout duration in rolling shutter mode (extends lines with dummy pixels). | |
| | | [15:8] | reserved | 0x00 | 0 | Reserved | |
| 2 | 194 | | integration_control | 0x0004 | 4 | | RW |
| | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | [2] | fr_mode | 0x1 | 1 | Representation of fr_length. '0': reset length '1': frame length | |
| | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | [5:4] | reserved | 0x0 | 0 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|------------------|-------------|---------|--|--------|
| | | [8] | subsampling_mode | 0x0 | 0 | Subsampling Mode '0' = Subsampling / Binning in x and y '1' = Subsampling / Binning in y, not in x | |
| | | [9] | binning_mode | 0x0 | 0 | Binning Mode '0' = Binning in x, subsample in y '1' = Binning in x and y | |
| | | [10] | reserved | 0x0 | 0 | Reserved | |
| 3 | 195 | | roi_active0 | 0x0001 | 1 | | RW |
| | | [0] | roi_active0 | 0x1 | 1 | Selection of ROI 0 '0' = inactive, '1' = active | |
| | | [1] | roi_active1 | 0x0 | 0 | Selection of ROI 1 '0' = inactive, '1' = active | |
| | | [2] | roi_active2 | 0x0 | 0 | Selection of ROI 2 '0' = inactive, '1' = active | |
| | | [3] | roi_active3 | 0x0 | 0 | Selection of ROI 3 '0' = inactive, '1' = active | |
| | | [4] | roi_active4 | 0x0 | 0 | Selection of ROI 4 '0' = inactive, '1' = active | |
| | | [5] | roi_active5 | 0x0 | 0 | Selection of ROI 5 '0' = inactive, '1' = active | |
| | | [6] | roi_active6 | 0x0 | 0 | Selection of ROI 6 '0' = inactive, '1' = active | |
| | | [7] | roi_active7 | 0x0 | 0 | Selection of ROI 7 '0' = inactive, '1' = active | |
| | | [8] | roi_active8 | 0x0 | 0 | Selection of ROI 8 '0' = inactive, '1' = active | |
| | | [9] | roi_active9 | 0x0 | 0 | Selection of ROI 9 '0' = inactive, '1' = active | |
| | | [10] | roi_active10 | 0x0 | 0 | Selection of ROI 10 '0' = inactive, '1' = active | |
| | | [11] | roi_active11 | 0x0 | 0 | Selection of ROI 11 '0' = inactive, '1' = active | |
| | | [12] | roi_active12 | 0x0 | 0 | Selection of ROI 12 '0' = inactive, '1' = active | |
| | | [13] | roi_active13 | 0x0 | 0 | Selection of ROI 13 '0' = inactive, '1' = active | |
| | | [14] | roi_active14 | 0x0 | 0 | Selection of ROI 14 '0' = inactive, '1' = active | |
| | | [15] | roi_active15 | 0x0 | 0 | Selection of ROI 15 '0' = inactive, '1' = active | |
| 4 | 196 | | roi_active1 | 0x0000 | 0 | | RW |
| | | [0] | roi_active16 | 0x0 | 0 | Selection of ROI 16 '0' = inactive, '1' = active | |
| | | [1] | roi_active17 | 0x0 | 0 | Selection of ROI 17 '0' = inactive, '1' = active | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|-----------------|-------------|---------|---|--------|
| | | [2] | roi_active18 | 0x0 | 0 | Selection of ROI 18 '0' = inactive, '1' = active | |
| | | [3] | roi_active19 | 0x0 | 0 | Selection of ROI 19 '0' = inactive, '1' = active | |
| | | [4] | roi_active20 | 0x0 | 0 | Selection of ROI 20 '0' = inactive, '1' = active | |
| | | [5] | roi_active21 | 0x0 | 0 | Selection of ROI 21 '0' = inactive, '1' = active | |
| | | [6] | roi_active22 | 0x0 | 0 | Selection of ROI 22 '0' = inactive, '1' = active | |
| | | [7] | roi_active23 | 0x0 | 0 | Selection of ROI 23 '0' = inactive, '1' = active | |
| | | [8] | roi_active24 | 0x0 | 0 | Selection of ROI 24 '0' = inactive, '1' = active | |
| | | [9] | roi_active25 | 0x0 | 0 | Selection of ROI 25 '0' = inactive, '1' = active | |
| | | [10] | roi_active26 | 0x0 | 0 | Selection of ROI 26 '0' = inactive, '1' = active | |
| | | [11] | roi_active27 | 0x0 | 0 | Selection of ROI 27 '0' = inactive, '1' = active | |
| | | [12] | roi_active28 | 0x0 | 0 | Selection of ROI 28 '0' = inactive, '1' = active | |
| | | [13] | roi_active29 | 0x0 | 0 | Selection of ROI 29 '0' = inactive, '1' = active | |
| | | [14] | roi_active30 | 0x0 | 0 | Selection of ROI 30 '0' = inactive, '1' = active | |
| | | [15] | roi_active31 | 0x0 | 0 | Selection of ROI 31 '0' = inactive, '1' = active | |
| 5 | 197 | | black_lines | 0x0102 | 258 | | RW |
| | | [7:0] | black_lines | 0x02 | 2 | Number of black lines. Range 1-255 | |
| | | [8] | gate_first_line | 0x1 | 1 | Blank out first line '0': No blank-out '1': Blank-out | |
| 6 | 198 | | dummy_lines | 0x0000 | 0 | | RW |
| | | [11:0] | dummy_lines | 0x000 | 0 | Number of Dummy lines (Rolling Shutter only) Range 0-4095 | |
| 7 | 199 | | mult_timer | 0x0001 | 1 | | RW |
| | | [15:0] | mult_timer | 0x0001 | 1 | Mult Timer (Global Shutter only) Defines granularity (unit = 1/68MHz) of exposure and reset_length | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|---------------|-------------|---------|---|--------|
| 8 | 200 | | fr_length | 0x0000 | 0 | | RW |
| | | [15:0] | fr_length | 0x0000 | 0 | Frame/Reset length (Global Shutter only) Reset length when fr_mode = '0', Frame Length when fr_mode = '1' Granularity defined by mult_timer | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------------|-------------|---------|---|--------|
| 9 | 201 | | exposure | 0x0000 | 0 | | RW |
| | | [15:0] | exposure | 0x0000 | 0 | Exposure Time Rolling Shutter: granularity lines Global Shutter: granularity defined by mult_timer | |
| 10 | 202 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 11 | 203 | | reserved | 0x0000 | 0 | | RW |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 12 | 204 | | gain_configuration | 0x01E2 | 482 | | RW |
| | | [4:0] | mux_gainsw | 0x02 | 2 | Column Gain Setting | |
| | | [12:5] | afe_gain | 0x0F | 15 | AFE Programmable Gain Setting | |
| | | [13] | gain_lat_comp | 0x0 | 0 | Postpone gain update by 1 frame when '1' to compensate for exposure time update latency. Gain is applied at start of next frame if '0' | |
| 13 | 205 | | digital_gain_configuration | 0x0080 | 128 | | RW |
| | | [11:0] | db_gain | 0x080 | 128 | Digital Gain 5.7 unsigned format | |
| 14 | 206 | | sync_configuration | 0x033F | 831 | | RW |
| | | [0] | sync_rs_x_length | 0x1 | 1 | Update of rs_x_length will not be sync'ed at start of frame when '0' | |
| | | [1] | sync_black_lines | 0x1 | 1 | Update of black_lines will not be sync'ed at start of frame when '0' | |
| | | [2] | sync_dummy_lines | 0x1 | 1 | Update of dummy_lines will not be sync'ed at start of frame when '0' | |
| | | [3] | sync_exposure | 0x1 | 1 | Update of exposure parameters will not be sync'ed at start of frame when '0' | |
| | | [4] | sync_gain | 0x1 | 1 | Update of gain parameters (gain_sw, afe_gain) will not be sync'ed at start of frame when '0' | |
| | | [5] | sync_roi | 0x1 | 1 | Update of roi updates (active_roi) will not be sync'ed at start of frame when '0' | |
| | | [8] | blank_roi_switch | 0x1 | 1 | Blank first frame after ROI switching | |
| | | [9] | blank_sub-sampling_ss | 0x1 | 1 | Blank first frame after sub-sampling/binning mode switching in Global shutter mode (always blanked out in rolling shutter mode) | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|---------------------|-------------|---------|---|--------|
| | | [10] | exposure_sync_mode | 0x0 | 0 | When '0', exposure parameters are sync'ed at the start of FOT. When '1', exposure parameters sync is disabled (continuously syncing). This mode is only relevant for Triggered Global - master mode, where the exposure parameters are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'. | |
| 16 | 208 | | mult_timer_status | 0x0000 | 0 | | RO |
| | | [15:0] | mult_timer | 0x0000 | 0 | Mult Timer Status (Master Global Shutter only) | |
| 17 | 209 | | reset_length_status | 0x0000 | 0 | | RO |
| | | [15:0] | reset_length | 0x0000 | 0 | Current Reset Length (not in Slave mode) | |
| 18 | 210 | | exposure_status | 0x0000 | 0 | | RO |
| | | [15:0] | exposure | 0x0000 | 0 | Current Exposure Time (not in Slave mode) | |
| 19 | 211 | | reserved | 0x0000 | 0 | | RO |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 20 | 212 | | reserved | 0x0000 | 0 | | RO |
| | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| 21 | 213 | | gain_status | 0x0000 | 0 | | RO |
| | | [4:0] | mux_gainsw | 0x00 | 0 | Current Column Gain Setting | |
| | | [12:5] | afe_gain | 0x00 | 0 | Current AFE Programmable Gain | |
| 22 | 214 | | digital_gain_status | 0x0000 | 0 | | RO |
| | | [11:0] | db_gain | 0x000 | 0 | Current Digital Gain | |
| | | [13:12] | reserved | 0x0 | 0 | Reserved | |
| 24 | 216 | | reserved | 0x7F00 | 32512 | | RW |
| | | [6:0] | reserved | 0x00 | 0 | Reserved | |
| | | [14:8] | reserved | 0x7F | 127 | Reserved | |
| 25 | 217 | | reserved | 0x261E | 9758 | | RW |
| | | [6:0] | reserved | 0x1E | 30 | Reserved | |
| | | [14:8] | reserved | 0x26 | 38 | Reserved | |
| 26 | 218 | | reserved | 0x160E | 5646 | | RW |
| | | [6:0] | reserved | 0xE | 14 | Reserved | |
| | | [14:8] | reserved | 0x16 | 22 | Reserved | |
| 27 | 219 | | reserved | 0x3E2E | 15918 | | RW |
| | | [6:0] | reserved | 0x2E | 46 | Reserved | |
| | | [14:8] | reserved | 0x3E | 62 | Reserved | |
| 28 | 220 | | reserved | 0x6750 | 26448 | | RW |
| | | [6:0] | reserved | 0x50 | 80 | Reserved | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|-----------------------------------|---------|-----------|---------------------|-------------|---------|-----------------------------|--------|
| | | [14:8] | reserved | 0x67 | 103 | Reserved | |
| 29 | 221 | | reserved | 0.0008 | 8 | | RW |
| | | [6:0] | reserved | 0x08 | 8 | Reserved | |
| ... | ... | | ... | | | ... | |
| 63 | 255 | | reserved | | | | RW |
| | | [13:0] | reserved | | | Reserved | |
| Sequencer ROI [Block Offset: 256] | | | | | | | |
| 0 | 256 | | roi0_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 0 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 0 X End Configuration | |
| 1 | 257 | | roi0_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 0 Y Start Configuration | |
| 2 | 258 | | roi0_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 0 Y End Configuration | |
| 3 | 259 | | roi1_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 1 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 1 X End Configuration | |
| 4 | 260 | | roi1_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 1 Y Start Configuration | |
| 5 | 261 | | roi1_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 1 Y End Configuration | |
| 6 | 262 | | roi2_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 2 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 2 X End Configuration | |
| 7 | 263 | | roi2_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 2 Y Start Configuration | |
| 8 | 264 | | roi2_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 2 Y End Configuration | |
| 9 | 265 | | roi3_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 3 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 3 X End Configuration | |
| 10 | 266 | | roi3_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 3 Y Start Configuration | |
| 11 | 267 | | roi3_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 3 Y End Configuration | |
| 12 | 268 | | roi4_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 4 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 4 X End Configuration | |
| 13 | 269 | | roi4_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 4 Y Start Configuration | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------|-------------|---------|------------------------------|--------|
| 14 | 270 | | roi4_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 4 Y End Configuration | |
| 15 | 271 | | roi5_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 5 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 5 X End Configuration | |
| 16 | 272 | | roi5_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 5 Y Start Configuration | |
| 17 | 273 | | roi5_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 5 Y End Configuration | |
| 18 | 274 | | roi6_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 6 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 6 X End Configuration | |
| 19 | 275 | | roi6_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 6 Y Start Configuration | |
| 20 | 276 | | roi6_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 6 Y End Configuration | |
| 21 | 277 | | roi7_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 7 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 7 X End Configuration | |
| 22 | 278 | | roi7_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 7 Y Start Configuration | |
| 23 | 279 | | roi7_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 7 Y End Configuration | |
| 24 | 280 | | roi8_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 8 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 8 X End Configuration | |
| 25 | 281 | | roi8_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 8 Y Start Configuration | |
| 26 | 282 | | roi8_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 8 Y End Configuration | |
| 27 | 283 | | roi9_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 9 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 9 X End Configuration | |
| 28 | 284 | | roi9_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 9 Y Start Configuration | |
| 29 | 285 | | roi9_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 9 Y End Configuration | |
| 30 | 286 | | roi10_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 10 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 10 X End Configuration | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------|-------------|---------|------------------------------|--------|
| 31 | 287 | | roi10_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 10 Y Start Configuration | |
| 32 | 288 | | roi10_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 10 Y End Configuration | |
| 33 | 289 | | roi11_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 11 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 11 X End Configuration | |
| 34 | 290 | | roi11_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 11 Y Start Configuration | |
| 35 | 291 | | roi11_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 11 Y End Configuration | |
| 36 | 292 | | roi12_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 12 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 12 X End Configuration | |
| 37 | 293 | | roi12_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 12 Y Start Configuration | |
| 38 | 294 | | roi12_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 12 Y End Configuration | |
| 39 | 295 | | roi13_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 13 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 13 X End Configuration | |
| 40 | 296 | | roi13_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 13 Y Start Configuration | |
| 41 | 297 | | roi13_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 13 Y End Configuration | |
| 42 | 298 | | roi14_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 14 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 14 X End Configuration | |
| 43 | 299 | | roi14_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 14 Y Start Configuration | |
| 44 | 300 | | roi14_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 14 Y End Configuration | |
| 45 | 301 | | roi15_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 15 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 15 X End Configuration | |
| 46 | 302 | | roi15_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 15 Y Start Configuration | |
| 47 | 303 | | roi15_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 15 Y End Configuration | |
| 48 | 304 | | roi16_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 16 X Start Configuration | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------|-------------|---------|------------------------------|--------|
| | | [15:8] | x_end | 0x4F | 79 | ROI 16 X End Configuration | |
| 49 | 305 | | roi16_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 16 Y Start Configuration | |
| 50 | 306 | | roi16_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 16 Y End Configuration | |
| 51 | 307 | | roi17_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 17 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 17 X End Configuration | |
| 52 | 308 | | roi17_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 17 Y Start Configuration | |
| 53 | 309 | | roi17_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 17 Y End Configuration | |
| 54 | 310 | | roi18_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 18 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 18 X End Configuration | |
| 55 | 311 | | roi18_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 18 Y Start Configuration | |
| 56 | 312 | | roi18_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 18 Y End Configuration | |
| 57 | 313 | | roi19_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 19 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 19 X End Configuration | |
| 58 | 314 | | roi19_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 19 Y Start Configuration | |
| 59 | 315 | | roi19_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 19 Y End Configuration | |
| 60 | 316 | | roi20_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 20 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 20 X End Configuration | |
| 61 | 317 | | roi20_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 20 Y Start Configuration | |
| 62 | 318 | | roi20_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 20 Y End Configuration | |
| 63 | 319 | | roi21_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 21 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 21 X End Configuration | |
| 64 | 320 | | roi21_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 21 Y Start Configuration | |
| 65 | 321 | | roi21_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 21 Y End Configuration | |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|----------------|---------|-----------|----------------------|-------------|---------|------------------------------|--------|
| 66 | 322 | | roi22_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 22 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 22 X End Configuration | |
| 67 | 323 | | roi22_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 22 Y Start Configuration | |
| 68 | 324 | | roi22_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 22 Y End Configuration | |
| 69 | 325 | | roi23_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 23 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 23 X End Configuration | |
| 70 | 326 | | roi23_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 23 Y Start Configuration | |
| 71 | 327 | | roi23_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 23 Y End Configuration | |
| 72 | 328 | | roi24_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 24 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 24 X End Configuration | |
| 73 | 329 | | roi24_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 24 Y Start Configuration | |
| 74 | 330 | | roi24_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 24 Y End Configuration | |
| 75 | 331 | | roi25_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 25 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 25 X End Configuration | |
| 76 | 332 | | roi25_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 25 Y Start Configuration | |
| 77 | 333 | | roi25_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 25 Y End Configuration | |
| 78 | 334 | | roi26_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 26 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 26 X End Configuration | |
| 79 | 335 | | roi26_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 26 Y Start Configuration | |
| 80 | 336 | | roi26_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 26Y End Configuration | |
| 81 | 337 | | roi27_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 27 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 27 X End Configuration | |
| 82 | 338 | | roi27_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 27 Y Start Configuration | |
| 83 | 339 | | roi27_configuration2 | 0x13FF | 5119 | | RW |

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Table 38. REGISTER MAP

| Address Offset | Address | Bit Field | Register Name | Default Hex | Default | Description | Access |
|---------------------------------------|---------|-----------|----------------------|-------------|---------|------------------------------|--------|
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 27 Y End Configuration | |
| 84 | 340 | | roi28_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 28 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 28 X End Configuration | |
| 85 | 341 | | roi28_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 28 Y Start Configuration | |
| 86 | 342 | | roi28_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 28 Y End Configuration | |
| 87 | 343 | | roi29_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 29 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 29 X End Configuration | |
| 88 | 344 | | roi29_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 29 Y Start Configuration | |
| 89 | 345 | | roi29_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 29 Y End Configuration | |
| 90 | 346 | | roi30_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 30 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 30 X End Configuration | |
| 91 | 347 | | roi30_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 30 Y Start Configuration | |
| 92 | 348 | | roi30_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 30 Y End Configuration | |
| 93 | 349 | | roi31_configuration0 | 0x4F00 | 20224 | | RW |
| | | [7:0] | x_start | 0x00 | 0 | ROI 31 X Start Configuration | |
| | | [15:8] | x_end | 0x4F | 79 | ROI 31 X End Configuration | |
| 94 | 350 | | roi31_configuration1 | 0x0000 | 0 | | RW |
| | | [12:0] | y_start | 0x0000 | 0 | ROI 31 Y Start Configuration | |
| 95 | 351 | | roi31_configuration2 | 0x13FF | 5119 | | RW |
| | | [12:0] | y_end | 0x13FF | 5119 | ROI 31 Y End Configuration | |
| Sequencer Program [Block Offset: 384] | | | | | | | |
| 0 | 384 | | reserved | | | | RW |
| | | [15:0] | reserved | | | Reserved | |
| ... | ... | | ... | | | ... | |
| 127 | 511 | | reserved | | | | RW |
| | | [15:0] | reserved | | | Reserved | |

NOTE: applicable to Production silicon only and is not backward compatible with “ES1” silicon

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PACKAGE INFORMATION

Pin Description

Refer to Electrical Specifications on page 4 for power supplies and references. The CMOS I/O follow the JEDEC Standard (JEDEC–JESD8C–01).

Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|--------------|--------|-----------|--|
| A01 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| A02 | mbs2_out | Analog | Out | For test purposes only. Do not connect |
| A03 | adc_dout1 | CMOS | Out | For test purposes only. Do not connect |
| A04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| A05 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| A06 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A07 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A08 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A09 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A10 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A11 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A12 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A13 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A14 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A15 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A16 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A17 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A18 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A19 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A20 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A21 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A22 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A23 | vdda_33 | Supply | | Analog supply - 3.3 V domain |
| A24 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| A25 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| B01 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| B02 | ibias_master | Analog | In/Out | Bias reference - Connect with 47 kΩ to ibias_out |
| B03 | adc_dout2 | CMOS | Out | For test purposes only. Do not connect |
| B04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| B05 | doutn30 | LVDS | Out | LVDS data out negative - Channel 30 |
| B06 | doutp28 | LVDS | Out | LVDS data out positive - Channel 28 |
| B07 | doutn27 | LVDS | Out | LVDS data out negative - Channel 27 |
| B08 | doutn25 | LVDS | Out | LVDS data out negative - Channel 25 |
| B09 | doutn23 | LVDS | Out | LVDS data out negative - Channel 23 |
| B10 | doutn21 | LVDS | Out | LVDS data out negative - Channel 21 |
| B11 | doutn19 | LVDS | Out | LVDS data out negative - Channel 19 |
| B12 | doutp17 | LVDS | Out | LVDS data out positive - Channel 17 |
| B13 | doutn16 | LVDS | Out | LVDS data out negative - Channel 16 |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|--|
| B14 | doutn14 | LVDS | Out | LVDS data out negative - Channel 14 |
| B15 | doutp12 | LVDS | Out | LVDS data out positive - Channel 12 |
| B16 | doutp10 | LVDS | Out | LVDS data out positive - Channel 10 |
| B17 | doutp8 | LVDS | Out | LVDS data out positive - Channel 8 |
| B18 | doutp6 | LVDS | Out | LVDS data out positive - Channel 6 |
| B19 | doutp4 | LVDS | Out | LVDS data out positive - Channel 4 |
| B20 | doutn3 | LVDS | Out | LVDS data out negative - Channel 3 |
| B21 | doutp1 | LVDS | Out | LVDS data out positive - Channel 1 |
| B22 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| B23 | clock_inp | LVDS | In | LVDS clock in positive |
| B24 | clock_inn | LVDS | In | LVDS clock in negative |
| B25 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| C01 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| C02 | ibias_out | Analog | In/Out | Bias ground reference – Connect with 47 kΩ to ibias_master |
| C03 | adc_dout9 | CMOS | Out | For test purposes only. Do not connect |
| C04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| C05 | doutp30 | LVDS | Out | LVDS data out positive - Channel 30 |
| C06 | doutn28 | LVDS | Out | LVDS data out negative - Channel 28 |
| C07 | doutp27 | LVDS | Out | LVDS data out positive - Channel 27 |
| C08 | doutp25 | LVDS | Out | LVDS data out positive - Channel 25 |
| C09 | doutp23 | LVDS | Out | LVDS data out positive - Channel 23 |
| C10 | doutp21 | LVDS | Out | LVDS data out positive - Channel 21 |
| C11 | doutp19 | LVDS | Out | LVDS data out positive - Channel 19 |
| C12 | doutn17 | LVDS | Out | LVDS data out negative - Channel 17 |
| C13 | doutp16 | LVDS | Out | LVDS data out positive - Channel 16 |
| C14 | doutp14 | LVDS | Out | LVDS data out positive - Channel 14 |
| C15 | doutn12 | LVDS | Out | LVDS data out negative - Channel 12 |
| C16 | doutn10 | LVDS | Out | LVDS data out negative - Channel 10 |
| C17 | doutn8 | LVDS | Out | LVDS data out negative - Channel 8 |
| C18 | doutn6 | LVDS | Out | LVDS data out negative - Channel 6 |
| C19 | doutn4 | LVDS | Out | LVDS data out negative - Channel 4 |
| C20 | doutp3 | LVDS | Out | LVDS data out positive - Channel 3 |
| C21 | doutn1 | LVDS | Out | LVDS data out negative - Channel 1 |
| C22 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| C23 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| C24 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| C25 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| D01 | mbs1_out | Analog | Out | For test purposes only. Do not connect |
| D02 | adc_dout5 | CMOS | Out | For test purposes only. Do not connect |
| D03 | adc_dout10 | CMOS | Out | For test purposes only. Do not connect |
| D04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|---|
| D05 | clock_outp | LVDS | Out | LVDS clock out positive |
| D06 | doutn31 | LVDS | Out | LVDS data out negative - Channel 31 |
| D07 | doutn29 | LVDS | Out | LVDS data out negative - Channel 29 |
| D08 | doutn26 | LVDS | Out | LVDS data out negative - Channel 26 |
| D09 | doutn24 | LVDS | Out | LVDS data out negative - Channel 24 |
| D10 | doutn22 | LVDS | Out | LVDS data out negative - Channel 22 |
| D11 | doutn20 | LVDS | Out | LVDS data out negative - Channel 20 |
| D12 | doutn18 | LVDS | Out | LVDS data out negative - Channel 18 |
| D13 | doutp15 | LVDS | Out | LVDS data out positive - Channel 15 |
| D14 | doutp13 | LVDS | Out | LVDS data out positive - Channel 13 |
| D15 | doutp11 | LVDS | Out | LVDS data out positive - Channel 11 |
| D16 | doutp9 | LVDS | Out | LVDS data out positive - Channel 9 |
| D17 | doutp7 | LVDS | Out | LVDS data out positive - Channel 7 |
| D18 | doutp5 | LVDS | Out | LVDS data out positive - Channel 5 |
| D19 | doutp2 | LVDS | Out | LVDS data out positive - Channel 2 |
| D20 | doutp0 | LVDS | Out | LVDS data out positive - Channel 0 |
| D21 | syncp | LVDS | Out | LVDS sync positive |
| D22 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| D23 | miso | CMOS | Out | SPI master in -slave out |
| D24 | mosi | CMOS | In | SPI master out - slave in |
| D25 | ss_n | CMOS | In | SPI slave select (active low) |
| E01 | adc_dout0 | CMOS | Out | For test purposes only. Do not connect |
| E02 | adc_dout4 | CMOS | Out | For test purposes only. Do not connect |
| E03 | srd2_n | Analog | | Not connected |
| E04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| E05 | clock_outn | LVDS | Out | LVDS clock out negative |
| E06 | doutp31 | LVDS | Out | LVDS data out positive - Channel 31 |
| E07 | doutp29 | LVDS | Out | LVDS data out positive - Channel 29 |
| E08 | doutp26 | LVDS | Out | LVDS data out positive - Channel 26 |
| E09 | doutp24 | LVDS | Out | LVDS data out positive - Channel 24 |
| E10 | doutp22 | LVDS | Out | LVDS data out positive - Channel 22 |
| E11 | doutp20 | LVDS | Out | LVDS data out positive - Channel 20 |
| E12 | doutp18 | LVDS | Out | LVDS data out positive - Channel 18 |
| E13 | doutn15 | LVDS | Out | LVDS data out negative - Channel 15 |
| E14 | doutn13 | LVDS | Out | LVDS data out negative - Channel 13 |
| E15 | doutn11 | LVDS | Out | LVDS data out negative - Channel 11 |
| E16 | doutn9 | LVDS | Out | LVDS data out negative - Channel 9 |
| E17 | doutn7 | LVDS | Out | LVDS data out negative - Channel 7 |
| E18 | doutn5 | LVDS | Out | LVDS data out negative - Channel 5 |
| E19 | doutn2 | LVDS | Out | LVDS data out negative - Channel 2 |
| E20 | doutn0 | LVDS | Out | LVDS data out negative - Channel 0 |
| E21 | syncn | LVDS | Out | LVDS sync negative |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|--|
| E22 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| E23 | trigger | CMOS | In | Trigger |
| E24 | sck | CMOS | In | SPI clock |
| E25 | reset_n | CMOS | In | Active low system reset |
| F01 | adc_dout3 | CMOS | Out | For test purposes only. Do not connect |
| F02 | adc_dout6 | CMOS | Out | For test purposes only. Do not connect |
| F03 | srd2_ngoard | Analog | | Not connected |
| F04 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F05 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F06 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F07 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F08 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F09 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F10 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F11 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F12 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F13 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F14 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F15 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F16 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F17 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F18 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F19 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F20 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F21 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F22 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| F23 | scan_in2 | CMOS | In | Scan chain input #2 - Connect to ground |
| F24 | scan_in1 | CMOS | In | Scan chain input #1 - Connect to ground |
| F25 | mux_mode | CMOS | In | Multiplexing mode selection. Connect to gndd_33 ('0') for 32 data channels, connect to vddd_33 ('1') for 16 data channels. |
| G01 | adc_dout8 | CMOS | Out | For test purposes only. Do not connect |
| G02 | adc_dout7 | CMOS | Out | For test purposes only. Do not connect |
| G03 | afe_clk | CMOS | Out | For test purposes only. Do not connect |
| G04 | srd1_ngoard | Analog | | Not connected |
| G05 | srd1_n | Analog | | Not connected |
| G06 | td_anode | Analog | In/Out | Temperature diode - Anode |
| G07 | td_cathode | Analog | In/Out | Temperature diode - Cathode |
| G08 | mbs3_in | Analog | In | Analog test input - Connect to ground |
| G09 | mbs4_in | Analog | In | Analog test input - Connect to ground |
| G10 | spare_ana | Analog | Out | For test purposes only. Do not connect |
| G11 | spare_ana | Analog | Out | For test purposes only. Do not connect |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------------|--------|-----------|--|
| G12 | spare_dig_in | CMOS | In | Digital test input - Connect to ground |
| G13 | spare_dig_in | CMOS | In | Digital test input - Connect to ground |
| G14 | spare_dig_in | CMOS | In | Digital test input - Connect to ground |
| G15 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G16 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G17 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G18 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G19 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G20 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G21 | gnd_colbias | Ground | | Column biasing ground - Connect to ground |
| G22 | scan_clk | CMOS | In | Scan chain clock - Connect to ground |
| G23 | monitor2 | CMOS | Out | Monitor output #2 |
| G24 | monitor1 | CMOS | Out | Monitor output #1 |
| G25 | monitor0 | CMOS | Out | Monitor output #0 |
| H21 | test_enable | CMOS | In | Test enable - Connect to ground |
| H22 | adc_mode | CMOS | In | ADC mode selection Connect to Gndd_33 ('0') for 10-bit mode operation, Connect to vddd_33 ('1') for 8-bit mode operation |
| H23 | spare_dig_out | CMOS | | Not connected |
| H24 | spare_dig_out | CMOS | | Not connected |
| H25 | spare_dig_out | CMOS | | Not connected |
| J01 | spare_vref6t_hv | Analog | | Not connected |
| J02 | spare_vref6t_hv | Analog | | Not connected |
| J03 | spare_vref6t_hv | Analog | | Not connected |
| J04 | spare_vref6t_hv | Analog | | Not connected |
| J05 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J06 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J07 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J08 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J09 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J10 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J11 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J12 | gndd_33 | Ground | | Digital ground - 3.3 V domain |
| J13 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J14 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J15 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J16 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J17 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J18 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J19 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J20 | gndd_18 | Ground | | Digital ground - 1.8 V domain |
| J21 | gndd_18 | Ground | | Digital ground - 1.8 V domain |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|--------------|--------|-----------|---|
| J22 | gnd_trans | Ground | | Pixel transfer ground - Connect to ground |
| J23 | gnd_respd | Supply | | Photo diode reset ground - sinking supply |
| J24 | gnd_resfd | Ground | | Floating diffusion reset ground - Connect to ground |
| J25 | gnd_resfd | Ground | | Floating diffusion reset ground - Connect to ground |
| K01 | spare_vref6t | Analog | | Not connected |
| K02 | spare_vref6t | Analog | | Not connected |
| K03 | spare_vref6t | Analog | | Not connected |
| K04 | spare_vref6t | Analog | | Not connected |
| K05 | spare_vref6t | Analog | | Not connected |
| K06 | spare_vref6t | Analog | | Not connected |
| K07 | spare_vref6t | Analog | | Not connected |
| K08 | spare_vref6t | Analog | | Not connected |
| K9 | vdd_pix | Supply | | Pixel array supply |
| K10 | vdd_pix | Supply | | Pixel array supply |
| K11 | vdd_pix | Supply | | Pixel array supply |
| K12 | vdd_pix | Supply | | Pixel array supply |
| K13 | vdd_pix | Supply | | Pixel array supply |
| K14 | vdd_pix | Supply | | Pixel array supply |
| K15 | vdd_pix | Supply | | Pixel array supply |
| K16 | vdd_pix | Supply | | Pixel array supply |
| K17 | gnd_sel | Ground | | Pixel select ground - Connect to ground |
| K18 | gnd_sel | Ground | | Pixel select ground - Connect to ground |
| K19 | gnd_sel | Ground | | Pixel select ground - Connect to ground |
| K20 | gnd_sel | Ground | | Pixel select ground - Connect to ground |
| K21 | vdd_trans | Supply | | Pixel transfer supply |
| K22 | gnd_trans | Ground | | Pixel transfer ground - Connect to ground |
| K23 | gnd_respd | Supply | | Photo diode reset ground - sinking supply |
| K24 | gnd_resfd | Ground | | Floating diffusion reset ground - Connect to ground |
| K25 | gnd_resfd | Ground | | Floating diffusion reset ground - Connect to ground |
| L01 | vref_colmux | Supply | | Column multiplexer reference supply |
| L02 | vdd_pix | Supply | | Pixel array supply |
| L03 | vdd_pix | Supply | | Pixel array supply |
| L04 | vdd_pix | Supply | | Pixel array supply |
| L05 | vdd_pix | Supply | | Pixel array supply |
| L06 | vdd_pix | Supply | | Pixel array supply |
| L07 | vdd_pix | Supply | | Pixel array supply |
| L08 | vdd_pix | Supply | | Pixel array supply |
| L09 | vdd_pix | Supply | | Pixel array supply |
| L10 | vdd_pix | Supply | | Pixel array supply |
| L11 | vdd_pix | Supply | | Pixel array supply |
| L12 | vdd_pix | Supply | | Pixel array supply |
| L13 | vdd_pix | Supply | | Pixel array supply |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|---|
| L14 | vdd_pix | Supply | | Pixel array supply |
| L15 | vdd_pix | Supply | | Pixel array supply |
| L16 | vdd_pix | Supply | | Pixel array supply |
| L17 | vdd_casc | Supply | | Cascode supply |
| L18 | vdd_casc | Supply | | Cascode supply |
| L19 | vdd_sel | Supply | | Pixel select supply |
| L20 | vdd_sel | Supply | | Pixel select supply |
| L21 | vdd_trans | Supply | | Pixel transfer supply |
| L22 | gnd_trans | Ground | | Pixel transfer ground - Connect to ground |
| L23 | gnd_respd | Supply | | Photo diode reset ground - sinking supply |
| L24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| L25 | vref_colmux | Supply | | Column multiplexer reference supply |
| M01 | vref_colmux | Supply | | Column multiplexer reference supply |
| M02 | vdd_pix | Supply | | Pixel array supply |
| M03 | vdd_pix | Supply | | Pixel array supply |
| M04 | vdd_pix | Supply | | Pixel array supply |
| M05 | vdd_pix | Supply | | Pixel array supply |
| M06 | vdd_pix | Supply | | Pixel array supply |
| M07 | vdd_pix | Supply | | Pixel array supply |
| M08 | vdd_pix | Supply | | Pixel array supply |
| M09 | vdd_pix | Supply | | Pixel array supply |
| M10 | vdd_pix | Supply | | Pixel array supply |
| M11 | vdd_pix | Supply | | Pixel array supply |
| M12 | vdd_pix | Supply | | Pixel array supply |
| M13 | vdd_pix | Supply | | Pixel array supply |
| M14 | vdd_pix | Supply | | Pixel array supply |
| M15 | vdd_pix | Supply | | Pixel array supply |
| M16 | vdd_pix | Supply | | Pixel array supply |
| M17 | vdd_casc | Supply | | Cascode supply |
| M18 | vdd_casc | Supply | | Cascode supply |
| M19 | vdd_sel | Supply | | Pixel select supply |
| M20 | vdd_sel | Supply | | Pixel select supply |
| M21 | vdd_trans | Supply | | Pixel transfer supply |
| M22 | gnd_trans | Ground | | Pixel transfer ground - Connect to ground |
| M23 | gnd_respd | Supply | | Photo diode reset ground - sinking supply |
| M24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| M25 | vref_colmux | Supply | | Column multiplexer reference supply |
| N01 | vddd_33 | Supply | | Digital supply - 3.3-V domain |
| N02 | vdd_pix | Supply | | Pixel array supply |
| N03 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N04 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N05 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------|--------|-----------|---|
| N06 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N07 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N08 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N09 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N10 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N11 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N12 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N13 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N14 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N15 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N16 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N17 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N18 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N19 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N20 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| N21 | vdd_trans | Supply | | Pixel transfer supply |
| N22 | vdd_respd | Supply | | Photo diode reset supply |
| N23 | vdd_respd | Supply | | Photo diode reset supply |
| N24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| N25 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| P01 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| P02 | vdd_pix | Supply | | Pixel array supply |
| P03 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P04 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P05 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P06 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P07 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P08 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P09 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P10 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P11 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P12 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P13 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P14 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P15 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P16 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P17 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P18 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P19 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P20 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P21 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| P22 | vdd_respd | Supply | | Photo diode reset supply |

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Table 39. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------|--------|-----------|---|
| P23 | vdd_respd | Supply | | Photo diode reset supply |
| P24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| P25 | vddd_33 | Supply | | Digital supply - 3.3 V domain |
| R01 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| R02 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| R03 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| R04 | gnd_colpc | Ground | | Column precharge ground - Connect to ground |
| R05 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R06 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R07 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R08 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R09 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R10 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R11 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R12 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R13 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R14 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R15 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R16 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R17 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R18 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R19 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R20 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R21 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R22 | gnda_33 | Ground | | Analog ground - 3.3 V domain |
| R23 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| R24 | vddd_18 | Supply | | Digital supply - 1.8 V domain |
| R25 | vddd_18 | Supply | | Digital supply - 1.8 V domain |

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Mechanical Specifications

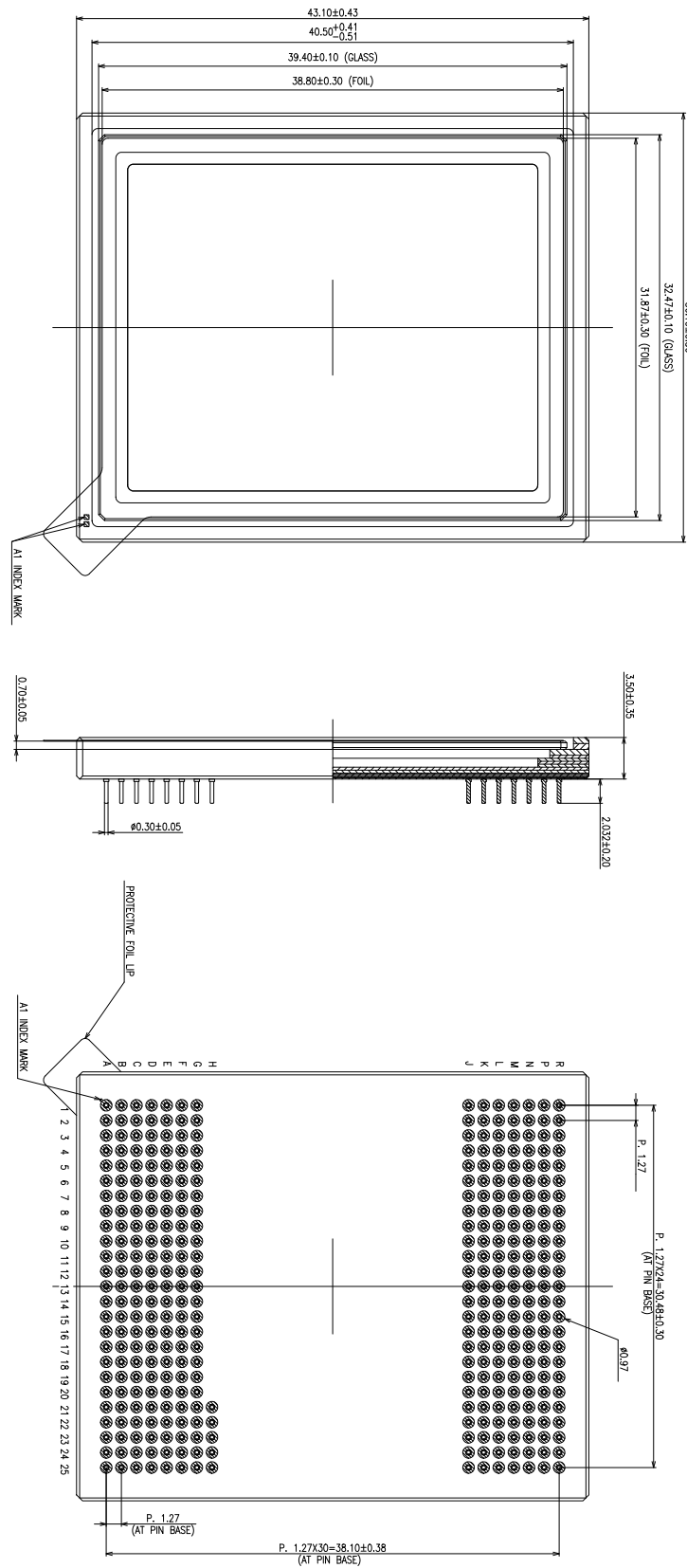
Table 40. MECHANICAL SPECIFICATIONS

| Parameter | Description | Min | Typ | Max | Units |
|--|--|-----------------------------|--------------|------|-----------------|
| Die (Refer to Figure 42 with Pin A1 bottom right) | Die thickness | | 725 | | μm |
| | Die size | | 25.5 x 32.5 | | mm ² |
| | Die center, X offset to the center of package | -50 | 0 | 50 | μm |
| | Die center, Y offset to the center of the package | -50 | 0 | 50 | μm |
| | Die position, tilt to the die attach pad plane | | 0 | | deg |
| | Die rotation accuracy between die scribe and lead fingers of package on all four sides | | 0 | | deg |
| | Optical center referenced from the package center with Pin1 located bottom right (X-dir) | | 0 | | μm |
| | Optical center referenced from the package center with Pin1 located bottom right (Y-dir) | | 3602 | | μm |
| | Distance from bottom of the package to top of the die surface | | 1.75 | | mm |
| | Distance from top of the die surface to top of the glass lid | | 1.45 | | mm |
| Glass Lid Specification | XY size | | 32.47 x 39.4 | | mm ² |
| | Thickness | | 0.7 | | mm |
| | Spectral range for glass window | 400 | | 1000 | nm |
| | Transmission of the Glass lid (refer to Figure 44) | | | 92 | % |
| Glass Lid Material | D263 Teco (no coatings on glass) | | | | |
| Mechanical Shock | JESD22-B104C; Condition G | | | 2000 | g |
| Vibration | JESD22-B103B; Condition 1 | | | 2000 | Hz |
| Mounting Profile | Pb-free wave soldering profile for pin grid array package | | | | |
| Recommended Socket | Andon Electronics Corporation (www.andonelectronics.com) | 10-31-13A-355-400T4-R27-L14 | | | |

NOTE: Optical center min/max tolerance is calculated on X/Y package tolerances with Pin 1 as a reference.

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Package Drawing



All dimensions are in mm, unless specified otherwise.

Figure 41. Package Diagram

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Optical Center Information

The center of the die (CD) is the center of the cavity

The center of the die (CD) is exactly at 50% between the outsides of the two outer seal rings

The center of the cavity is exactly at 50% between the insides of the finger pads.

- Die outer dimensions:
 - ◆ B4 is the reference for the Die (0,0) in μm
 - ◆ B1 is at (0,32500) μm
 - ◆ B2 is at (25500,32500) μm
 - ◆ B3 is at (25500,0) μm
- Active Area outer dimensions (VITA 16K)
 - ◆ A1 is at (2960, 29084) μm
 - ◆ A2 is at (22540, 29084) μm
 - ◆ A3 is at (22540, 10620) μm
 - ◆ A4 is at (2960, 10620) μm
- Active Area outer dimensions (VITA 12K)
 - ◆ A1* is at (2960, 26780) μm
 - ◆ A2* is at (22540, 26780) μm
 - ◆ A3* is at (22540, 12924) μm
 - ◆ A4* is at (2960, 12924) μm
- Center of the Active Area
 - ◆ AA is at (12750, 19852) μm
- Center of the Die
 - ◆ CD is at (12750, 16250) μm

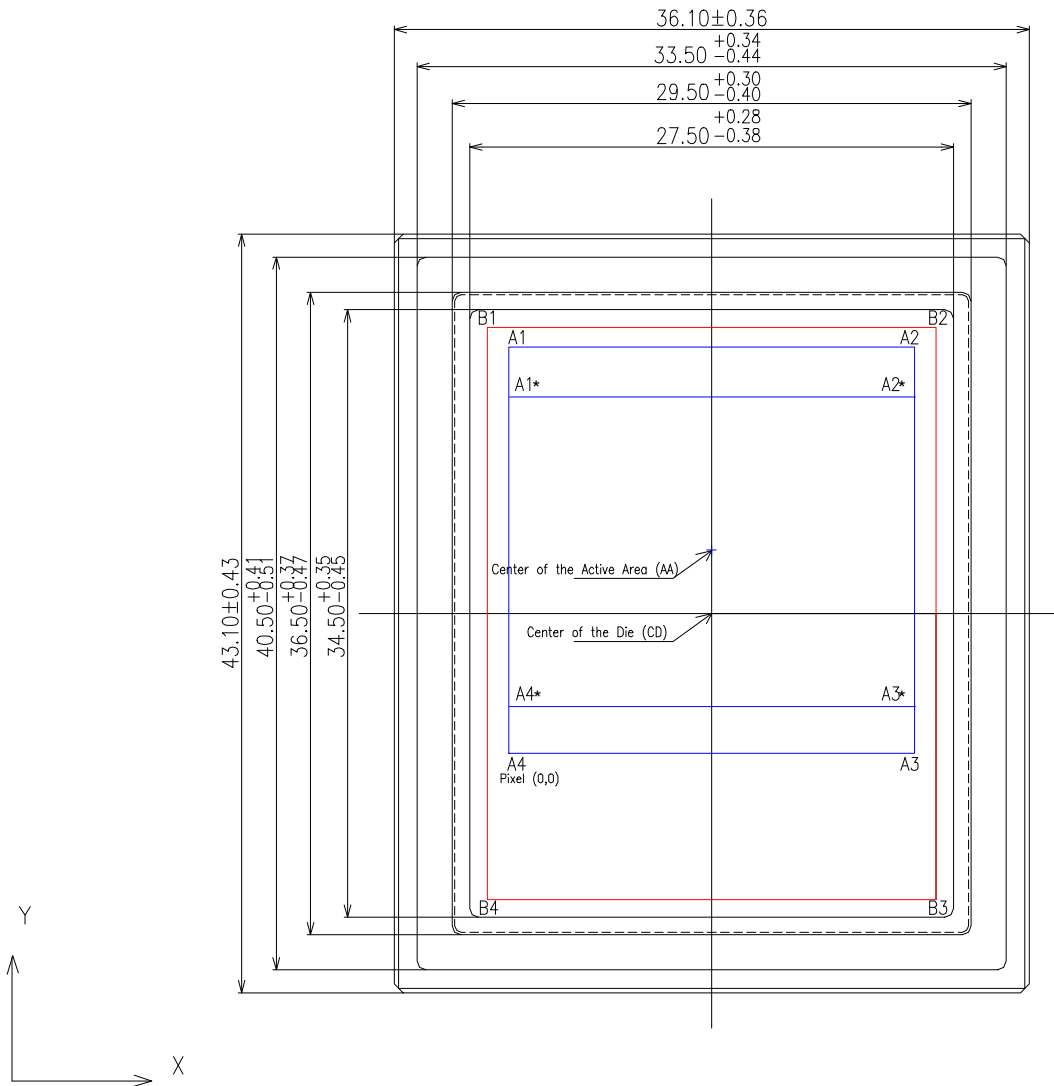


Figure 42. Graphical Representation of the Optical Center

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Glass Lid

The VITA image sensor uses a glass lid without any coating. Figure 43 shows the transmission characteristics of the glass lid.

As seen in Figure 43, the sensor does not have an infrared attenuating filter glass. A filter must be provided in the optical path when color devices are used (source: <http://www.pgo-online.com>).

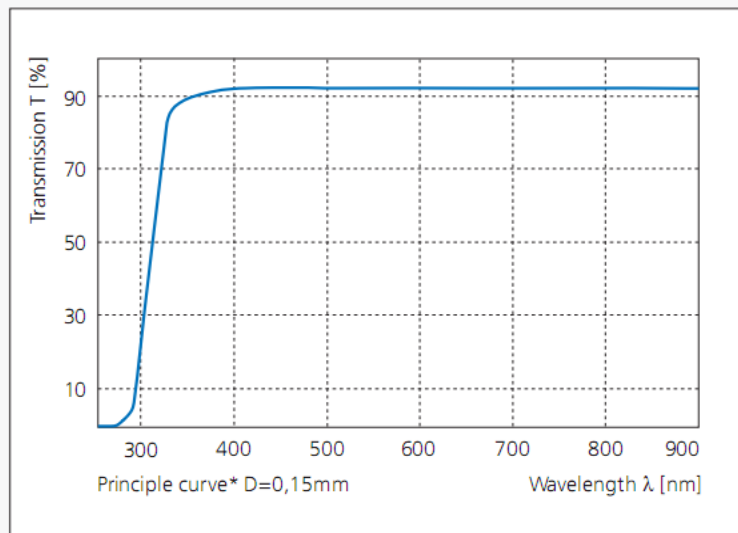


Figure 43. Transmission Characteristics of Glass Lid

SPECIFICATIONS AND USEFUL REFERENCES

Specifications, Application Notes and useful resources can be accessible via customer login account at MyON - CISP Extranet.

<https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do>

Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](#) from www.onsemi.com.

Application Note and References

- AND9049 VITA Family Global Reset
- AN66426 FPN and PRNU Correction for the VITA family
- AN65466 VITA 25K HSMC Cyclone Reference Board
- VITA 25K Delivery Specification
- VITA 25K Layout DSN drawing
- VITA 25K 3D package STP file for CAD
- AN5606 Zero ROT Application Note
- AND9123 VITA 25K Temperature Curves

Acceptance Criteria Specification

The Product Acceptance Criteria is available on request. This document contains the criteria to which the VITA xK is tested prior to being shipped.

Return Material Authorization (RMA)

Refer to the ON Semiconductor RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

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ACRONYMS

| Acronym | Description |
|---------|---|
| ADC | Analog-to-Digital Converter |
| AFE | Analog Front End |
| BL | Black pixel data |
| CDM | Charged Device Model |
| CDS | Correlated Double Sampling |
| CMOS | Complementary Metal Oxide Semiconductor |
| CRC | Cyclic Redundancy Check |
| DAC | Digital-to-Analog Converter |
| DDR | Double Data Rate |
| DNL | Differential Non-Linearity |
| DS | Double Sampling |
| EIA | Electronic Industries Alliance |
| ESD | Electrostatic Discharge |
| FE | Frame End |
| FOT | Frame Overhead Time |
| FPGA | Field Programmable Gate Array |
| FPN | Fixed Pattern Noise |
| FPS | Frames per Second |
| FS | Frame Start |
| HBM | Human Body Model |
| IMG | Image data (regular pixel data) |
| INL | Integral Non-Linearity |
| IP | Intellectual Property |


| Acronym | Description |
|----------------|---|
| LE | Line End |
| LS | Line Start |
| LSB | least significant bit |
| LVDS | Low-Voltage Differential Signaling |
| MSB | most significant bit |
| PGA | Programmable Gain Amplifier |
| PLS | Parasitic Light Sensitivity |
| PRBS | Pseudo-Random Binary Sequence |
| PRNU | Photo Response Non-Uniformity |
| QE | Quantum Efficiency |
| RGB | Red-Green-Blue |
| RMA | Return Material Authorization |
| RMS | Root Mean Square |
| ROI | Region of Interest |
| ROT | Row Overhead Time |
| S/H | Sample and Hold |
| SNR | Signal-to-Noise Ratio |
| SPI | Serial Peripheral Interface |
| TIA | Telecommunications Industry Association |
| T _J | Junction temperature |
| TR | Training pattern |
| % RH | Percent Relative Humidity |

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GLOSSARY

| | |
|-------------------|---|
| conversion gain | A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron ($1.602E-19$ Coulomb) and C is the capacitance of the photodiode or sense node. |
| CDS | Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light. |
| CFA | Color filter array. The materials deposited on top of pixels that selectively transmit color. |
| DNL | Differential non-linearity (for ADCs) |
| DSNU | Dark signal non-uniformity. This parameter characterizes the degree of non-uniformity in dark leakage currents, which can be a major source of fixed pattern noise. |
| fill-factor | A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured. |
| INL | Integral nonlinearity (for ADCs) |
| IR | Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm. |
| Lux | Photometric unit of luminance (at 550 nm, $1\text{lux} = 1 \text{lumen/m}^2 = 1/683 \text{ W/m}^2$) |
| pixel noise | Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane. |
| photometric units | Units for light measurement that take into account human physiology. |
| PLS | Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes. |
| PRNU | Photo-response non-uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination. |
| QE | Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent. |
| read noise | Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal. |
| reset | The process by which a pixel photodiode or sense node is cleared of electrons. "Soft" reset occurs when the reset transistor is operated below the threshold. "Hard" reset occurs when the reset transistor is operated above threshold. |
| reset noise | Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS. |
| responsivity | The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| ROI | Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane. |
| sense node | In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself. |
| sensitivity | A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically $V/(W/m^2)/\text{sec}$ and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2 ; the units of sensitivity are quoted in $V/\text{lux}/\text{sec}$. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| spectral response | The photon wavelength dependence of sensitivity or responsivity. |
| SNR | Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency. |
| temporal noise | Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels. |

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