

74LVCV2G66

Overvoltage tolerant bilateral switch

Rev. 8 — 5 November 2018

Product data sheet

1. General description

The 74LVCV2G66 is a low-power, low-voltage, high-speed Si-gate CMOS device.

The 74LVCV2G66 provides two single pole single throw analog or digital switches. Each switch includes an overvoltage tolerant input/output terminal (pin nZ), an output/input terminal (pin nY) and low-power active HIGH enable input (pin nE).

The overvoltage tolerant switch terminals allow the switching of signals in excess of V_{CC} . The low-power enable input eliminates the necessity of using current limiting resistors in portable applications when using control logic signals much lower than V_{CC} . These inputs are also overvoltage tolerant.

2. Features and benefits

- Wide supply voltage range from 2.3 V to 5.5 V
- Ultra low-power operation
- Very low ON resistance:
 - 8.0 Ω (typical) at $V_{CC} = 2.7$ V
 - 7.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 7.3 Ω (typical) at $V_{CC} = 5.0$ V.
- 5 V tolerant input for interfacing with 5 V logic
- High noise immunity
- Switch handling capability of 32 mA
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Incorporates overvoltage tolerant analog switch technology
- Switch accepts voltages up to 5.5 V independent of V_{CC}
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVCV2G66DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVCV2G66GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVCV2G66GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVCV2G66DC	Y66
74LVCV2G66GT	Y66
74LVCV2G66GM	Y66

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

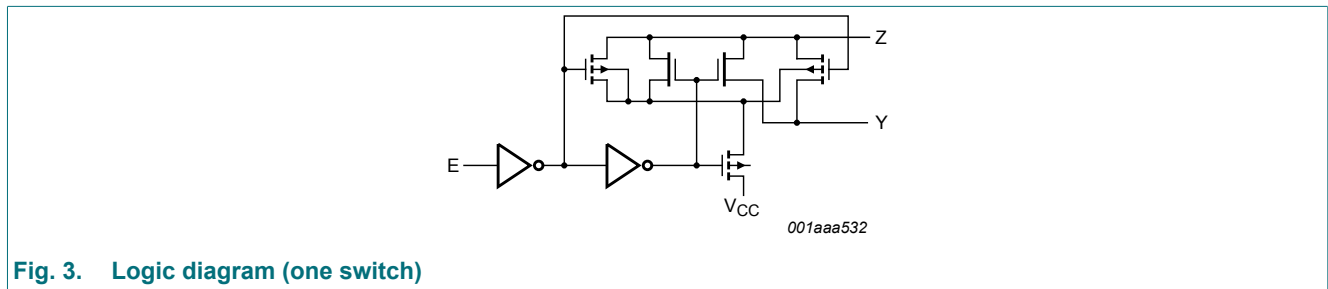
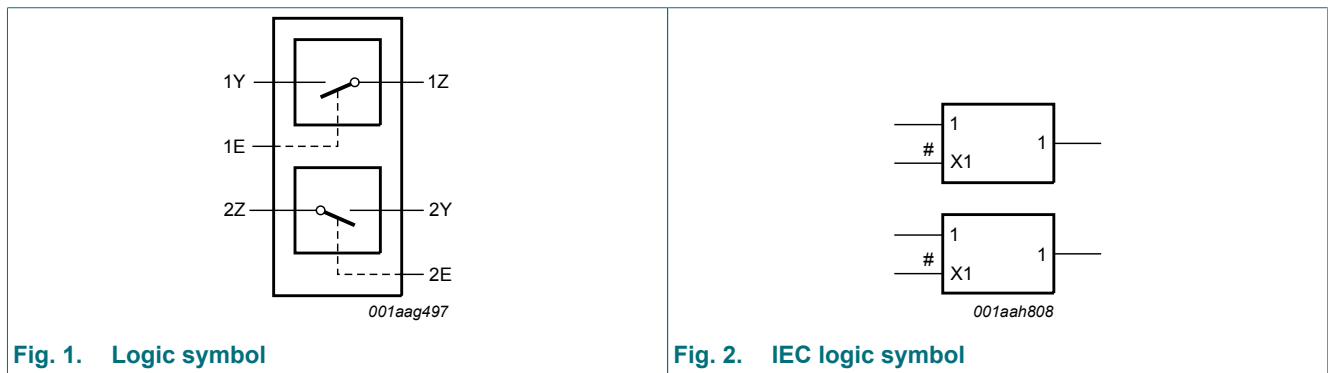
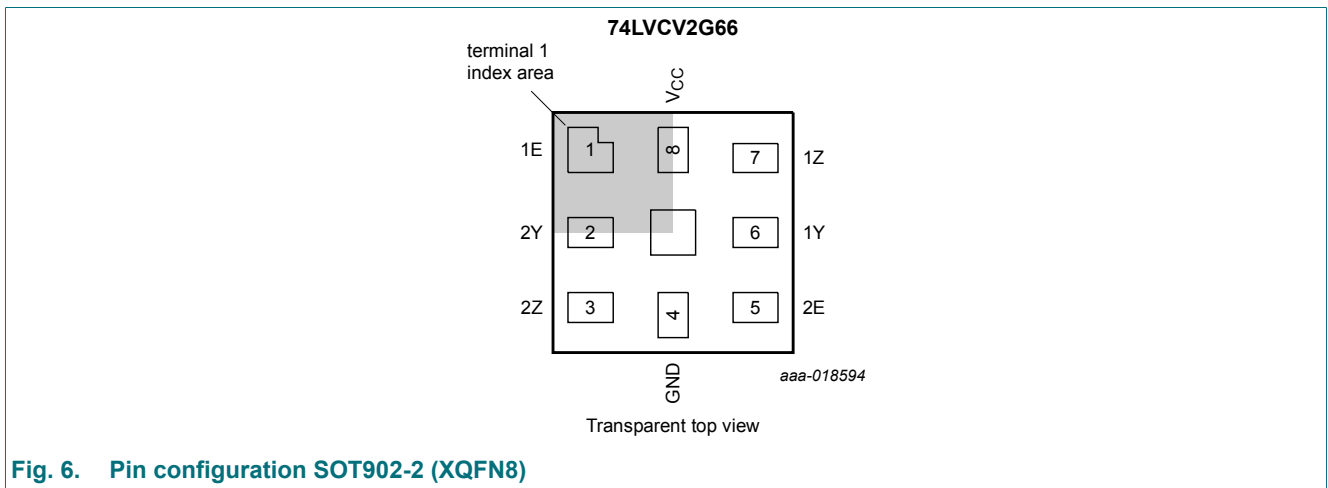
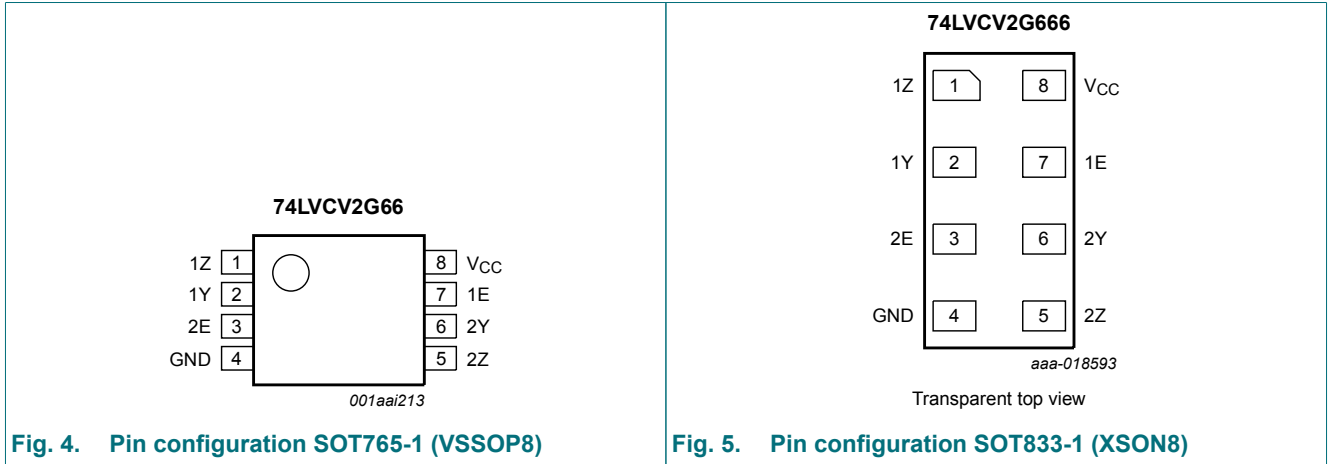


Fig. 3. Logic diagram (one switch)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1 and SOT833-1	SOT902-2	
1Z	1	7	independent input or output (overvoltage tolerant)
1Y	2	6	independent input or output
2E	3	5	enable input (active HIGH)
GND	4	4	ground (0 V)
2Z	5	3	independent input or output (overvoltage tolerant)
2Y	6	2	independent input or output
1E	7	1	enable input (active HIGH)
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
L	OFF-state
H	ON-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > 6.5 \text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5 \text{ V}$ or $V_I > 6.5 \text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode	-0.5	+6.5	V
I_{SW}	switch current	$V_{SW} > -0.5 \text{ V}$ or $V_{SW} < 6.5 \text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 package: above 110 °C, the value of P_{tot} derates linearly with 8 mW/K.

For XSON8 and XQFN8 packages: above 118 °C, the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.3	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode [1]	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3 \text{ V}$ to 2.7 V [2]	-	-	20	ns/V
		$V_{CC} = 2.7 \text{ V}$ to 5.5 V [2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current flows from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

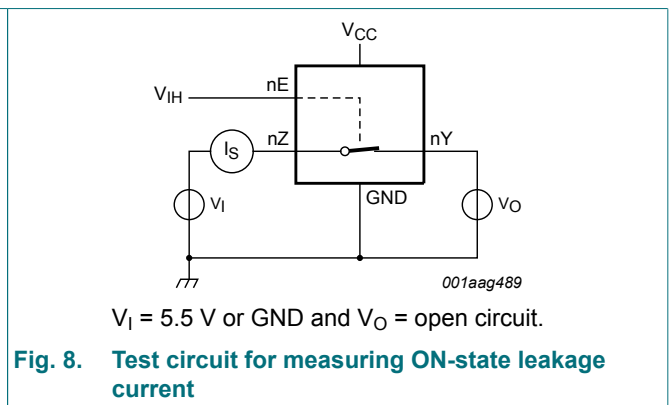
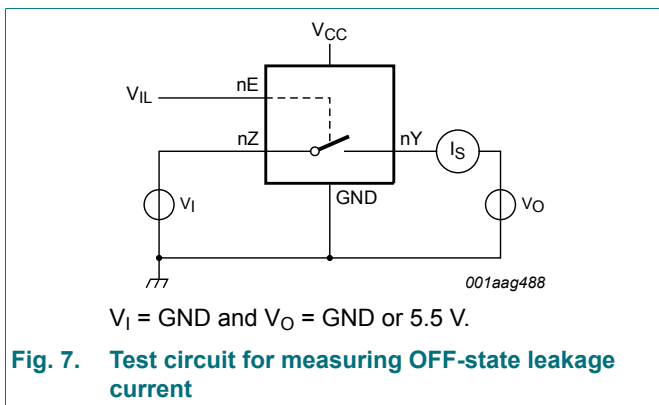
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	0.6V _{CC}	-	-	0.6V _{CC}	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.55V _{CC}	-	-	0.55V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.1V _{CC}	-	0.1V _{CC}	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.5	-	0.5	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.15V _{CC}	-	0.15V _{CC}	V
I _I	input leakage current	pin nE; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 2.3 V to 5.5 V; see Fig. 7	-	±0.1	±0.4	-	±1	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 2.3 V to 5.5 V; see Fig. 8	-	±0.1	±2	-	±4	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 2.3 V to 5.5 V	-	0.1	4	-	4	µA
ΔI _{CC}	additional supply current	pin nE; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.0 V to 5.5 V	-	0.1	5	-	5	µA
C _I	input capacitance		-	2.5	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	8.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	16	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] These typical values are measured at V_{CC} = 3.3 V.
- [3] For overvoltage signals (V_{SW} > V_{CC}), the condition V_V < V_Z must be observed.

10.1. Test circuits



10.2. ON resistance

Table 8. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Fig. 10](#) and [Fig. 11](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_{SW} = GND$ to V_{CC} ; $V_I = V_{IH}$; see Fig. 9						
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	13	30	-	30	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	10	25	-	25	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	8.3	20	-	20	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	7.4	15	-	15	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{SW} = GND$; $V_I = V_{IH}$; see Fig. 9						
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	8.5	20	-	20	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	8.0	18	-	18	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	7.5	15	-	15	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	7.3	10	-	10	Ω
		$V_{SW} = V_{CC}$; $V_I = V_{IH}$						
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	8.5	20	-	20	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	7.2	18	-	18	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	6.5	15	-	15	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	5.7	10	-	10	Ω
$R_{ON(flat)}$	ON resistance (flatness)	$V_{SW} = GND$ to V_{CC} ; $V_I = V_{IH}$ [2]						
		$I_{SW} = 8$ mA; $V_{CC} = 2.5$ V	-	17	-	-	-	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	10	-	-	-	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.3$ V	-	5	-	-	-	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 5.0$ V	-	3	-	-	-	Ω

[1] All typical values are measured at $T_{amb} = 25$ °C and nominal V_{CC} .

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs

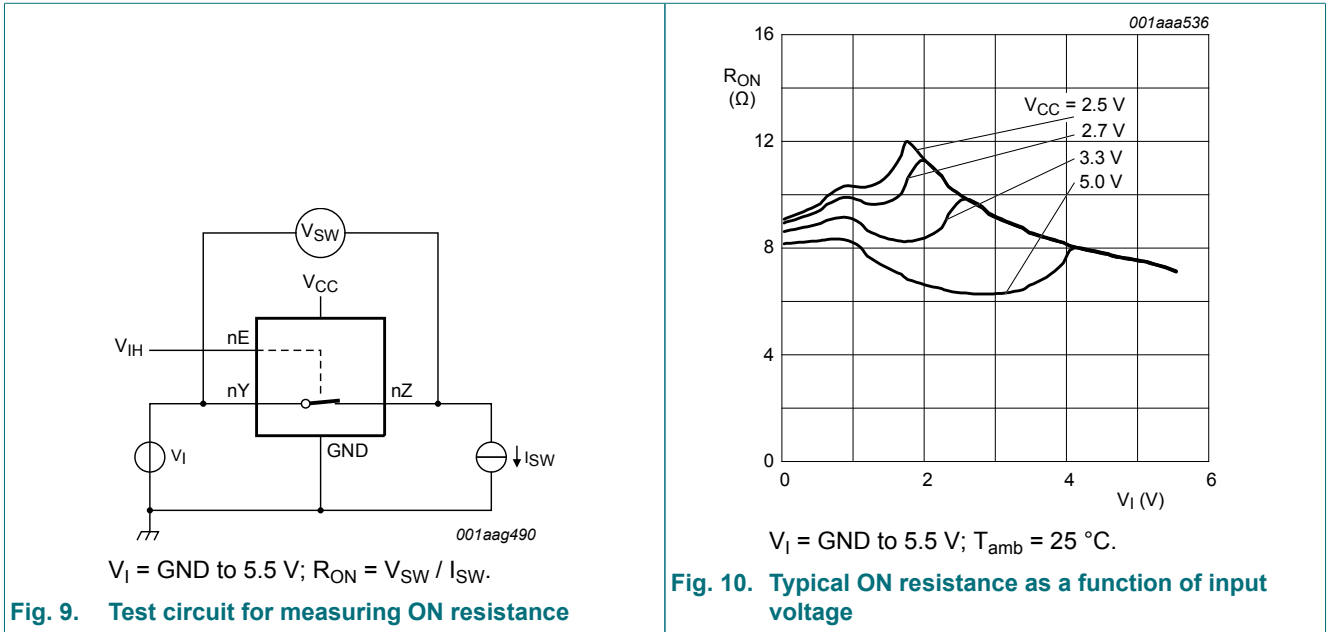
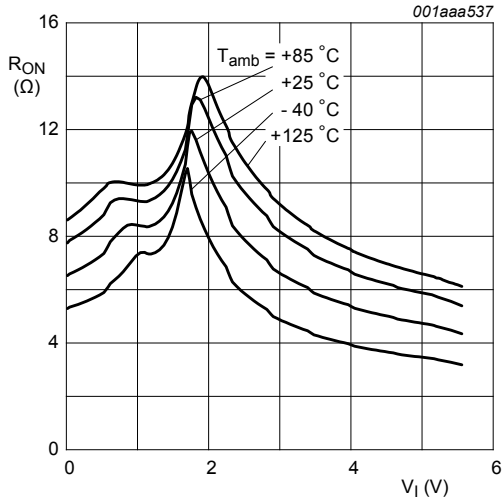
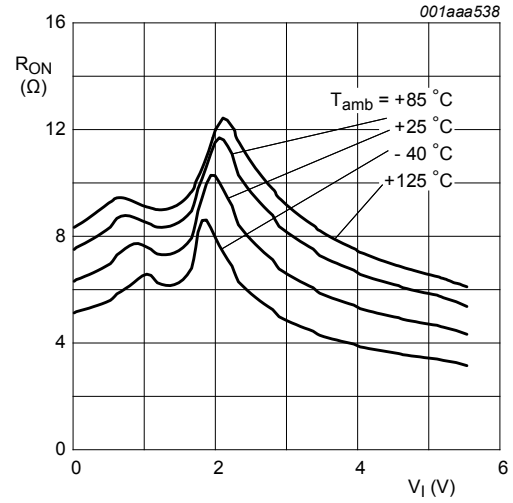


Fig. 9. Test circuit for measuring ON resistance

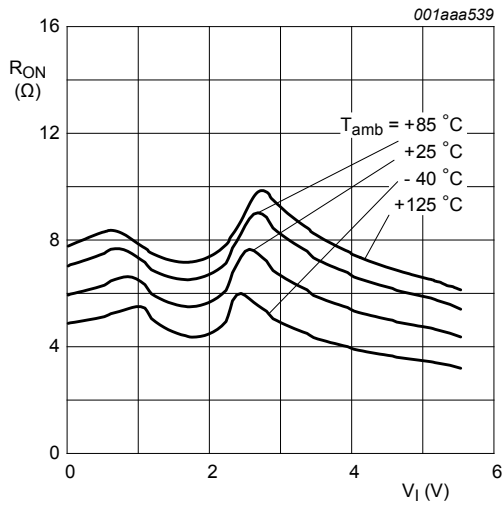
Fig. 10. Typical ON resistance as a function of input voltage



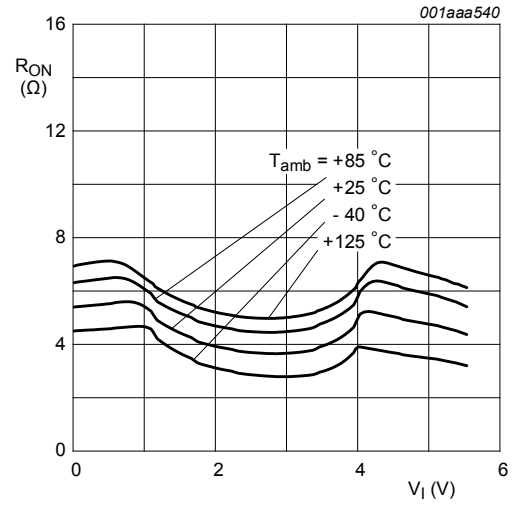
a. $V_{CC} = 2.5 \text{ V}$



b. $V_{CC} = 2.7 \text{ V}$



c. $V_{CC} = 3.3 \text{ V}$



d. $V_{CC} = 5.0 \text{ V}$

Fig. 11. ON resistance as a function of input voltage at various supply voltages

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 14.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nY to nZ or nZ to nY; see Fig. 12 [2][3]						
		V _{CC} = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V _{CC} = 2.7 V	-	0.4	1.0	-	1.5	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V _{CC} = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns
t _{en}	enable time	nE to nY or nZ; see Fig. 13 [4]						
		V _{CC} = 2.3 V to 2.7 V	1.0	4.7	12	1.0	15	ns
		V _{CC} = 2.7 V	1.0	4.4	8.5	1.0	11	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.8	7.5	1.0	9.5	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	2.7	5.0	1.0	6.5	ns
t _{dis}	disable time	nE to nY or nZ; see Fig. 13 [5]						
		V _{CC} = 2.3 V to 2.7 V	1.0	6.0	16	1.0	20	ns
		V _{CC} = 2.7 V	1.0	7.9	15	1.0	19	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	6.5	13.5	1.0	17	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	4.4	9.0	1.0	11.5	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 10 MHz; V _I = GND to 5.5 V[6]						
		V _{CC} = 2.5 V	-	9.7	-	-	-	pF
		V _{CC} = 3.3 V	-	10.3	-	-	-	pF
		V _{CC} = 5.0 V	-	11.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum \{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

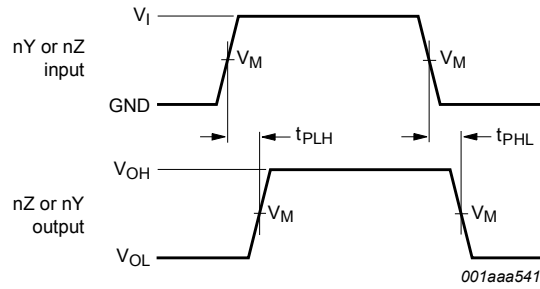
C_{S(ON)} = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

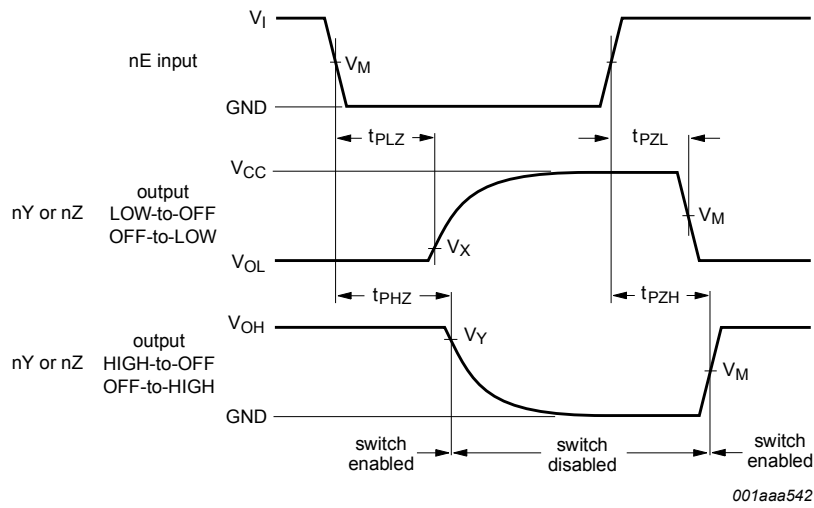
$\sum \{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

11.1. Waveforms and test circuit



Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Input (nY or nZ) to output (nZ or nY) propagation delays

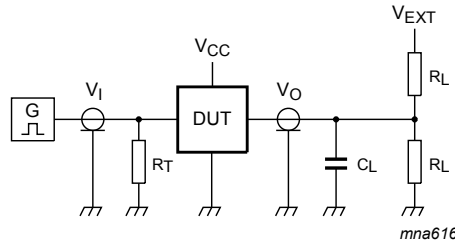


Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 11](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig. 14. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

11.2. Additional dynamic characteristics

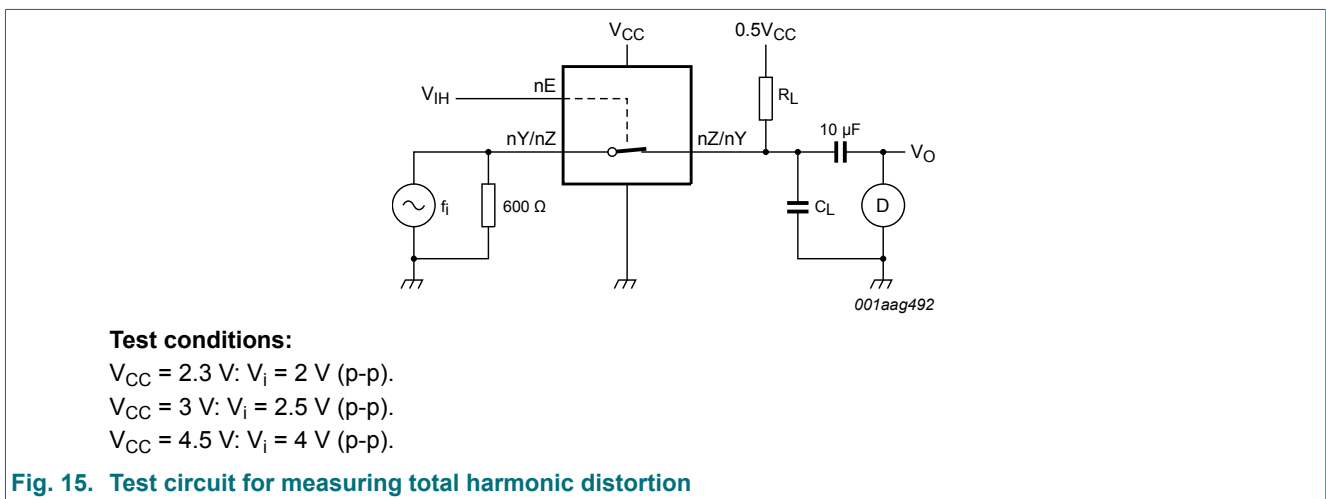
Table 12. Additional dynamic characteristics

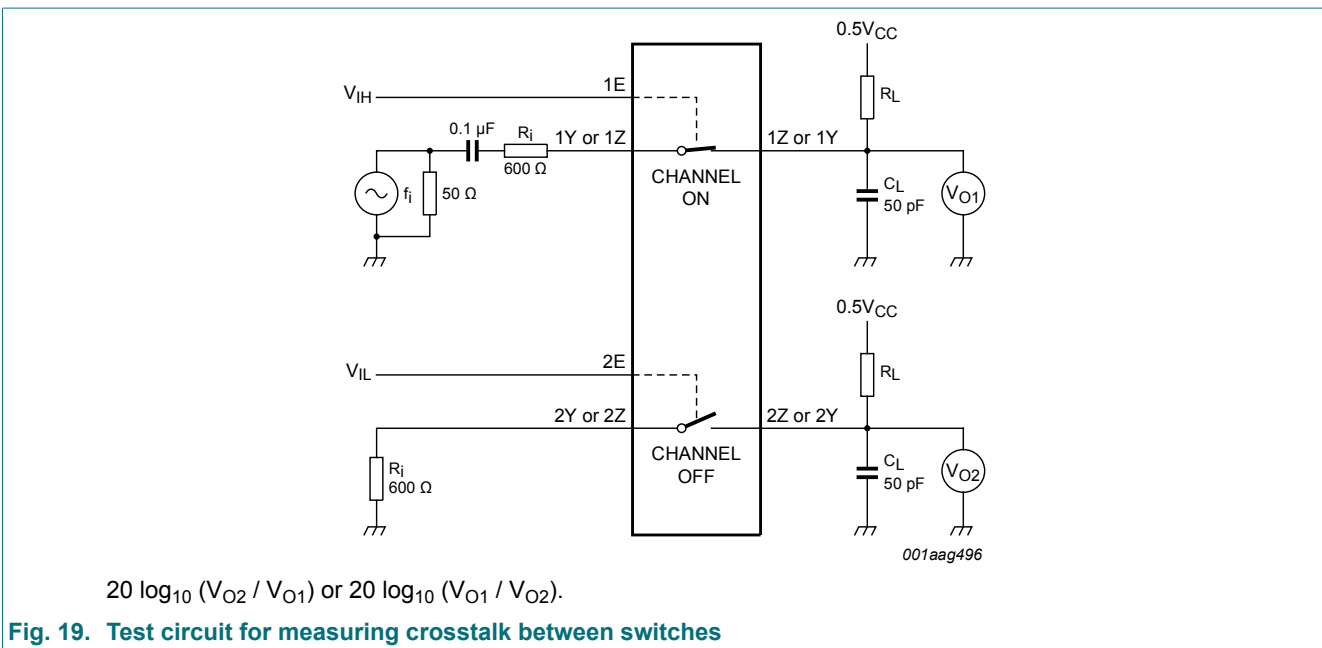
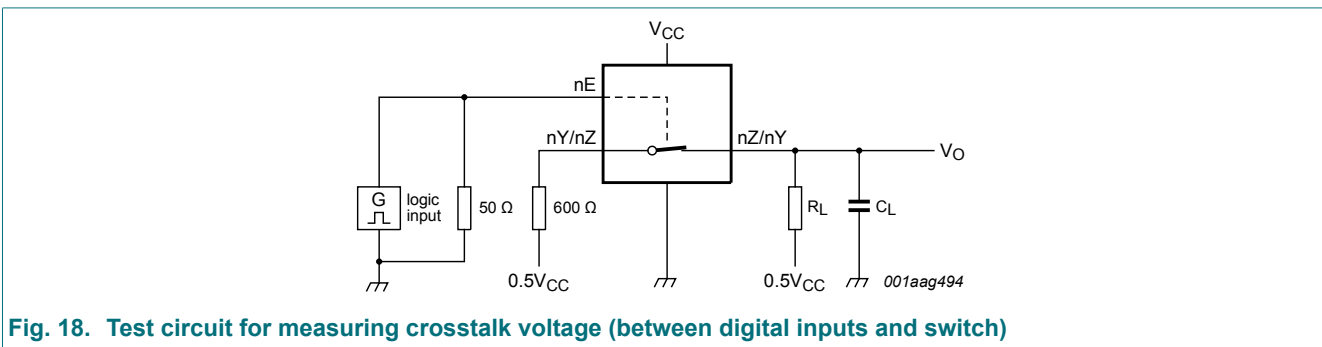
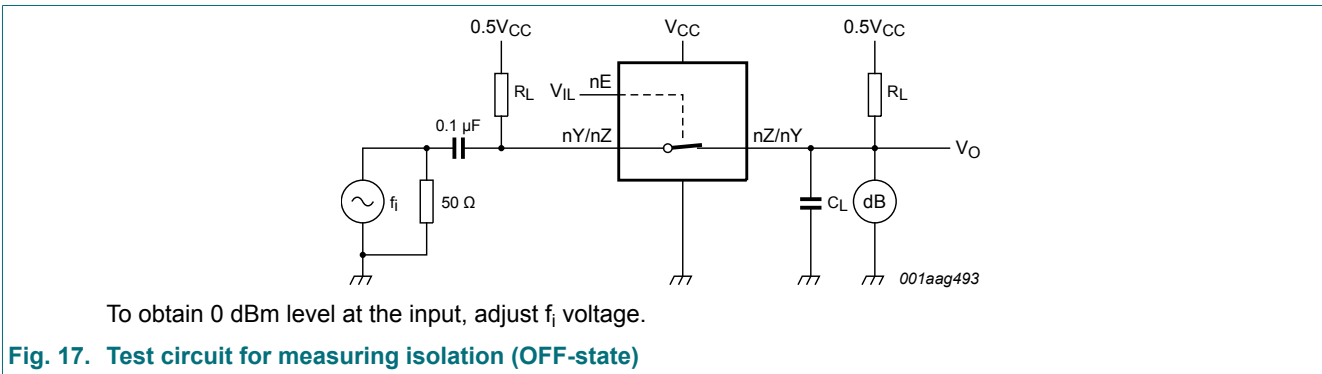
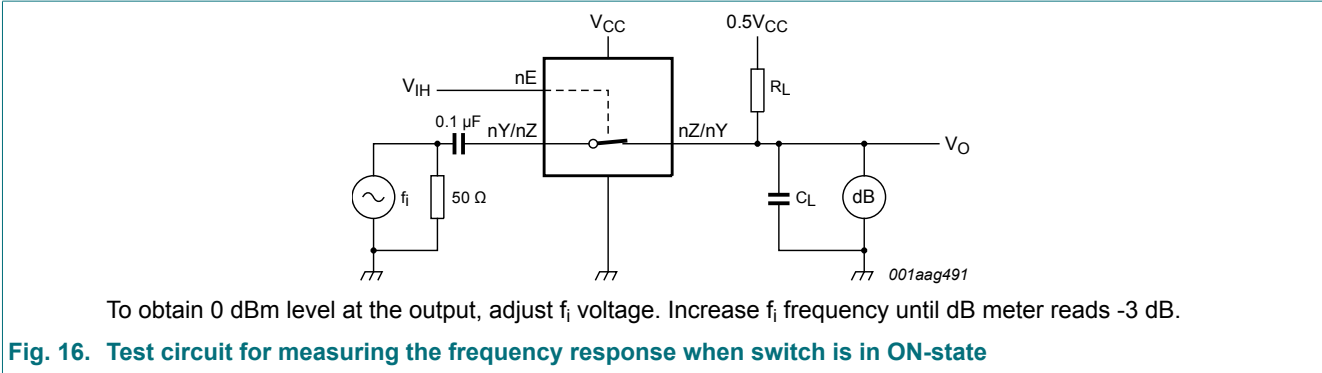
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25$ °C.

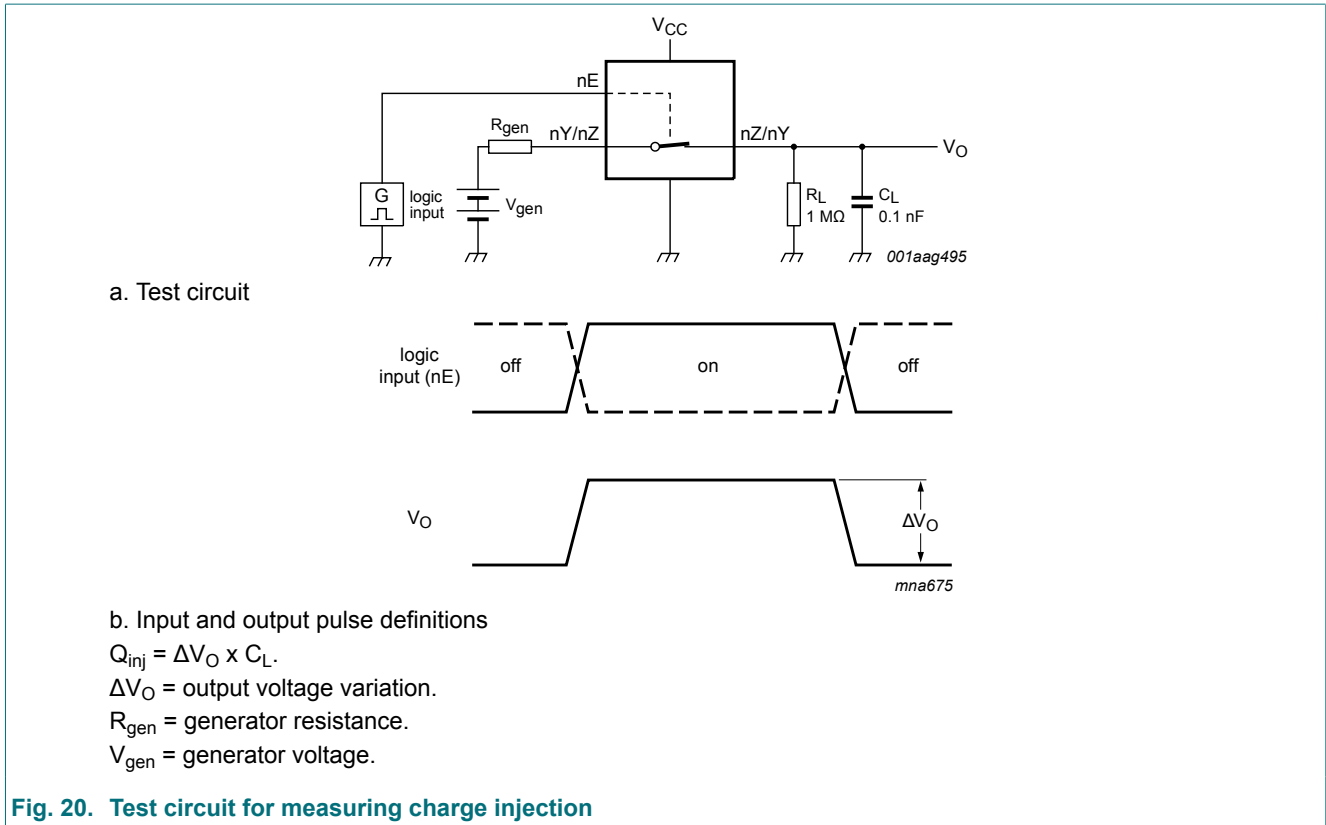
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1$ kHz; $R_L = 10$ k Ω ; $C_L = 50$ pF; see Fig. 15				
		$V_{CC} = 2.3$ V	-	0.42	-	%
		$V_{CC} = 3.0$ V	-	0.36	-	%
		$V_{CC} = 4.5$ V	-	0.47	-	%
		$f_i = 10$ kHz; $R_L = 10$ k Ω ; $C_L = 50$ pF; see Fig. 15				
		$V_{CC} = 2.3$ V	-	0.11	-	%
		$V_{CC} = 3.0$ V	-	0.07	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 600$ Ω ; $C_L = 50$ pF; see Fig. 16				
		$V_{CC} = 2.3$ V	-	160	-	MHz
		$V_{CC} = 3.0$ V	-	200	-	MHz
		$V_{CC} = 4.5$ V	-	210	-	MHz
		$R_L = 50$ Ω ; $C_L = 5$ pF; see Fig. 16				
		$V_{CC} = 2.3$ V	-	180	-	MHz
		$V_{CC} = 3.0$ V	-	180	-	MHz
$V_{CC} = 4.5$ V	-	180	-	MHz		

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{iso}	isolation (OFF-state)	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 17				
		$V_{CC} = 2.3 \text{ V}$	-	-65	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-65	-	dB
		$V_{CC} = 4.5 \text{ V}$	-	-62	-	dB
		$R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 17				
		$V_{CC} = 2.3 \text{ V}$	-	-37	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-36	-	dB
$V_{CC} = 4.5 \text{ V}$	-	-36	-	dB		
V_{ct}	crosstalk voltage	between digital inputs and switch; $R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $t_r = t_f = 2 \text{ ns}$; see Fig. 18				
		$V_{CC} = 2.3 \text{ V}$	-	91	-	mV
		$V_{CC} = 3.0 \text{ V}$	-	119	-	mV
		$V_{CC} = 4.5 \text{ V}$	-	205	-	mV
Xtalk	crosstalk	between switches; $R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 19				
		$V_{CC} = 2.3 \text{ V}$	-	-56	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-55	-	dB
		$V_{CC} = 4.5 \text{ V}$	-	-55	-	dB
		between switches; $R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 19				
		$V_{CC} = 2.3 \text{ V}$	-	-29	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-28	-	dB
$V_{CC} = 4.5 \text{ V}$	-	-28	-	dB		
Q_{inj}	charge injection	$C_L = 0.1 \text{ nF}$; $V_{gen} = 0 \text{ V}$; $R_{gen} = 0 \Omega$; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ M}\Omega$; see Fig. 20				
		$V_{CC} = 2.5 \text{ V}$	-	< 0.003	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	0.003	-	pC
		$V_{CC} = 4.5 \text{ V}$	-	0.0035	-	pC
		$V_{CC} = 5.5 \text{ V}$	-	0.0035	-	pC

11.3. Test circuits



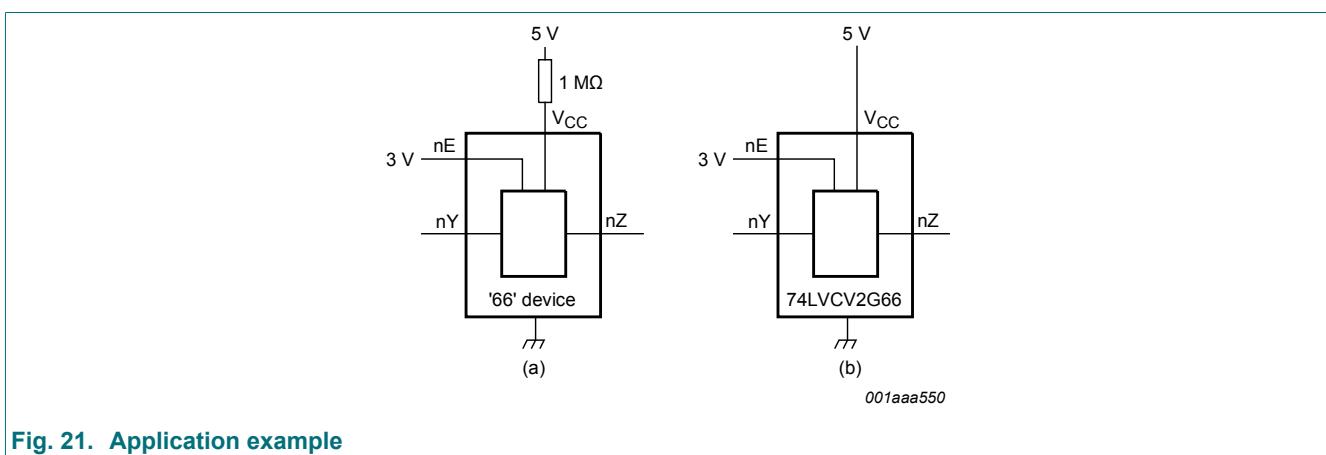




12. Application information

The 74LVCV2G66 is used to reduce component count and footprint in low-power portable applications.

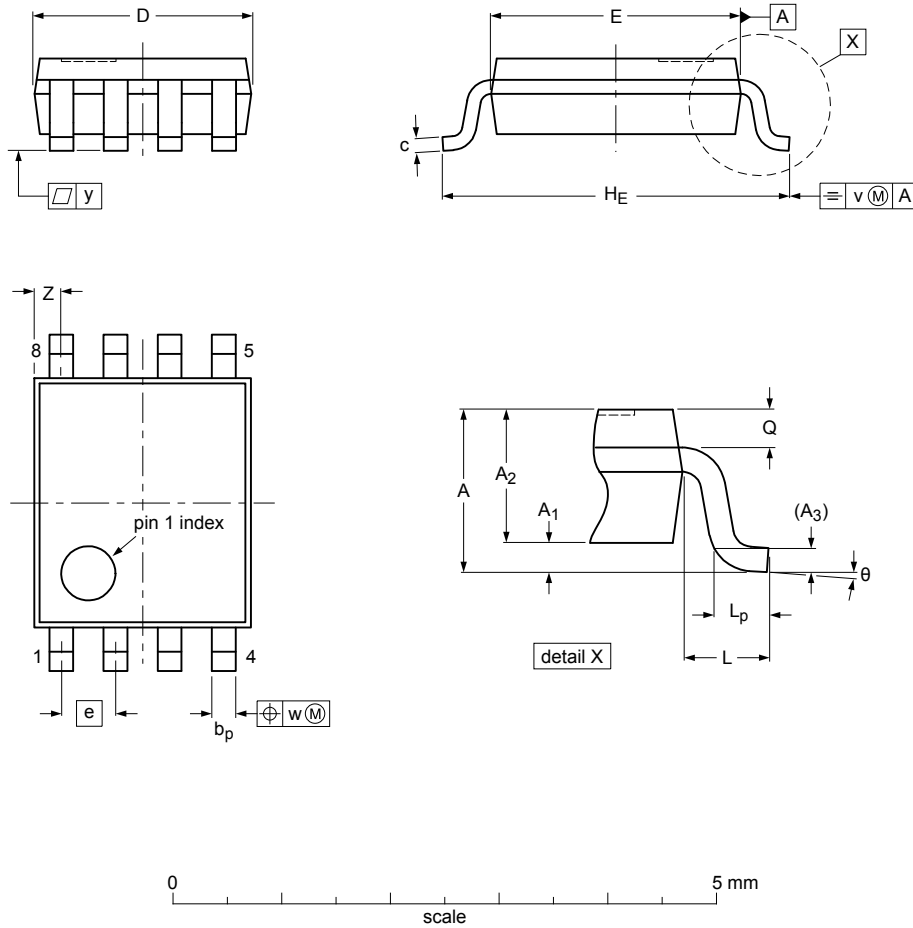
Typical '66' devices do not have low-power enable inputs causing a high ΔI_{CC} . To reduce power consumption in portable (battery) applications, a current limiting resistor is used. (see Fig. 21a). The low-power enable inputs of the 74LVCV2G66 have much lower ΔI_{CC} , eliminating the necessity of the current limiting resistor (see Fig. 21b).



13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
max	1	0.15	0.85		0.27	0.23	2.1	2.4		3.2	0.40	0.21		0.2	0.08	0.1	0.4	8°
nom				0.12					0.5		0.4							
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0	0.15	0.19					0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

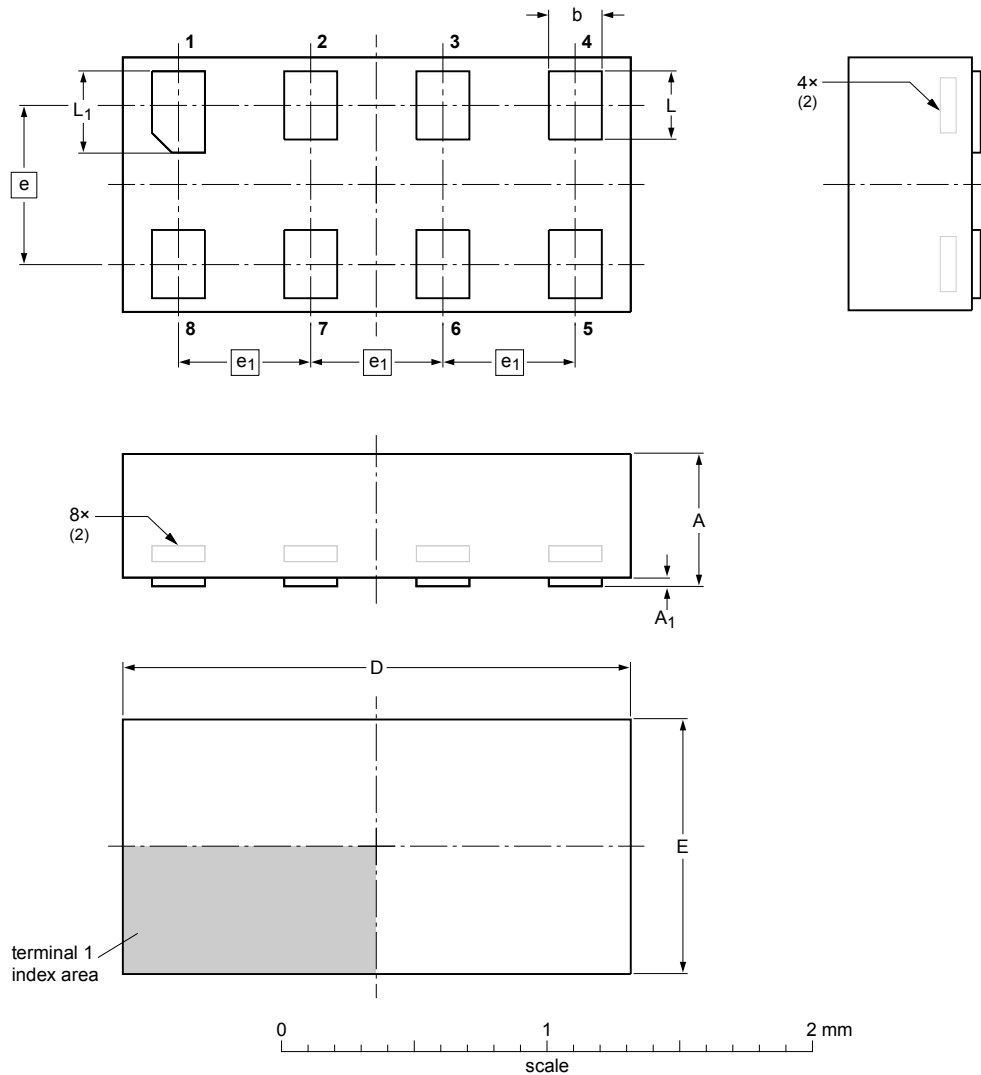
sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				07-06-02 16-05-31

Fig. 22. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

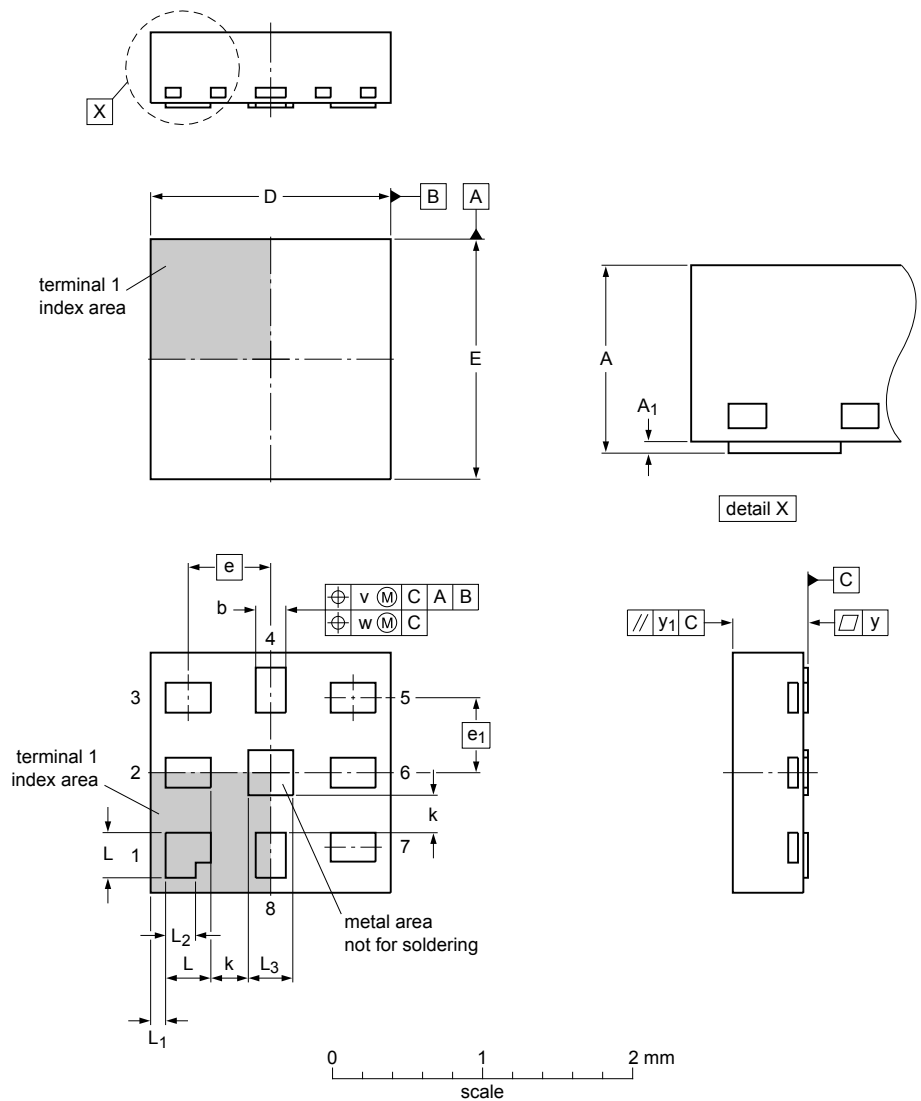
- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		-07-11-14 07-12-07

Fig. 23. Package outline SOT833-1 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2



Dimensions

Unit ⁽¹⁾	A	A ₁	b	D	E	e	e ₁	k	L	L ₁	L ₂	L ₃	v	w	y	y ₁
max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25	0.35				
mm	nom		0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.30	0.1	0.05	0.05	0.05
min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15	0.25				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT902-2	---	MO-255	---		16-07-14 16-11-08

Fig. 24. Package outline SOT902-2 (XQFN8)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCV2G66 v.8	20181105	Product data sheet	-	74LVCV2G66 v.7
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVCV2G66GD (SOT996-2/XSON8) removed. 			
74LVCV2G66 v.7	20161215	Product data sheet	-	74LVCV2G66 v.6
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. Type number 74LVCV2G66DP (SOT505-2) removed. 			
74LVCV2G66 v.6	20150722	Product data sheet	-	74LVCV2G66 v.5
Modifications:	<ul style="list-style-type: none"> Added type numbers 74LVCV2G66GT and 74LVCV2G66GM 			
74LVCV2G66 v.5	20130329	Product data sheet	-	74LVCV2G66 v.4
Modifications:	<ul style="list-style-type: none"> For type number 74LVCV2G66GD XSON8U has changed to XSON8. 			
74LVCV2G66 v.4	20111122	Product data sheet	-	74LVCV2G66 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVCV2G66 v.3	20100616	Product data sheet	-	74LVCV2G66 v.2
74LVCV2G66 v.2	20080703	Product data sheet	-	74LVCV2G66 v.1
74LVCV2G66 v.1	20040402	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Marking	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	3
7. Functional description	4
8. Limiting values	4
9. Recommended operating conditions	4
10. Static characteristics	5
10.1. Test circuits.....	5
10.2. ON resistance.....	6
10.3. ON resistance test circuit and graphs.....	7
11. Dynamic characteristics	9
11.1. Waveforms and test circuit.....	10
11.2. Additional dynamic characteristics.....	11
11.3. Test circuits.....	12
12. Application information	14
13. Package outline	15
14. Abbreviations	18
15. Revision history	18
16. Legal information	19

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Date of release: 5 November 2018