

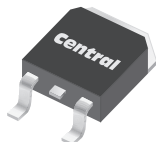
CJD112 NPN
CJD117 PNP

**SURFACE MOUNT SILICON
COMPLEMENTARY
POWER DARLINGTON TRANSISTORS**



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DPAK
POWER!



DPAK CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CJD112 and CJD117 are complementary silicon power Darlington transistors manufactured in a surface mount package designed for low speed switching and amplifier applications.

MARKING: FULL PART NUMBER

MAXIMUM RATINGS: ($T_C=25^\circ\text{C}$ unless otherwise noted)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CB0}	100	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	2.0	A
Peak Collector Current	I_{CM}	4.0	A
Continuous Base Current	I_B	50	mA
Power Dissipation	P_D	20	W
Power Dissipation ($T_A=25^\circ\text{C}$)	P_D	1.75	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Thermal Resistance	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance	θ_{JA}	71.4	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS: ($T_C=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CEO}	$V_{CE}=50\text{V}$		20	μA
I_{CEV}	$V_{CE}=80\text{V}, V_{BE(off)}=1.5\text{V}$		10	μA
I_{CEV}	$V_{CE}=80\text{V}, V_{BE(off)}=1.5\text{V}, T_C=125^\circ\text{C}$		500	μA
I_{CBO}	$V_{CB}=80\text{V}$		10	μA
I_{CBO}	$V_{CB}=100\text{V}$		20	μA
I_{EBO}	$V_{EB}=5.0\text{V}$		2.0	mA
BV_{CEO}	$I_C=30\text{mA}$		100	V
$V_{CE(SAT)}$	$I_C=2.0\text{A}, I_B=8.0\text{mA}$		2.0	V
$V_{CE(SAT)}$	$I_C=4.0\text{A}, I_B=40\text{mA}$		3.0	V
$V_{BE(SAT)}$	$I_C=4.0\text{A}, I_B=40\text{mA}$		4.0	V
$V_{BE(ON)}$	$V_{CE}=3.0\text{V}, I_C=2.0\text{A}$		2.8	V
h_{FE}	$V_{CE}=3.0\text{V}, I_C=0.5\text{A}$	500		
h_{FE}	$V_{CE}=3.0\text{V}, I_C=2.0\text{A}$	1000	12000	
h_{FE}	$V_{CE}=3.0\text{V}, I_C=4.0\text{A}$	200		
f_T	$V_{CE}=10\text{V}, I_C=750\text{mA}, f=1.0\text{MHz}$	25		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=0.1\text{MHz}$ (CJD112)		100	pF
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=0.1\text{MHz}$ (CJD117)		200	pF

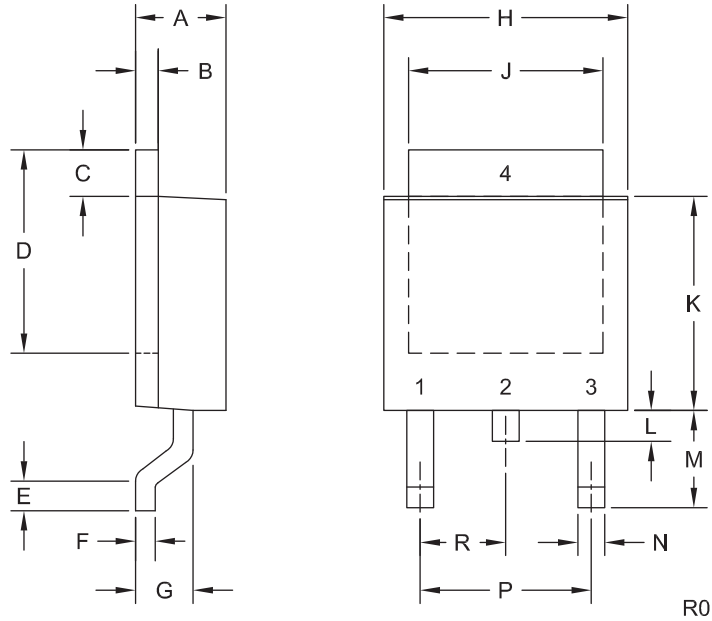
R3 (21-January 2013)

CJD112 NPN
CJD117 PNP



**SURFACE MOUNT SILICON
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DPAK CASE - MECHANICAL OUTLINE



LEAD CODE:

- 1) Base
- 2) Collector
- 3) Emitter
- 4) Collector

MARKING:

FULL PART NUMBER

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.083	0.108	2.10	2.75
B	0.016	0.032	0.40	0.81
C	0.035	0.063	0.89	1.60
D	0.203	0.228	5.15	5.79
E	0.020	-	0.51	-
F	0.018	0.024	0.45	0.60
G	0.051	0.071	1.30	1.80
H	0.248	0.268	6.30	6.81
J	0.197	0.217	5.00	5.50
K	0.209	0.245	5.30	6.22
L	0.025	0.040	0.64	1.02
M	0.090	0.115	2.30	2.91
N	0.012	0.045	0.30	1.14
P	0.180		4.60	
R	0.090		2.30	

DPAK (REV: R0)

R3 (21-January 2013)

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CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

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