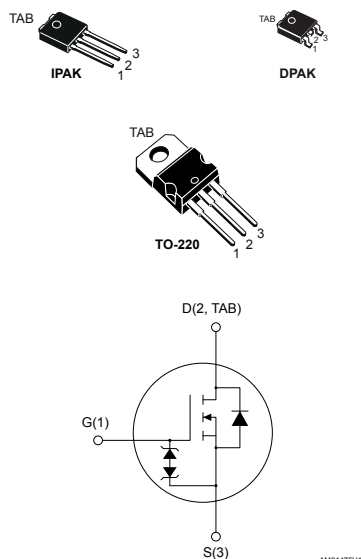


N-channel 1000 V, 6.25 Ω typ., 1.85 A SuperMESH™ Power MOSFETs in DPAK, TO-220 and IPAK packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STD2NK100Z	1000 V	8.5 Ω	1.85 A	DPAK
STP2NK100Z				TO-220
STU2NK100Z				IPAK

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STD2NK100Z](#)
[STP2NK100Z](#)
[STU2NK100Z](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1000	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	1.85	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.16	A
$I_{DM}^{(1)}$	Drain current (pulsed)	7.4	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	W
ESD	Gate-source human body model ($C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$)	3	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	2.5	V/ns
T_j	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 1.85\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.79			$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	-	-	
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	100	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not-repetitive	1.85	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	170	mJ

1. Pulse width limited by T_{jmax} .

2. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	1000			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.9\text{ A}$		6.25	8.5	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	499	-	pF
C_{oss}	Output capacitance			53		
C_{rss}	Reverse transfer capacitance			9		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 800\text{ V}$	-	28	-	pF
R_G	Gate input resistance	$f = 1\text{ MHz}$, open drain	-	6.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 800\text{ V}$, $I_D = 1.85\text{ A}$, $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	16	-	nC
Q_{gs}	Gate-source charge			3		
Q_{gd}	Gate-drain charge			9		

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 500 V, I _D = 0.9 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	7.2	-	ns
t _r	Rise time			6.5		
t _{d(off)}	Turn-off delay time	(see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)		41.5		
t _f	Fall time			32.5		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1.85	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		7.4	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1.85\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.85\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	476		ns
Q_{rr}	Reverse recovery charge		-	1.6		μC
I_{RRM}	Reverse recovery current		-	6.9		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.85\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	532		ns
Q_{rr}	Reverse recovery charge		-	1.9		μC
I_{RRM}	Reverse recovery current		-	88		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

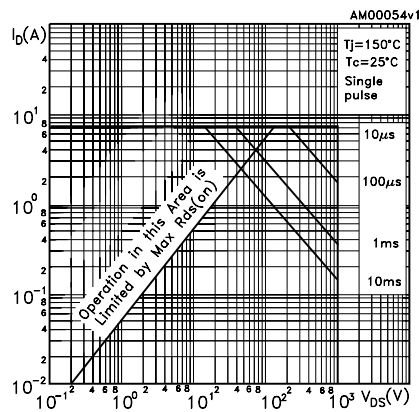
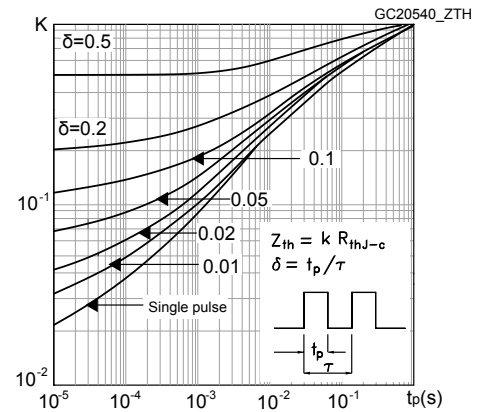
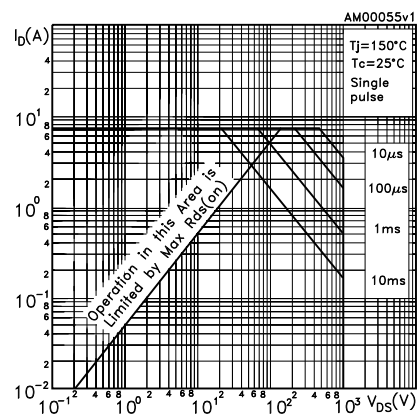
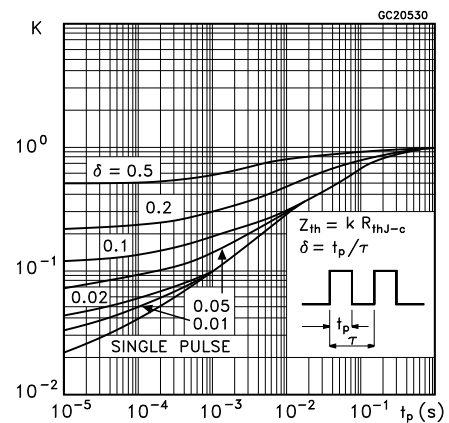
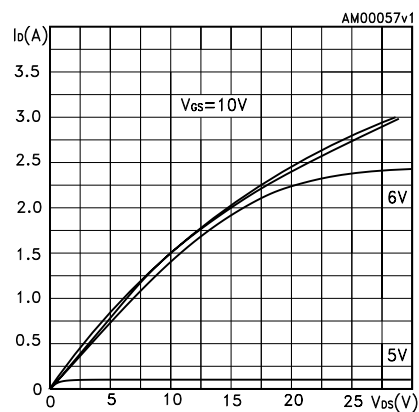
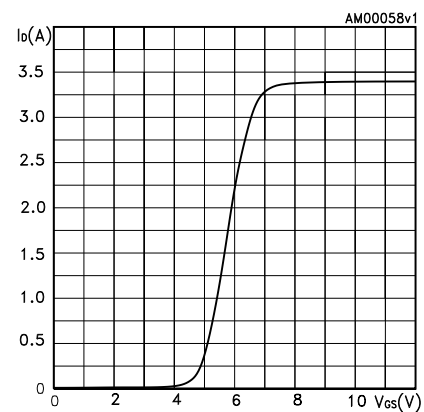
Figure 1. Safe operating area for IPAK, DPAK

Figure 2. Thermal impedance for IPAK, DPAK

Figure 3. Safe operating area for TO-220

Figure 4. Thermal impedance for TO-220

Figure 5. Output characteristics

Figure 6. Transfer characteristics


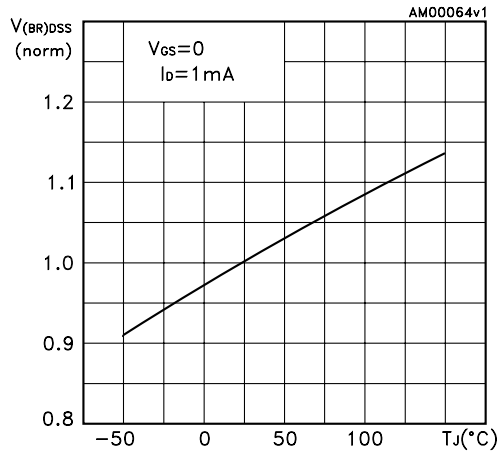
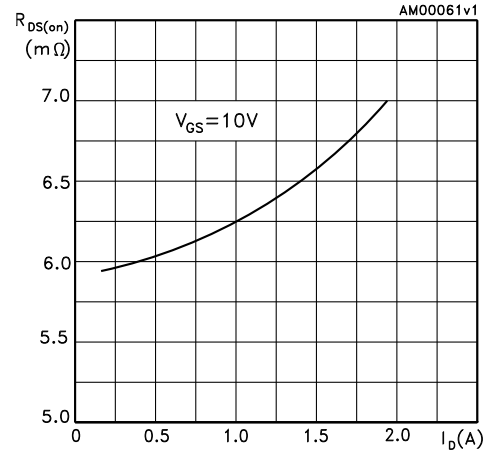
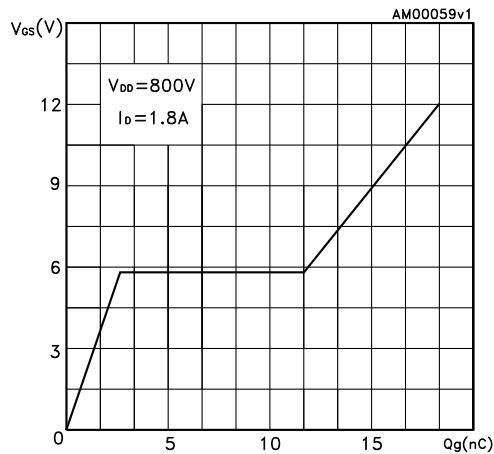
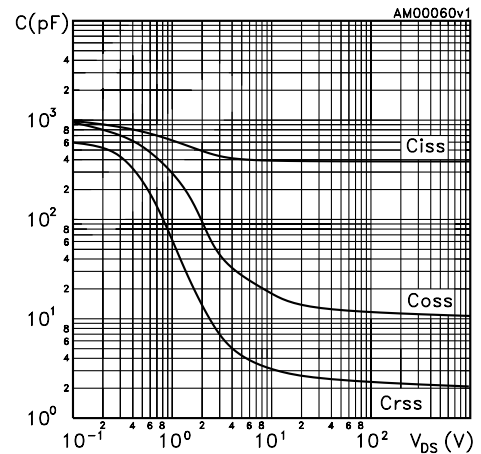
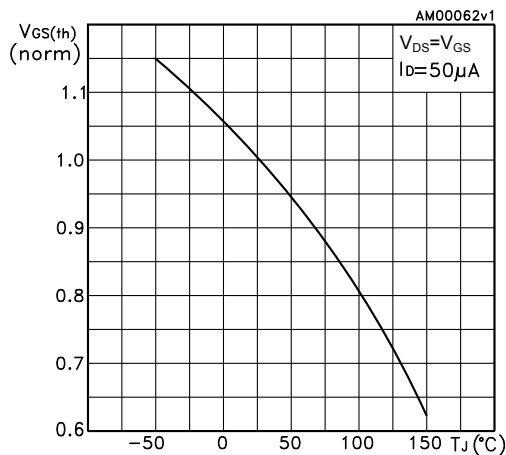
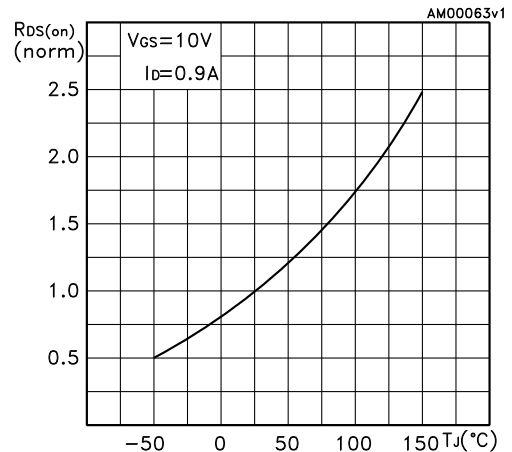
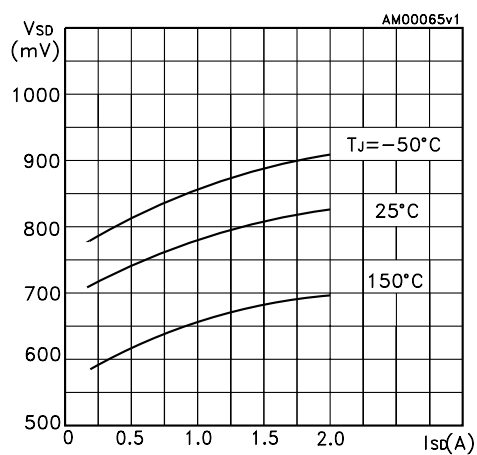
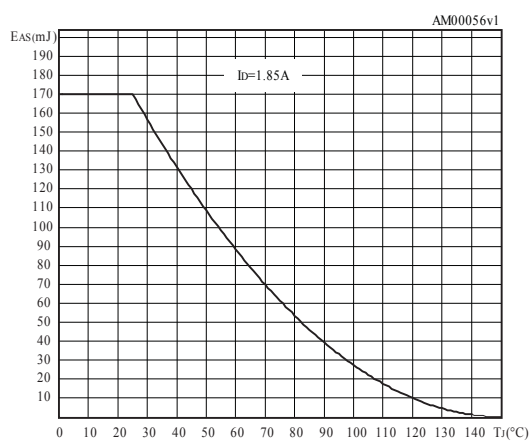
Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

Figure 8. Static drain-source on resistance

Figure 9. Gate charge vs gate-source voltage

Figure 10. Capacitance variations

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature


Figure 13. Source-drain diode forward characteristics

Figure 14. Maximum avalanche energy vs temperature


3 Test circuits

Figure 15. Test circuit for resistive load switching times


AM01468v1

Figure 16. Test circuit for gate charge behavior


AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform

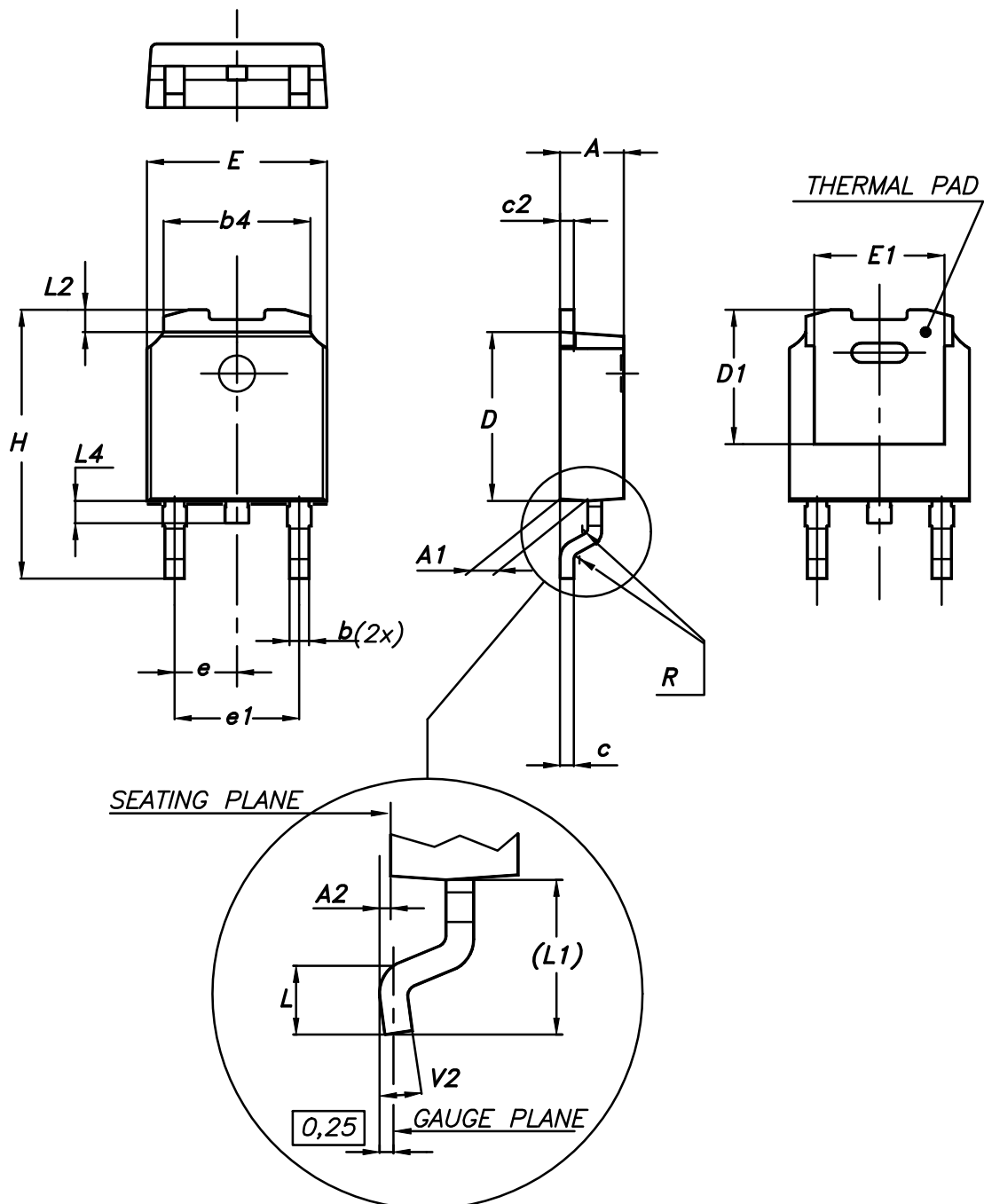

AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 21. DPAK (TO-252) type A package outline



0068772_A_25

Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type E package information

Figure 22. DPAK (TO-252) type E package outline

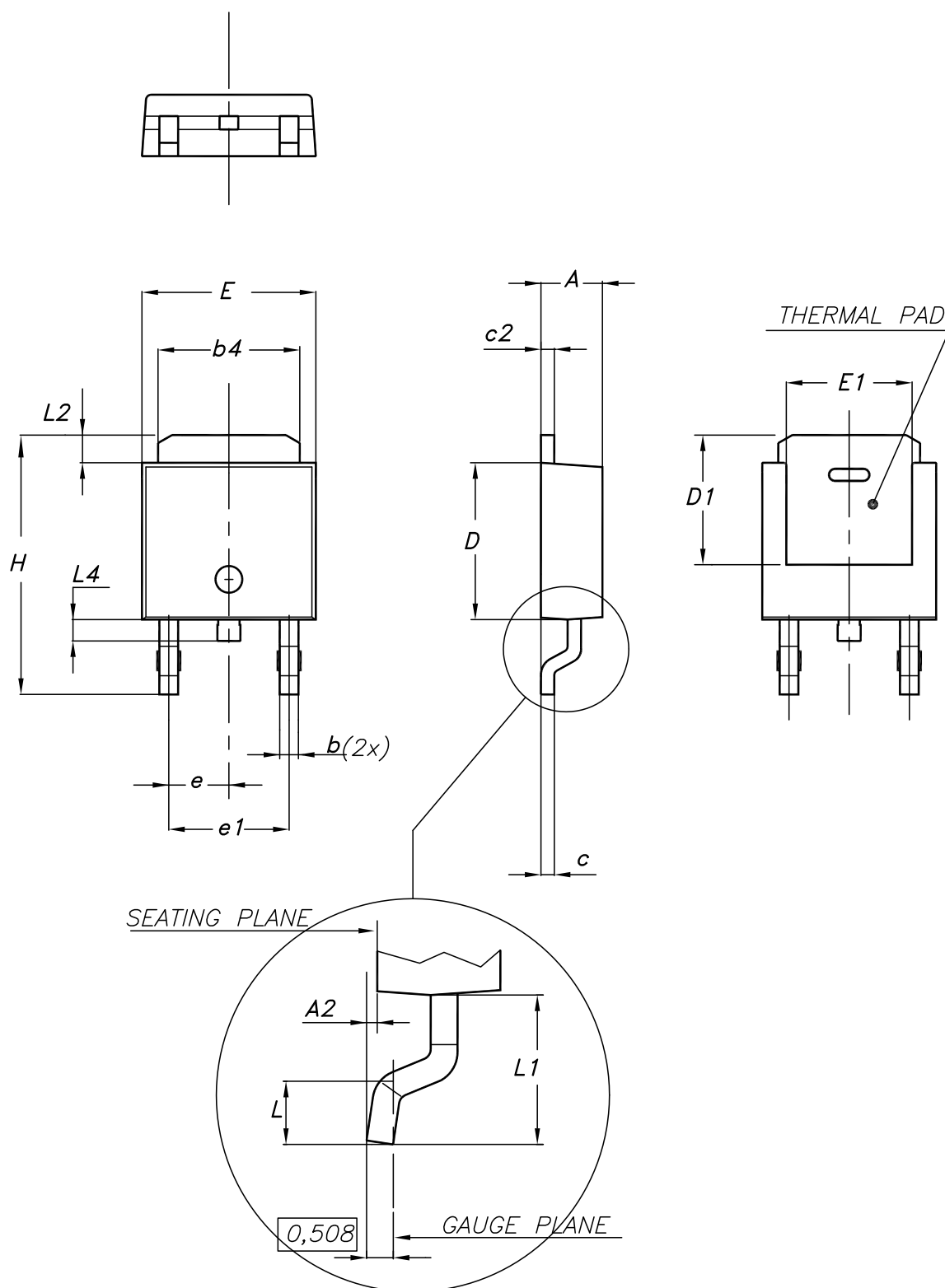
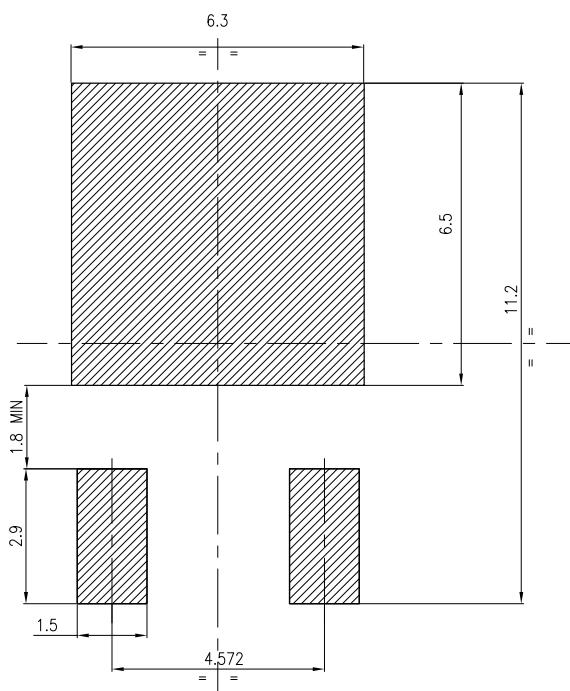


Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

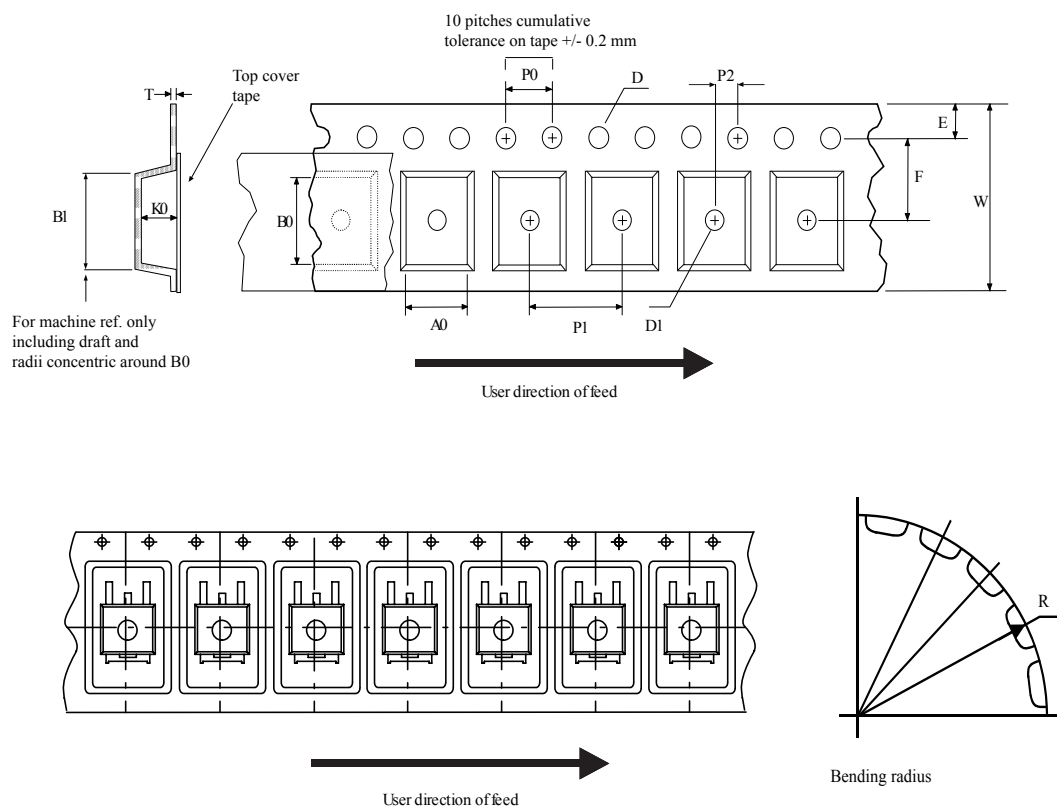
Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



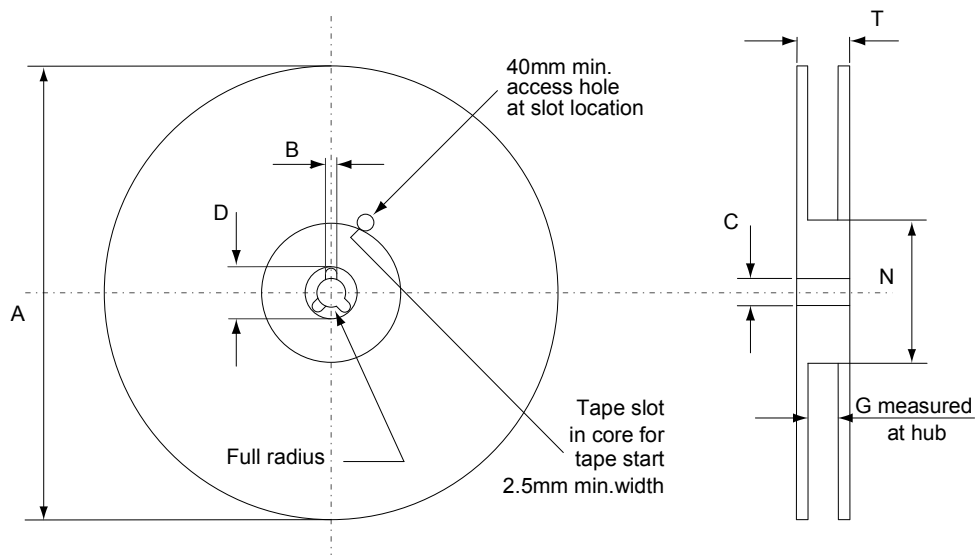
FP_0068772_25

4.3 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



AM08852v1

Figure 25. DPAK (TO-252) reel outline


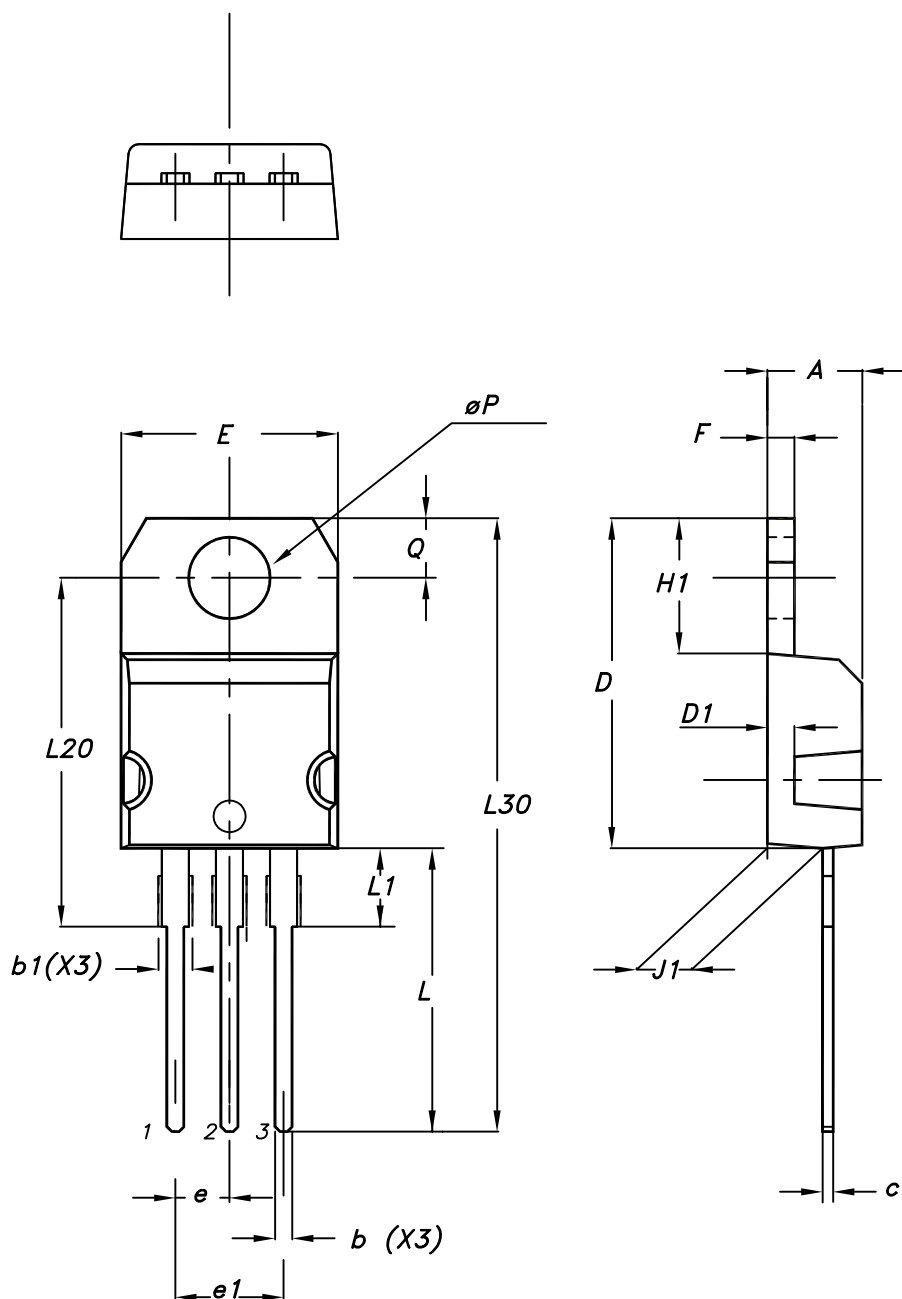
AM06038v1

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 26. TO-220 type A package outline



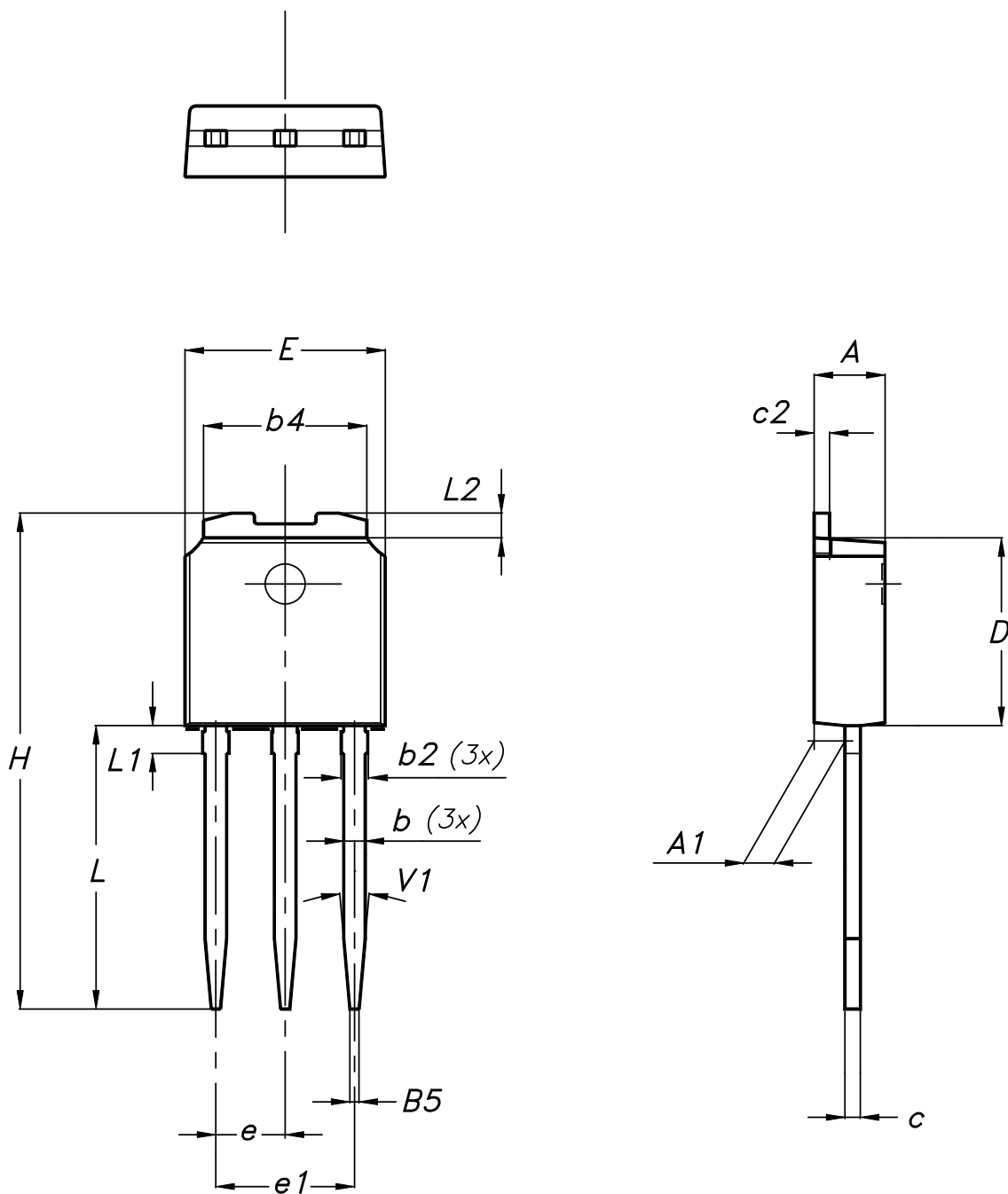
0015988_typeA_Rev_21

Table 12. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 IPAK (TO-251) type A package information

Figure 27. IPAK (TO-251) type A package outline



0068771_IK_typeA_rev14

Table 13. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STD2NK100Z	2NK100Z	DPAK	Tape and reel
STP2NK100Z		TO-220	Tube
STU2NK100Z		IPAK	

Revision history

Table 15. Document revision history

Date	Version	Changes
24-Oct-2007	1	First release
18-Jun-2008	2	– Inserted new package, mechanical data IPAK – Document status promoted from preliminary data to datasheet.
28-Jun-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	DPAK (TO-252) type A package information	9
4.2	DPAK (TO-252) type E package information	11
4.3	DPAK (TO-252) packing information	13
4.4	TO-220 type A package information	15
4.5	IPAK (TO-251) type A package information	17
5	Ordering information	20
	Revision history	21

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved