

## Middle Power Class-D Speaker Amplifiers

# Class-D Speaker Amplifier for Digital Input with Built-in DSP



**BM5446EFV**

No.10075EBT13

### ●Description

BM5446EFV is a Class D Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 86% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

### ●Features

- 1) This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
- 2) This IC has two input systems of digital audio interface.  
(I<sup>2</sup>S/LJ/RJ format, LRCLK: 32 kHz/ 44.1kHz / 48kHz, SYS\_CLK: 256fs / 512fs,  
BCLK: 48fs / 64fs, SDATA: 16 / 20 / 24bit)
- 3) With wide range of power supply voltage, it is possible to operate with single power supply. (V<sub>cc</sub> = 10~26V)
- 4) With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
- 5) S/N of the system can be optimized by adjusting the gain selection in 16 steps. (20~35dB, 1dB/step)
- 6) With built-in feedback circuitry at the output, prevents the decrease in sound quality due to change in power supply voltage. In addition, low noise and low distortion are achieved.
- 7) With a built-in DAC provides best stereo-output for headphone function. As a result, the selection of output of the digital input in two systems is possible.
- 8) It has additional S/PDIF output for the LINE output usage.
- 9) Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
- 10) This IC is built-in with various protection functions for highly reliability design.  
(High temperature protection, Under voltage protection, Output short protection, Output DC-Voltage protection and Clock stop protection).

### ●Applications

Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.

### ●Absolute maximum ratings (Ta=25°C)

| Parameter                    | Symbol            | Ratings    | Unit | Conditions                  |
|------------------------------|-------------------|------------|------|-----------------------------|
| Supply voltage               | V <sub>CC</sub>   | 30         | V    | Pin 27, 30, 31, 51, 52 *1*2 |
| Power dissipation            | P <sub>d</sub>    | 2.0        | W    | *3                          |
|                              |                   | 4.5        | W    | *4                          |
|                              |                   | 6.2        | W    | *5                          |
| Input voltage                | V <sub>IN</sub>   | -0.3 ~ 4.5 | V    | Pin 5 ~ 14, 22 *1           |
| Open-drain terminal voltage  | V <sub>ERR</sub>  | -0.3 ~ 30  | V    | Pin 26 *1                   |
| Operating temperature range  | T <sub>opr</sub>  | -25 ~ +85  | °C   |                             |
| Storage temperature range    | T <sub>stg</sub>  | -55 ~ +150 | °C   |                             |
| Maximum junction temperature | T <sub>jmax</sub> | +150       | °C   |                             |

\*1 The voltage that can be applied reference to GND (Pin 4, 36, 37, 45, 46) and VSS (Pin 15, 20).

\*2 Do not, however exceed P<sub>d</sub> and T<sub>jmax</sub>=150°C.

\*3 70mm×70mm×1.6mm, FR4, 1-layer glass epoxy board (Copper on bottom layer 0%)

Derating in done at 16mW/°C for operating above Ta=25°C.

\*4 70mm×70mm×1.6mm, FR4, 2-layer glass epoxy board (Copper on bottom layer 100%)

Derating in done at 36mW/°C for operating above Ta=25°C. There are thermal via on the board.

\*5 70mm×70mm×1.6mm, FR4, 4-layer glass epoxy board (Copper on bottom layer 100%)

Derating in done at 49.6mW/°C for operating above Ta=25°C. There are thermal via on the board.

### ●Operating conditions (Ta=25°C)

| Parameter                                  | Symbol            | Ratings | Unit | Conditions                   |
|--------------------------------------------|-------------------|---------|------|------------------------------|
| Supply voltage                             | V <sub>CC</sub>   | 10 ~ 26 | V    | Pin 27, 30, 31, 51, 52 *1 *2 |
| Minimum load impedance<br>(Speaker Output) | R <sub>L_SP</sub> | 5.4     | Ω    | *6                           |
| Minimum load impedance<br>(DAC Output)     | R <sub>L_DA</sub> | 20      | kΩ   | Pin 24, 25                   |

\*6 Do not, however exceed P<sub>d</sub>.

\* No radiation-proof design.

# ●Electrical characteristics

(Unless otherwise specified Ta=25°C, Vcc=13V, f=1kHz, RL\_SP=8Ω, RL\_DA=20kΩ, RESETX=3.3V, MUTEX=3.3V, PDX=3.3V, Gain=20dB, DSP: Through, fs=48kHz)

| Parameter                                             | Symbol              | Limits |       |      | Unit  | Conditions                                                     |
|-------------------------------------------------------|---------------------|--------|-------|------|-------|----------------------------------------------------------------|
|                                                       |                     | Min.   | Typ.  | Max. |       |                                                                |
| Total circuit                                         |                     |        |       |      |       |                                                                |
| Circuit current                                       | I <sub>CC1</sub>    | -      | 60    | 120  | mA    | Pin 27, 30, 31, 51, 52, No load                                |
| Circuit current<br>(Power down mode)                  | I <sub>CC2</sub>    | -      | 2.5   | 5    | mA    | Pin 27, 30, 31, 51, 52, No load<br>RESETX=0V, MUTEX=0V, PDX=0V |
| Open-drain terminal<br>Low level voltage              | V <sub>ERR</sub>    | -      | -     | 0.8  | V     | Pin 26, I <sub>O</sub> =0.5mA                                  |
| Regulator output voltage 1                            | V <sub>REG_G</sub>  | 5.0    | 5.5   | 6.0  | V     | Pin 28, 54                                                     |
| Regulator output voltage 2                            | V <sub>REG_3</sub>  | 3.0    | 3.3   | 3.6  | V     | Pin 3                                                          |
| Regulator output voltage 3                            | V <sub>REG_15</sub> | 1.3    | 1.5   | 1.7  | V     | Pin 16                                                         |
| High level input voltage                              | V <sub>IH</sub>     | 2.5    | -     | 3.3  | V     | Pin 5 ~ 14, 22                                                 |
| Low level input voltage                               | V <sub>IL</sub>     | 0      | -     | 0.8  | V     | Pin 5 ~ 14, 22                                                 |
| Input current<br>(Input pull-up terminal)             | I <sub>IL</sub>     | 50     | 100   | 150  | μA    | Pin 5 ~ 9, VIN = 0V                                            |
| Input current<br>(Input pull-down terminal)           | I <sub>IH</sub>     | 30     | 70    | 105  | μA    | Pin 10 ~ 12, 22, VIN = 3.3V                                    |
| Input current<br>(SCL, SDA terminal)                  | I <sub>I</sub>      | -      | 0     | 1    | μA    | Pin 13, 14, VIN = 3.3V                                         |
| Output current<br>(SCL, SDA terminal)                 | I <sub>O</sub>      | -1     | 0     | -    | μA    | Pin 13, 14, VIN = 0V                                           |
| High level output voltage<br>(S/PDIF output terminal) | V <sub>OH</sub>     | 2.75   | 3.3   | -    | V     | Pin 23, I <sub>O</sub> =-0.6mA                                 |
| Low level output voltage<br>(S/PDIF output terminal)  | V <sub>OL</sub>     | -      | 0     | 0.55 | V     | Pin 23, I <sub>O</sub> = 0.6mA                                 |
| Speaker Output                                        |                     |        |       |      |       |                                                                |
| Maximum momentary<br>output power 1                   | P <sub>O1</sub>     | -      | 10    | -    | W     | THD+n=10%, Gain=26dB *7                                        |
| Maximum momentary<br>output power 2                   | P <sub>O2</sub>     | -      | 20    | -    | W     | Vcc=18V, THD+n=10%, Gain=26dB *7                               |
| Total harmonic distortion                             | THD <sub>SP</sub>   | -      | 0.07  | -    | %     | P <sub>O</sub> =1W, BW=20~20kHz *7                             |
| Crosstalk                                             | CT <sub>SP</sub>    | 65     | 80    | -    | dB    | P <sub>O</sub> =1W, BW=IHF-A *7                                |
| Output noise voltage<br>(Sampling mode)               | V <sub>NO_SP</sub>  | -      | 140   | 280  | μVrms | -∞dBFS, BW=IHF-A *7                                            |
| Residual noise voltage<br>(Mute mode)                 | V <sub>NOR_SP</sub> | -      | 5     | 10   | μVrms | MUTEX=0V, -∞dBFS, BW=IHF-A *7                                  |
| PWM sampling frequency                                | f <sub>PWM1</sub>   | -      | 512   | -    | kHz   | fs=32kHz *7                                                    |
|                                                       | f <sub>PWM2</sub>   | -      | 705.6 | -    | kHz   | fs=44.1kHz *7                                                  |
|                                                       | f <sub>PWM3</sub>   | -      | 768   | -    | kHz   | fs=48kHz *7                                                    |
| DAC Output                                            |                     |        |       |      |       |                                                                |
| Maximum output voltage                                | V <sub>OMAX</sub>   | 0.85   | 1.0   | -    | Vrms  | 0dBFS, THD+n=1%                                                |
| Channel Balance                                       | CB                  | -1     | 0     | 1    | dB    | 0dBFS                                                          |
| Total harmonic distortion                             | THD <sub>DA</sub>   | -      | 0.05  | 0.5  | %     | -20dBFS, BW=20~20kHz                                           |
| Crosstalk                                             | CT <sub>DA</sub>    | 65     | 80    | -    | dB    | 0dBFS, BW=IHF-A                                                |
| Output noise voltage                                  | V <sub>NO_DA</sub>  | -      | 10    | 20   | μVrms | -∞dBFS, BW=IHF-A                                               |
| Residual noise voltage                                | V <sub>NOR_DA</sub> | -      | 3     | 10   | μVrms | MUTEX=0V, PDX=0V,<br>-∞dBFS, BW=IHF-A                          |

\*7 These items show the typical performance of device and depend on board layout, parts, and power supply.  
The standard value is in mounting device and parts on surface of ROHM's board directly.

# DSP Block Functional Overview

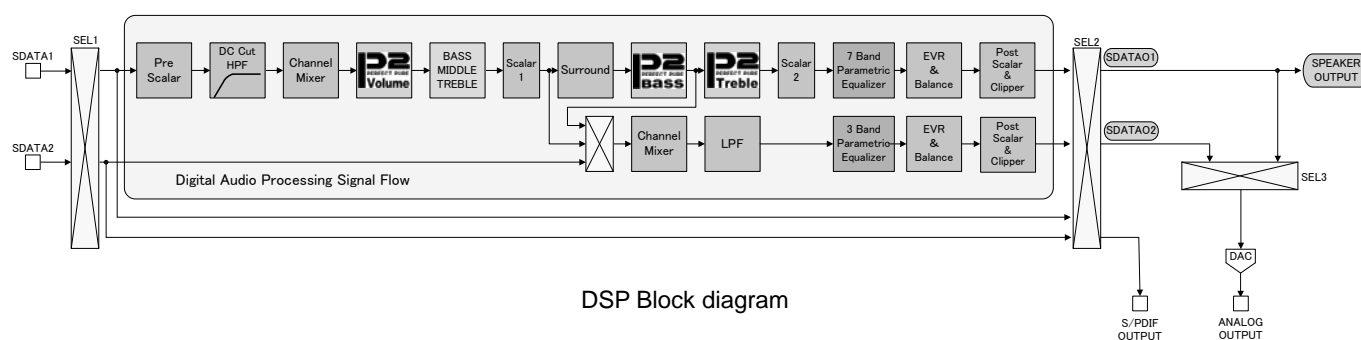
## 1) Main Signal line function

| No. | Function                                       | Specification                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                       |
|-----|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | Pre-scalar                                     | <ul style="list-style-type: none"> <li>• Lch / Rch synchronous control</li> <li>• +24 ~ -103dB (0.5dB step), -∞dB</li> </ul>                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                       |
| 2   | DC cut HPF                                     | <ul style="list-style-type: none"> <li>• FC : 1Hz</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                       |
| 3   | Channel Mixer                                  | <ul style="list-style-type: none"> <li>• Mixing of the sound of the left and right channel of the input digital signal to DSP is set up.</li> </ul>                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                       |
| 4   | P <sup>2</sup> Volume<br>(Perfect Pure Volume) | <ul style="list-style-type: none"> <li>• There are some scenes when sound becomes large suddenly, like the explosion-scene in TV commercial or in an action movie. The "P<sup>2</sup>Volume" function controls volume automatically and adjusts the output level.</li> <li>• It makes easy to hear small whisper voice, and is adjusted.</li> <li>• Attack time : 1ms ~ 40ms (8steps)</li> <li>• Recovery time : 0.25s ~ 10s (16 steps)</li> </ul> |                                                                                                                                                                                                                                                                                                                                       |
| 5   | BASS                                           | <ul style="list-style-type: none"> <li>• Peaking filter is used.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Fc Select : Same as 7 Band Parametric Equalizer</li> <li>• Gain Select : ±18dB (0.5dB step)</li> <li>• Q (Quality Factor) : Same as 7 Band Parametric Equalizer</li> </ul>                                                                                                                 | <ul style="list-style-type: none"> <li>• Low shelf filter is used.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Fc Select : Same as 7 Band Parametric Equalizer</li> <li>• Gain Select : ±18dB (0.5dB step)</li> <li>• Q (Quality Factor) : Same as 7 Band Parametric Equalizer</li> </ul>  |
| 6   | MIDDLE                                         | <ul style="list-style-type: none"> <li>• Peaking filter is used.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Fc Select : Same as 7 Band Parametric Equalizer</li> <li>• Gain Select : ±18dB (0.5dB step)</li> <li>• Q (Quality Factor) : Same as 7 Band Parametric Equalizer</li> </ul>                                                                                                                 |                                                                                                                                                                                                                                                                                                                                       |
| 7   | TREBLE                                         | <ul style="list-style-type: none"> <li>• Peaking filter is used.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Fc Select : Same as 7 Band Parametric Equalizer</li> <li>• Gain Select : ±18dB (0.5dB step)</li> <li>• Q (Quality Factor) : Same as 7 Band Parametric Equalizer</li> </ul>                                                                                                                 | <ul style="list-style-type: none"> <li>• High shelf filter is used.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Fc Select : Same as 7 Band Parametric Equalizer</li> <li>• Gain Select : ±18dB (0.5dB step)</li> <li>• Q (Quality Factor) : Same as 7 Band Parametric Equalizer</li> </ul> |
| 8   | Scalar 1                                       | <ul style="list-style-type: none"> <li>• Lch / Rch Concurrent control</li> <li>• +24 ~ -103dB (0.5dB step), -∞dB</li> </ul>                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                       |
| 9   | Pseudo Stereo                                  | <ul style="list-style-type: none"> <li>• A stereo-feel sound is reproduced for a monophonic sound by signal processing.</li> <li>• 3 steps : Pseudo Stereo OFF / Pseudo Stereo ON (Weak) / Pseudo Stereo ON (Strong)</li> </ul>                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                       |
| 10  | Matrix Surround 3D                             | <ul style="list-style-type: none"> <li>• Matrix Surround 3D of a wider sweet spot, and it also with little prolonged viewing and listening with a feeling of fatigue.</li> <li>• The acoustic field which does not spoil a vocal feeling of the normal position is played back.</li> <li>• Surround : ON / OFF function</li> <li>• Loop : ON / OFF function</li> <li>• Surround gain select : 16 steps</li> </ul>                                  |                                                                                                                                                                                                                                                                                                                                       |
| 11  | P <sup>2</sup> Bass<br>(Perfect Pure Bass)     | <ul style="list-style-type: none"> <li>• Clear deep Bass with low distortion.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Frequency select : 4 steps</li> <li>• Gain select : 0 ~ 15dB (1dB step)</li> </ul>                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                       |
| 12  | P <sup>2</sup> Treble<br>(Perfect Pure Treble) | <ul style="list-style-type: none"> <li>• Real, pure and crystal clear sound.</li> <li>• Lch / Rch Concurrent control</li> <li>• Soft transition function</li> <li>• Gain select : 0 ~ 15dB (1dB step)</li> </ul>                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                       |
| 13  | Scalar 2                                       | <ul style="list-style-type: none"> <li>• Lch / Rch Concurrent control</li> <li>• +24 ~ -103dB (0.5dB step), -∞dB</li> </ul>                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                       |

| No. | Function                    | Specification                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14  | 7-Band Parametric Equalizer | <ul style="list-style-type: none"> <li>Peaking filter is used. (Possible to set the 5 coefficients directly for b0,b1,b2,a1,a2)</li> <li>Lch / Rch Concurrent control</li> <li>Fc select : Setup of 61 divisions (20Hz ~ 20kHz) is possible.</li> <li>Gain select : <math>\pm 18\text{dB}</math> ( 0.5dB step )</li> <li>Q(Quality Factor) : 0.33, 0.43, 0.56, 0.75, 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2</li> </ul> |
| 15  | Volume                      | <ul style="list-style-type: none"> <li>+24 ~ -103dB ( 0.5dB step ), -<math>\infty\text{dB}</math></li> <li>Soft transition and soft mute function</li> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control</li> </ul>                                                                                                                                                                                                      |
| 16  | Balance                     | <ul style="list-style-type: none"> <li>It decreases by 1dB step from a volume setting value.</li> <li>( Lch/Rch : 0dB/-<math>\infty\text{dB}</math>, 0dB/-126dB, 0dB/-125dB, <math>\dots</math>, 0dB/0dB, <math>\dots</math>, -125dB/0dB, -126dB/0dB, -<math>\infty\text{dB}</math>/0dB )</li> </ul>                                                                                                                                       |
| 17  | Post-scaler                 | <ul style="list-style-type: none"> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control</li> <li>+24 ~ -103dB (0.5dB step), -<math>\infty\text{dB}</math></li> </ul>                                                                                                                                                                                                                                                        |
| 18  | Output Clipper              | <ul style="list-style-type: none"> <li>A clip with an arbitrary output amplitude is possible.</li> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control</li> </ul>                                                                                                                                                                                                                                                          |

## 2) Sub Signal line function

| No. | Function                    | Specification                                                                                                                                                                                                                                                                                        |
|-----|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19  | Channel Mixer               | <ul style="list-style-type: none"> <li>Mixing of the sound of the left and right channel of the input digital signal to DSP is set up.</li> <li>Lch (Lch is input, (Lch+Rch)/2 is input, Rch is input), Rch (Rch is input, (Lch+Rch)/2 is input, Lch is input)</li> </ul>                            |
| 20  | LPF                         | <ul style="list-style-type: none"> <li>LPF for Sub-Woofer</li> <li>Fc= 60Hz, 80Hz, 100Hz, 120Hz, 160Hz, 200Hz, 240Hz, 280Hz</li> </ul>                                                                                                                                                               |
| 21  | 3-Band Parametric Equalizer | <ul style="list-style-type: none"> <li>Peaking or low shelf or high shelf filter is used.</li> <li>Lch / Rch Concurrent control</li> </ul>                                                                                                                                                           |
| 22  | Volume                      | <ul style="list-style-type: none"> <li>+24 ~ -103dB ( 0.5dB step ), -<math>\infty\text{dB}</math></li> <li>Soft transition and soft mute function</li> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control</li> </ul>                                                                |
| 23  | Balance                     | <ul style="list-style-type: none"> <li>It decreases by 1dB step from a volume setting value.</li> <li>( Lch/Rch : 0dB/-<math>\infty\text{dB}</math>, 0dB/-126dB, 0dB/-125dB, <math>\dots</math>, 0dB/0dB, <math>\dots</math>, -125dB/0dB, -126dB/0dB, -<math>\infty\text{dB}</math>/0dB )</li> </ul> |
| 24  | Post-scaler                 | <ul style="list-style-type: none"> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control.</li> <li>+24 ~ -103dB (0.5dB step), -<math>\infty\text{dB}</math></li> </ul>                                                                                                                 |
| 25  | Output Clipper              | <ul style="list-style-type: none"> <li>A clip with an arbitrary output amplitude is possible.</li> <li>Lch / Rch Concurrent control, Sub-Woofer ch Independent control.</li> </ul>                                                                                                                   |



● **Electrical characteristic curves** ( $V_{CC}=13V$ ,  $R_{L\_SP}=8\Omega$ ,  $R_{L\_DA}=20k\Omega$ ,  $Gain=20dB$ ,  $f_{in}=1kHz$ ,  $f_s=48kHz$ , by passing DSP)  
Measured by ROHM designed 4 layer board.

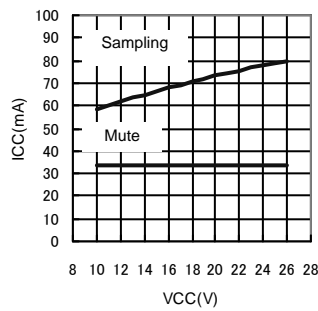


Fig.1

Current consumption  
- Power supply voltage

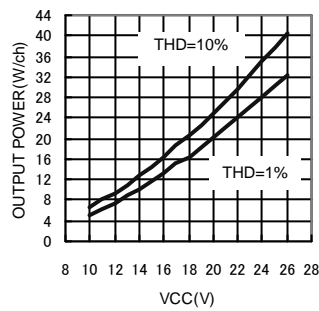


Fig.2

Output power  
- Power supply voltage

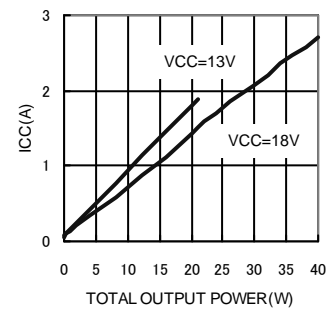


Fig.3

Current consumption  
- Output power

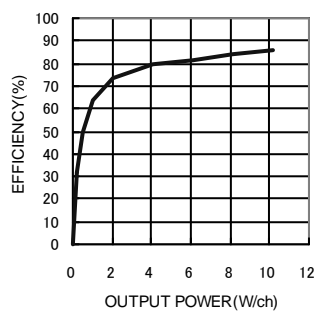


Fig.4

Efficiency - Output power

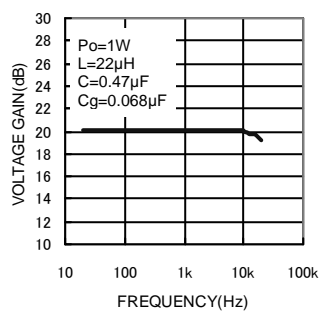


Fig.5

Voltage gain - Frequency

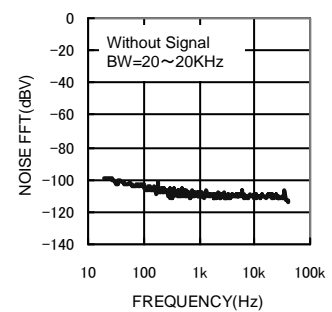


Fig.6

FFT of Output noise voltage

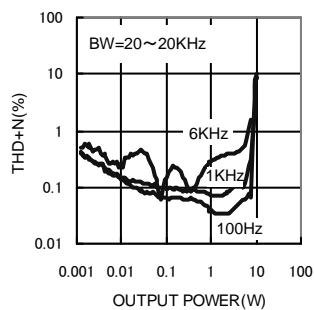


Fig.7

THD+N - Output power

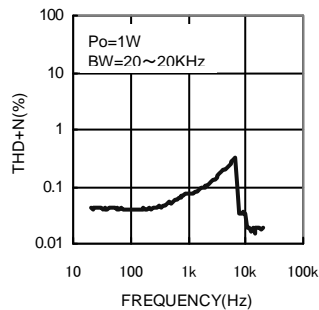


Fig.8

THD+N - Frequency

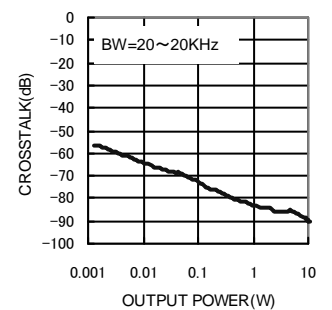


Fig.9

Crosstalk - Output power

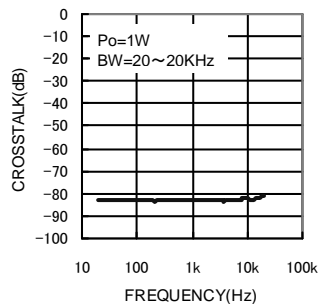


Fig.10

Crosstalk - Frequency

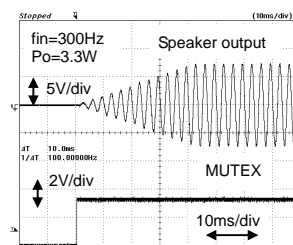


Fig.11

Wave form when  
Releasing Soft-start

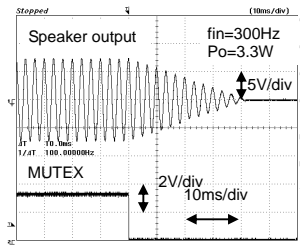


Fig.12

Wave form when  
Activating Soft-mute

● **Electrical characteristic curves**( $V_{CC}=18V$ ,  $R_{L\_SP}=8\Omega$ ,  $R_{L\_DA}=20k\Omega$ ,  $Gain=20dB$ ,  $f_{in}=1kHz$ ,  $f_s=48kHz$ , by passing DSP)  
Measured by ROHM designed 4 layer board.

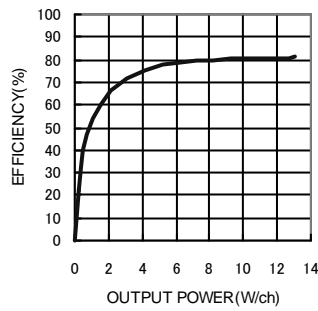


Fig.13

Efficiency – Output power

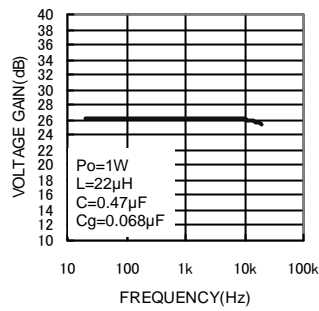


Fig.14

Voltage gain - Frequency

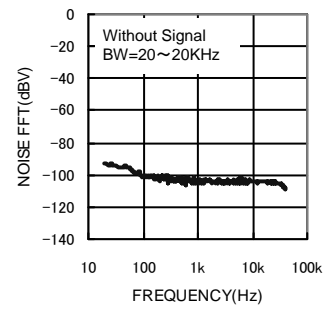


Fig.15

FFT of output noise voltage

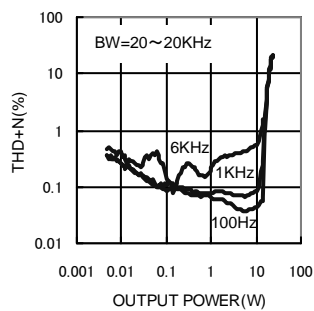


Fig.16

THD+N - Output power

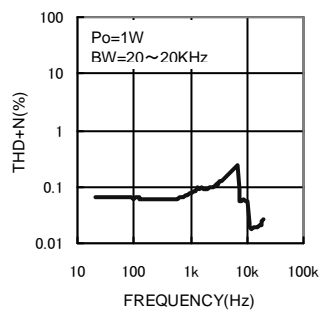


Fig.17

THD+N - Frequency

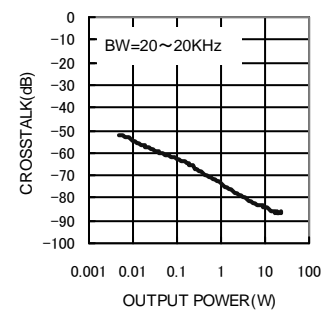


Fig.18

Crosstalk – Output power

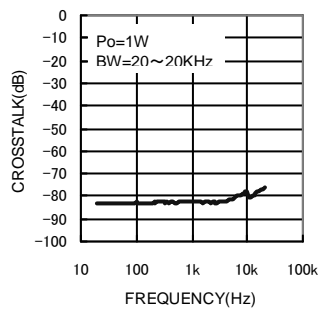
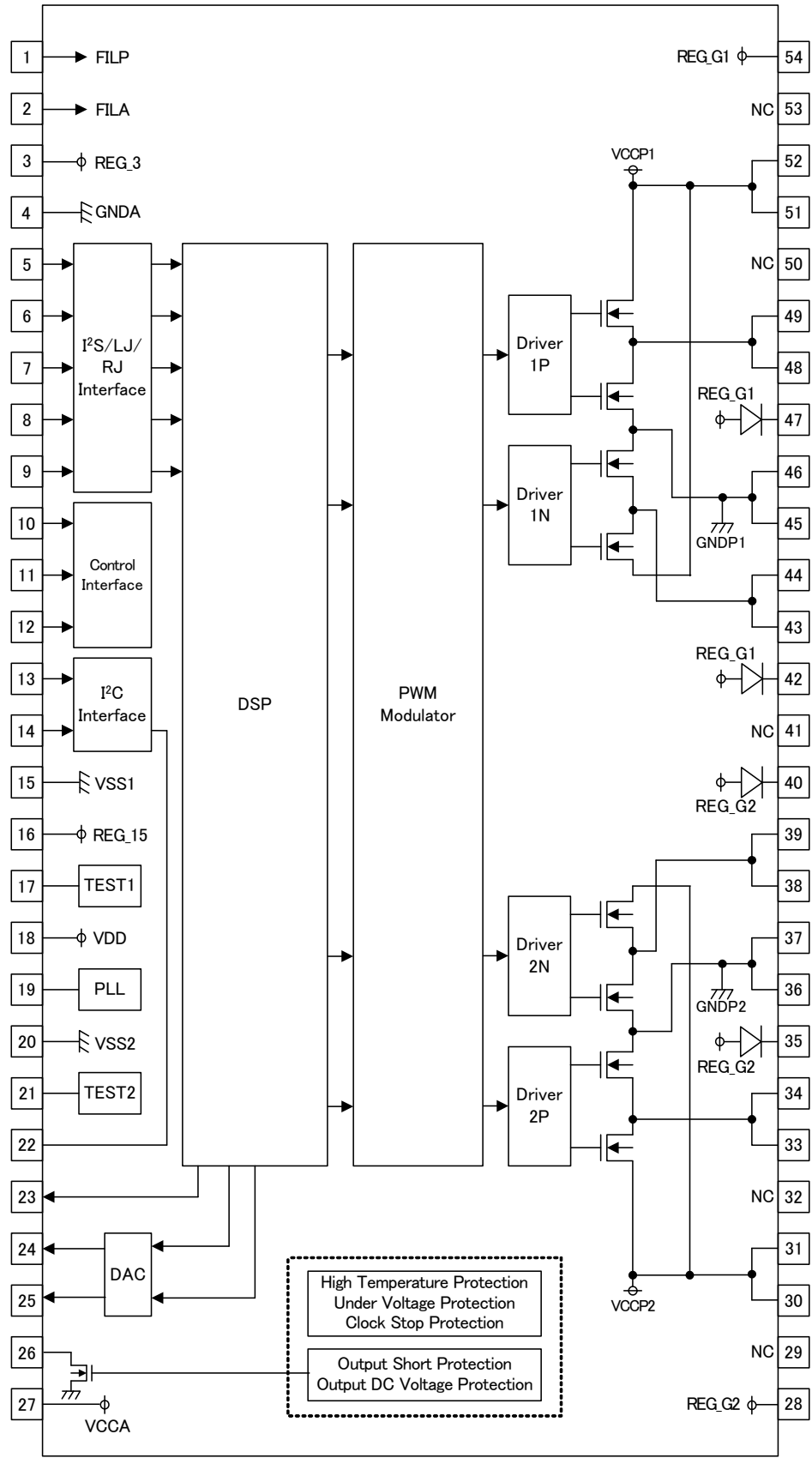


Fig.19

Crosstalk - Frequency

●Pin configuration and Block diagram





●Pin function explanation (Provided pin voltages are typ. Values)

| Pin No.          | Pin name                          | Pin voltage | Pin explanation                                                                                                                     | Internal equivalence circuit |
|------------------|-----------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| 54<br>28         | REG_G1<br>REG_G2                  | 5.5V        | Internal power supply pin for ch1 Gate driver<br>Internal power supply pin for ch2 Gate driver<br><br>Please connect the capacitor. |                              |
| 1                | FILP                              | 1.75~2.55V  | Bias pin for PWM signal<br><br>Please connect the capacitor.                                                                        |                              |
| 2                | FILA                              | 2.5V        | Bias pin for Analog signal<br><br>Please connect the capacitor.                                                                     |                              |
| 3                | REG3                              | 3.3V        | Internal power supply pin for Digital circuit<br><br>Please connect the capacitor.                                                  |                              |
| 4                | GNDA                              | 0V          | GND pin for Analog signal                                                                                                           | —                            |
| 5                | SYS_CLK                           | 3.3V        | System-Clock input pin                                                                                                              |                              |
| 6<br>7<br>8<br>9 | BCLK<br>LRCLK<br>SDATA1<br>SDATA2 | 3.3V        | Digital audio signal input pin                                                                                                      |                              |
| 10               | RESETX                            | 0V          | Reset pin for Digital circuit<br>H: Reset OFF<br>L: Reset ON                                                                        |                              |
| 11               | MUTEX                             |             | Speaker output mute control pin<br>H: Mute OFF<br>L: Mute ON                                                                        |                              |
| 12               | PDX                               |             | Power down control pin<br>H: Power down OFF<br>L: Power down ON                                                                     |                              |

| Pin No.  | Pin name     | Pin voltage | Pin explanation                               | Internal equivalence circuit |
|----------|--------------|-------------|-----------------------------------------------|------------------------------|
| 13       | SCL          | —           | I <sup>2</sup> C transmit clock input pin     |                              |
| 14       | SDA          | —           | I <sup>2</sup> C data input/output pin        |                              |
| 15<br>20 | VSS1<br>VSS2 | 0V          | GND pin for Digital I/O                       | —                            |
| 16       | REG_15       | 1.5V        | Internal power supply pin for Digital circuit |                              |
| 17       | TEST1        | —           | Test pin<br>Please connect to VSS.            |                              |
| 18       | VDD          | 3.3V        | Power supply pin for Digital I/O              | —                            |
| 19       | PLL          | 1V          | PLL's filter pin                              |                              |
| 21       | TEST2        | 0V          | Test pin<br>Please connect to VSS.            |                              |
| 22       | ADDR         | 0V          | I <sup>2</sup> C Slave address select pin     |                              |

| Pin No.                    | Pin name             | Pin voltage | Pin explanation                                                                                                       | Internal equivalence circuit |
|----------------------------|----------------------|-------------|-----------------------------------------------------------------------------------------------------------------------|------------------------------|
| 23                         | OUT_SPDIF            | —           | S/PDIF output pin                                                                                                     |                              |
| 24<br>25                   | OUT_DAC2<br>OUT_DAC1 | 2.5V        | ch2 DAC output pin<br>ch1 DAC output pin<br><br>Please connect it with the latter part circuit through the capacitor. |                              |
| 26                         | ERROR                | 3.3V        | Error flag pin<br><br>Please connect pull-up resistor.<br>H: While Normal<br>L: While Error                           |                              |
| 27                         | VCCA                 | Vcc         | Power supply pin for Analog signal                                                                                    | —                            |
| 30<br>31                   | VCCP2                | Vcc         | Power supply pin for ch2 PWM signal                                                                                   |                              |
| 33<br>34                   | OUT2P                | Vcc~0V      | Output pin of ch2 positive PWM signal<br>Please connect to Output LPF.                                                |                              |
| 35                         | BSP2P                | —           | Boot-strap pin of ch2 positive<br>Please connect the capacitor.                                                       |                              |
| 36<br>37                   | GNDP2                | 0V          | GND pin for ch2 PWM signal                                                                                            |                              |
| 38<br>39                   | OUT2N                | Vcc~0V      | Output pin of ch2 negative PWM signal<br>Please connect to Output LPF.                                                |                              |
| 40                         | BSP2N                | —           | Boot-strap pin of ch2 negative<br>Please connect the capacitor.                                                       |                              |
| 42                         | BSP1N                | —           | Boot-strap pin of ch1 negative<br>Please connect the capacitor.                                                       |                              |
| 43<br>44                   | OUT1N                | Vcc~0V      | Output pin of ch1 negative PWM signal<br>Please connect to Output LPF.                                                |                              |
| 45<br>46                   | GNDP1                | 0V          | GND pin for ch1 PWM signal                                                                                            |                              |
| 47                         | BSP1P                | —           | Boot-strap pin of ch1 positive<br>Please connect the capacitor.                                                       |                              |
| 48<br>49                   | OUT1P                | Vcc~0V      | Output pin of ch1 positive PWM signal<br>Please connect to Output LPF.                                                |                              |
| 51<br>52                   | VCCP1                | —           | Power supply pin for ch1 PWM signal                                                                                   |                              |
| 29<br>32<br>41<br>50<br>53 | N.C.                 | —           | Non connection pin                                                                                                    | —                            |

### ●RESETX pin function

| RESETX<br>(10pin) | State of Digital block |
|-------------------|------------------------|
| L                 | Reset ON               |
| H                 | Reset OFF              |

### ●PDX pin,MUTEX pin function

| PDX<br>(12pin) | MUTEX<br>(11pin) | Power Down | DAC output<br>(24,25pin) | PWM output<br>(33,34,38,39,43,44,48pin) |
|----------------|------------------|------------|--------------------------|-----------------------------------------|
| L              | L or H           | ON         | HiZ_Low                  | HiZ_Low                                 |
| H              | L                | OFF        | Normal operation         |                                         |
| H              | H                |            |                          | Normal operation                        |

### ●Input digital audio sampling frequency (fs) explanation

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

| Sampling frequency of the<br>Digital audio input<br>(fs) | PWM sampling frequency<br>(fpwm) | Soft-start / Soft-mute time | DC voltage protection in<br>the speaker detection time |
|----------------------------------------------------------|----------------------------------|-----------------------------|--------------------------------------------------------|
| 32kHz                                                    | 512kHz                           | 64msec.                     | 64msec.                                                |
| 44.1kHz                                                  | 705.6kHz                         | 46msec.                     | 46msec.                                                |
| 48kHz                                                    | 768kHz                           | 43msec.                     | 43msec.                                                |

### ●For voltage gain (Gain setting)

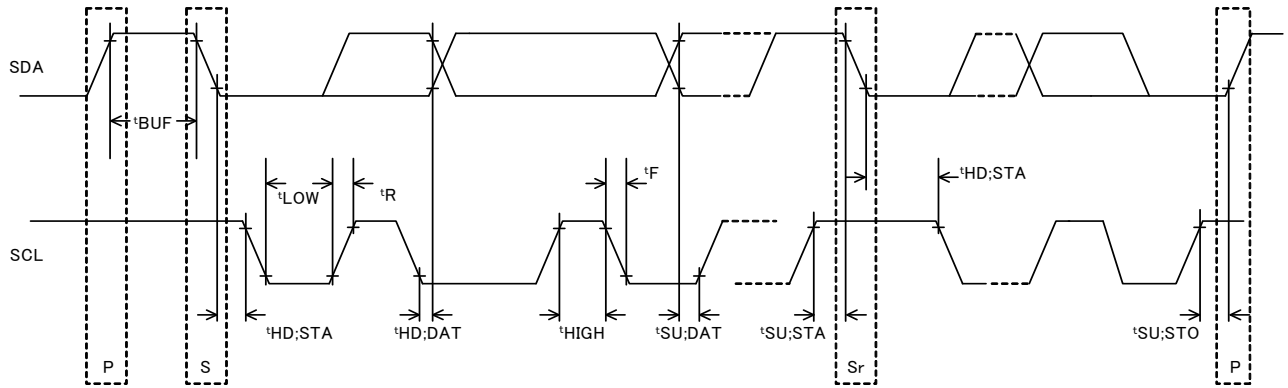
BM5446EFV prescribe voltage gain at speaker output (BTL output) under the definition 0dBV (1Vrms) as full scale input of the digital audio input signal. For example, digital audio input signal = Full scale input, Gain setting = 20dB, Load resistance  $R_{L\_SP} = 8\Omega$  will give speaker output (BTL output) amplitude as 10Vrms. (Output power  $P_o = V_o^2/R_{L\_SP} = 12.5W$  )

### ●Speaker output

DSP output signal SDATAO1 will be output to the speaker. (SDATAO2 will not be output to the speaker. DAC output can be selected either from DSP output signal SDATAO1 or SDATAO2.)

## ●I<sup>2</sup>C Bus control signal specification

### 1) Electrical characteristics and Timing of Bus line and I/O stage



SDA and SCL bus line characteristics (Unless otherwise specified Ta=25°C, V<sub>CC</sub>=13V)

| Parameter                                                                                              | Symbol              | High speed mode |      | Unit |
|--------------------------------------------------------------------------------------------------------|---------------------|-----------------|------|------|
|                                                                                                        |                     | Min.            | Max. |      |
| 1 SCL clock frequency                                                                                  | f <sub>SCL</sub>    | 0               | 400  | kHz  |
| 2 Bus free time between "Stop" condition and "Start" condition                                         | t <sub>BUF</sub>    | 1.3             | -    | μs   |
| 3 Hold-time of (sending again)"Start" condition. After this period the first clock pulse is generated. | t <sub>HD;STA</sub> | 0.6             | -    | μs   |
| 4 SCL clock's LOW state Hold-time                                                                      | t <sub>LOW</sub>    | 1.3             | -    | μs   |
| 5 SCL clock's HIGH state Hold-time                                                                     | t <sub>HIGH</sub>   | 0.6             | -    | μs   |
| 6 Set-up time of sending again "Start" condition                                                       | t <sub>SU;STA</sub> | 0.6             | -    | μs   |
| 7 Data hold time                                                                                       | t <sub>HD;DAT</sub> | 0 <sup>*1</sup> | -    | μs   |
| 8 Data set-up time <sup>*2</sup>                                                                       | t <sub>SU;DAT</sub> | 500/250/150     | -    | ns   |
| 9 Rise-time of SDA and SCL signal                                                                      | t <sub>R</sub>      | 20+Cb           | 300  | ns   |
| 10 Fall-time of SDA and SCL signal                                                                     | t <sub>F</sub>      | 20+Cb           | 300  | ns   |
| 11 Set-up time of "Stop" condition                                                                     | t <sub>SU;STO</sub> | 0.6             | -    | μs   |
| 12 Capacitive load of each bus line                                                                    | Cb                  | -               | 400  | pF   |

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.

\*1 To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.

\*2 The data set-up time is different according to the setting of SYS\_CLK.

When SYS\_CLK=128fs it is 500ns, for SYS\_CLK=256fs it is 250ns, for SYS\_CLK=512fs it will be 150ns.

\*3 SCL and SDA pin is not corresponding to threshold tolerance of 5V.

Please use it within 4.5V of the absolute maximum rating.

### 2) Command interface

I<sup>2</sup>C Bus control is used for command interface between host CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to "Slave Address", set and write 1 byte of "Select Address" to read out the data. I<sup>2</sup>C bus Slave mode format is illustrated below.

| MSB | LSB           | MSB | LSB            | MSB | LSB  |
|-----|---------------|-----|----------------|-----|------|
| S   | Slave Address | A   | Select Address | A   | Data |
|     |               |     |                |     | A P  |

S : Start Condition

Slave Address : The data of eight bits in total is sent putting up bit of Read mode (H) or Write mode (L) after slave address (7bit) set with the terminal ADDR. (MSB first)

A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.

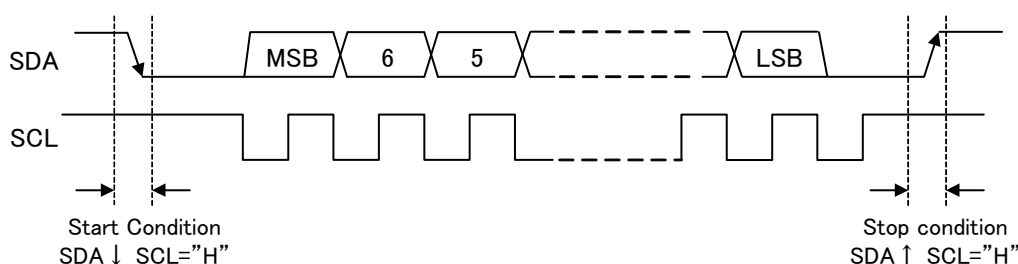
When data is correctly sent and received, "L" is sent and received.

There was no acknowledgement for "H".

Select Address : The select address in one byte is used. (MSB first)

Data : Data byte is sent and received data (MSB first)

P : Stop Condition



## 3) Slave Address

- While ADDR pin (22pin) is "L"

| MSB |    |    |    |    |    |    | LSB |
|-----|----|----|----|----|----|----|-----|
| A6  | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| 1   | 0  | 0  | 0  | 0  | 0  | 0  | 1/0 |

- While ADDR pin (22pin) is "H"

| MSB |    |    |    |    |    |    | LSB |
|-----|----|----|----|----|----|----|-----|
| A6  | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| 1   | 0  | 0  | 0  | 0  | 0  | 1  | 1/0 |

## 4) Writing of data

- Basic format

|   |               |   |                |   |      |   |   |
|---|---------------|---|----------------|---|------|---|---|
| S | Slave Address | A | Select Address | A | Data | A | P |
|---|---------------|---|----------------|---|------|---|---|

☐ : Master to Slave, ☐ : Slave to Master

- Auto-increment format

|   |               |   |                |   |        |   |        |   |            |   |   |
|---|---------------|---|----------------|---|--------|---|--------|---|------------|---|---|
| S | Slave Address | A | Select Address | A | Data 1 | A | Data 2 | A | Data 3...N | A | P |
|---|---------------|---|----------------|---|--------|---|--------|---|------------|---|---|

☐ : Master to Slave, ☐ : Slave to Master

## 5) Reading of data

First of all, the address ( 20h in the example) for reading is written in the register of the D0h address at the time of reading. In the following stream, data is read after the slave address. Please do not return the acknowledge when you end the reception.

|   |               |   |          |   |                |   |   |
|---|---------------|---|----------|---|----------------|---|---|
| S | Slave Address | A | Req_Addr | A | Select Address | A | P |
|---|---------------|---|----------|---|----------------|---|---|

(ex.) 80h                      D0h                      20h

|   |               |   |        |   |        |   |  |   |        |           |   |
|---|---------------|---|--------|---|--------|---|--|---|--------|-----------|---|
| S | Slave Address | A | Data 1 | A | Data 2 | A |  | A | Data N | $\bar{A}$ | P |
|---|---------------|---|--------|---|--------|---|--|---|--------|-----------|---|

(ex.) 81h                      \*\*h                      \*\*h                      \*\*h

☐ : Master to Slave, ☐ : Slave to Master, A : With Acknowledge,  $\bar{A}$  : Without Acknowledge

## 6) Instruction Code Chart (Select Address)

| MSB \ LSB |                                      | 0                     | 1                             | 2                               | 3                               | 4                               | 5                                 | 6                                 | 7                                   |
|-----------|--------------------------------------|-----------------------|-------------------------------|---------------------------------|---------------------------------|---------------------------------|-----------------------------------|-----------------------------------|-------------------------------------|
| 0         | I/O Setting<br>CLK Setting           |                       | RAM<br>Clear                  |                                 | Input SEL<br>S-P2,S-P1          | Output SEL<br>P-S2,P-S1         | SPDIFO<br>Output SEL              |                                   |                                     |
| 1         | SPDIF                                | MUTE<br>Setting       | SPDIF OUT<br>Setting1         | SPDIF OUT<br>Setting2           | SPDIF OUT                       |                                 |                                   |                                   |                                     |
| 2         | DSP<br>Volume                        | PRE Scaler<br>Setting | DC Cut<br>HPF                 | CH Mixer1<br>DSP                | CH Mixer2<br>DF2, DF1           | Scaler1<br>Setting              | Scaler2<br>Setting                | Main Volume<br>Setting            | Main Balance<br>Setting             |
| 3         | Sub Clipper<br>P <sup>2</sup> Volume | Sub Clipper<br>ON/OFF | Sub Clipper<br>Setting1       | Sub Clipper<br>Setting2         | P <sup>2</sup> V Setting1       | P <sup>2</sup> V_MIN            | P <sup>2</sup> V_MAX              | P <sup>2</sup> V_K                | P <sup>2</sup> V_OFS                |
| 4         | DSP<br>TONE                          | BASS<br>Control       | BASS<br>Frequency             | BASS<br>Quality factor          | BASS<br>Gain                    | MIDDLE<br>Control               | MIDDLE<br>Frequency               | MIDDLE<br>Quality factor          | MIDDLE<br>Gain                      |
| 5         | DSP<br>7BandP-EQ                     | 7Band1<br>Control     | 7Band1<br>Frequency           | 7Band1<br>Quality factor        | 7Band1<br>Gain                  | 7Band2<br>Control               | 7Band2<br>Frequency               | 7Band2<br>Quality factor          | 7Band2<br>Gain                      |
| 6         | DSP<br>7BandP-EQ                     | 7Band5<br>Control     | 7Band5<br>Frequency           | 7Band5<br>Quality factor        | 7Band5<br>Gain                  | 7Band6<br>Control               | 7Band6<br>Frequency               | 7Band6<br>Quality factor          | 7Band6<br>Gain                      |
| 7         | DSP<br>Sound Effect                  | Surround<br>Setting   | Pseudo<br>Stereo              | P <sup>2</sup> Bass<br>Setting1 | P <sup>2</sup> Bass<br>Setting2 | P <sup>2</sup> Bass<br>Setting3 | P <sup>2</sup> Treble<br>Setting1 | P <sup>2</sup> Treble<br>Setting2 | P <sup>2</sup> Bass<br>Soft_T Start |
| 8         | DSP<br>3BandP-EQ                     | 3Band1<br>Control     | 3Band1<br>Frequency           | 3Band1<br>Quality factor        | 3Band1<br>Gain                  | 3Band2<br>Control               | 3Band2<br>Frequency               | 3Band2<br>Quality factor          | 3Band2<br>Gain                      |
| 9         |                                      |                       |                               |                                 |                                 |                                 |                                   |                                   |                                     |
| A         | PLLA                                 | PLLA<br>Setting1      |                               |                                 |                                 |                                 |                                   | Sync<br>Detect1                   | Sync<br>Detect2                     |
| B         | Power<br>Stage                       | Power Stage<br>Gain   | Power Stage<br>Test1          | Power Stage<br>Test2            | Power Stage<br>Test3            | Power Stage<br>Test4            | Power Stage<br>Test5              | Power Stage<br>Test6              | Power Stage<br>Test7                |
| C         |                                      |                       |                               |                                 |                                 |                                 |                                   |                                   |                                     |
| D         | Read Base<br>Address                 | Read Base<br>Address  |                               |                                 |                                 |                                 |                                   |                                   |                                     |
| E         |                                      |                       |                               |                                 |                                 |                                 |                                   |                                   |                                     |
| F         | TEST<br>Mode                         | PU<br>Setting         | Initial Setting<br>TEST Mode1 | TEST Mode2                      | MCLK DIV<br>Setting             | PLLA Initial<br>Setting1        | PLLA Initial<br>Setting2          | PLLA Initial<br>Setting3          | PLLA Initial<br>Setting4            |

| MSB \ LSB |                            | 8                                     | 9                      | A                         | B                                | C                                | D                                | E                                | F                     |
|-----------|----------------------------|---------------------------------------|------------------------|---------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-----------------------|
| 0         | I/O Setting<br>CLK Setting | SYSCLK SEL1<br>DSP                    |                        |                           | I <sup>2</sup> S Format1<br>S-P1 | I <sup>2</sup> S Format2<br>S-P2 | I <sup>2</sup> S Format3<br>P-S1 | I <sup>2</sup> S Format4<br>P-S2 |                       |
| 1         | SPDIF                      |                                       |                        |                           |                                  |                                  |                                  |                                  |                       |
| 2         | DSP<br>Volume              | Main Post<br>Scalar Setting           | Main Clipper<br>ON/OFF | Main Clipper<br>Setting1  | Main Clipper<br>Setting2         | Sub Volume<br>Setting            | Sub Balance<br>Setting           | Sub Post<br>Scalar Setting       | Sub Input<br>Selector |
| 3         | P <sup>2</sup> Volume      | A_RATE<br>R_RATE                      | A_TIME<br>R_TIME       | A_RATE_Low<br>R_RATE_Low  | AR_TIME_<br>Low                  | Pulse Sound<br>Setting1          |                                  |                                  |                       |
| 4         | DSP<br>TONE                | TREBLE<br>Control                     | TREBLE<br>Frequency    | TREBLE<br>Quality factor  | TREBLE<br>Gain                   | TONE Control<br>Soft_T Start     |                                  |                                  |                       |
| 5         | DSP<br>7Band P-EQ          | 7Band3<br>Control                     | 7Band3<br>Frequency    | 7Band3<br>Quality factor  | 7Band3<br>Gain                   | 7Band4<br>Control                | 7Band4<br>Frequency              | 7Band4<br>Quality factor         | 7Band4<br>Gain        |
| 6         | DSP<br>7Band P-EQ          | 7Band7<br>Control                     | 7Band7<br>Frequency    | 7Band7<br>Quality factor  | 7Band7<br>Gain                   |                                  | CRAM Auto<br>Over Write          | CRAM Auto<br>Setting1            | CRAM Auto<br>Setting2 |
| 7         | DSP<br>Sound Effect        | P <sup>2</sup> Treble<br>Soft_T Start |                        | Sub Woofer<br>LPF Setting |                                  |                                  |                                  |                                  |                       |
| 8         | DSP<br>3BandP-EQ           | 3Band3<br>Control                     | 3Band3<br>Frequency    | 3Band3<br>Quality factor  | 3Band3<br>Gain                   | P-EQ<br>Setting1                 | P-EQ<br>Setting2                 | P-EQ<br>Setting3                 | P-EQ<br>Setting4      |
| 9         |                            |                                       |                        |                           |                                  |                                  |                                  |                                  |                       |
| A         | PLLA                       | Sync<br>Detect3                       | Sync<br>Detect4        |                           |                                  |                                  |                                  |                                  |                       |
| B         | Power Stage                | C2D speed                             | Refresh                | Test8                     |                                  |                                  |                                  |                                  |                       |
| C         |                            |                                       |                        |                           |                                  |                                  |                                  |                                  |                       |
| D         | Read Base<br>Address       |                                       |                        |                           |                                  |                                  |                                  |                                  |                       |
| E         |                            |                                       |                        |                           |                                  |                                  |                                  |                                  |                       |
| F         | TEST<br>Mode               | RAM Test<br>Setting1                  | RAM Test<br>Setting2   | RAM Test<br>Setting3      | RAM Test<br>Setting4             | RAM Test<br>Setting5             | DSP Mute<br>Set                  |                                  |                       |

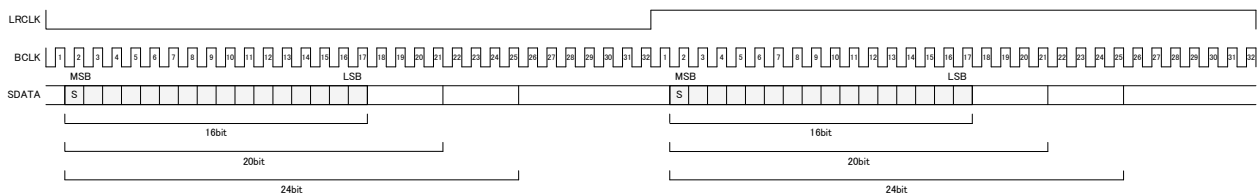
### ●Format of digital audio input

- **SYS\_CLK:** It is System Clock input signal.  
It will input LRCLK, BCLK, SDATA1 (SDATA2) that synchronizes with this clock that are 128 times of sampling frequency (128fs), 256 times of sampling frequency (256fs), or 512 times frequency (512fs) of sampling frequency (fs).
- **LRCLK:** It is L/R clock input signal.  
It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs) .  
The audio data of a left channel and a right channel for one sample is input to this section.
- **BCLK:** It is Bit Clock input signal.  
It is used for the latch of data in every one bit by sampling frequency's 48 times frequency (48fs) or 64 times sampling frequency (64fs). However if the 48fs being selected, the input will be Right-justified data format and held static.
- **SDATA1 & SDATA2:** It is Data input signal.  
It is amplitude data. The data length is different according to the resolution of the input digital data.  
It corresponds to 16/ 20/ 24 bit.

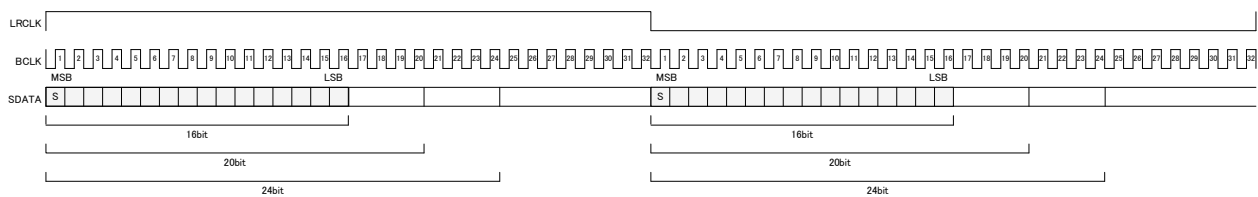
The digital input has I2S, Left-justified and Right-justified formats.

The figure below shows the timing chart of each transmission mode.

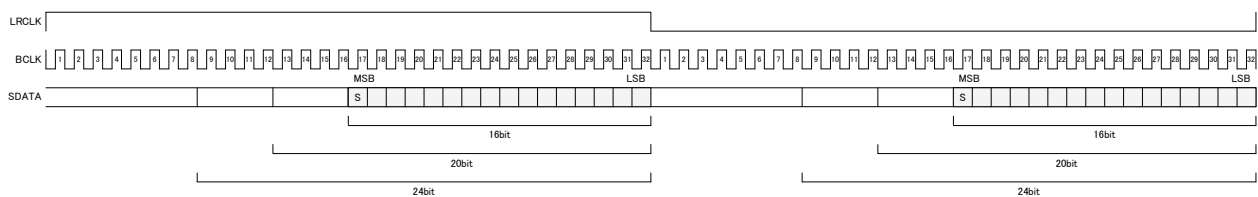
I<sup>2</sup>S data format



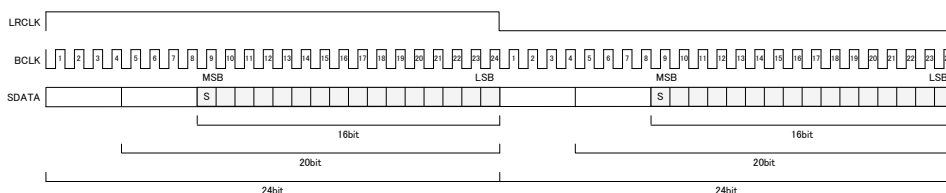
Left-justified data format



Right-justified data format

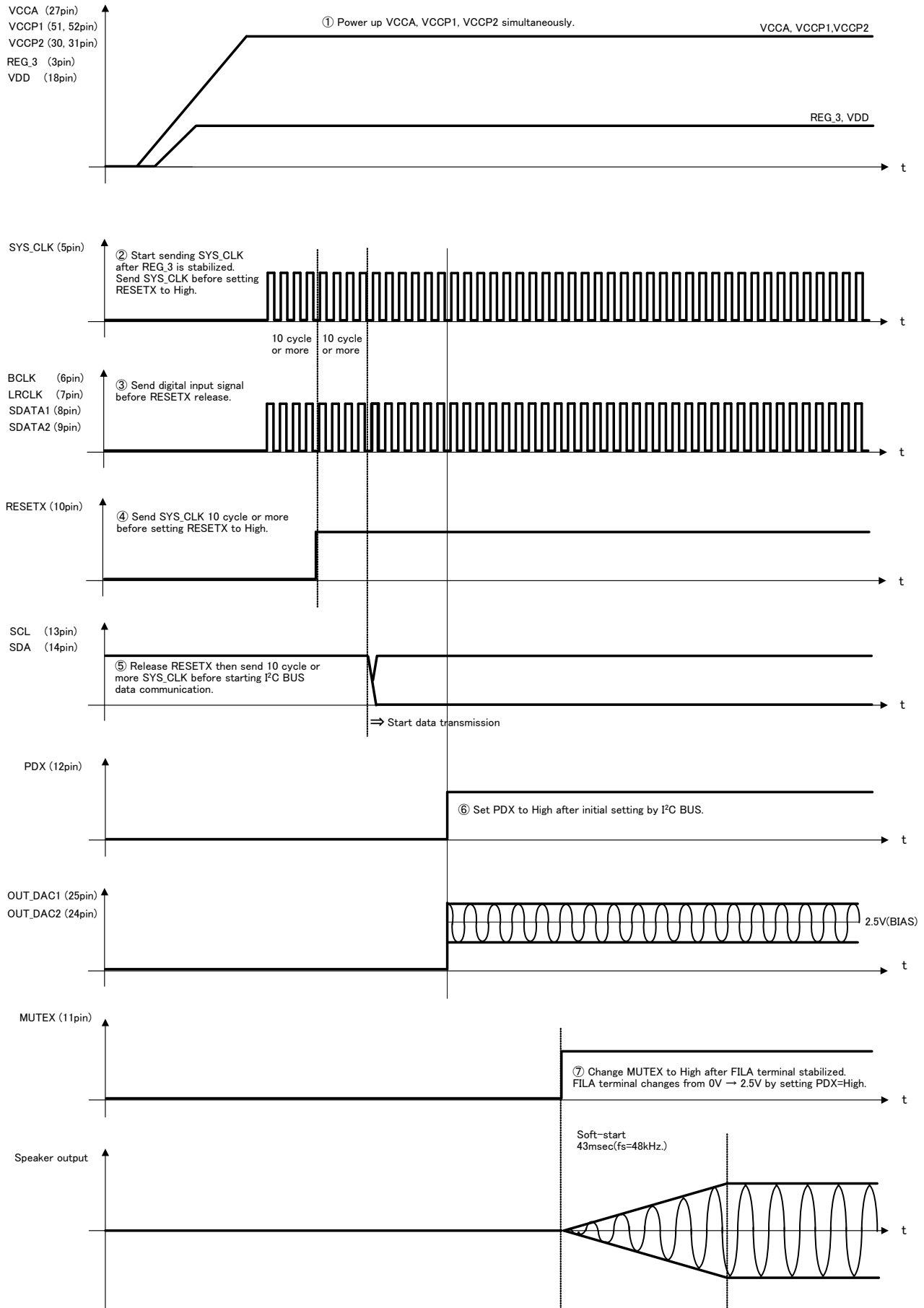


Right-justified data format (48fs)

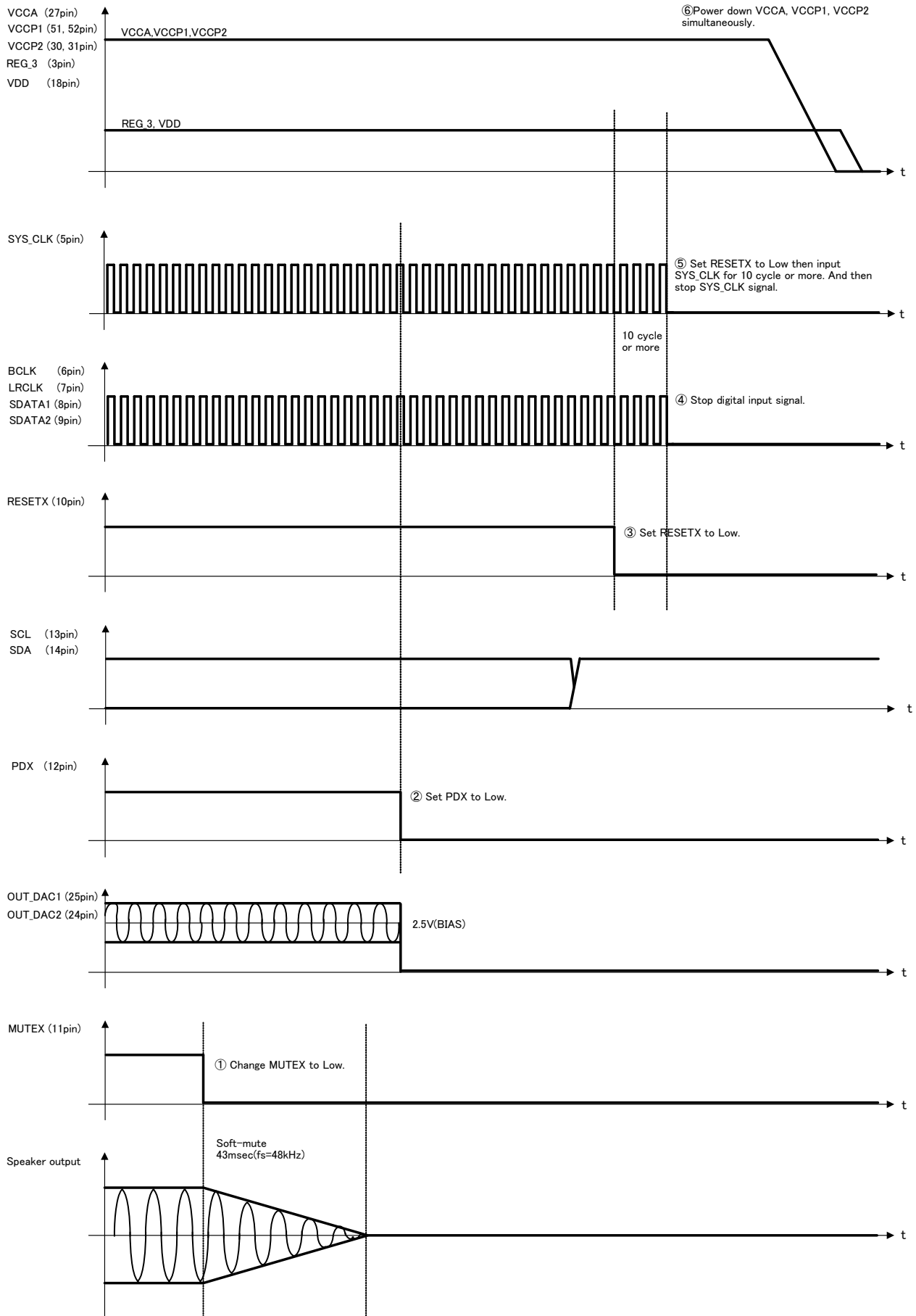




## ●Power supply start-up sequence



# ●Power supply shut-down sequence



●About the protection function

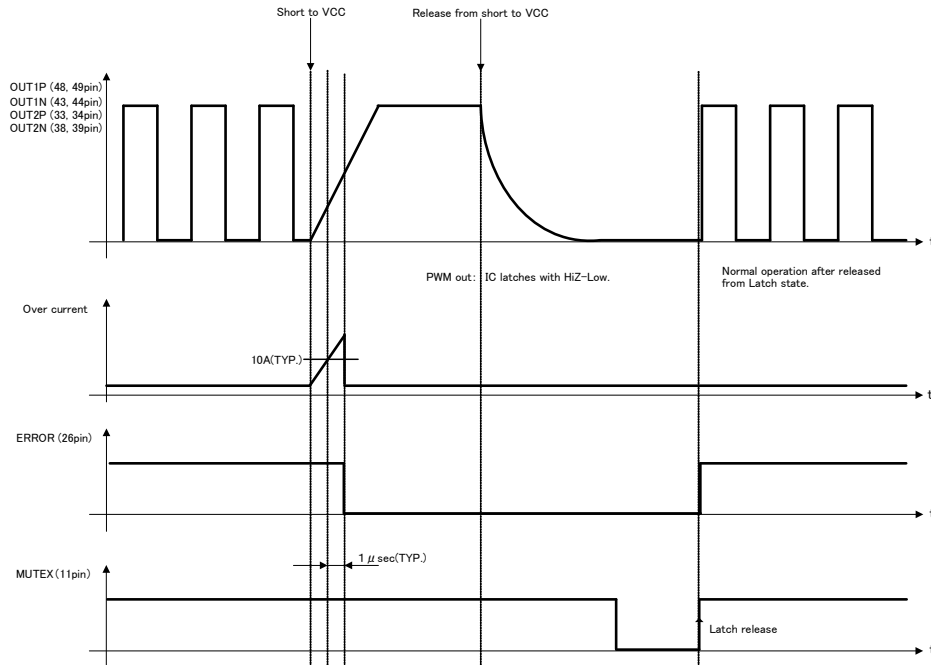
| Protection function                  | Detecting & Releasing condition |                                                         | DAC Output       | PWM Output       | ERROR Output |
|--------------------------------------|---------------------------------|---------------------------------------------------------|------------------|------------------|--------------|
| Output short protection              | Detecting condition             | Detecting current = 10A (TYP.)                          | Normal operation | HiZ_Low (Latch)  | L (Latch)    |
| DC voltage protection in the speaker | Detecting condition             | PWM output Duty=0% or 100% 43msec(fs=48kHz) above fixed |                  | HiZ_Low (Latch)  | L (Latch)    |
| High temperature protection          | Detecting condition             | Chip temperature to be above 150°C (TYP.)               | Normal operation | HiZ_Low          | H            |
|                                      | Releasing condition             | Chip temperature to be below 120°C (TYP.)               |                  | Normal operation |              |
| Under voltage protection             | Detecting condition             | Power supply voltage to be below 8V (TYP.)              | Normal operation | HiZ_Low          | H            |
|                                      | Releasing condition             | Power supply voltage to be above 9V (TYP.)              |                  | Normal operation |              |
| Clock stop protection                | Detecting condition             | No change to SYS_CLK more than 1usec (TYP.)             | Irregular output | HiZ_Low          | H            |
|                                      | Releasing condition             | Input to SYS_CLK                                        | Normal operation | Normal operation |              |

### 1) Output short protection(Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After the MUTE pin is set Low once, the MUTE pin is set High again.  
②Turning on the power supply again.

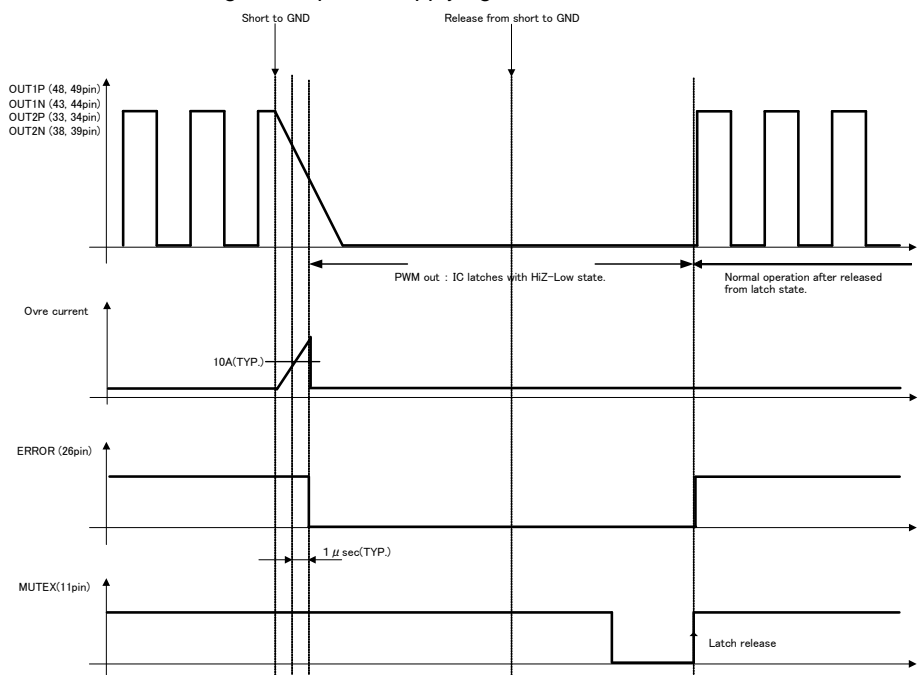


### 2) Output short protection(Short to GND)

BM5446EFV has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After the MUTE pin is set Low once, the MUTE pin is set High again.  
②Turning on the power supply again.



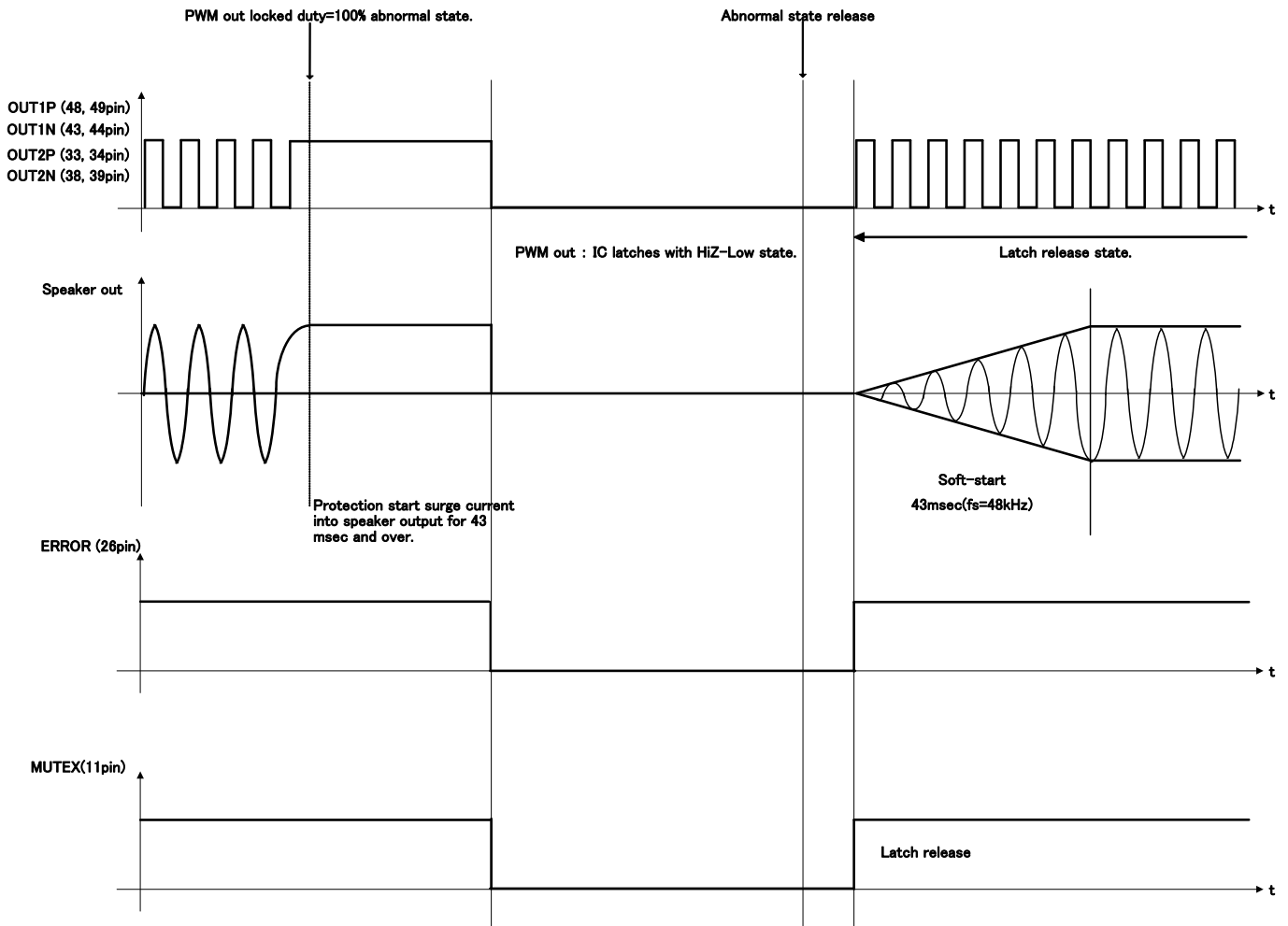
### 3) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTE pin is set High and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After the MUTE pin is set Low once, the MUTE pin is set High again.

②Turning on the power supply again

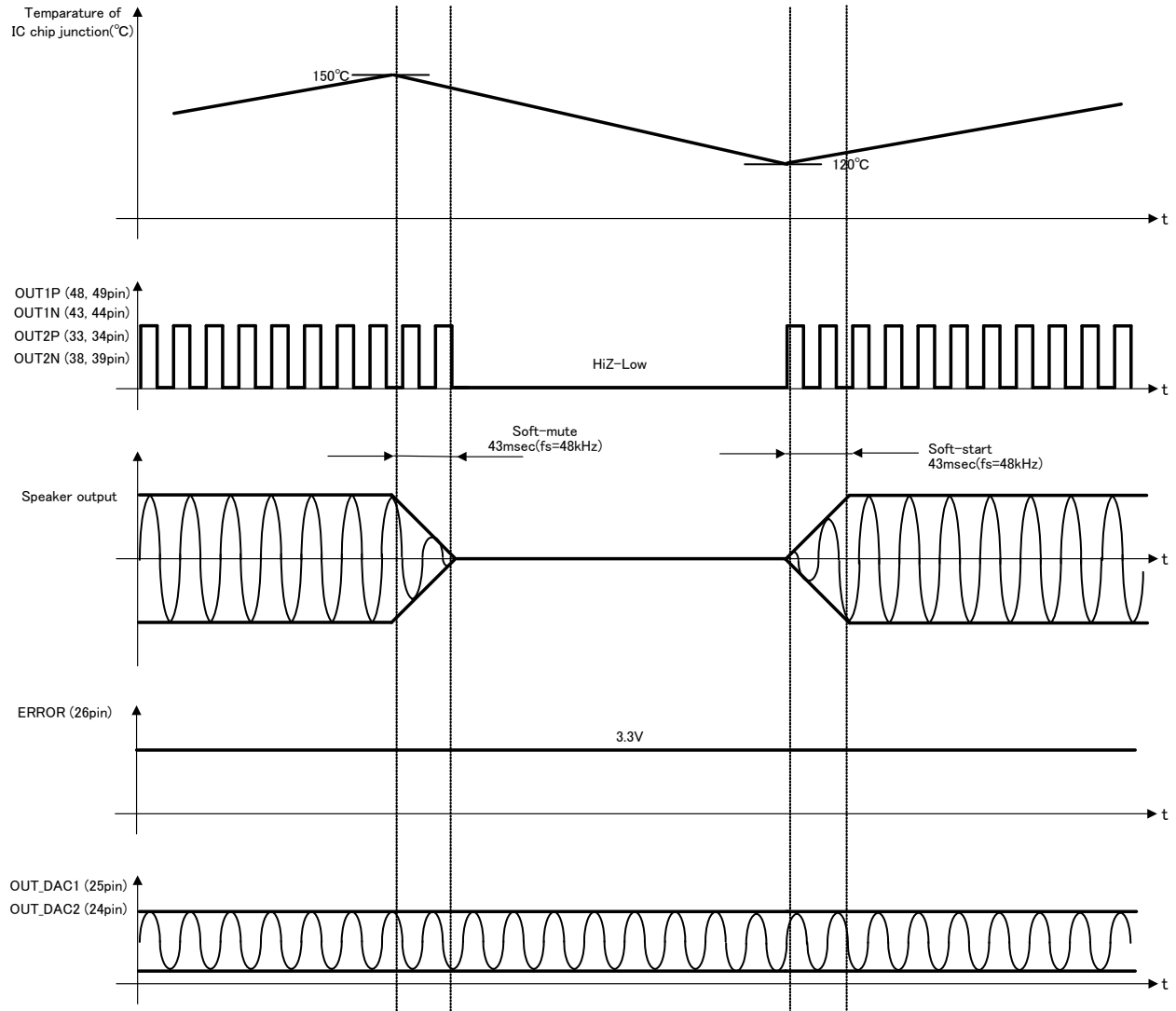


## 4) High temperature protection

BM5446EFV has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed  $T_{jmax}=150^{\circ}\text{C}$ .

Detecting condition - It will detect when MUTE pin is set High and the temperature of the chip becomes  $150^{\circ}\text{C}$ (TYP.) or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the temperature of the chip becomes  $120^{\circ}\text{C}$ (TYP.) or less. The speaker output is outputted through a soft-start when released.

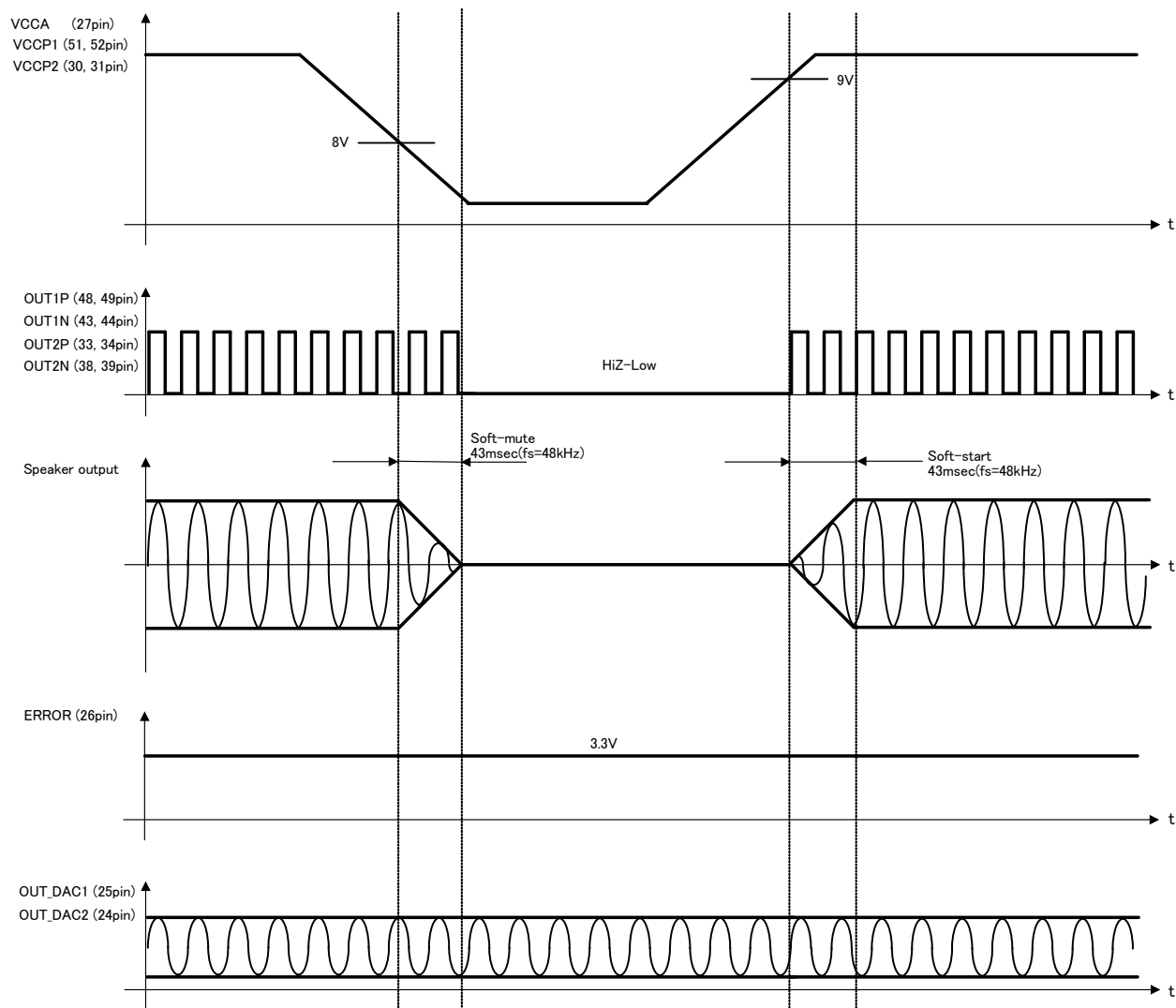


## 5) Under voltage protection

BM5446EFV has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTE pin is set High and the power supply voltage becomes lower than 8V.  
The speaker output is muted through a soft-mute when detected.

Releasing condition – It will release when MUTE pin is set High and the power supply voltage becomes more than 9V.  
The speaker output is outputted through a soft-start when released.

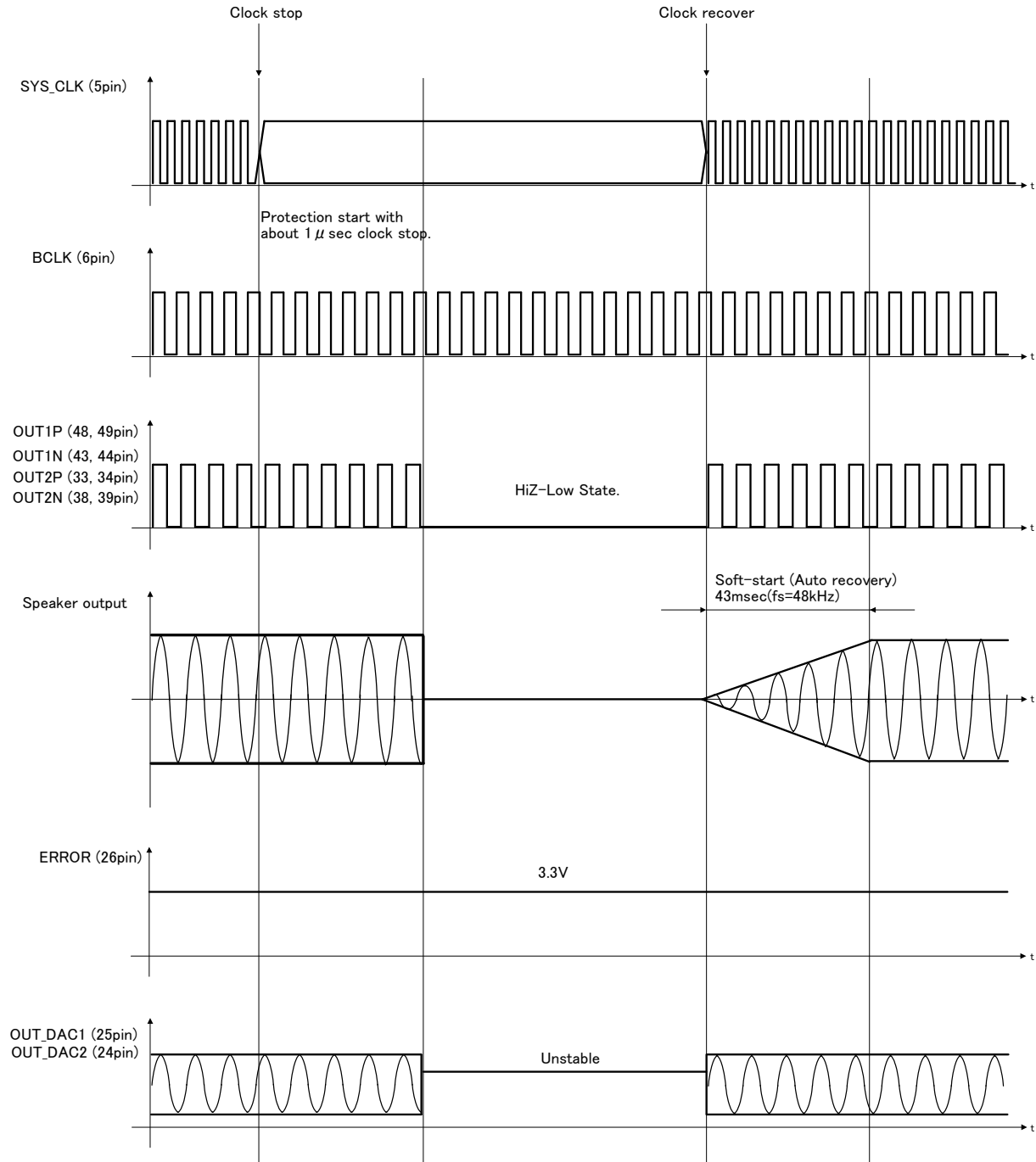


## 6) Clock stop protection

BM5446EFV has the clock stop protection circuit that make the speaker output mute when the SYS\_CLK signal of the digital audio input stops.

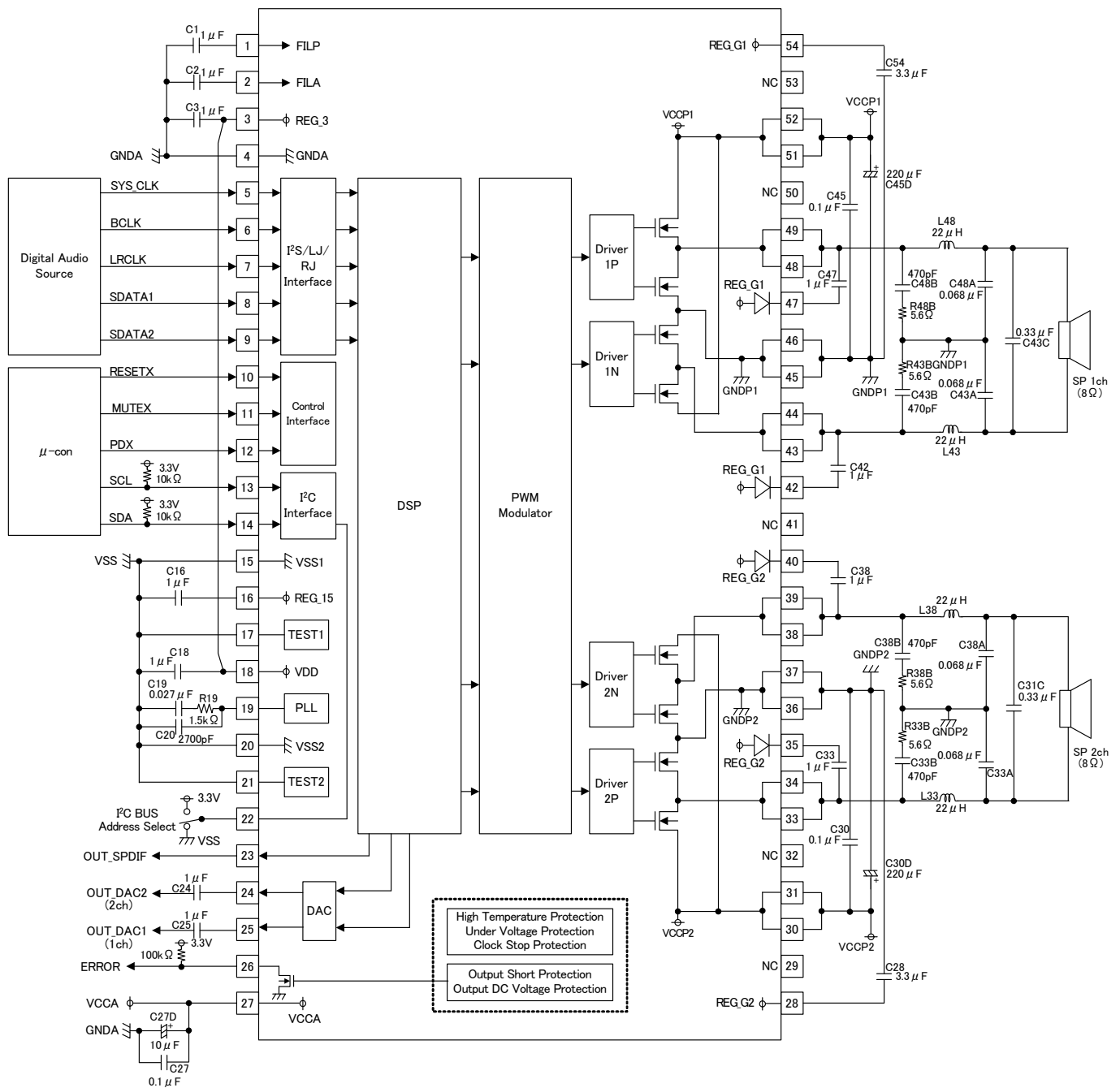
Detecting condition - It will detect when MUTE pin is set High and the SYS\_CLK signal doesn't change for about 1usec or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the SYS\_CLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.





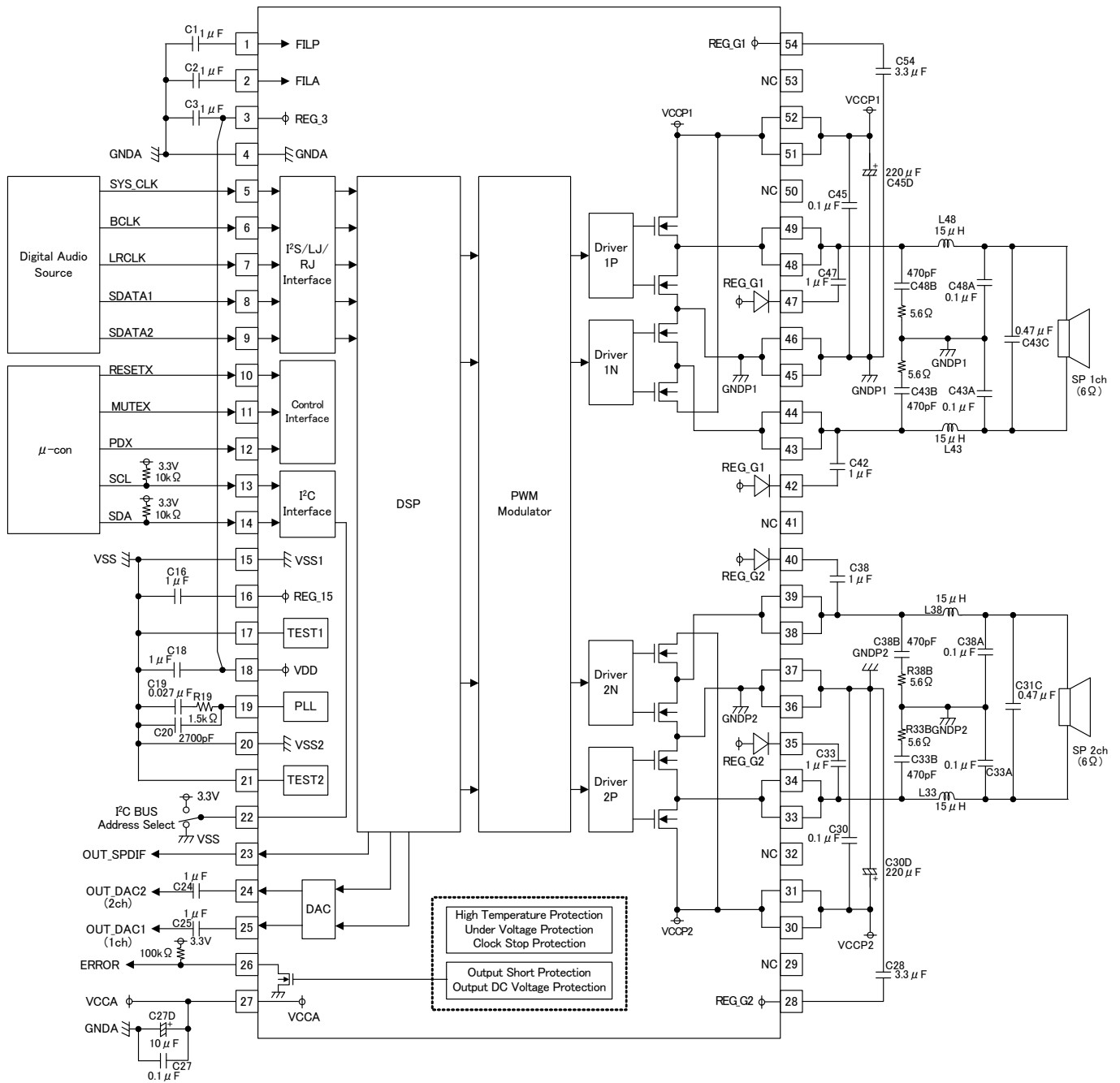
## ● Application Circuit Example (RL\_SP=8Ω)



## ●BOM list(RL\_SP =8Ω)

| Parts                  | Parts No.                        | Value   | Company   | Product No.       | Rated Voltage | Tolerance | Size         |
|------------------------|----------------------------------|---------|-----------|-------------------|---------------|-----------|--------------|
| IC                     | U1                               | -       | ROHM      | BM5446EFV         | -             | -         | 18.5mm×9.5mm |
| Inductor               | L33, L38, L43, L48               | 22μH    | TOKO      | 1168ER-0001       | -             | (±20%)    | 10.3mm×7.6mm |
|                        |                                  |         | SAGAMI    | DBE7210H-220M     | -             | (±20%)    | 10.5mm×6.4mm |
| Resistor               | R33B, R38B<br>R43B, R48B         | 5.6Ω    | ROHM      | MCR18PZHFL5R60    | 1/4W          | F(±1%)    | 3.2mm×1.6mm  |
|                        | R19                              | 1.5kΩ   |           | MCR01MZPF1501     | -             | -         | 1.0mm×0.5mm  |
| Capacitor              | C33, C38, C42, C47               | 1μF     | MURATA    | GRM185B31C105KE43 | 16V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C27, C30, C45                    | 0.1μF   |           | GRM188B31H104KA92 | 50V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C33A, C38A<br>C43A, C48A         | 0.068μF |           | GRM21BB11H683KA01 | 50V           | B(±10%)   | 2.0mm×1.25mm |
|                        | C31C, C43C                       | 0.33μF  |           | GRM219B31H334KA87 | 50V           | B(±10%)   | 2.0mm×1.25mm |
|                        | C28, C54                         | 3.3μF   |           | GRM188B31A335KE15 | 10V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C1, C2, C3<br>C16, C18, C25, C24 | 1μF     |           | GRM185B30J105KE25 | 6.3V          | B(±10%)   | 1.6mm×0.8mm  |
|                        | C33B, C38B<br>C43B, C48B         | 470pF   |           | GRM188B11H471KA   | 50V           | B(±10%)   | 2.0mm×1.2mm  |
|                        | C19                              | 0.027μF |           | GRM188B11C273KA01 | 16V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C20                              | 2700pF  |           | GRM188B11E272KA01 | 25V           | B(±10%)   | 1.6mm×0.8mm  |
|                        |                                  |         |           |                   |               |           |              |
| Electrolytic Capacitor | C30D, C45D                       | 220μF   | Panasonic | ECA1VMH221        | 35V           | ±20%      | φ8mm×11.5mm  |
|                        | C27D                             | 10μF    |           | EEUFC1H100L       | 50V           | ±20%      | φ5mm×11mm    |

● Application Circuit Example (RL\_SP = 6Ω)



## ●BOM list(RL\_SP =6Ω)

| Parts                  | Parts No.                                | Value   | Company   | Product No.       | Rated Voltage | Tolerance | Size         |
|------------------------|------------------------------------------|---------|-----------|-------------------|---------------|-----------|--------------|
| IC                     | U1                                       | —       | ROHM      | BM5446EFV         | —             | —         | 18.5mm×9.5mm |
| Inductor               | L33, L38, L43, L48                       | 15μH    | SAGAMI    | DBE7210H-150M     | —             | (±20%)    | 10.5mm×6.4mm |
| Resistor               | R33B, R38B<br>R43B, R48B                 | 5.6Ω    | ROHM      | MCR18PZHFL5R60    | 1/4W          | F(±1%)    | 3.2mm×1.6mm  |
|                        | R19                                      | 1.5kΩ   |           | MCR01MZPF1501     |               |           | 1.0mm×0.5mm  |
| Capacitor              | C33, C38, C42, C47                       | 1μF     | MURATA    | GRM185B31C105KE43 | 16V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C27, C30, C45, C33A,<br>C38A, C43A, C48A | 0.1μF   |           | GRM188B31H104KA92 | 50V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C31C, C43C                               | 0.47μF  |           | GRM21BB31H474KA87 | 50V           | B(±10%)   | 2.0mm×1.2mm  |
|                        | C28, C54                                 | 3.3μF   |           | GRM188B31A335KE15 | 10V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C1, C2, C3<br>C16, C18, C25, C24         | 1μF     |           | GRM185B30J105KE25 | 6.3V          | B(±10%)   | 1.6mm×0.8mm  |
|                        | C33B, C38B<br>C43B, C48B                 | 470pF   |           | GRM188B11H471KA   | 50V           | B(±10%)   | 2.0mm×1.2mm  |
|                        | C19                                      | 0.027μF |           | GRM188B11C273KA01 | 16V           | B(±10%)   | 1.6mm×0.8mm  |
|                        | C20                                      | 2700pF  |           | GRM188B11E272KA01 | 25V           | B(±10%)   | 1.6mm×0.8mm  |
| Electrolytic Capacitor | C30D, C45D                               | 220μF   | Panasonic | ECA1VMH221        | 35V           | ±20%      | φ8mm×11.5mm  |
|                        | C27D                                     | 10μF    |           | EEUFC1H100L       | 50V           | ±20%      | φ5mm×11mm    |

### ●Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 200kHz to 400kHz in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown in Fig.12, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker  $R_L$ . This filter reduces unwanted emission this way. In addition, coil L and capacitor  $C_g$  compose a filter against in-phase components, reducing unwanted emission further.

Filter constants depend on load impedances. The following are formulas to calculate values of  $L$ ,  $C$ , and  $C_g$  when  $Q=0.707$  is specified.

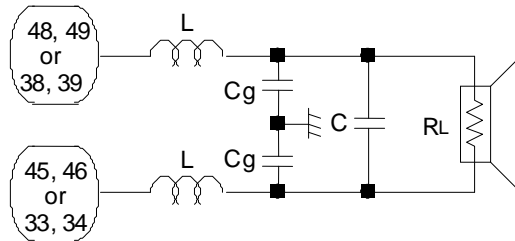


Fig. 12

$$L = \frac{R_L \sqrt{2}}{4 \pi f_C} \text{ (H)}$$

$$C = \frac{1}{2 \pi f_C R_L \sqrt{2}} \text{ (F)}$$

$$C_g = 0.2 C \text{ (F)}$$

$R_L$  : Load impedance ( $\Omega$ )  
 $f_C$  : LPF cut off frequency (Hz)

Following presents output LC filter constants with typical load impedances.

| $f_C = 30\text{kHz}$ |                  |                    |                     | $f_C = 40\text{kHz}$ |                  |                    |                     |
|----------------------|------------------|--------------------|---------------------|----------------------|------------------|--------------------|---------------------|
| $R_L$                | L                | C                  | $C_g$               | $R_L$                | L                | C                  | $C_g$               |
| 6 $\Omega$           | 22 $\mu\text{H}$ | 0.68 $\mu\text{F}$ | 0.15 $\mu\text{F}$  | 6 $\Omega$           | 15 $\mu\text{H}$ | 0.47 $\mu\text{F}$ | 0.1 $\mu\text{F}$   |
| 8 $\Omega$           | 33 $\mu\text{H}$ | 0.47 $\mu\text{F}$ | 0.1 $\mu\text{F}$   | 8 $\Omega$           | 22 $\mu\text{H}$ | 0.33 $\mu\text{F}$ | 0.068 $\mu\text{F}$ |
| 16 $\Omega$          | 68 $\mu\text{H}$ | 0.22 $\mu\text{F}$ | 0.047 $\mu\text{F}$ | 16 $\Omega$          | 47 $\mu\text{H}$ | 0.15 $\mu\text{F}$ | 0.033 $\mu\text{F}$ |

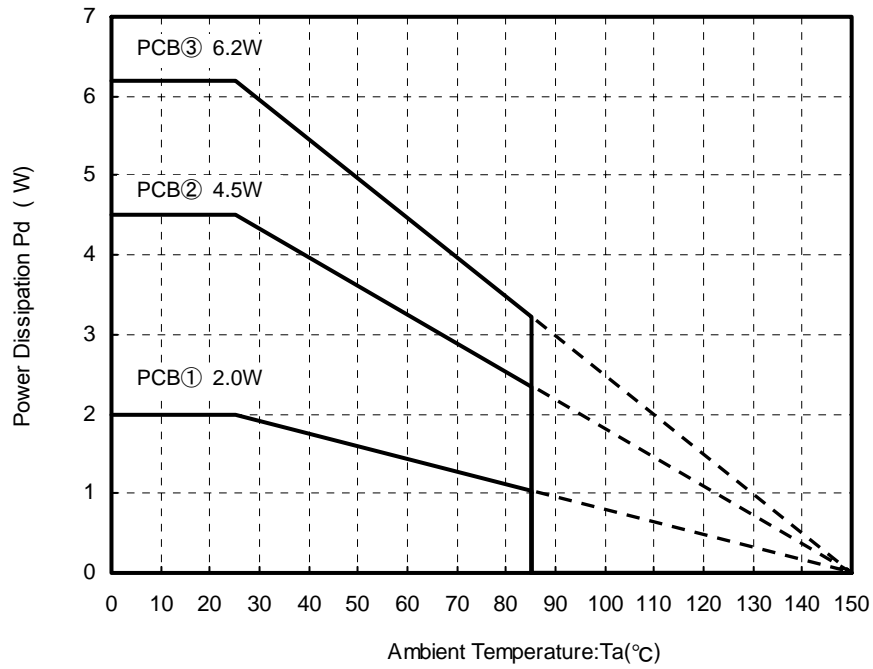
Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

# ●Notes for use

- 1) Absolute maximum ratings  
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) Power supply lines  
As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as a electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.
- 3) GND potential (Pin 4, 36, 37, 45, 46), VSS potential (Pin 15, 20)  
Any state must become the lowest voltage about GND terminal and VSS terminal.
- 4) Input terminal  
The parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND and VSS. Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed.
- 5) Setting of heat  
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.  
Class D speaker amplifier is high efficiency and low heat generation by comparison with conventional Analog power amplifier. However, In case it is operated continuously by maximum output power, Power dissipation (Pdiss) may exceed package dissipation. Please consider about heat design that Power dissipation (Pdiss) does not exceed Package dissipation (Pd) in average power (Poav). (Tjmax : Maximum junction temperature=150 °C, Ta : Peripheral temperature[°C], θja : Thermal resistance of package[°C/W], Poav : Average power[W], η : Efficiency)  
Package dissipation :  $P_d(W) = (T_{jmax} - T_a) / \theta_{ja}$   
Power dissipation :  $P_{diss}(W) = Poav \times (1 / \eta - 1)$
- 6) Actions in strong magnetic field  
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.
- 7) Thermal shutdown circuit  
This product is provided with a built-in thermal shutdown circuit. When the thermal shutdown circuit operates, the output transistors are placed under open status. The thermal shutdown circuit is primarily intended to shut down the IC avoiding thermal runaway under abnormal conditions with a chip temperature exceeding Tjmax = 150°C.
- 8) Shorts between pins and misinstallation  
When mounting the IC on a board, pay adequate attention to orientation and placement discrepancies of the IC. If it is misinstalled and the power is turned on, the IC may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the IC or between a pin and a power supply or a pin and a GND.
- 9) Power supply on/off (Pin 27, 30, 31, 51, 52)  
In case power supply is started up, RESETX(Pin 10), MUTEX(Pin 11) and PDX (Pin 12) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.
- 10) ERROR terminal(Pin 26)  
A error flag is outputted when Output short protection and DC voltage protection in the speaker are operated. These flags are the function which the condition of this product is shown in.
- 11) N.C. terminal (Pin 29, 32, 41, 50, 53)  
N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.
- 12) TEST terminal (Pin 17, 21)  
TEST terminal connects with ground to prevent the malfunction by external noise.
- 13) Precautions for Speaker-setting  
If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

# ● Allowable Power Dissipation



Measuring instrument: TH-156(Shibukawa Kuwano Electrical Instruments Co., Ltd.)

Measuring conditions: Installation on ROHM's board

Board size: 70mm×70mm×1.6mm(with thermal via on board)

Material: FR4

• The board on exposed heat sink on the back of package are connected by soldering.

PCB① : 1-layer board(back copper foil size: 0mm×0mm),  $\theta_{ja}=62.5^\circ\text{C/W}$

PCB② : 2-layer board(back copper foil size: 70mm×70mm),  $\theta_{ja}=27.8^\circ\text{C/W}$

PCB③ : 4-layer board(back copper foil size: 70mm×70mm),  $\theta_{ja}=20.2^\circ\text{C/W}$

●Ordering part number

|   |   |
|---|---|
| B | M |
|---|---|

Part No.

|   |   |   |   |
|---|---|---|---|
| 5 | 4 | 4 | 6 |
|---|---|---|---|

Part No.

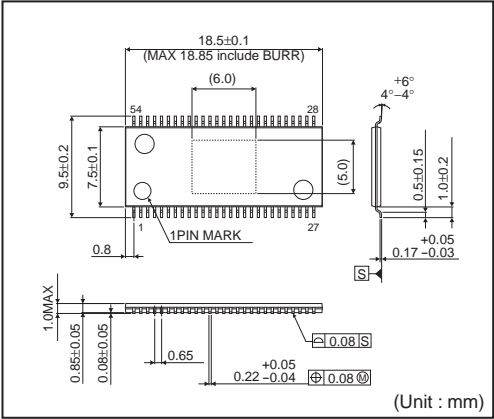
|   |   |   |
|---|---|---|
| E | F | V |
|---|---|---|

Package  
EFV : HTSSOP-B54

|   |   |
|---|---|
| E | 2 |
|---|---|

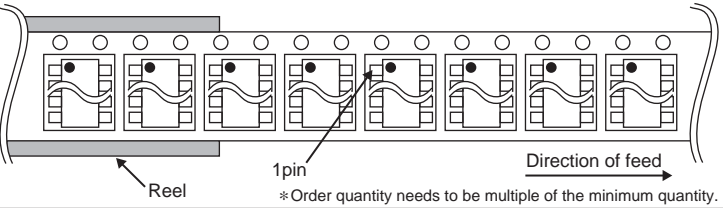
Packaging and forming specification  
E2: Embossed tape and reel

HTSSOP-B54



<Tape and Reel information>

|                   |                                                                                                                                                     |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| Tape              | Embossed carrier tape (with dry pack)                                                                                                               |
| Quantity          | 1500pcs                                                                                                                                             |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |





# Notice

## Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment <sup>(Note 1)</sup>, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
  - Installation of protection circuits or other protective devices to improve system safety
  - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
  - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
  - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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