2.7 V to 5.25 V, Micropower, 2-Channel, 125 kSPS, 12-Bit ADC in 8-Lead MSOP

Data Sheet **AD7887**

FEATURES

- **Specified for V_{DD} of 2.7 V to 5.25 V**
- **Flexible power/throughput rate management**
- **Shutdown mode: 1 µA max**
- **One or two single-ended inputs**
- **Serial interface: SPI®/QSPI™/MICROWIRE™/DSP compatible**
- **8-lead narrow SOIC and MSOP packages**
- **Qualified for automotive applications**

APPLICATIONS

- **Battery-powered systems (personal digital assistants, medical instruments, mobile communications)**
- **Instrumentation and control systems**
- **High speed modems**

FUNCTIONAL BLOCK DIAGRAM

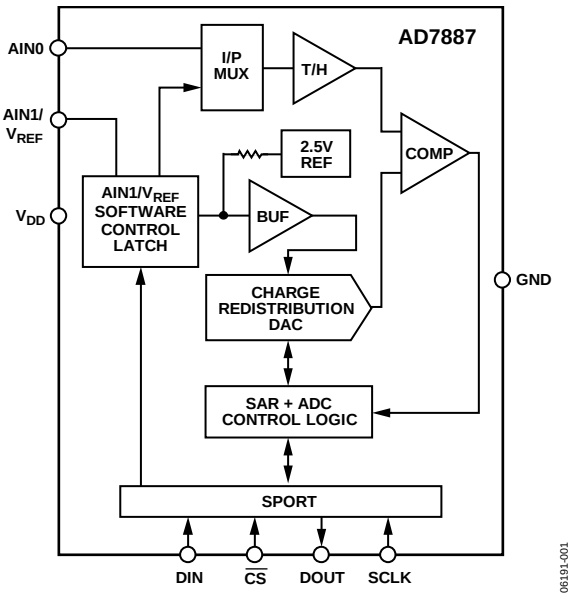

Figure 1.

GENERAL DESCRIPTION

The AD7887 is a high speed, low power, 12-bit analog-to-digital converter (ADC) that operates from a single 2.7 V to 5.25 V power supply. The AD7887 is capable of 125 kSPS throughput rate. The input track-and-hold acquires a signal in 500 ns and features a single-ended sampling scheme. The output coding for the AD7887 is straight binary, and the part is capable of converting full power signals of up to 2.5 MHz.

The AD7887 can be configured for either dual- or single-channel operation via the on-chip control register. There is a default single-channel mode that allows the AD7887 to be operated as a read-only ADC. In single-channel operation, there is one analog input (AIN0) and the AIN1/V_{REF} pin assumes its V_{REF} function. This V_{REF} pin allows the user access to the part's internal 2.5 V reference, or the V_{REF} pin can be overdriven by an external reference to provide the reference voltage for the part. This external reference voltage has a range of 2.5 V to V_{DD}. The analog input range on AIN0 is 0 to V_{REF}.

In dual-channel operation, the AIN1/V_{REF} pin assumes its AIN1 function, providing a second analog input channel. In this case, the reference voltage for the part is provided via the V_{DD} pin. As a result, the input voltage range on both the AIN0 and AIN1 inputs is 0 to V_{DD}.

CMOS construction ensures low power dissipation of typically 2 mW for normal operation and 3 µW in power-down mode. The part is available in an 8-lead, 0.15-inch-wide narrow body SOIC and an 8-lead MSOP package.

PRODUCT HIGHLIGHTS

1. Smallest 12-bit dual-/single-channel ADC; 8-lead MSOP package.
2. Lowest power 12-bit dual-/single-channel ADC.
3. Flexible power management options, including automatic power-down after conversion.
4. Read-only ADC capability.
5. Analog input range from 0 V to V_{REF}.
6. Versatile serial input/output port (SPI/QSPI/MICROWIRE/DSP compatible).

Rev. E Document Feedback

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SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V, external/internal reference unless otherwise noted, f_{SCLK} = 2 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio (SNR)[2, 3]	71	71	dB typ	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 125 kSPS
Total Harmonic Distortion (THD)[2]	−80	−80	dB typ	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 125 kSPS
Peak Harmonic or Spurious Noise[2]	−80	−80	dB typ	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 125 kSPS
Intermodulation Distortion (IMD)[2]				
Second-Order Terms	−80	−80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 125 kSPS
Third-Order Terms	−80	−80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 125 kSPS
Channel-to-Channel Isolation[2]	−80	−80	dB typ	f_{IN} = 25 kHz
Full-Power Bandwidth	2.5	2.5	MHz typ	@ 3 dB
DC ACCURACY				Any channel
Resolution	12	12	Bits	
Integral Nonlinearity[2]	±2	±1	LSB max	
Differential Nonlinearity[2]	±2	±1	LSB max	Guaranteed no missing codes to 11 bits (A Grade)
Offset Error[2]	±3	±3	LSB max	V_{DD} = 5 V, dual-channel mode
	±4	±4	LSB max	V_{DD} = 3 V, dual-channel mode
	±6	±6	LSB typ	Single-channel mode
Offset Error Match[2]	0.5	0.5	LSB max	
Gain Error[2]	±2	±2	LSB max	Dual-channel mode
	±1	±1	LSB max	Single-channel mode, external reference
	±6	±6	LSB typ	Single-channel mode, internal reference
Gain Error Match[2]	2	2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	
Leakage Current	±5	±5	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	10	10	kΩ typ	Very high impedance if internal reference disabled
REF_{OUT} Output Voltage	2.45/2.55	2.45/2.55	V min/max	
REF_{OUT} Temperature Coefficient	±50	±50	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 4.75 V to 5.25 V
	2.1	2.1	V min	V_{DD} = 2.7 V to 3.6 V
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 2.7 V to 5.25 V
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}				I_{SOURCE} = 200 µA
	V_{DD} − 0.5	V_{DD} − 0.5	V min	V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	±1	µA max	
Floating-State Output Capacitance[5]	10	10	pF max	
Output Coding	Straight (Natural) Binary			

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
CONVERSION RATE				
Throughput Time	16	16	SCLK cycles	Conversion time plus acquisition time is 125 kSPS, with 2 MHz Clock
Track/Hold Acquisition Time[2]	1.5	1.5	SCLK cycles	
Conversion Time	14.5	14.5	SCLK cycles	7.25 µs (2 MHz Clock)
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}				
Normal Mode[5] (Mode 2)				
Static	700	700	µA max	
Operational (f_{SAMPLE} = 125 kSPS)	850	850	µA typ	Internal reference enabled
	700	700	µA typ	Internal reference disabled
Using Standby Mode (Mode 4)	450	450	µA typ	f_{SAMPLE} = 50 kSPS
Using Shutdown Mode (Modes 1, 3)	120	120	µA typ	f_{SAMPLE} = 10 kSPS
	12	12	µA typ	f_{SAMPLE} = 1 kSPS
Standby Mode[6]	210	210	µA max	V_{DD} = 2.7 V to 5.25 V
Shutdown Mode[6]	1	1	µA max	V_{DD} = 2.7 V to 3.6 V
	2	2	µA max	V_{DD} = 4.75 V to 5.25 V
Normal Mode Power Dissipation	3.5	3.5	mW max	V_{DD} = 5 V
	2.1	2.1	mW max	V_{DD} = 3 V
Shutdown Power Dissipation	5	5	µW max	V_{DD} = 5 V
	3	3	µW max	V_{DD} = 3 V
Standby Power Dissipation	1.05	1.05	mW max	V_{DD} = 5 V
	630	630	µW max	V_{DD} = 3 V

[1] Temperature range for A and B versions is −40°C to +125°C.
[2] See the Terminology section.
[3] SNR calculation includes distortion and noise components.
[4] Sample tested at +25°C to ensure compliance.
[5] All digital inputs at GND except $\overline{CS}$ at V_{DD}. No load on the digital outputs. Analog inputs at GND.
[6] SCLK at GND when SCLK off. All digital inputs at GND except for $\overline{CS}$ at V_{DD}. No load on the digital outputs. Analog inputs at GND.

TIMING SPECIFICATIONS[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions)		Unit	Description
	4.75 V to 5.25 V	2.7 V to 3.6 V		
f_{SCLK}[2]	2	2	MHz max	
$t_{CONVERT}$	14.5 × t_{SCLK}	14.5 × t_{SCLK}		
t_{ACQ}	1.5 × t_{SCLK}	1.5 × t_{SCLK}		Throughput time = $t_{CONVERT}$ + t_{ACQ} = 16 t_{SCLK}
t_1	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_2[3]	30	60	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_3[3]	75	100	ns max	Data access time after SCLK falling edge
t_4	20	20	ns min	Data setup time prior to SCLK rising edge
t_5	20	20	ns min	Data valid to SCLK hold time
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_8[4]	80	80	ns max	$\overline{CS}$ rising edge to DOUT high impedance
t_9	5	5	µs typ	Power-up time from shutdown

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

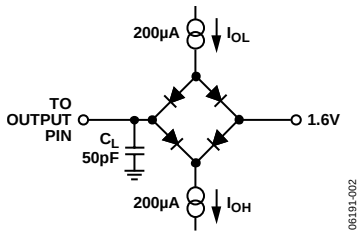


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
Analog Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial Temperature Range	
A, B Versions	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
SOIC or MSOP Package Power Dissipation	450 mW
θ_{JA} Thermal Impedance	157°C/W (SOIC)
	205.9°C/W (MSOP)
θ_{JC} Thermal Impedance	56°C/W (SOIC)
	43.74°C/W (MSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Pb-Free Temperature, Soldering Reflow	260(0)°C
ESD	4 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

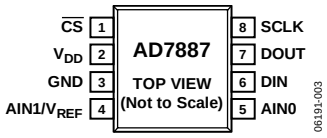


Figure 3. SOIC_N Pin Configuration

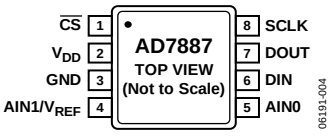


Figure 4. MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7887 and also frames the serial data transfer. When the AD7887 operates in its default mode, the $\overline{CS}$ pin also acts as the shutdown pin such that with the $\overline{CS}$ pin high, the AD7887 is in its power-down mode.
2	V_{DD}	Power Supply Input. The V_{DD} range for the AD7887 is from 2.7 V to 5.25 V. When the AD7887 is configured for two-channel operation, this pin also provides the reference source for the part.
3	GND	Ground Pin. This pin is the ground reference point for all circuitry on the AD7887. In systems with separate AGND and DGND planes, these planes should be tied together as close as possible to this GND pin. Where this is not possible, this GND pin should connect to the AGND plane.
4	AIN1/V_{REF}	Analog Input 1/Voltage Reference Input. In single-channel mode, this pin becomes the reference input/output. In this case, the user can either access the internal 2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally applied reference is 1.2 V to V_{DD}. In two-channel mode, this pin provides the second analog input channel, AIN1. The input voltage range on AIN1 is 0 to V_{DD}.
5	AIN0	Analog Input 0. In single-channel mode, this is the analog input and the input voltage range is 0 to V_{REF}. In dual-channel mode, it has an analog input range of 0 to V_{DD}.
6	DIN	Data In. Logic Input. Data to be written to the AD7887's control register is provided on this input and clocked into the register on the rising edge of SCLK (see the Control Register section). The AD7887 can be operated as a single-channel, read-only ADC by tying the DIN line permanently to GND.
7	DOUT	Data Out. Logic output. The conversion result from the AD7887 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data, which is provided MSB first.
8	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part and writing serial data to the control register. This clock input is also used as the clock source for the AD7887's conversion process.

TYPICAL PERFORMANCE CHARACTERISTICS

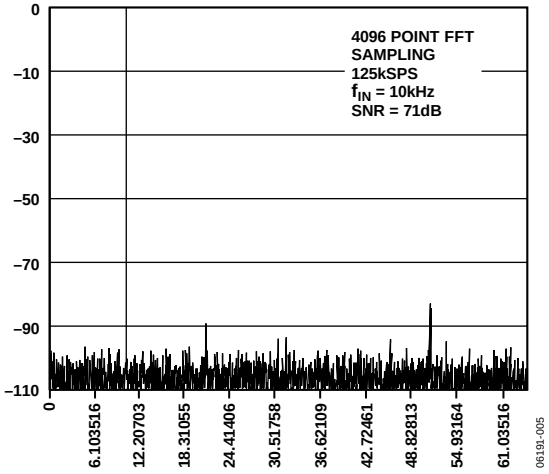


Figure 5. Dynamic Performance

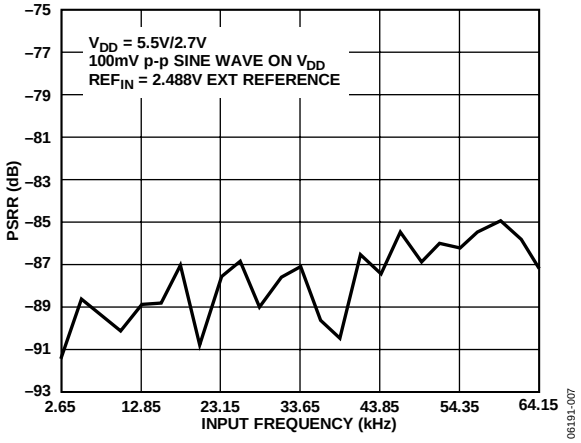


Figure 7. PSRR vs. Frequency

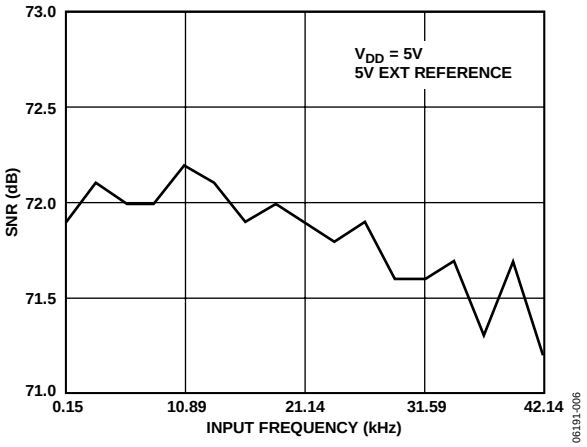


Figure 6. SNR vs. Input Frequency

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (that is, V_{REF} − 1.5 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Track/Hold Acquisition Time
The track/hold amplifier returns to track mode at the end of conversion. Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of a conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7887, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic could be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7887 is tested using the CCIF standard in which two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 25 kHz sine wave signal to the nonselected input channel and determining how much that signal is attenuated in the selected channel. The figure given is the worst case across both channels for the AD7887.

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition, but not the converter's linearity. PSR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value. See Figure 7.

PSRR is defined as the ratio of the power in the ADC output at frequency f to the power of a full-scale sine wave applied to the ADC of frequency f_S:

$$PSRR\ (\text{dB}) = 10 \log(Pf/Pfs)$$

where *Pf* is the power at frequency f in ADC output and *Pfs* is the power at frequency f_S in ADC full-scale input.

CONTROL REGISTER

The control register on the AD7887 is an 8-bit, write-only register. Data is loaded from the DIN pin of the AD7887 on the rising edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. This requires 16 serial clocks for every data transfer. Only the information provided on the first eight rising clock edges after $\overline{CS}$ falling edge is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 5. The contents of the control register on power up is all 0s.

MSB

DONTC	ZERO	REF	SIN/DUAL	CH	ZERO	PM1	PM0

Table 5. Control Register

Bit	Mnemonic	Comment
7	DONTC	Don't Care. The value written to this bit of the control register is a don't care, that is, it doesn't matter if the bit is 0 or 1.
6	ZERO	A zero must be written to this bit to ensure correct operation of the AD7887.
5	REF	Reference Bit. With a 0 in this bit, the on-chip reference is enabled. With a 1 in this bit, the on-chip reference is disabled.
4	SIN/DUAL	Single/Dual Bit. This bit determines whether the AD7887 operates in single-channel or dual-channel mode. A 0 in this bit selects single-channel operation and the AIN1/V_{REF} pin assumes its V_{REF} function. A 1 in this bit selects dual-channel mode, with the reference voltage for the ADC internally connected to V_{DD} and the AIN1/V_{REF} pin assuming its AIN1 function as the second analog input channel. To obtain best performance from the AD7887, the internal reference should be disabled when operating in the dual-channel mode, that is, REF = 1.
3	CH	Channel Bit. When the part is selected for dual-channel mode, this bit determines which channel is converted for the next conversion. A 0 in this bit selects the AIN0 input, and a 1 in this bit selects the AIN1 input. In single-channel mode, this bit should always be 0.
2	ZERO	A 0 must be written to this bit to ensure correct operation of the AD7887.
1, 0	PM1, PM0	Power Management Bits. These two bits decode the mode of operation of the AD7887 as described in Table 6.

Table 6. Power Management Options

PM1	PM0	Mode
0	0	Mode 1. In this mode, the AD7887 enters shutdown if the $\overline{CS}$ input is 1 and is in full power mode when $\overline{CS}$ is 0. Thus the part comes out of shutdown on the falling edge of $\overline{CS}$ and enters shutdown on the rising edge of $\overline{CS}$.
0	1	Mode 2. In this mode, the AD7887 is always fully powered up, regardless of the status of any of the logic inputs.
1	0	Mode 3. In this mode, the AD7887 automatically enters shutdown mode at the end of each conversion, regardless of the state of $\overline{CS}$.
1	1	Mode 4. In this standby mode, portions of the AD7887 are powered down but the on-chip reference voltage remains powered up. This mode is similar to Mode 3, but allows the part to power up much faster. The REF bit should be 0 to ensure that the on-chip reference is enabled.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7887 is a fast, low power, 12-bit, single-supply, single-channel/dual-channel ADC. The part can be operated from a 3 V (2.7 V to 3.6 V) supply or from a 5 V (4.75 V to 5.25 V) supply. When operated from either a 5 V or 3 V supply, the AD7887 is capable of throughput rates of 125 kSPS when provided with a 2 MHz clock.

The AD7887 provides the user with an on-chip, track/hold analog-to-digital converter reference and a serial interface housed in an 8-lead package. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The part can be configured for single-channel or dual-channel operation. When configured as a single-channel part, the analog input range is 0 to V_{REF} (where the externally applied V_{REF} can be between 1.2 V and V_{DD}). When the AD7887 is configured for two input channels, the input range is determined by internal connections to be 0 to V_{DD}.

If single-channel operation is required, the AD7887 can be operated in a read-only mode by tying the DIN line permanently to GND. For applications where the user wants to change the mode of operation or wants to operate the AD7887 as a dual-channel ADC, the DIN line can be used to clock data into the part's control register.

CONVERTER OPERATION

The AD7887 is a successive approximation ADC built around a charge-redistribution DAC. Figure 8 and Figure 9 show simplified schematics of the ADC. Figure 8 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on AIN.

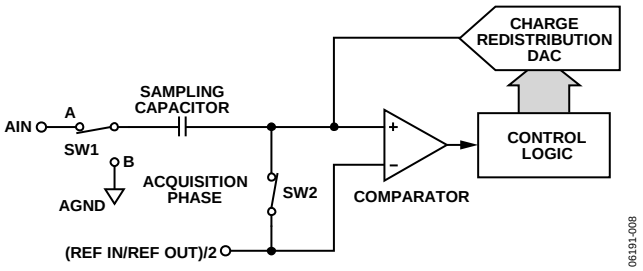


Figure 8. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 9), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge-redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 10 shows the ADC transfer function.

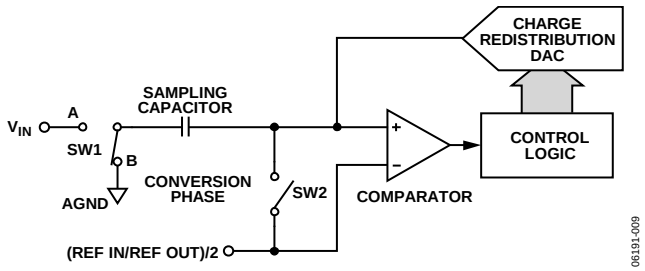


Figure 9. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7887 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is $V_{REF}/4096$. The ideal transfer characteristic for the AD7887 is shown in Figure 10.

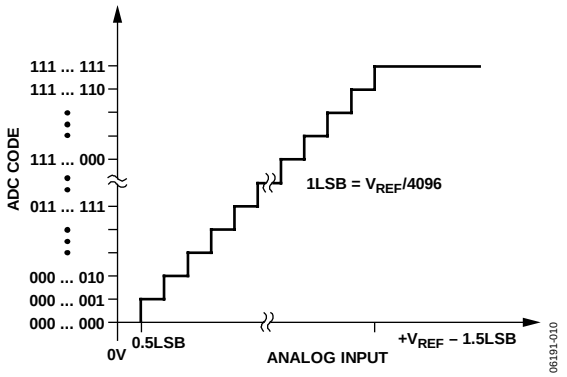


Figure 10. Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 11 shows a typical connection diagram for the AD7887. The GND pin is connected to the analog ground plane of the system. The part is in dual-channel mode so V_{REF} is internally connected to a well-decoupled V_{DD} pin to provide an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. For applications where power consumption is of concern, the automatic power-down at the end of conversion should be used to improve power performance. See the Modes of Operation section.

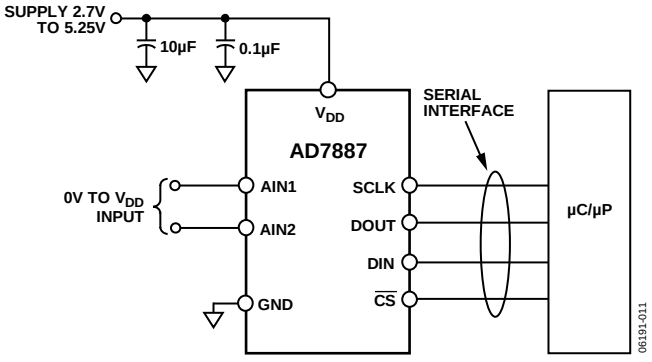


Figure 11. Typical Connection Diagram

ANALOG INPUT

Figure 12 shows an equivalent circuit of the analog input structure of the AD7887. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceed the supply rails by more than 200 mV. Exceeding this value causes the diodes to become forward biased and to start conducting into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 20 mA. However, it is worth noting that a small amount of current (1 mA) being conducted into the substrate due to an overvoltage on an unselected channel can cause inaccurate conversions on a selected channel. Capacitor C1 in Figure 12 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a multiplexer and a switch. This resistor is typically about 100 Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 20 pF.

Note that the analog input capacitance seen when in track mode is typically 38 pF, whereas in hold mode it is typically 4 pF.

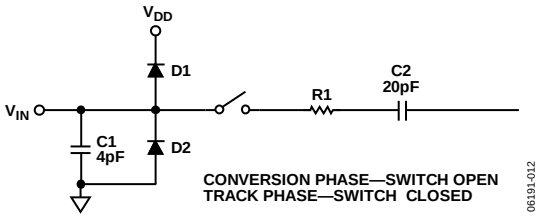


Figure 12. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 13 shows a graph of the total harmonic distortion vs. the analog input signal frequency for different source impedances.

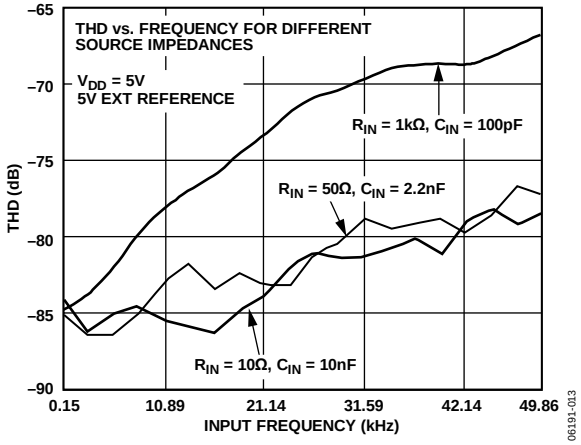


Figure 13. THD vs. Analog Input Frequency

On-Chip Reference

The AD7887 has an on-chip 2.5 V reference. This reference can be enabled or disabled by clearing or setting the REF bit in the control register, respectively. If the on-chip reference is to be used externally in a system, it must be buffered before it is applied elsewhere. If an external reference is applied to the device, the internal reference is automatically overdriven. However, it is advised to disable the internal reference by setting the REF bit in the control register when an external reference is applied in order to obtain optimum performance from the device. When the internal reference is disabled, SW1, shown in Figure 14, opens and the input impedance seen at the AIN1/V_{REF} pin is the input impedance of the reference buffer, which is in the region of gigaohms. When the internal reference is enabled, the input impedance seen at the pin is typically 10 kΩ. When the AD7887 is operated in two-channel mode, the reference is taken from V_{DD} internally, not from the on-chip 2.5 V reference.

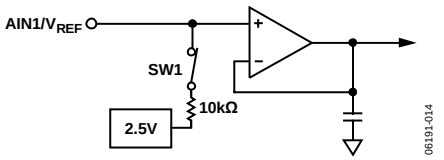


Figure 14. On-Chip Reference Circuitry

POWER-DOWN OPTIONS

The AD7887 provides flexible power management to allow the user to achieve the best power performance for a given throughput rate.

The power management options are selected by programming the power management bits (that is, PM1 and PM0) in the control register. Table 6 summarizes the available options. When the power management bits are programmed for either of the auto power-down modes, the part enters power-down mode on the 16th rising SCLK edge after the falling edge of $\overline{CS}$. The first falling SCLK edge after the $\overline{CS}$ falling edge causes the part to power up again. When the AD7887 is in Mode 1, that is, PM1 = PM0 = 0, the part enters shutdown on the rising edge of $\overline{CS}$ and power up from shutdown on the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high during the conversion in this mode, the part immediately enters shutdown.

Power-Up Times

The AD7887 has an approximate 1 µs power-up time when powering up from standby or when using an external reference. When V_{DD} is first connected the AD7887 powers up in Mode 1, that is, PM1 = PM0 = 0. The part is put into shutdown on the rising edge of $\overline{CS}$ in this mode. A subsequent power-up from shutdown takes approximately 5 µs. The AD7887 wake-up time is very short in the autostandby mode; therefore, it is possible to wake up the part and carry out a valid conversion in the same read/write operation.

POWER VS. THROUGHPUT RATE

By operating the AD7887 in autoshutdown mode, autostandby mode, or Mode 1, the average power consumption of the AD7887 decreases at lower throughput rates. Figure 15 shows how as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

For example, if the AD7887 is operated in a continuous sampling mode with a throughput rate of 10 kSPS and a SCLK of 2 MHz (V_{DD} = 5 V), PM1 = 1 and PM0 = 0, that is, the device is in auto-shutdown mode, and the on-chip reference is used, the power consumption is calculated as follows: The power dissipation during normal operation is 3.5 mW (V_{DD} = 5 V). If the power-up time is 5 µs and the remaining conversion plus acquisition time is 15.5 t_{SCLK}, that is, approximately 7.75 µs (see Figure 18), the AD7887 can be said to dissipate 3.5 mW for 12.75 µs during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 µs and the average power dissipated during each cycle is (12.75/100) × (3.5 mW) = 446.25 µW. If V_{DD} = 3 V, SCLK = 2 MHz, and the device is in autoshutdown mode using the on-chip reference, the power dissipation during normal operation is 2.1 mW. The AD7887 can now be said to dissipate 2.1 mW for 12.75 µs during each conversion cycle. With a throughput rate of 10 kSPS, the average power dissipated during each cycle is (12.75/100) × (2.1 mW) = 267.75 µW. Figure 15 shows the power vs. throughput rate for automatic shutdown with both 5 V and 3 V supplies.

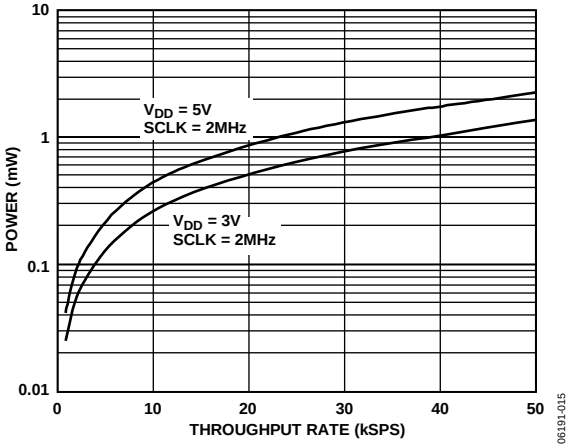


Figure 15. Power vs. Throughput Rate

MODES OF OPERATION

The AD7887 has several modes of operation that are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The modes of operation are controlled by the PM1 and PM0 bits of the control register, as previously outlined in Table 6. For read-only operation of the AD7887, the default mode of all 0s in the control register can be set up by tying the DIN line permanently low.

Mode 1 (PM1 = 0, PM0 = 0)

This mode allows the user to control the powering down of the part via the $\overline{CS}$ pin. Whenever $\overline{CS}$ is low, the AD7887 is fully powered up; whenever $\overline{CS}$ is high, the AD7887 is in full shutdown. When $\overline{CS}$ goes from high to low, all on-chip circuitry starts to power up. It takes approximately 5 µs for the AD7887 internal circuitry to be fully powered up. As a result, a conversion (or sample-and-hold acquisition) should not be initiated during this 5 µs.

Figure 16 shows a general diagram of the operation of the AD7887 in this mode. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5 µs elapses between the falling edge of $\overline{CS}$ and the second rising edge of SCLK. In microcontroller applications, this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontrollers serial port) is not initiated for 5 µs. In DSP applications, where $\overline{CS}$ is generally derived from the serial frame synchronization line, it is usually not possible to separate the $\overline{CS}$ falling edge and second SCLK rising edge by up to 5 µs without affecting the speed of the rest of the serial clock. Therefore, the user must write to the control register to exit this mode and (by writing PM1 = 0 and PM0 = 1) put the part into Mode 2, that is, normal mode. A second conversion needs to be initiated when the part is powered up to get a conversion result. The write operation that takes place in conjunction with this

second conversion can put the part back into Mode 1, and the part goes into power-down mode when $\overline{CS}$ returns high.

Mode 2 (PM1 = 0, PM0 = 1)

In this mode of operation, the AD7887 remains fully powered up regardless of the status of the $\overline{CS}$ line. It is intended for fastest throughput rate performance because the user does not have to worry about the 5 µs power-up time previously mentioned. Figure 17 shows the general diagram of the operation of the AD7887 in this mode.

The data presented to the AD7887 on the DIN line during the first eight clock cycles of the data transfer are loaded to the control register. To continue to operate in this mode, the user must ensure that PM1 is loaded with 0 and PM0 is loaded with 1 on every data transfer.

The falling edge of $\overline{CS}$ initiates the sequence, and the input signal is sampled on the second rising edge of the SCLK input. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. Once a data transfer is complete (that is, once $\overline{CS}$ returns high), another conversion can be initiated immediately by bringing $\overline{CS}$ low again.

Mode 3 (PM1 = 1, PM0 = 0)

In this mode, the AD7887 automatically enters its full shutdown mode at the end of every conversion. It is similar to Mode 1 except that the status of $\overline{CS}$ does not have any effect on the power-down status of the AD7887.

Figure 18 shows the general diagram of the operation of the AD7887 in this mode. On the first falling SCLK edge after $\overline{CS}$ goes low, all on-chip circuitry starts to power up. It takes approximately 5 µs for the AD7887 internal circuitry to be fully powered up. As a result, a conversion (or sample-and-hold acquisition) should not be initiated during this 5 µs. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5 µs elapses between the first falling edge of $\overline{SCLK}$ and the second rising edge of SCLK after the $\overline{CS}$ falling edge, as shown in Figure 18. In microcontroller applications (or with a slow serial clock), this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontroller's serial port) is not initiated for 5 µs. However, for higher speed serial clocks, it will not be possible to have a 5 µs delay between powering up and the first rising edge of the SCLK. Therefore, the user must write to the control register to exit this mode and (by writing PM1 = 0 and PM0 = 1) put the part into Mode 2. A second conversion needs to be initiated when the part is powered up to get a conversion result, as shown in Figure 19. The write operation that takes place in conjunction with this second conversion can put the part back into Mode 3, and the part goes into power-down mode when the conversion sequence ends.

Mode 4 (PM1 = 1, PM0 = 1)

In this mode, the AD7887 automatically enters a standby (or sleep) mode at the end of every conversion. In this standby mode, all on-chip circuitry, apart from the on-chip reference, is powered down. This mode is similar to Mode 3, but, in this case, the power-up time is much shorter because the on-chip reference remains powered up at all times.

Figure 20 shows the general diagram of the operation of the AD7887 in this mode. On the first falling SCLK edge after $\overline{CS}$ goes low, the AD7887 comes out of standby. The AD7887 wake-up time is very short in this mode, so it is possible to wake up the part and carry out a valid conversion in the same read/write operation. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. At the end of conversion (last rising edge of SCLK), the part automatically enters its standby mode.

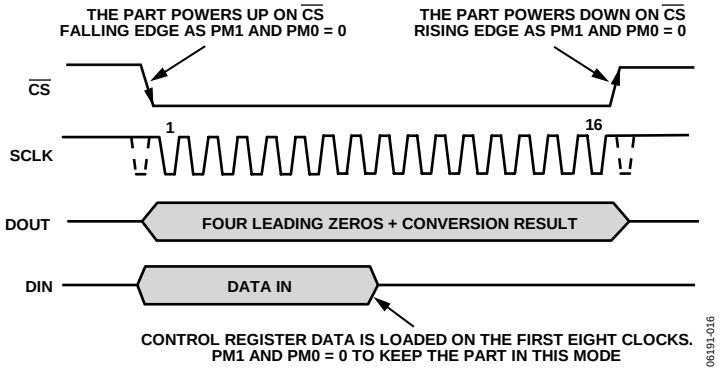


Figure 16. Mode 1 Operation

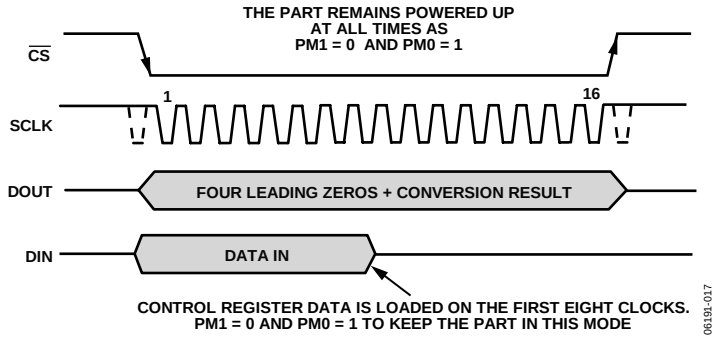


Figure 17. Mode 2 Operation

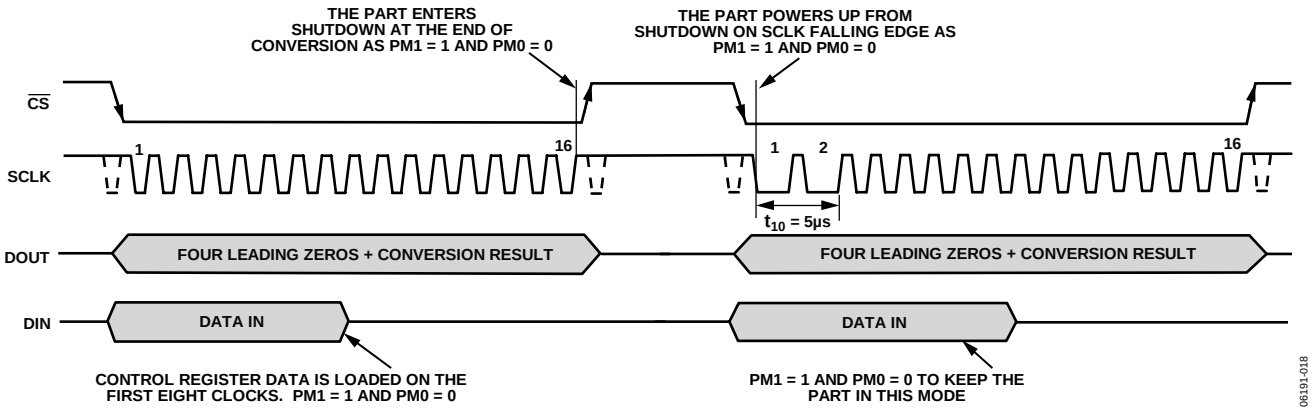


Figure 18. Mode 3 Operation (Microcontroller for Slow SCLKs)

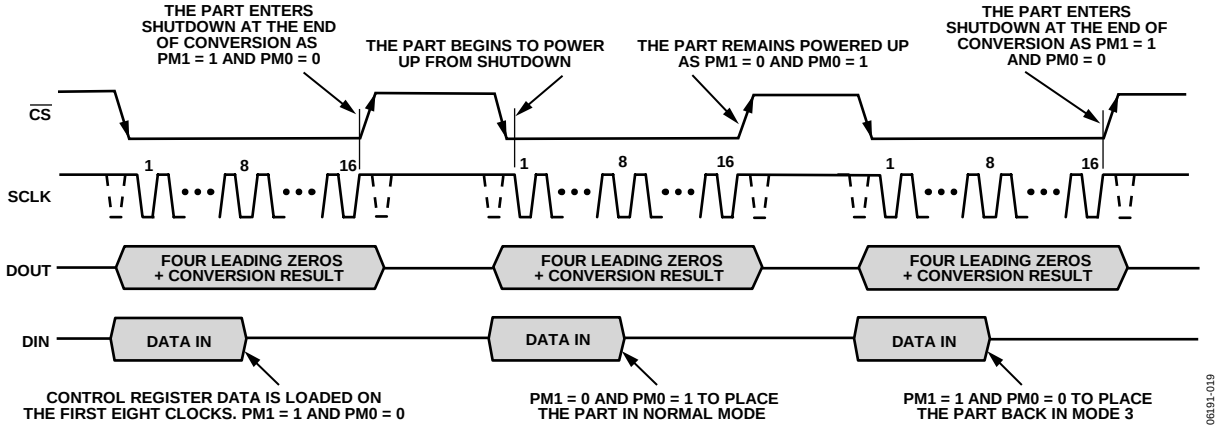


Figure 19. Mode 3 Operation (Microcontroller for High Speed SCLKs)

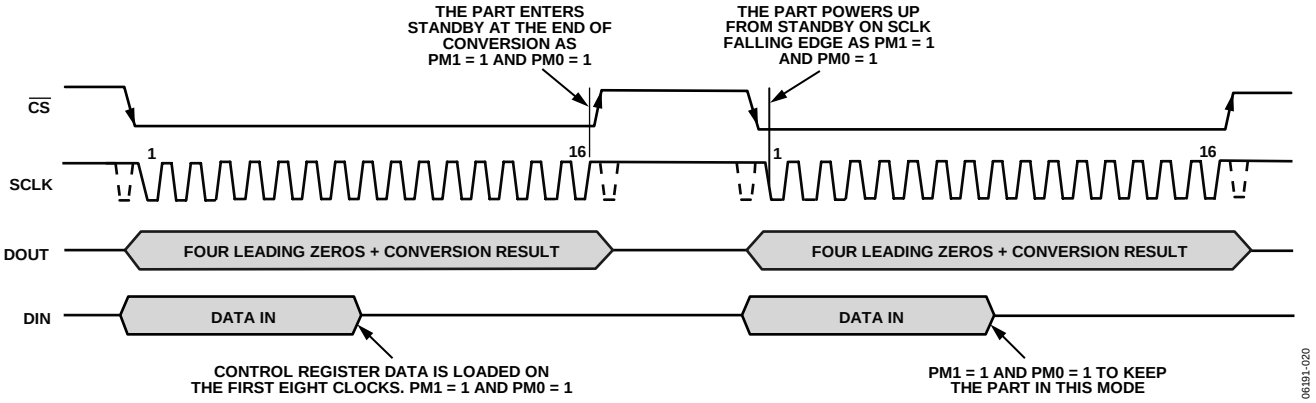


Figure 20. Mode 4 Operation

SERIAL INTERFACE

Figure 21 shows the detailed timing diagrams for serial interfacing to the AD7887. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7887 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. For some modes, the falling edge of $\overline{CS}$ wakes up the part. In all cases, it gates the serial clock to the AD7887 and puts the on-chip track/hold into track mode. The input signal is sampled on the second rising edge of the SCLK input after the falling edge of $\overline{CS}$. Thus, the first one and one-half clock cycles after the falling edge of $\overline{CS}$ are when the acquisition of the input signal takes place. This time is denoted as the acquisition time (t_{ACQ}). In modes where the falling edge of $\overline{CS}$ wakes up the part, the acquisition time must allow for the wake-up time of 5 µs. The on-chip track/hold goes from track mode to hold mode on the second rising edge of SCLK, and a conversion is also initiated on this edge. The conversion process takes an additional fourteen and one-half SCLK cycles to complete. The rising edge of $\overline{CS}$ puts the bus back into three-state. If $\overline{CS}$ is left low, a new conversion can be initiated.

In dual-channel operation, the input channel that is sampled is the one that was selected in the previous write to the control register. Thus, in dual-channel operation, the user must write the channel address for the next conversion while the present conversion is in progress.

Writing of information to the control register takes place on the first eight rising edges of SCLK in a data transfer. The control register is always written to when a data transfer takes place. However, the AD7887 can be operated in a read-only mode by tying DIN low, thereby loading all 0s to the control register every time. When operating the AD7887 in write/read mode, the user must be careful to always set up the correct information on the DIN line when reading data from the part.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7887. In applications where the first serial clock edge following $\overline{CS}$ going low is a falling edge, this edge clocks out the first leading zero. Thus, the first rising clock edge on the SCLK clock has the first leading zero provided. In applications where the first serial clock edge following $\overline{CS}$ going low is a rising edge, the first leading zero may not be set up in time for the processor to read it correctly. However, subsequent bits are clocked out on the falling edge of SCLK so that they are provided to the processor on the following rising edge. Thus, the second leading zero is clocked out on the falling edge subsequent to the first rising edge. The final bit in the data transfer is valid on the 16th rising edge, having been clocked out on the previous falling edge.

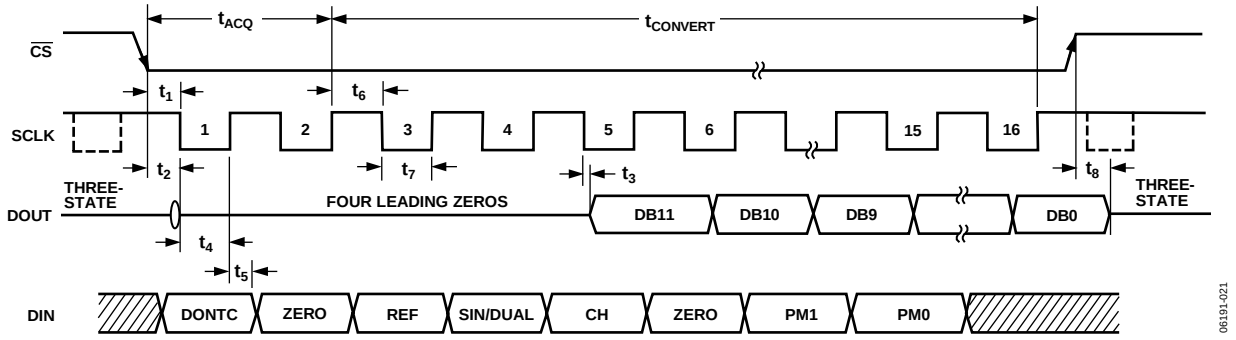


Figure 21. Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7887 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7887 with some of the more common microcontroller and DSP serial interface protocols.

AD7887 to TMS320C5x

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7887. The $\overline{CS}$ input allows easy interfacing with an inverter between the serial clock of the TMS320C5x and the AD7887 being the only glue logic required. The serial port of the TMS320C5x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The connection diagram is shown in Figure 22.

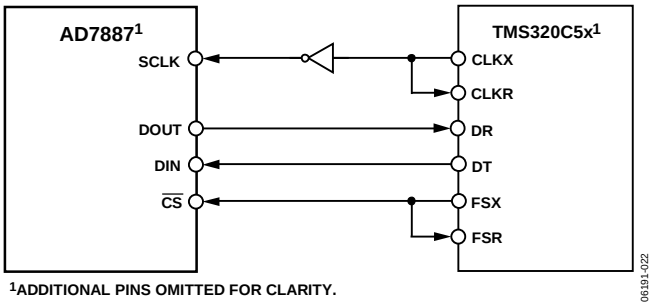


Figure 22. Interfacing to the TMS320C5x

AD7887 to ADSP-21xx

The ADSP-21xx family of DSPs are easily interfaced to the AD7887 with an inverter between the serial clock of the ADSP-21xx and the AD7887. This is the only glue logic required. The SPORT control register should be set up as follows:

Table 7. SPORT0 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternative framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right justify data
SLEN = 1111	16-bit data-word
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

The connection diagram is shown in Figure 23. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode, and the SPORT control register is set up as described in Table 7. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. In this example however, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling cannot be achieved.

The timer registers are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high again before a transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

This situation results in nonequidistant sampling because the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer number of N, equidistant sampling will be implemented by the DSP.

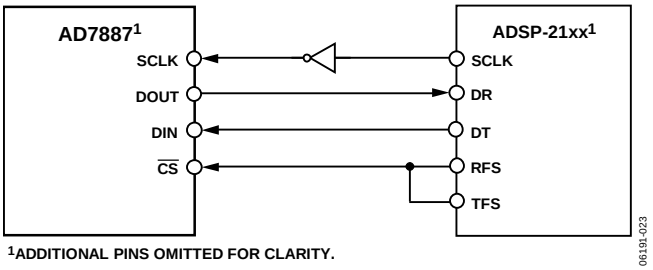


Figure 23. Interfacing to the ADSP-21xx

AD7887 to DSP56xxx

The connection diagram in Figure 24 shows how the AD7887 can be connected to the SSI (synchronous serial interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in synchronous mode (SYN bit in CRB = 1) with an internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 1 and FSL0 = 0 in CRB). Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. An inverter is also necessary between the SCLK from the DSP56xxx and the SCLK pin of the AD7887, as shown in Figure 24.

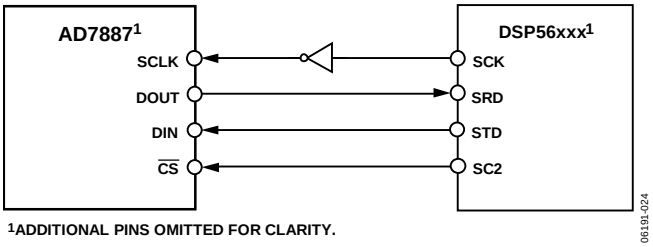


Figure 24. Interfacing to the DSP56xxx

AD7887 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1) when the clock polarity bit (CPOL) = 1 and the clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see the M68HC11 reference manual from Freescale Semiconductor, Inc., for more information. The serial transfer takes place as two 8-bit operations. A connection diagram is shown in Figure 25.

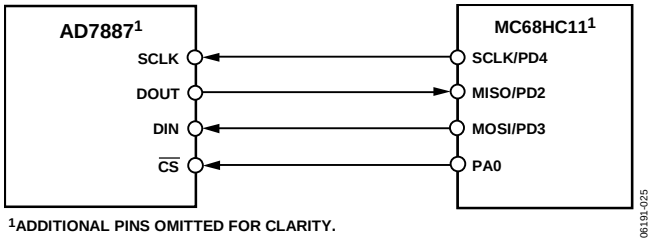


Figure 25. Interfacing to the MC68HC11

AD7887 to 8051

It is possible to implement a serial interface using the data ports on the 8051. This allows a full duplex serial transfer to be implemented. The technique involves bit-banging an input/output port (for example, P1.0) to generate a serial clock and using two other input/output ports (for example, P1.1 and P1.2) to shift data in and out—see Figure 26.

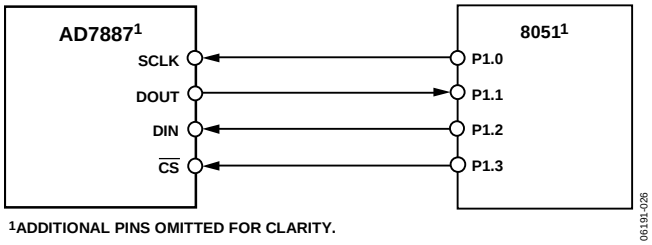


Figure 26. Interfacing to the 8051 Using Input/Output Ports

AD7887 to PIC16C6x/PIC16C7x

The PIC16C6x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit = 1. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/PIC17 Microcontroller User Manual*. Figure 27 shows the hardware connections needed to interface to the PIC16C6x/PIC16C7x. In this example, input/output port RA1 is being used to pulse $\overline{CS}$. This microcontroller only transfers eight bits of data during each serial transfer operation. Therefore, two consecutive read/write operations are needed.

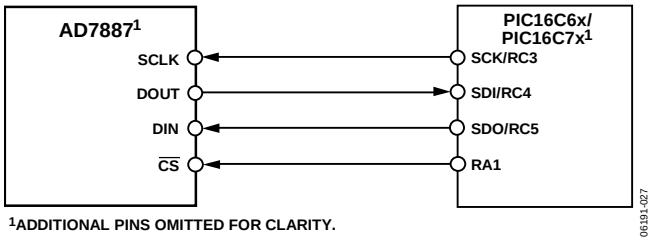


Figure 27. Interfacing to the PIC16C6x/PIC16C7x

APPLICATION HINTS

Grounding and Layout

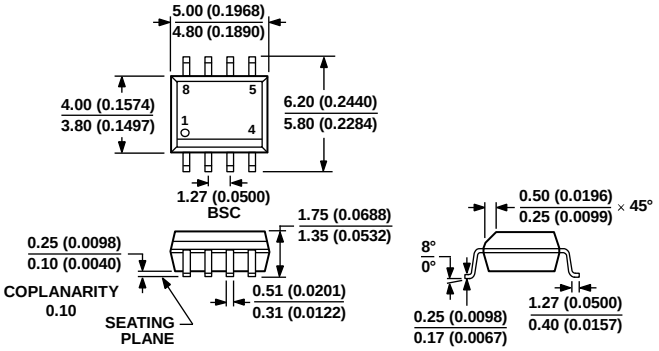
The AD7887 has very good immunity to noise on the power supplies, as can be seen in Figure 7. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7887 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it results in the best shielding. Digital and analog ground planes should be joined in only one place, as close as possible to the GND pin of the AD7887. If the AD7887 is in a system where multiple devices require AGND-to-DGND connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7887.

Avoid running digital lines under the device because these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7887 to avoid noise coupling. The power supply lines to the AD7887 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best approach, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device.

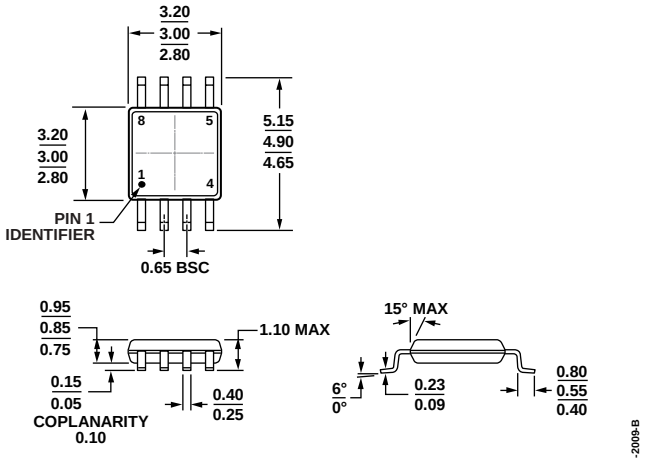
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8) Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 29. 8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Linearity Error[3]	Temperature	Package Description	Package Option	Branding
AD7887AR	±2 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887AR-REEL7	±2 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887ARM	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A
AD7887ARM-REEL7	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A
AD7887ARMZ	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A#
AD7887ARMZ-REEL	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A#
AD7887ARMZ-REEL7	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A#
AD7887ARZ	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	R-8	
AD7887ARZ-REEL7	±2 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887BR	±1 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887BR-REEL7	±1 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887BRZ	±1 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887BRZ-REEL	±1 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887BRZ-REEL7	±1 LSB	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD7887WARMZ	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A#
AD7887WARMZ-RL	±2 LSB	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	C5A#
EVAL-AD7887SDZ			Evaluation Board		
EVAL-SDP-CB1Z			System Demonstration Platform		

[1] Z = RoHS Compliant Part, # denotes lead-free product, may be top or bottom marked.
[2] W = Qualified for Automotive Applications.
[3] Linearity error here refers to integral linearity error.

AUTOMOTIVE PRODUCTS

The AD7887W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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