

# Configurable Six Supply Monitor with Adjustable Reset and Watchdog Timers

## FEATURES

- Simultaneously Monitors Six Supplies
- 16 User Selectable Combinations of 5V, 3.3V, 3V, 2.5V, 1.8V, 1.5V and  $\pm$  Adjustable Voltage Thresholds
- Guaranteed Threshold Accuracy:  $\pm 1.5\%$
- Adjustable Reset and Watchdog Timeout
- Low Supply Current: 52 $\mu$ A
- Comparator/Monitor Output for Each Supply
- Power Supply Glitch Immunity
- Guaranteed  $\overline{\text{RST}}$  for  $V_{CC} \geq 1V$
- High Temperature Operation to 125°C
- 20-Lead TSSOP Package

## APPLICATIONS

- Desktop and Notebook Computers
- Multivoltage Systems
- Telecom Equipment
- Portable Battery-Powered Equipment
- Network Servers
- Automotive

## DESCRIPTION

The LTC<sup>®</sup>2931 is a configurable supply monitor for systems with up to six supply voltages. One of 16 preset or adjustable voltage monitor combinations can be selected using an external resistive divider connected to the mode select pin. The preset voltage thresholds are accurate to  $\pm 1.5\%$  over temperature. The LTC2931 also features adjustable inputs with a 0.5V nominal threshold. All six open-drain voltage comparator outputs are connected to separate pins for individual supply monitoring.

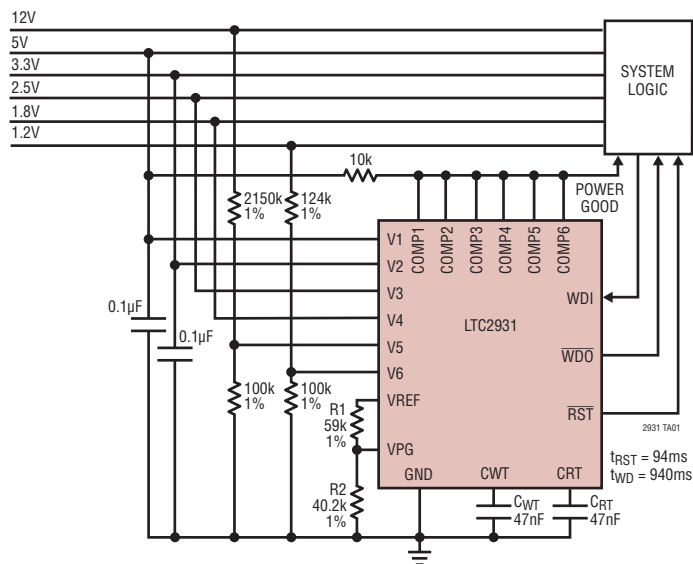
The reset and watchdog timeout periods are adjustable using external capacitors. Tight voltage threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The  $\overline{\text{RST}}$  output is guaranteed to be in the correct state for  $V_{CC}$  down to 1V. Each status output has a weak internal pull-up and may be externally pulled up to a user defined voltage.

The 52 $\mu$ A supply current makes the LTC2931 ideal for power conscious systems and it may be configured to monitor fewer than six inputs.

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## TYPICAL APPLICATION

Six Supply Monitor 12V (ADJ), 5V, 3.3V, 2.5V, 1.8V, 1.2V (ADJ)



Voltage Threshold Configuration Table

| V1 (V) | V2 (V) | V3 (V) | V4 (V) | V5 (V) | V6 (V) |
|--------|--------|--------|--------|--------|--------|
| 5.0    | 3.3    | 2.5    | 1.8    | ADJ    | ADJ    |
| 5.0    | 3.3    | 2.5    | 1.5    | ADJ    | ADJ    |
| 5.0    | 3.3    | 2.5    | ADJ    | ADJ    | ADJ    |
| 5.0    | 3.3    | 1.8    | ADJ    | ADJ    | ADJ    |
| 5.0    | 3.3    | 1.8    | -ADJ   | ADJ    | ADJ    |
| 5.0    | 3.3    | ADJ    | ADJ    | ADJ    | ADJ    |
| 5.0    | 3.3    | ADJ    | -ADJ   | ADJ    | ADJ    |
| 5.0    | 3.0    | 2.5    | ADJ    | ADJ    | ADJ    |
| 5.0    | 3.0    | 1.8    | ADJ    | ADJ    | ADJ    |
| 5.0    | 3.0    | ADJ    | ADJ    | ADJ    | ADJ    |
| 3.3    | 2.5    | 1.8    | 1.5    | ADJ    | ADJ    |
| 3.3    | 2.5    | 1.8    | ADJ    | ADJ    | ADJ    |
| 3.3    | 2.5    | 1.8    | -ADJ   | ADJ    | ADJ    |
| 3.3    | 2.5    | 1.5    | ADJ    | ADJ    | ADJ    |
| 3.3    | 2.5    | ADJ    | ADJ    | ADJ    | ADJ    |
| 3.3    | 2.5    | ADJ    | -ADJ   | ADJ    | ADJ    |

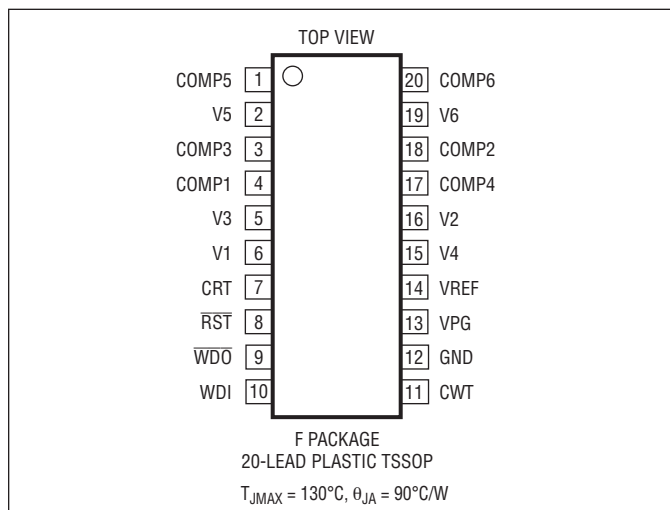
# LTC2931

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

|                                       |                              |
|---------------------------------------|------------------------------|
| V1, V2, V3, V4, V5, V6, VPG           | –0.3V to 7V                  |
| RST, COMP1-6                          | –0.3V to 7V                  |
| CWT, WDO                              | –0.3V to 7V                  |
| CRT, VREF, WDI                        | –0.3V to ( $V_{CC} + 0.3V$ ) |
| Reference Load Current ( $I_{VREF}$ ) | $\pm 1mA$                    |
| V4 Input Current (–ADJ Mode)          | –1mA                         |
| RST, WDO, COMP1-6 Currents            | $\pm 10mA$                   |
| Operating Temperature Range           |                              |
| LTC2931C                              | 0°C to 70°C                  |
| LTC2931I                              | –40°C to 85°C                |
| LTC2931H                              | –40°C to 125°C               |
| Storage Temperature Range             | –65°C to 150°C               |
| Lead Temperature (Soldering, 10 sec)  | 300°C                        |

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL   | PART MARKING | PACKAGE DESCRIPTION   | TEMPERATURE RANGE |
|------------------|-----------------|--------------|-----------------------|-------------------|
| LTC2931CF#PBF    | LTC2931CF#TRPBF | LTC2931F     | 20-Lead Plastic TSSOP | 0°C to 70°C       |
| LTC2931IF#PBF    | LTC2931IF#TRPBF | LTC2931F     | 20-Lead Plastic TSSOP | –40°C to 85°C     |
| LTC2931HF#PBF    | LTC2931HF#TRPBF | LTC2931F     | 20-Lead Plastic TSSOP | –40°C to 125°C    |

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ C$ .  $V_{CC} = 5V$ , unless otherwise specified. (Note 3)

| SYMBOL       | PARAMETER                           | CONDITIONS                                      | MIN   | TYP   | MAX   | UNITS |
|--------------|-------------------------------------|-------------------------------------------------|-------|-------|-------|-------|
| $V_{CC}$     | Minimum Internal Operating Voltage  | RST, COMP <sub>n</sub> in Correct Logic State ● |       |       | 1     | V     |
| $V_{CCMINP}$ | Minimum Required for Mode Selection | $V_{CC}$ Rising ●                               |       |       | 2.4   | V     |
| $V_{CCMINC}$ | Minimum Required for Comparators    | $V_{CC}$ Falling ●                              |       |       | 2.3   | V     |
| $V_{RT50}$   | 5V, 5% Reset Threshold              | V1 Input Threshold ●                            | 4.600 | 4.675 | 4.750 | V     |
| $V_{RT33}$   | 3.3V, 5% Reset Threshold            | V1, V2 Input Threshold ●                        | 3.036 | 3.086 | 3.135 | V     |
| $V_{RT30}$   | 3V, 5% Reset Threshold              | V2 Input Threshold ●                            | 2.760 | 2.805 | 2.850 | V     |
| $V_{RT25}$   | 2.5V, 5% Reset Threshold            | V2, V3 Input Threshold ●                        | 2.300 | 2.338 | 2.375 | V     |
| $V_{RT18}$   | 1.8V, 5% Reset Threshold            | V3, V4 Input Threshold ●                        | 1.656 | 1.683 | 1.710 | V     |
| $V_{RT15}$   | 1.5V, 5% Reset Threshold            | V3, V4 Input Threshold ●                        | 1.380 | 1.403 | 1.425 | V     |
| $V_{RTA}$    | ADJ Reset Threshold                 | V3, V4, V5, V6 Input Threshold ●                | 492.5 | 500   | 507.5 | mV    |
| $V_{RTAN}$   | –ADJ Reset Threshold                | V4 Input Threshold ●                            | –18   | 0     | 18    | mV    |

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ , unless otherwise specified. (Note 3)

| SYMBOL        | PARAMETER                                                                                        | CONDITIONS                                                                                           |             | MIN            | TYP          | MAX             | UNITS                     |
|---------------|--------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|-------------|----------------|--------------|-----------------|---------------------------|
| $V_{REF}$     | Reference Voltage                                                                                | $V_{CC} \geq 2.3\text{V}$ , $I_{VREF} = \pm 1\text{mA}$ ,<br>$C_{REF} \leq 1000\text{pF}$            | ●           | 1.192          | 1.210        | 1.228           | V                         |
| $V_{PG}$      | Mode Selection Voltage Range                                                                     | $V_{CC} \geq V_{CCMINP}$                                                                             | ●           | 0              |              | $V_{REF}$       | V                         |
| $I_{VPG}$     | VPG Input Current                                                                                | $V_{PG} = V_{REF}$                                                                                   | ●           |                |              | $\pm 20$        | nA                        |
| $I_{V1}$      | V1 Input Current                                                                                 | $V1 = 5\text{V}$ , $I_{VREF} = 12\mu\text{A}$ (Note 4)                                               | ●           |                | 52           | 75              | $\mu\text{A}$             |
| $I_{V2}$      | V2 Input Current                                                                                 | $V2 = 3.3\text{V}$                                                                                   | ●           |                | 0.8          | 2               | $\mu\text{A}$             |
| $I_{V3}$      | V3 Input Current                                                                                 | $V3 = 2.5\text{V}$<br>$V3 = 0.55\text{V}$ (ADJ Mode)                                                 | ●<br>●      | <br>-15        | 0.52         | 1.2<br>15       | $\mu\text{A}$<br>nA       |
| $I_{V4}$      | V4 Input Current                                                                                 | $V4 = 1.8\text{V}$<br>$V4 = 0.55\text{V}$ (ADJ Mode)<br>$V4 = -0.02\text{V}$ (-ADJ Mode)             | ●<br>●<br>● | <br>-15<br>-15 | 0.34         | 0.8<br>15<br>15 | $\mu\text{A}$<br>nA<br>nA |
| $I_{V5, V6}$  | V5, V6 Input Current                                                                             | $V5, V6 = 0.55\text{V}$                                                                              | ●           | -15            |              | 15              | nA                        |
| $I_{CRT(UP)}$ | CRT Pull-Up Current                                                                              | $V_{CRT} = \text{GND}$                                                                               | ●           | -1.4           | -2           | -2.6            | $\mu\text{A}$             |
| $I_{CRT(DN)}$ | CRT Pull-Down Current                                                                            | $V_{CRT} = 1.3\text{V}$                                                                              | ●           | 10             | 20           | 30              | $\mu\text{A}$             |
| $t_{RST}$     | Reset Timeout Period                                                                             | $C_{RT} = 1500\text{pF}$                                                                             | ●           | 2              | 3            | 4               | ms                        |
| $t_{UV}$      | $V_n$ Undervoltage Detect to $\overline{\text{RST}}$ or $\text{COMP}_n$                          | $V_n$ Less Than Reset Threshold by More than 1%                                                      |             |                | 150          |                 | $\mu\text{s}$             |
| $V_{OL}$      | Voltage Output Low $\overline{\text{RST}}$ , $\text{COMP}_n$                                     | $I_{SINK} = 3\text{mA}$ , $V_{CC} = 3\text{V}$<br>$I_{SINK} = 100\mu\text{A}$ , $V_{CC} = 1\text{V}$ | ●<br>●      |                | 0.15<br>0.05 | 0.4<br>0.3      | V<br>V                    |
| $I_{COMP_n}$  | $\text{COMP}_n$ Pull-Up Current                                                                  | $V_{COMP_n} = \text{GND}$                                                                            | ●           | -2             | -6           | -12             | $\mu\text{A}$             |
| $V_{OL}$      | Voltage Output Low $\overline{\text{WDO}}$                                                       | $I_{SINK} = 3\text{mA}$                                                                              | ●           |                | 0.15         | 0.4             | V                         |
| $V_{OH}$      | Voltage Output High $\overline{\text{RST}}$ , $\overline{\text{WDO}}$ , $\text{COMP}_n$ (Note 5) | $I_{SOURCE} = -1\mu\text{A}$                                                                         | ●           | $V2-1$         |              |                 | V                         |
| $I_{CWT(UP)}$ | CWT Pull-Up Current                                                                              | $V_{CWT} = \text{GND}$                                                                               | ●           | -1.4           | -2           | -2.6            | $\mu\text{A}$             |
| $I_{CWT(DN)}$ | CWT Pull-Down Current                                                                            | $V_{CWT} = 1.3\text{V}$                                                                              | ●           | 10             | 20           | 30              | $\mu\text{A}$             |
| $t_{WD}$      | Watchdog Timeout Period                                                                          | $C_{WT} = 1500\text{pF}$                                                                             | ●           | 20             | 30           | 40              | ms                        |
| $V_{IH}$      | WDI Input Threshold High                                                                         | $V_{CC} = 3.3\text{V}$ to $5.5\text{V}$                                                              | ●           | 1.6            |              |                 | V                         |
| $V_{IL}$      | WDI Input Threshold Low                                                                          | $V_{CC} = 3.3\text{V}$ to $5.5\text{V}$                                                              | ●           |                |              | 0.4             | V                         |
| $t_{WP}$      | WDI Input Pulse Width                                                                            | $V_{CC} = 3.3\text{V}$                                                                               | ●           | 150            |              |                 | ns                        |
| $I_{WDI}$     | WDI Pull-Up Current                                                                              | $V_{WDI} = 1\text{V}$                                                                                | ●           | -4             | -10          | -16             | $\mu\text{A}$             |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

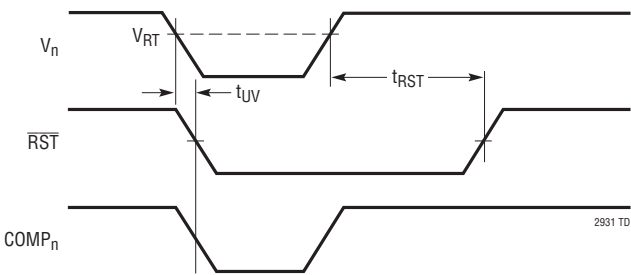
**Note 3:** The greater of  $V1$ ,  $V2$  is the internal supply voltage ( $V_{CC}$ ).

**Note 4:** Under static no-fault conditions,  $V1$  will necessarily supply quiescent current. If at any time  $V2$  is larger than  $V1$ ,  $V2$  must be capable of supplying the quiescent current, programming (transient) current and reference load current.

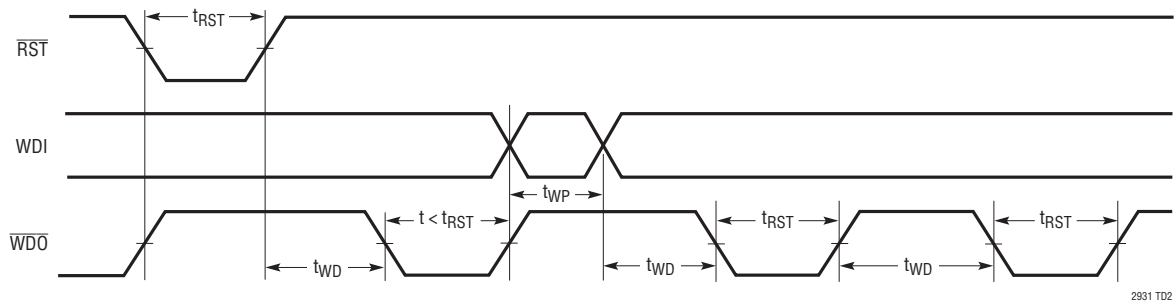
**Note 5:** The output pins  $\overline{\text{RST}}$ ,  $\overline{\text{WDO}}$ , and  $\text{COMP}_n$  have diode protected internal pull-ups to  $V2$  of typically  $6\mu\text{A}$ . However, external pull-up resistors may be used when faster rise times are required or for  $V_{OH}$  voltages greater than  $V2$ .

TIMING DIAGRAMS

V<sub>n</sub> Monitor Timing

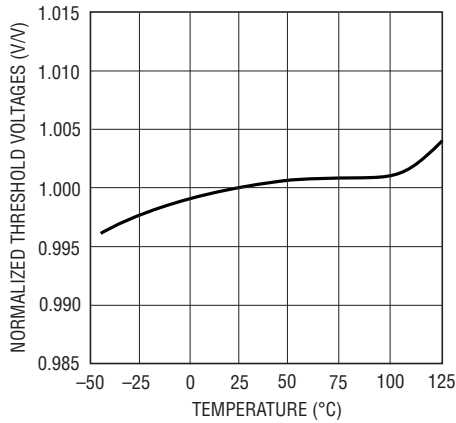


Watchdog Timing

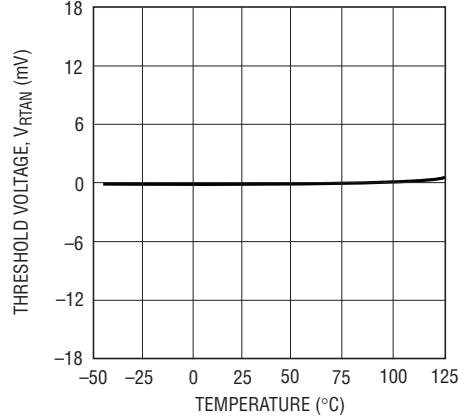
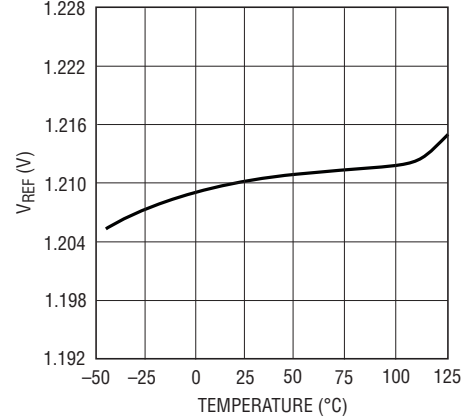


## TYPICAL PERFORMANCE CHARACTERISTICS

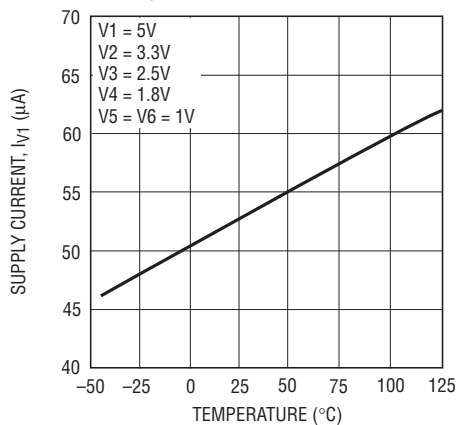
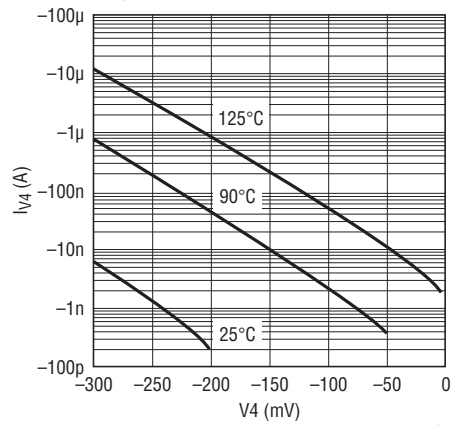
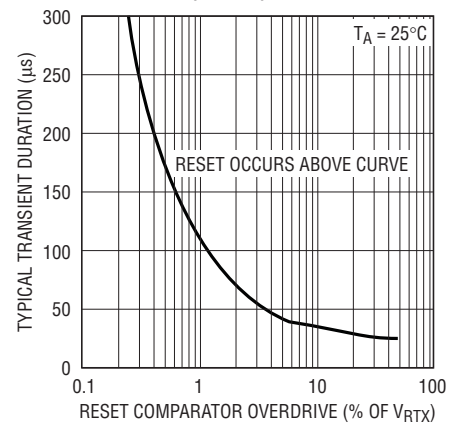
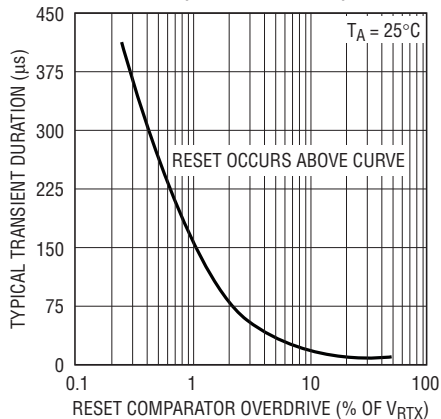
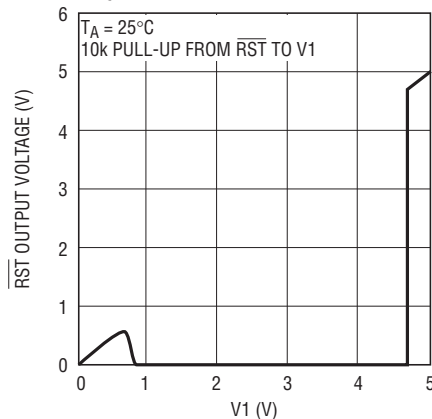
Normalized Threshold Voltages vs Temperature



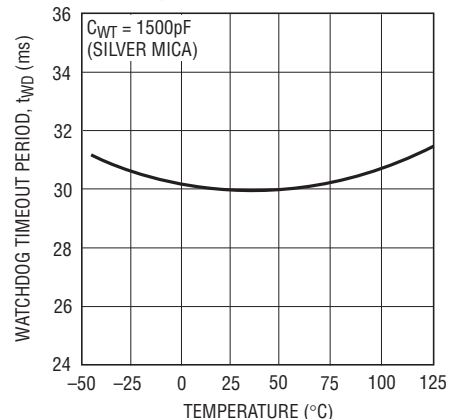
-ADJ Threshold Voltage vs Temperature

V<sub>REF</sub> vs Temperature

Supply Current vs Temperature

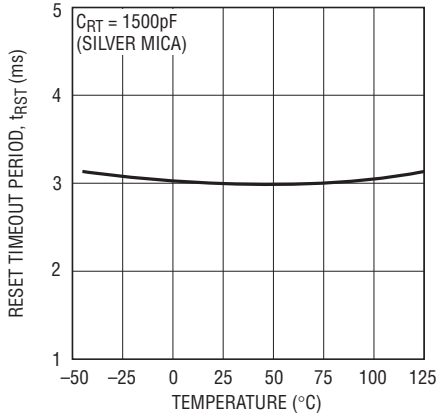
I(V<sub>4</sub>) vs V<sub>4</sub> in Negative Adjust ModeTransient Duration vs Comparator Overdrive (V<sub>1</sub>, V<sub>2</sub>)Transient Duration vs Comparator Overdrive (V<sub>3</sub>, V<sub>4</sub>, V<sub>5</sub>, V<sub>6</sub>)RST Output Voltage vs V<sub>1</sub>, V<sub>PG</sub> = GND

Watchdog Timeout Period vs Temperature



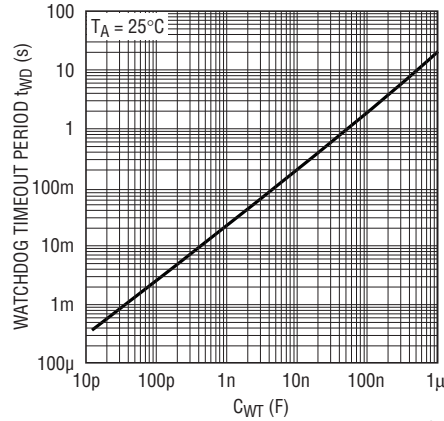
# TYPICAL PERFORMANCE CHARACTERISTICS

**Reset Timeout Period vs Temperature**



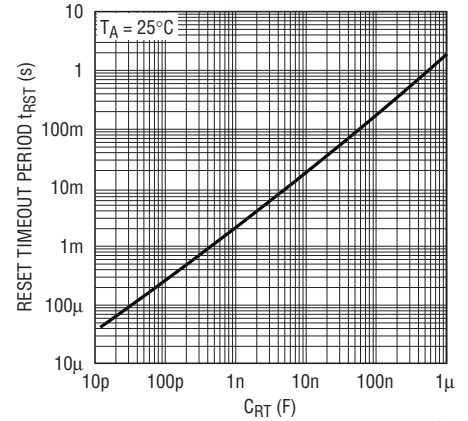
2931 G10

**Watchdog Timeout Period vs  $C_{WT}$**



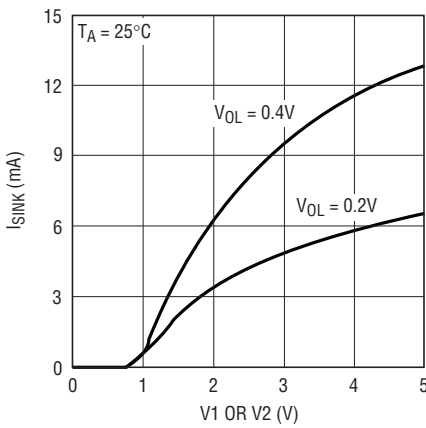
2931 G11

**Reset Timeout Period vs  $C_{RT}$**



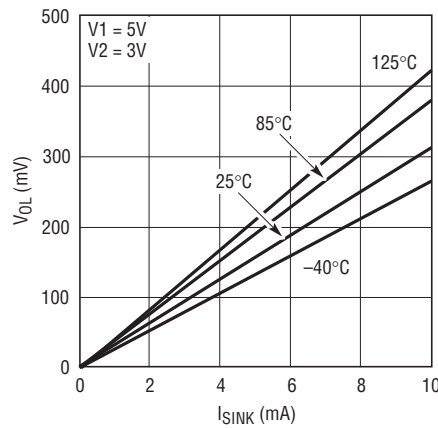
2931 G12

**$I_{SINK}$  vs Supply Voltage (RST, WDO, COMP<sub>n</sub>)**



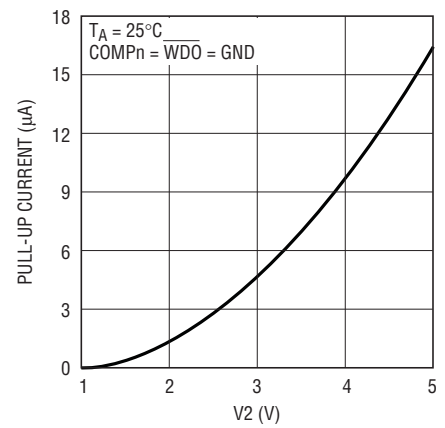
2931 G13

**Voltage Output Low vs Output Sink Current (RST, WDO, COMP<sub>n</sub>)**



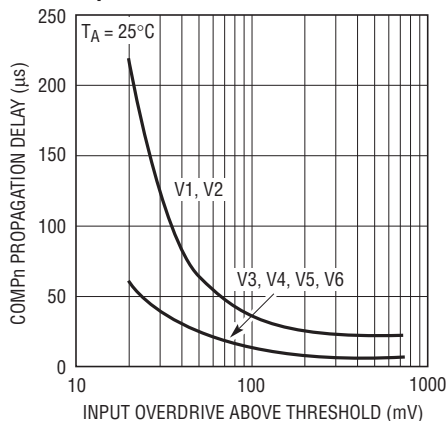
2931 G14

**COMP<sub>n</sub> and WDO Pull-Up Current vs V2**



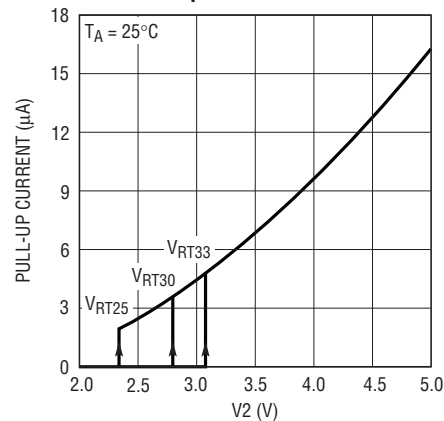
2931 G15

**COMP<sub>n</sub> Propagation Delay vs Input Overdrive Above Threshold**



2931 G16

**RST Pull-Up Current vs V2**



2931 G17

## PIN FUNCTIONS

**COMP5 (Pin 1):** Comparator Output 5. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V5 is above reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

**V5 (Pin 2):** Adjustable Voltage Input 5. High impedance comparator input with 0.5V typical threshold. See Applications Information for details. Tie to V1 if unused.

**COMP3 (Pin 3):** Comparator Output 3. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V3 is above its reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

**COMP1 (Pin 4):** Comparator Output 1. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V1 is above its reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

**V3 (Pin 5):** Voltage Input 3. Select from 2.5V, 1.8V, 1.5V, or ADJ. See Applications Information for details. Tie to V1 if unused.

**V1 (Pin 6):** Voltage Input 1. Select from 5V or 3.3V. See Applications Information for details. The greater of V1 or V2 is also V<sub>CC</sub> for the device. Bypass this pin to ground with a 0.1 $\mu$ F (or greater) capacitor.

**CRT (Pin 7):** Reset Timeout Capacitor. Attach an external capacitor (C<sub>RT</sub>) to GND to set a reset timeout of 2ms/nF. Leaving the pin open generates a minimum delay of approximately 25 $\mu$ s. A 47nF capacitor generates a 94ms reset delay time.

**RST (Pin 8):** Reset Output. Logic output with weak 6 $\mu$ A pull-up to V2. Pulls low when any voltage input is below the reset threshold and held low for the configured delay time after all voltage inputs are above threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

**WDO (Pin 9):** Watchdog Output. Logic output with weak 6 $\mu$ A pull-up to V2. May be pulled greater than V2 using external pull-up. The watchdog timer is enabled when  $\overline{\text{RST}}$  is high. The watchdog output pulls low if the watchdog timer times out and remains low for one reset timeout period. The watchdog output is cleared with a WDI transition or anytime  $\overline{\text{RST}}$  is low. The output will toggle between high

and low as long as the watchdog and reset timers are allowed to time out. Leave open if unused.

**WDI (Pin 10):** Watchdog Input. A logic input whose rising or falling edge must occur on this pin (while  $\overline{\text{RST}}$  is high) within the selected watchdog time-out period, prohibiting a high-to-low transition on the  $\overline{\text{WDO}}$  pin. The capacitor attached to the CWT pin sets the watchdog time-out period. A rising or falling edge on the WDI pin clears the voltage on the C<sub>WT</sub> capacitor, preventing  $\overline{\text{WDO}}$  from going low. Tie WDI to V1 or GND if unused. Tie CWT to GND to disable the watchdog function.

**CWT (Pin 11):** Watchdog Timeout Capacitor. Attach a capacitor (C<sub>WT</sub>) between CWT and GND to set a watchdog time-out period of 20ms/nF. Leaving the pin open generates a minimum timeout of approximately 200 $\mu$ s. A 47nF capacitor generates a 940ms watchdog time-out period. Tie CWT to GND to disable the watchdog function.

**GND (Pin 12):** Ground.

**VPG (Pin 13):** Threshold Select Input. Connect to an external 1% resistive divider between VREF and GND to select 1 of 16 combinations and/or  $\pm$ adjustable voltage thresholds (See Table 1). Do not add capacitance on the VPG pin.

**VREF (Pin 14):** Buffered Reference Voltage Output. A 1.210V nominal reference used for the mode selection voltage (V<sub>PG</sub>) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

**V4 (Pin 15):** Voltage Input 4. Select from 1.8V, 1.5V, ADJ or  $-\text{ADJ}$ . See Applications Information for details. Tie to V1 if unused and configured for positive voltage.

**V2 (Pin 16):** Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Applications Information for details. The greater of V1, V2 is also V<sub>CC</sub> for the device. Bypass this pin to ground with a 0.1 $\mu$ F (or greater) capacitor. All status outputs are weakly pulled up to V2.

**COMP4 (Pin 17):** Comparator Output 4. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V4 is above its reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

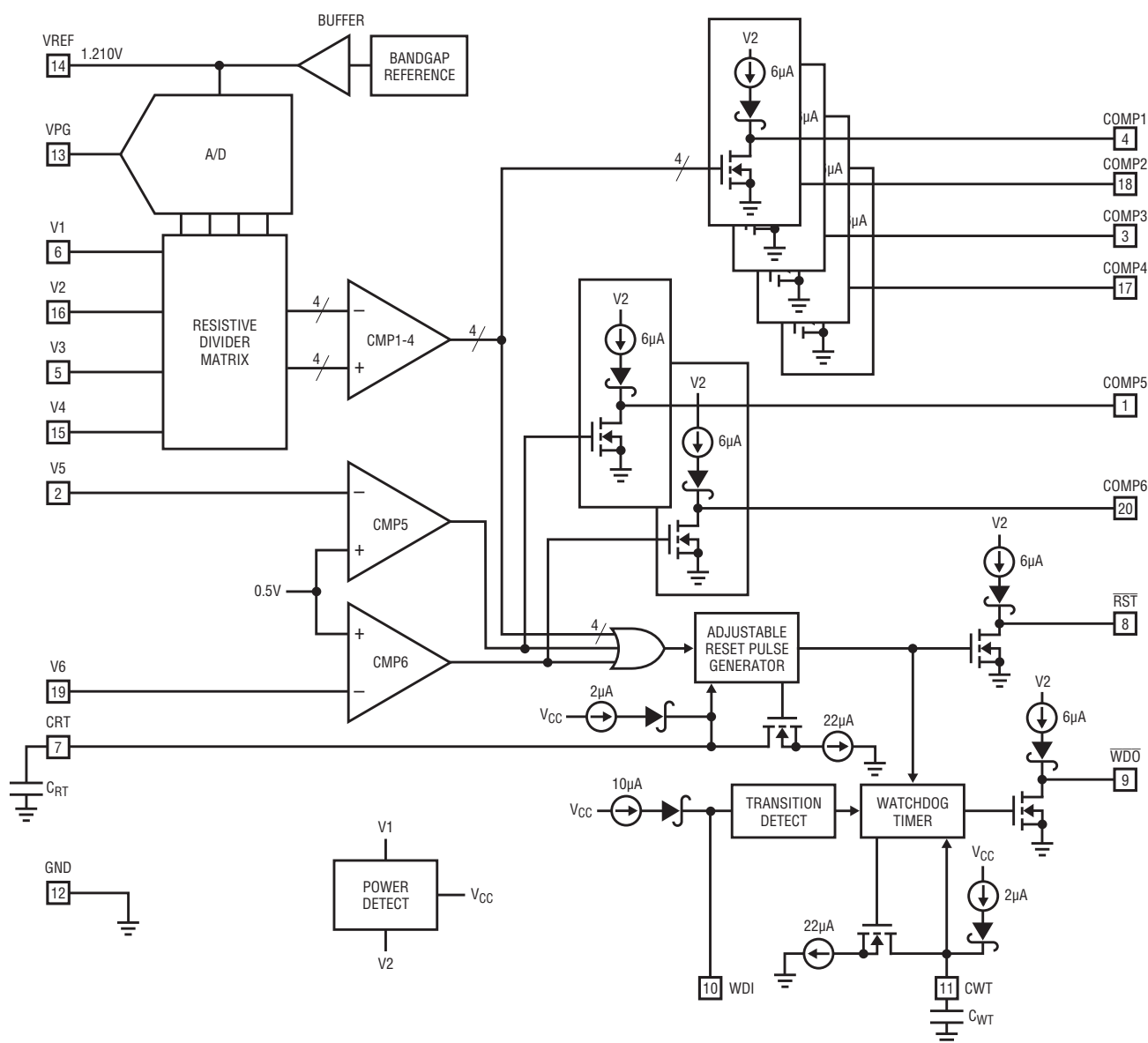
## PIN FUNCTIONS

**COMP2 (Pin 18):** Comparator Output 2. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V2 is above its reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

**V6 (Pin 19):** Adjustable Voltage Input 6. High impedance comparator input with 0.5V typical threshold. See Applications Information for details. Tie to V1 if unused.

**COMP6 (Pin 20):** Comparator Output 6. Real-time logic output with weak 6 $\mu$ A pull-up to V2. Pulls high when V6 is above its reset threshold. May be pulled greater than V2 using external pull-up. Leave open if unused.

## BLOCK DIAGRAM



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## APPLICATIONS INFORMATION

### Supply Monitoring

The LTC2931 is a low power, high accuracy configurable six supply monitoring circuit with six real-time monitor outputs, a common reset output and a watchdog timer. External capacitors set the reset and watchdog timeout periods. An external resistive divider between VREF, VPG and GND selects 1 of 16 possible input voltage monitor combinations. All six voltage inputs must be above their predetermined thresholds for the reset not to be activated. The LTC2931 asserts the reset and comparator outputs during power-up, power-down and brownout conditions on any one of the voltage inputs.

### Power-Up

The greater of V1 and V2 serves as the internal supply voltage ( $V_{CC}$ ). On power-up,  $V_{CC}$  powers the drive circuits for the  $\overline{RST}$  pin. This ensures that the  $\overline{RST}$  output will be low as soon as either V1 or V2 reaches 1V. The  $\overline{RST}$  output remains low until the part is configured. Once voltage thresholds are set, if any of the supply monitor inputs is below its configured threshold,  $\overline{RST}$  will be a logic low. Once all the monitor inputs rise above their thresholds, an internal timer is started and  $\overline{RST}$  is released after the delay time. If  $V_{CC} < (V3 - 1.0V)$  and  $V_{CC} < 2.4V$ , the V3 input impedance will be low (10k $\Omega$  typical).

### Threshold Accuracy

Consider a 5V system with  $\pm 5\%$  tolerance. The 5V supply may vary between 4.75V to 5.25V. System ICs powered by this supply must operate reliably within this band (and a little more as explained below). A perfectly accurate supervisor for this supply generates a reset at exactly 4.75V, however no supervisor is this perfect. The actual reset threshold of a supervisor varies over a specified band; the LTC2931 varies  $\pm 1.5\%$  around its nominal threshold voltage (see Figure 1) over temperature.

The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band.

The LTC2931 has a  $\pm 1.5\%$  reset threshold accuracy, so a “5%” threshold is typically set to 6.5% below the nominal input voltage. Therefore, a typical 5V, “5%” threshold is

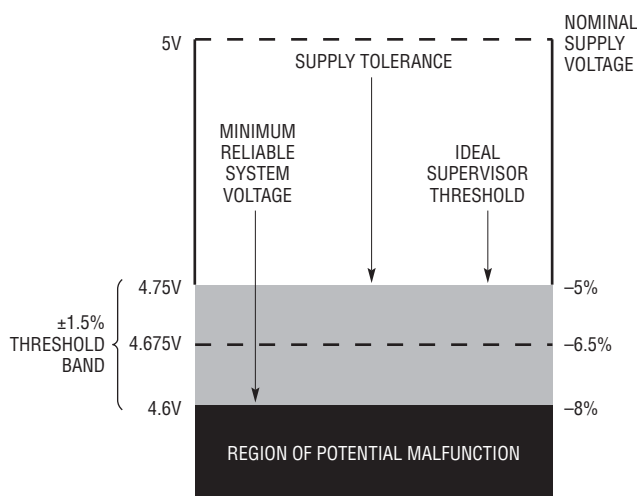


Figure 1. 1.5% Threshold Accuracy Improves System Reliability

4.675V. The threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued.

A less accurate supervisor increases the required system voltage margin and increases the probability of system malfunction. The LTC2931  $\pm 1.5\%$  specification improves the reliability of the system over supervisors with wider threshold tolerances.

### Monitor Configuration

Select the LTC2931 input voltage combination by placing the recommended resistive divider from VREF to GND and connecting the tap point to VPG, as shown in Figure 2. Table 1 offers recommended 1% resistor values for each of the 16 modes. The last column in Table 1 specifies optimum  $V_{PG}/V_{REF}$  ratios ( $\pm 0.01$ ), when configuring with a ratiometric DAC.

At power-up, once V1 or V2 reaches 2.4V, the monitor enters a setup period of approximately 150 $\mu$ s. During the setup time, the voltage on the VPG pin is sampled and the monitor is configured to the desired input combina-

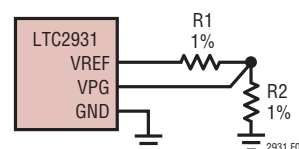


Figure 2. Mode Selection

## APPLICATIONS INFORMATION

Table 1. Voltage Threshold Modes\*

| MODE | V1 (V) | V2 (V) | V3 (V) | V4 (V) | R1 (k $\Omega$ ) | R2 (k $\Omega$ ) | $\frac{V_{PG}}{V_{REF}}$ |
|------|--------|--------|--------|--------|------------------|------------------|--------------------------|
| 0    | 5.0    | 3.3    | ADJ    | ADJ    | Open             | Short            | 0.000                    |
| 1    | 5.0    | 3.3    | ADJ    | –ADJ   | 93.1             | 9.53             | 0.094                    |
| 2    | 3.3    | 2.5    | ADJ    | ADJ    | 86.6             | 16.2             | 0.156                    |
| 3    | 3.3    | 2.5    | ADJ    | –ADJ   | 78.7             | 22.1             | 0.219                    |
| 4    | 3.3    | 2.5    | 1.5    | ADJ    | 71.5             | 28.0             | 0.281                    |
| 5    | 5.0    | 3.3    | 2.5    | ADJ    | 66.5             | 34.8             | 0.344                    |
| 6    | 5.0    | 3.3    | 2.5    | 1.8    | 59.0             | 40.2             | 0.406                    |
| 7    | 5.0    | 3.3    | 2.5    | 1.5    | 53.6             | 47.5             | 0.469                    |
| 8    | 5.0    | 3.0    | 2.5    | ADJ    | 47.5             | 53.6             | 0.531                    |
| 9    | 5.0    | 3.0    | ADJ    | ADJ    | 40.2             | 59.0             | 0.594                    |
| 10   | 3.3    | 2.5    | 1.8    | 1.5    | 34.8             | 66.5             | 0.656                    |
| 11   | 3.3    | 2.5    | 1.8    | ADJ    | 28.0             | 71.5             | 0.719                    |
| 12   | 3.3    | 2.5    | 1.8    | –ADJ   | 22.1             | 78.7             | 0.781                    |
| 13   | 5.0    | 3.3    | 1.8    | –ADJ   | 16.2             | 86.6             | 0.844                    |
| 14   | 5.0    | 3.3    | 1.8    | ADJ    | 9.53             | 93.1             | 0.906                    |
| 15   | 5.0    | 3.0    | 1.8    | ADJ    | Short            | Open             | 1.000                    |

\*V5 and V6 are always adjustable (ADJ).

tion. The comparators are enabled and supply monitoring begins. Do not add capacitance to the VPG pin.

## Using The Adjustable Thresholds

The reference inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 3). The reference inputs on the V5 and V6 comparators are always set to 0.5V. The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high

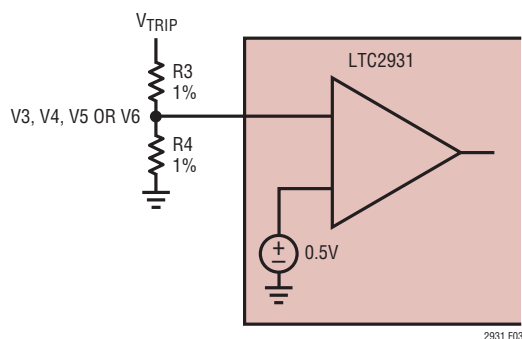


Figure 3. Setting the Positive Adjustable Trip Point

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

| V <sub>SUPPLY</sub> (V) | V <sub>TRIP</sub> (V) | R3 (k $\Omega$ ) | R4 (k $\Omega$ ) |
|-------------------------|-----------------------|------------------|------------------|
| 12                      | 11.25                 | 2150             | 100              |
| 10                      | 9.4                   | 1780             | 100              |
| 8                       | 7.5                   | 1400             | 100              |
| 7.5                     | 7                     | 1300             | 100              |
| 6                       | 5.6                   | 1020             | 100              |
| 5                       | 4.725                 | 845              | 100              |
| 3.3                     | 3.055                 | 511              | 100              |
| 3                       | 2.82                  | 464              | 100              |
| 2.5                     | 2.325                 | 365              | 100              |
| 1.8                     | 1.685                 | 237              | 100              |
| 1.5                     | 1.410                 | 182              | 100              |
| 1.2                     | 1.120                 | 124              | 100              |
| 1                       | 0.933                 | 86.6             | 100              |
| 0.9                     | 0.840                 | 68.1             | 100              |

Table 3. Suggested 1% Resistor Values for the –ADJ Inputs

| V <sub>SUPPLY</sub> (V) | V <sub>TRIP</sub> (V) | R3 (k $\Omega$ ) | R4 (k $\Omega$ ) |
|-------------------------|-----------------------|------------------|------------------|
| –2                      | –1.87                 | 187              | 121              |
| –5                      | –4.64                 | 464              | 121              |
| –5.2                    | –4.87                 | 487              | 121              |
| –10                     | –9.31                 | 931              | 121              |
| –12                     | –11.30                | 1130             | 121              |

impedance, adjustable inputs (V3, V4, V5, V6). Calculate the trip voltage from:

$$V_{TRIP} = 0.5V \cdot \left(1 + \frac{R3}{R4}\right)$$

In the negative adjustable mode, the reference level on the V4 comparator is connected to ground (Figure 4). The tap point on an external resistive divider, connected between

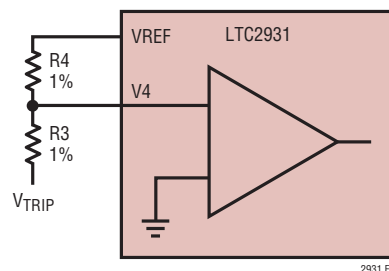


Figure 4. Setting the Negative Adjustable Trip Point

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## APPLICATIONS INFORMATION

the negative voltage being sensed and the VREF pin, is connected to the high impedance adjustable input (V4). VREF provides the necessary level shift required to operate at ground. The negative trip voltage is calculated from:

$$V_{TRIP} = -V_{REF} \cdot \frac{R3}{R4}; V_{REF} = 1.210V \text{ Nominal}$$

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of VREF ( $\pm 1mA$ ). With no other load on VREF, R4 (minimum) is:

$$\frac{1.210V}{1mA} = 1.210k\Omega$$

Tables 2 and 3 offer suggested 1% resistor values for various positive and negative supply adjustable applications assuming 5% monitor thresholds.

Although all six supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the VCC for the device. Filter capacitors on the V3, V4, V5 and V6 inputs are allowed.

### Power-Down

On power-down, once any of the monitor inputs drops below its threshold,  $\overline{RST}$  is held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid ( $V_{CC} < 2V$  typical), the LTC2931 will enter the 150 $\mu s$  setup period when VCC rises above 2.4V max.

### Watchdog Timer

The watchdog circuit monitors a microprocessor's ( $\mu P$ ) activity. The  $\mu P$  is required to change the logic state of the WDI pin on a periodic basis in order to clear the watchdog timer. Whenever  $\overline{RST}$  is low, the watchdog timer is cleared and  $\overline{WDO}$  is set high. The watchdog timer starts when  $\overline{RST}$  goes high. Subsequent edges received on the WDI pin clear the watchdog timer. The watchdog timer continues to run until it times out. Once it times out, internal circuitry brings the  $\overline{WDO}$  pin low.  $\overline{WDO}$  remains low for one reset timeout period unless it is cleared by another edge on the WDI pin or  $\overline{RST}$  goes low.  $\overline{WDO}$  toggles between high and

low as long as the watchdog and reset timers are allowed to time out repeatedly.

To disable the watchdog timer, simply ground the CWT pin (Pin 11). With CWT held at ground, any reset event forces  $\overline{WDO}$  high indefinitely. It is safe to leave the WDI pin unconnected because the weak internal pull-up (10 $\mu A$  typical) pulls WDI high. Tying WDI to V1 or ground is also allowed, but grounding the WDI pin forces the pull-up current to be drawn continuously.

### Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period,  $t_{RST}$ , is adjusted by connecting a capacitor,  $C_{RT}$ , between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{RT} = \frac{t_{RST}}{2M\Omega} = 500[pF/ms] \cdot t_{RST}$$

Leaving the CRT pin unconnected generates a minimum reset timeout of approximately 25 $\mu s$ . Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor leakage (the nominal charging current is 2 $\mu A$ ) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

### Selecting The Watchdog Timing Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog timeout period,  $t_{WD}$ , is adjusted by connecting a capacitor,  $C_{WT}$ , between the CWT pin and ground. The value of this capacitor is determined by:

$$C_{WT} = \frac{t_{WD}}{20M\Omega} = 50[pF/ms] \cdot t_{WD}$$

Leaving the CWT pin unconnected generates a minimum watchdog timeout of approximately 200 $\mu s$ . Maximum watchdog timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor leakage (the nominal charging current is 2 $\mu A$ ) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

## APPLICATIONS INFORMATION

### Supply and Temperature Monitor

Figure 5 illustrates how to configure the LTC2931 to monitor temperature. Temperature is sensed by a thermistor, RNTC, as part of a voltage divider driving adjustable input V6. Output COMP6 goes low when the temperature is higher than the trip point, and is fed back through RHYST to provide hysteresis.

Assume a thermistor (RNTC) with values RHOT at the upper threshold and RCOLD at the lower threshold. Minimize errors arising from V6 input current (15nA maximum) by choosing  $RCOLD \leq 100k\Omega$ , and to limit the loading on VREF, choose  $RHOT \geq 1k\Omega$ . RBIAS and RHYST are calculated from:

$$RBIAS = (RHOT/V_{RTA}) \cdot (V_{REF} - V_{RTA}) = 1.42 \cdot RHOT$$

$$RHYST = \frac{V1}{V_{RTA}} \cdot \frac{(RCOLD \cdot RHOT)}{(RCOLD - RHOT)}$$

V1 is the nominal operating voltage at input V1,  $V_{REF} = 1.210V$ ,  $V_{RTA} = 0.5V$ , and  $RPU < RHYST$ . The closest 1% value was chosen for RHYST.

In Figure 5, the trip points are 115°C with  $RHOT = 11.1k\Omega$  (COMP6 goes low) and 100°C with  $RCOLD = 18.5k\Omega$  (COMP6 goes high). A reset is generated in the event of an over-temperature condition. COMP6 (Temp Good) and COMP5 (Power Good) distinguish over-temperature and undervoltage faults.

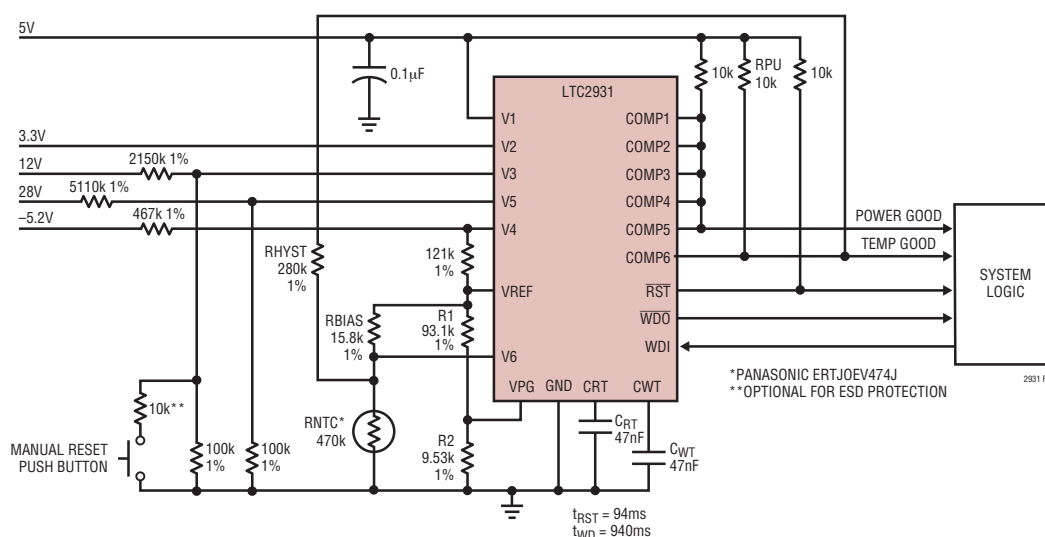


Figure 5. Supply and Temperature Monitor (5V, 3.3V, 28V, -5.2V, 12V, 115°C)

### Five Supply Power-up Sequencer

In Figure 6, the LTC2931's real-time COMP outputs are used to enable DC/DC converters sequentially. The system is powered by a 12V source.

The system is started when the push-button is pressed and the LTC2950-1 brings the RUN pin of the LTM4600 high. Subsequently, the LTM4600 generates a 5V output which applies power to each of the 4 DC/DC converters.

The LTC2931 is configured to mode 13 (see Table 1). When the threshold is reached on V1, COMP1 pulls high. COMP1 then enables the 3.3V converter first. When the threshold is reached on V2, COMP2 pulls high and enables the 1.8V converter next. When all the converters have been enabled and are good, COMP5 pulls high.  $\overline{RST}$  pulls high 9.4ms after COMP5. Figure 7 shows the power-up sequence of the five supplies and the DONE and  $\overline{RST}$  outputs.

If the  $\overline{KILL}$  input on the LTC2950-1 does not receive a logic high within 512ms of initial power-up, EN pulls low and the LTM4600 is powered down.

In the event that the external 12V supply drops below 9.6V, COMP6 and  $\overline{RST}$  will pull low. The LTC2950-1 then receives a logic low on the  $\overline{KILL}$  input, which powers down the LTM4600 and the sequencing circuit.



## APPLICATIONS INFORMATION

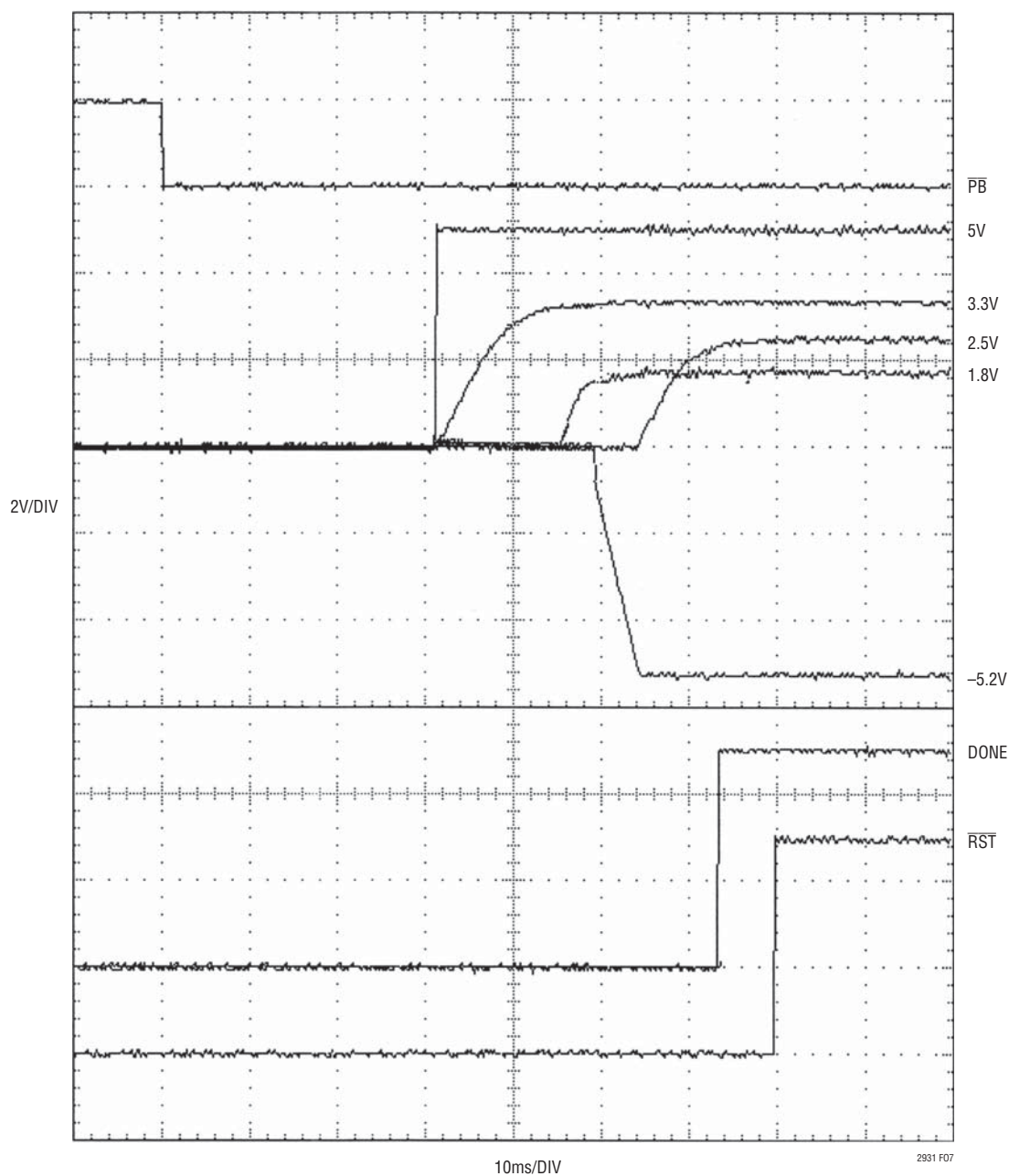
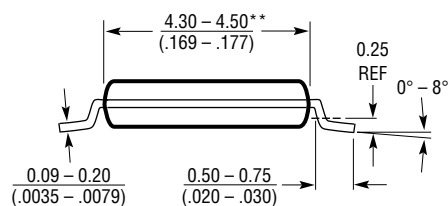
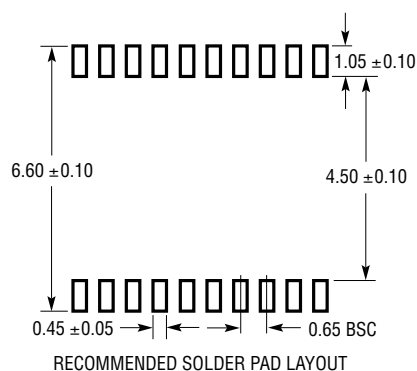


Figure 7. Five Supply Power-Up Sequencing (Based on Circuit in Figure 6)

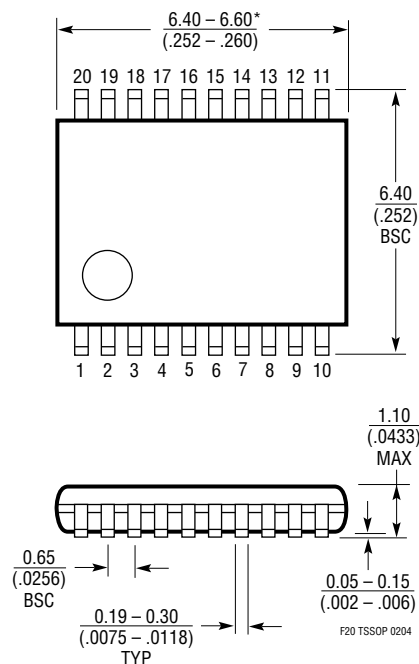
# PACKAGE DESCRIPTION

## F Package 20-Lead Plastic TSSOP (4.4mm) (Reference LTC DWG # 05-08-1650)



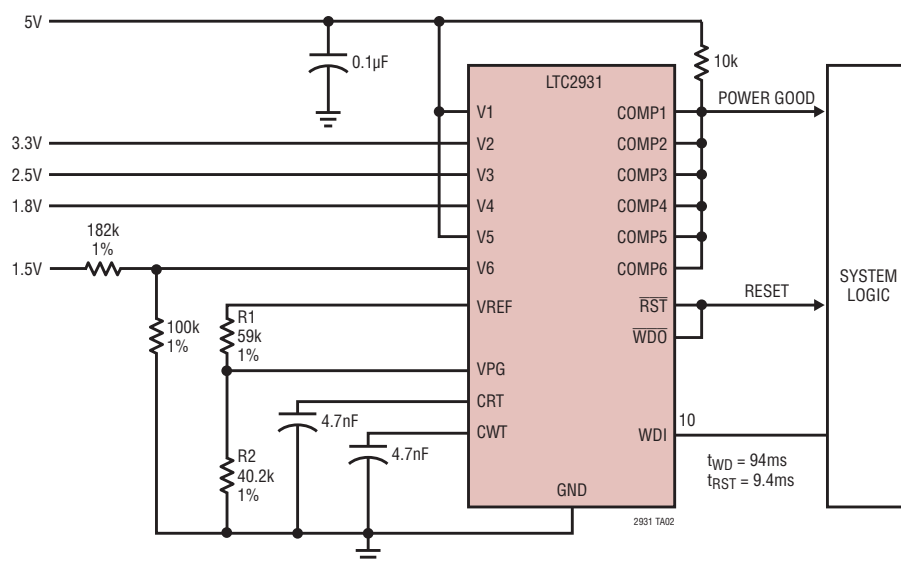
### NOTE:

1. CONTROLLING DIMENSION: MILLIMETERS
  2. DIMENSIONS ARE IN  $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
  3. DRAWING NOT TO SCALE
- \*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
- \*\*DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE



## TYPICAL APPLICATION

System Reset Generated by Watchdog Timing or Supply Voltage Failure



## RELATED PARTS

| PART NUMBER     | DESCRIPTION                                                     | COMMENTS                                                                                            |
|-----------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| LTC690          | 5V Supply Monitor, Watchdog Timer and Battery Backup            | 4.65 Threshold                                                                                      |
| LTC694-3.3      | 3.3V Supply Monitor, Watchdog Timer and Battery Backup          | 2.9V Threshold                                                                                      |
| LTC1232         | 5V Supply Monitor, Watchdog Timer and Pushbutton Reset          | 4.37V/4.62V Threshold                                                                               |
| LTC1326         | Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ      | 4.725V, 3.118V, 1V Threshold ( $\pm 0.75\%$ ) and ADJ                                               |
| LTC1726         | Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ      | Adjustable Reset and Watchdog Timeouts                                                              |
| LTC1727         | Micropower Triple Supply Monitor with Open-Drain Reset          | Individual Monitor Outputs in MSOP                                                                  |
| LTC1728         | Micropower Triple Supply Monitor with Open-Drain Reset          | 5-Lead SOT-23 Package                                                                               |
| LTC1985         | Micropower Triple Supply Monitor with Push-Pull Reset Output    | 5-Lead SOT-23 Package                                                                               |
| LTC2900         | Programmable Quad Supply Monitor                                | Adjustable Reset, 10-Lead MSOP and DFN Packages                                                     |
| LTC2901         | Programmable Quad Supply Monitor                                | Adjustable Reset and Watchdog Timer                                                                 |
| LTC2902         | Programmable Quad Supply Monitor                                | Adjustable Reset and Tolerance                                                                      |
| LTC2903         | Precision Quad Supply Monitor                                   | 6-Lead SOT-23 Package                                                                               |
| LTC2904-LTC2907 | Three-State Programmable Precision Dual Supply Monitor          | 8-Lead SOT-23 and DFN Packages                                                                      |
| LTC2908         | Precision Six Supply Monitor (Four Fixed & Two Adjustable)      | 8-Lead TSOT-23 and DFN Packages                                                                     |
| LTC2909         | Precision Triple/Dual Input UV, OV and Negative Voltage Monitor | Shunt Regulated $V_{CC}$ Pin, Adjustable Threshold and Reset, 8-Lead SOT-23 and DFN Packages        |
| LTC2910         | Precision Octal Positive/Negative Voltage Supply Monitor        | 16-Lead SSOP and 5mm $\times$ 3mm DFN Packages, H-Grade Temperature Range                           |
| LTC2912-LTC2914 | Single/Dual/Quad UV and OV Voltage Monitors                     | Separate $V_{CC}$ Pin, Adjustable Reset Timer, H-Grade Temperature Range                            |
| LTC2915-LTC2918 | Single Supply Monitor with 27 Pin-Selectable Thresholds         | Manual Reset, Watchdog, TSOT-8/MSOP-10 and 3mm $\times$ 2mm DFN Packages, H-Grade Temperature Range |
| LTC2928         | Quad Power Supply Sequencer and Supervisor                      | Easily Configure Power Management without Software, 36-Lead 5mm $\times$ 7mm QFN and SSOP Packages  |

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