

## INTELLIGENT POWER LOW SIDE SWITCH

### Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Up to 50kHz
- Logic level input
- ESD protection

### Description

The AUIPS1025R is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current, over-temperature, ESD protection and drain to source active clamp. This device offers protections and the high reliability required in harsh environments. The switch provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 170°C or when the drain current reaches 22A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

### Product Summary

Rds(on)	35mΩ (max.)
Vclamp	39V
Ishutdown	15A (min.)

### Package

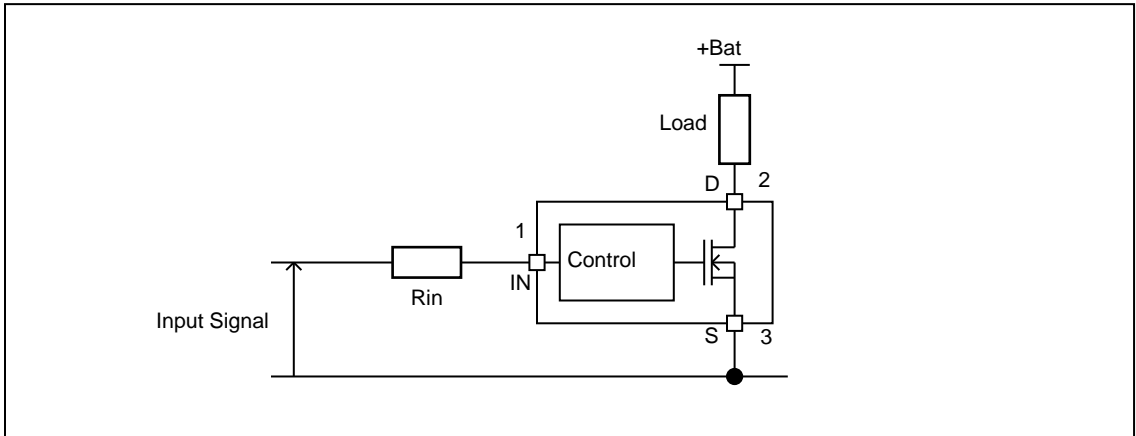


D-Pak  
AUIPS1025R

### Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS1025R	D-Pak-3-Lead	Tube	75	AUIPS1025R
		Tape and reel left	3000	AUIPS1025RTRL

### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (T<sub>ambient</sub>=25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
V <sub>ds</sub>	Maximum drain to source voltage	-0.3	36	V
V <sub>ds cont.</sub>	Maximum continuous drain to source voltage	—	28	V
V <sub>in</sub>	Maximum input voltage	-0.3	6	V
I <sub>sd cont.</sub>	Max. diode continuous current (limited by thermal dissipation)	—	4.5	A
P <sub>d</sub>	Maximum power dissipation (internally limited by thermal protection) R <sub>th</sub> =50°C/W AUIPS1025R 1" sqr. footprint	—	2.5	W
T <sub>j max.</sub>	Maximum operating junction temperature	-40	150	°C
	Maximum storage temperature	-55	150	

## Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
R <sub>th1</sub>	Thermal resistance junction to ambient D-Pak std. footprint	70	—	°C/W
R <sub>th2</sub>	Thermal resistance junction to ambient D-Pak 1" sqr. footprint	50	—	
R <sub>th3</sub>	Thermal resistance junction to case D-Pak	2.6	—	

## Recommended Operating Conditions

These values are given for a quick design.

Symbol	Parameter	Min.	Max.	Units
V <sub>in_On</sub>	High level input voltage	4.5	5.5	V
V <sub>in_Off</sub>	Low level input voltage	0	0.5	
I <sub>ds</sub>	Continuous drain current, T <sub>ambient</sub> =85°C, T <sub>j</sub> =150°C, V <sub>in</sub> =5V R <sub>th</sub> =50°C/W AUIPS1025R 1" sqr. footprint	—	4.9	A
Max F	Max. frequency	—	50	kHz
R <sub>in</sub>	Recommended resistor in series with IN pin (1)	10	1000	Ω
Max Tr <sub>in</sub>	Max. input rising time (from 10% to 90%) (2)	—	50	ns

(1) Input signal of the pulse generator not the voltage on the IN pin of the device. Do not connect any other component on the input.

(2) Max. Tr<sub>in</sub> is for the input signal of the pulse generator not on the IN pin voltage of the device.

## Static Electrical Characteristics

T<sub>j</sub> = -40..150°C, V<sub>cc</sub>=6..28V (unless otherwise specified), typical value are given for T<sub>j</sub>=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>ds(on)</sub>	ON state resistance T <sub>j</sub> =25°C	—	28	35	mΩ	V <sub>in</sub> =5V, I <sub>ds</sub> =10A
	ON state resistance T <sub>j</sub> =150°C (2)	—	47	55		
I <sub>dss1</sub>	Drain to source leakage current	—	15	25	μA	V <sub>cc</sub> =14V, V <sub>in</sub> =0V, T <sub>j</sub> =25°C
I <sub>dss2</sub>	Drain to source leakage current	—	45	60		V <sub>cc</sub> =28V, V <sub>in</sub> =0V, T <sub>j</sub> =25°C
V <sub>clamp1</sub>	Drain to source clamp voltage 1	36	39	—	V	I <sub>d</sub> =20mA
V <sub>clamp2</sub>	Drain to source clamp voltage 2	—	39	—		I <sub>d</sub> =2A
V <sub>in clamp</sub>	IN to source pin clamp voltage	5.5	6.5	7		I <sub>in</sub> =1mA
V <sub>th</sub>	Input threshold voltage	—	1.4	—		V <sub>ds</sub> -V <sub>in</sub> =6V, I <sub>d</sub> =1mA
I <sub>in, on</sub>	ON state IN positive current	50	130	230	μA	V <sub>in</sub> =5V, R <sub>in</sub> =10Ω
T <sub>in_delay</sub>	Delay before turn ON by input signal	1	—	—	ms	V <sub>drain</sub> >6V

## Switching Electrical Characteristics

T<sub>j</sub> = -40..150°C, V<sub>cc</sub>=14V (unless otherwise specified), typical value are given for T<sub>j</sub>=25°C

Resistive load=2Ω, R<sub>input</sub>=10Ω, V<sub>in</sub>=5V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T <sub>d(on)</sub>	Turn-on delay time to 10%	—	100	450	ns	See figure 2
T <sub>r</sub>	Rise time 10% to 90%	—	250	900		
T <sub>d(off)</sub>	Turn-off delay time to 90%	—	500	1650		
T <sub>f</sub>	Fall time 90% to 10%	—	300	1000		

T<sub>j</sub> = -40..150°C, V<sub>cc</sub>=14V (unless otherwise specified), typical value are given for T<sub>j</sub>=25°C

Resistive load=2Ω, R<sub>input</sub>=1000Ω, V<sub>in</sub>=5V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T <sub>d(on)</sub>	Turn-on delay time to 10%	—	750	2500	ns	See figure 2
T <sub>r</sub>	Rise time 10% to 90%	—	1400	4700		
T <sub>d(off)</sub>	Turn-off delay time to 90%	—	3800	12000		
T <sub>f</sub>	Fall time 90% to 10%	—	2200	7000		

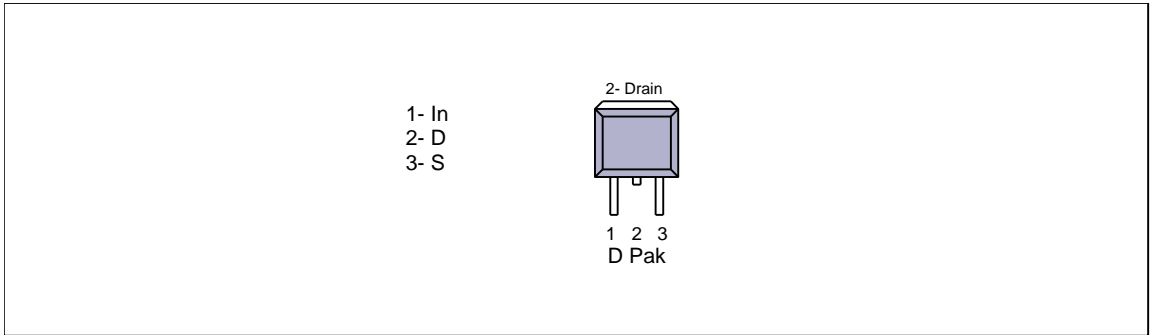
## Protection Characteristics

T<sub>j</sub> = -40..150°C, V<sub>cc</sub>=6..28V (unless otherwise specified), typical value are given for T<sub>j</sub>=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T <sub>sd</sub>	Over temperature threshold	150	170	—	°C	See figure 1
I <sub>sd</sub>	Over current threshold	15	22	32	A	See figure 1
V <sub>reset</sub>	IN protection reset threshold	1	2	3	V	
T <sub>reset</sub>	Time to reset protection	5	30	200	μs	V <sub>in</sub> =0V

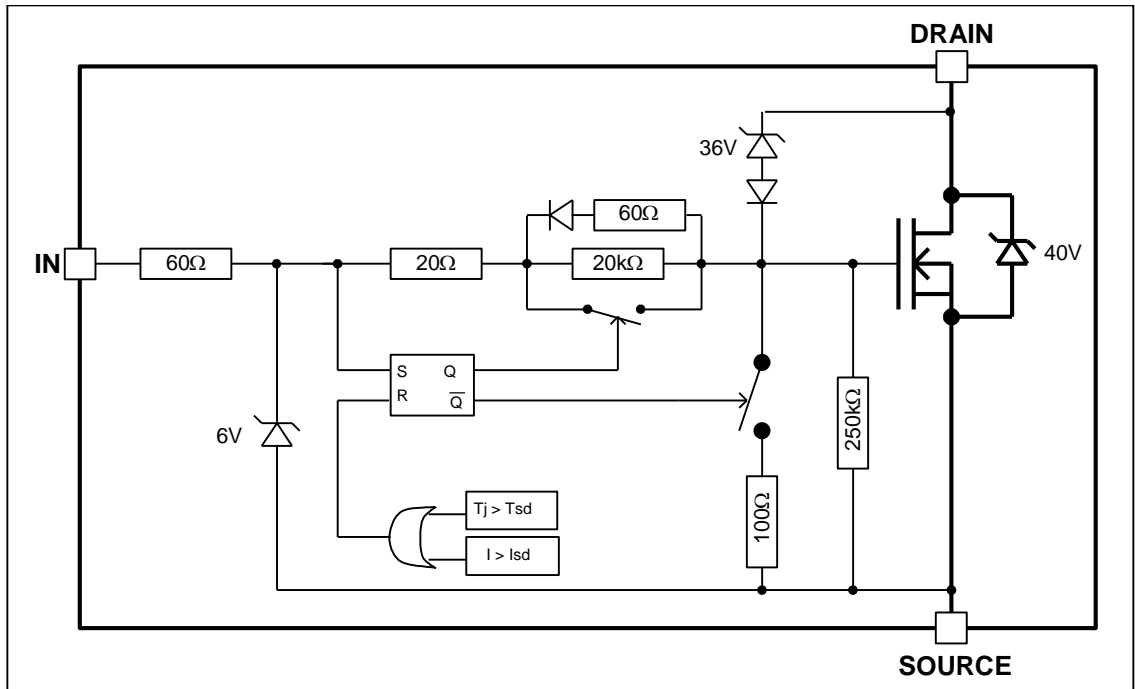
(3) Guaranteed by design

## Lead Assignments



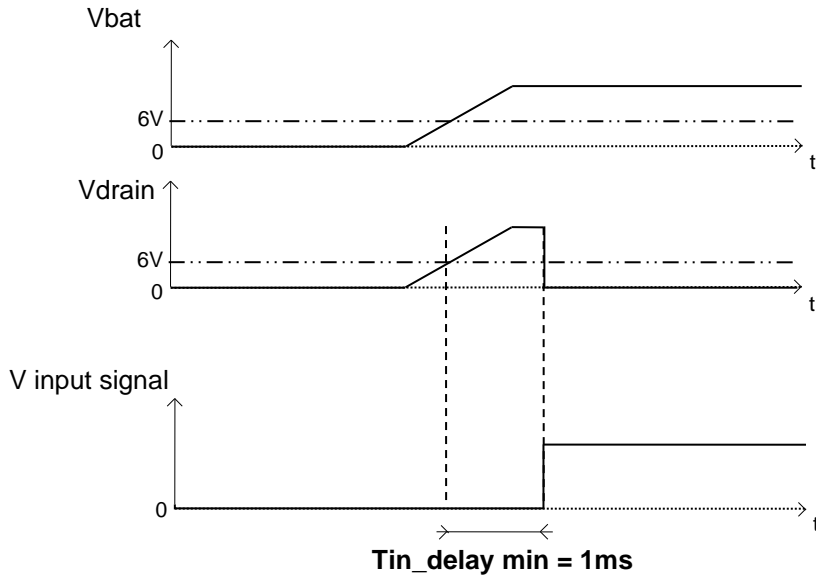
## Functional Block Diagram

All values are typical



## Tin\_delay explanation

The voltage in Drain pin of AUIPS1025R is must be above 6V more than 1ms before turning ON the part by applying the input signal. Otherwise the part could be latched.



All curves are typical values..

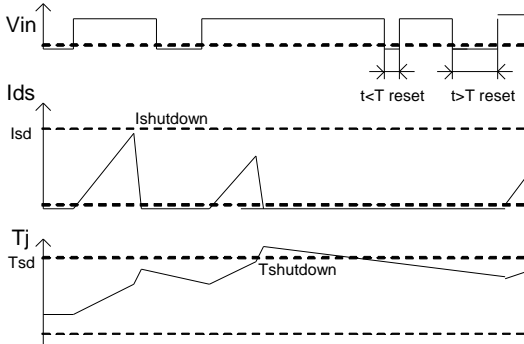


Figure 1 – Timing diagram

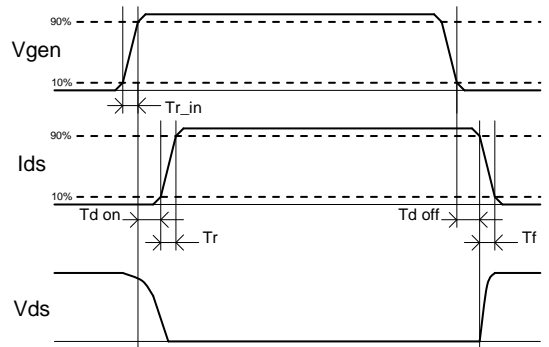
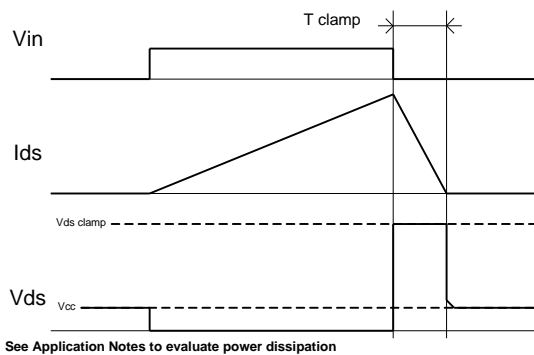


Figure 2 – IN rise time & switching definitions



See Application Notes to evaluate power dissipation

Figure 3 – Active clamp waveforms

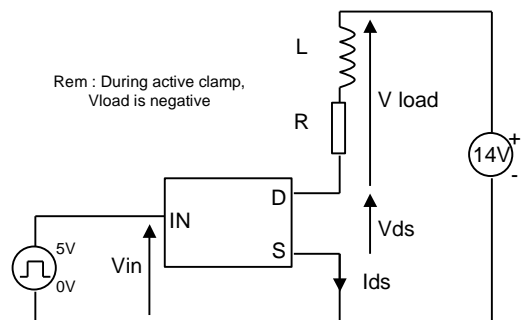
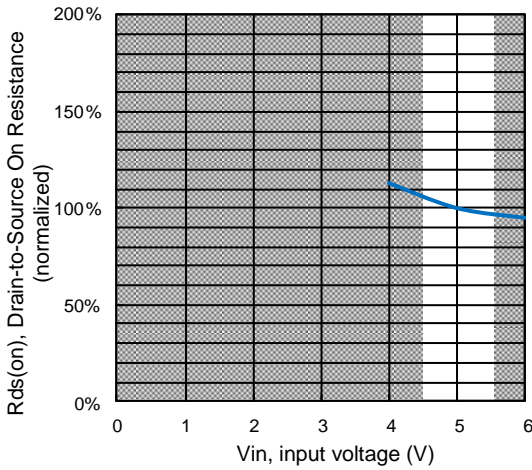
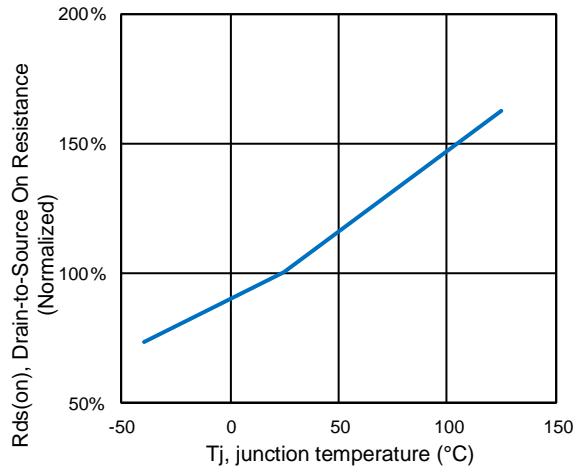


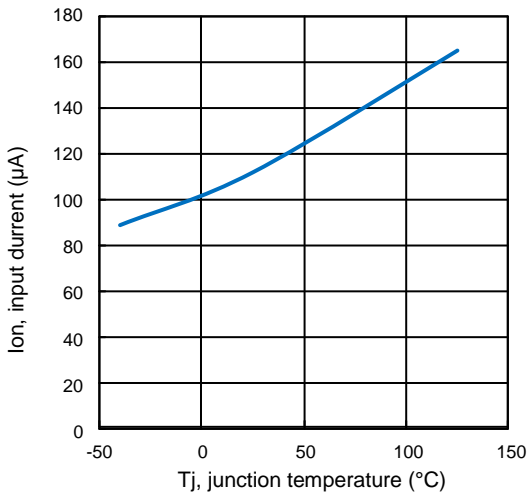
Figure 4 – Active clamp test circuit



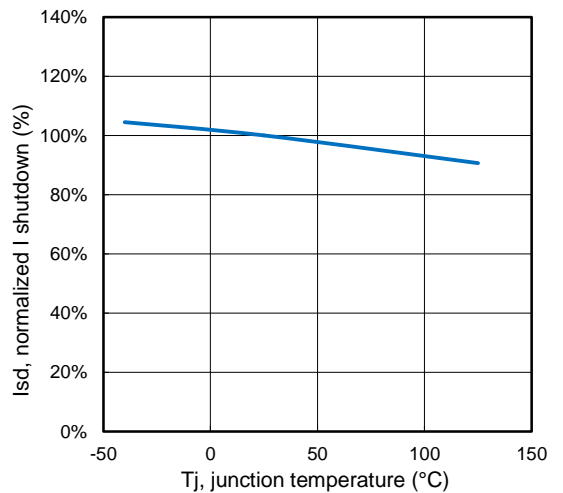
**Figure 5 – Normalized R<sub>ds(on)</sub> (%) Vs Input voltage (V)**



**Figure 6 - Normalized R<sub>ds(on)</sub> (%) Vs T<sub>j</sub> (°C)**

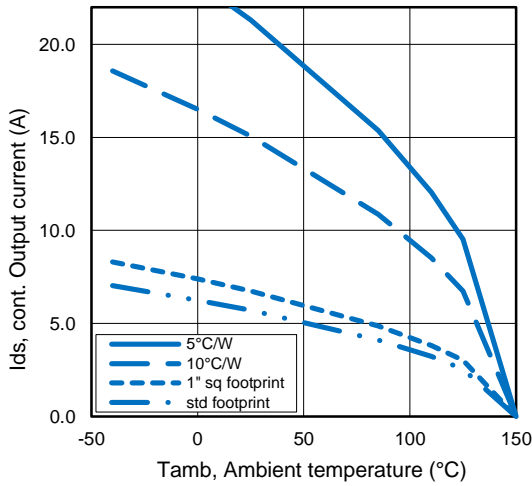


**Figure 7 – Input current (µA) On Vs junction temperature (°C)**

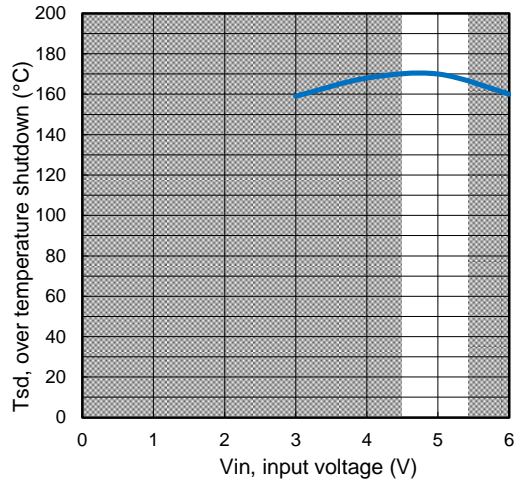


**Figure 8 – Normalized I shutdown (%) Vs junction temperature (°C)**

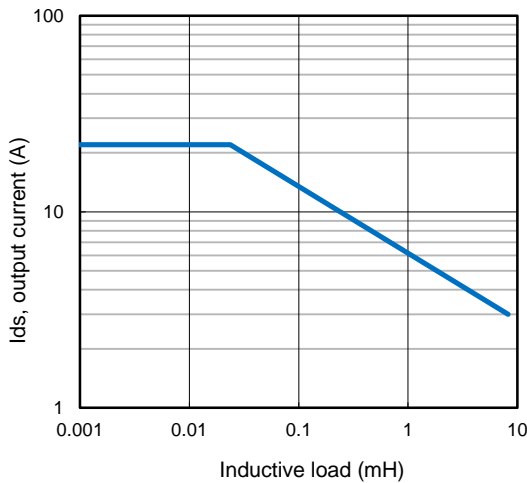




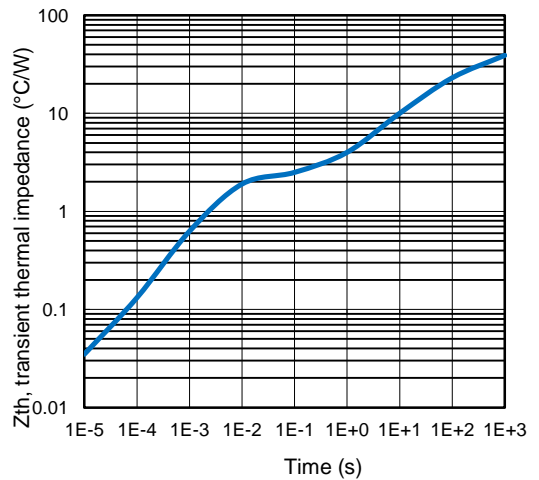
**Figure 9 – Max. continuous output current (A) Vs Ambient temperature (°C)**



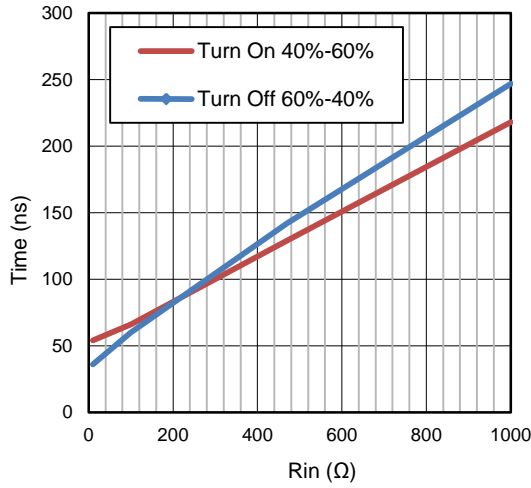
**Figure 10 – Over temperature shutdown (°C) Vs input voltage (V)**



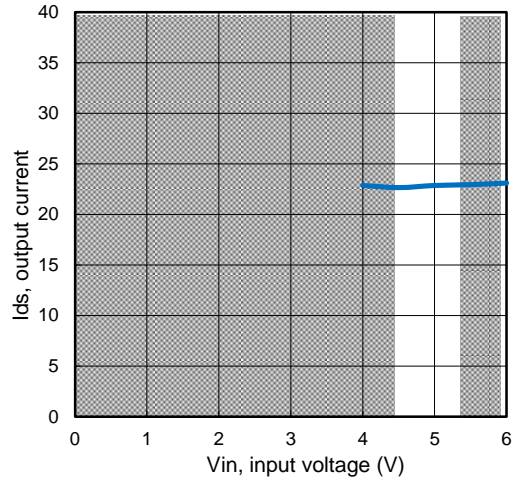
**Figure 11 – Max. output current (A) Vs Inductive load (mH)**



**Figure 12 – Transient thermal impedance (°C/W) Vs time (s)**

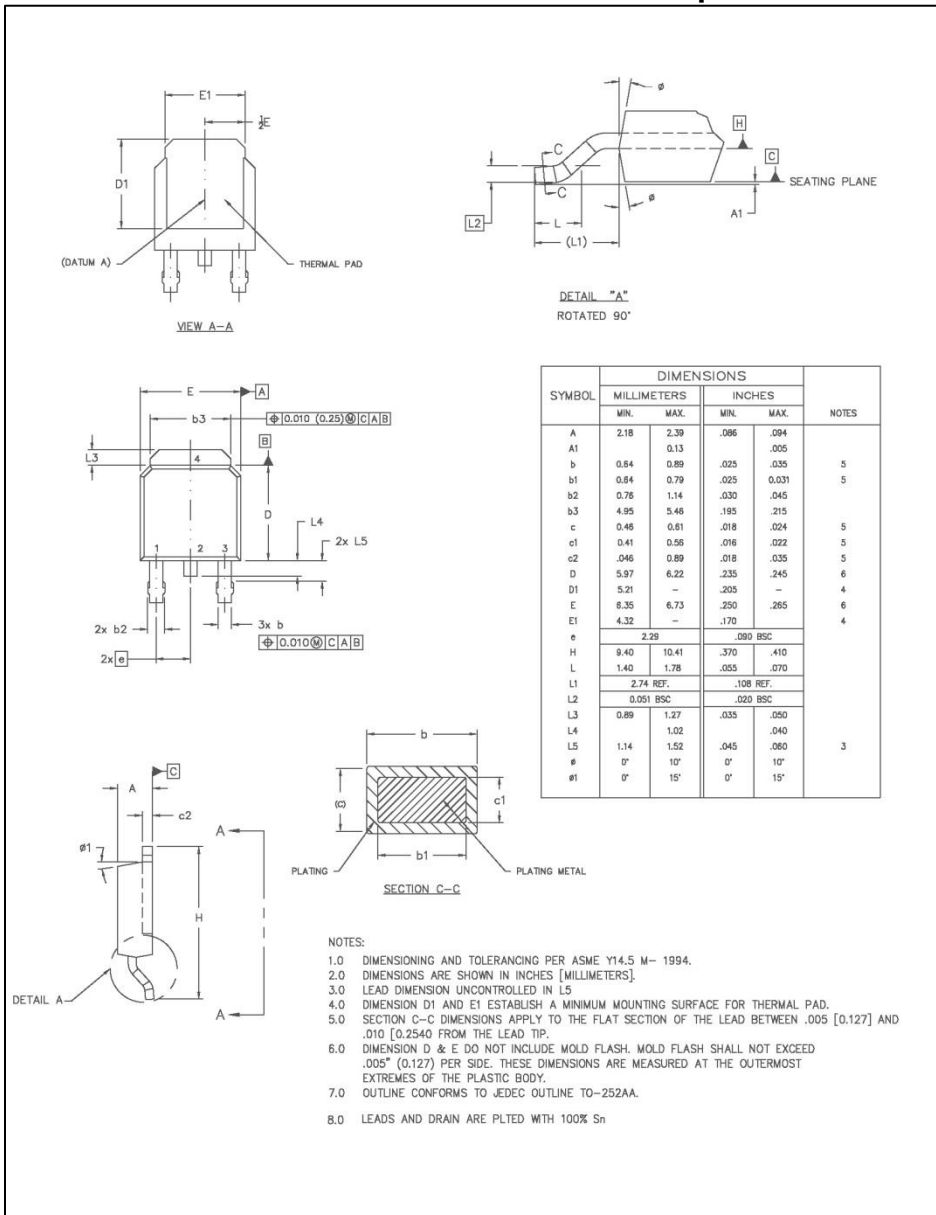


**Figure 13 – time (ns) vs Rin (Ω)**



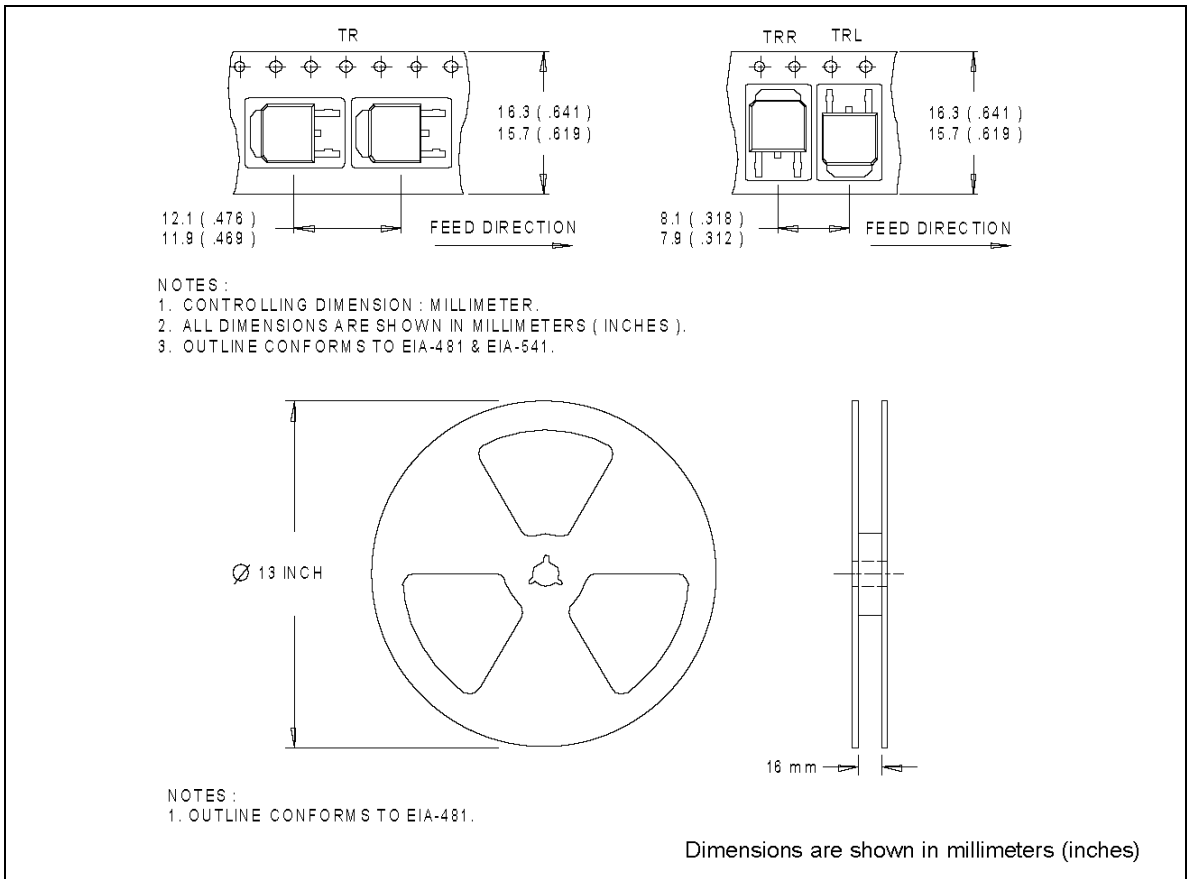
**Figure 14 – Current shutdown (A) Vs Input voltage (V)**

## Case Outline – D-Pak - Automotive Q100 PbF MSL1 qualified



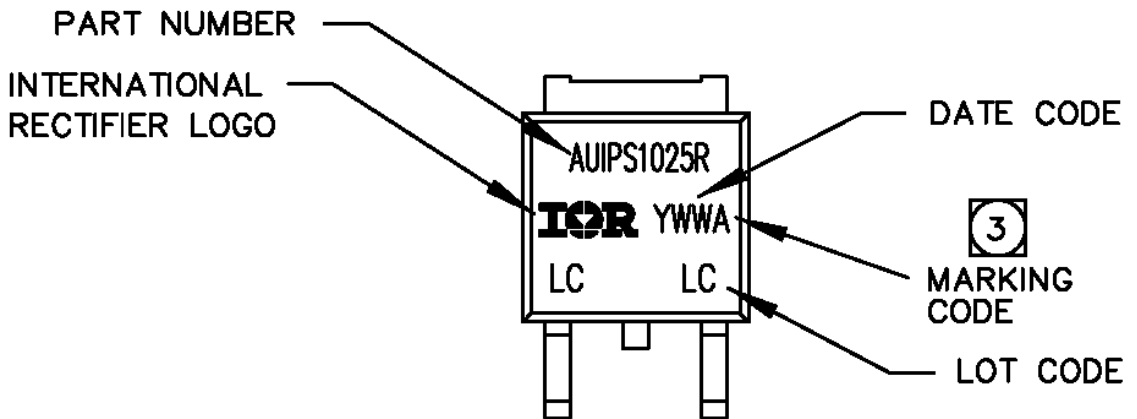
Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

## Tape & Reel - D-Pak



Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

## Part Marking Information



## Qualification Information†

<b>Qualification Level</b>		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		DPAK-3L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M4 (+/-500V) (per AEC-Q100-003)	
	Human Body Model	Class 3A (+/-4500V) (per AEC-Q100-002)	
	Charged Device Model	Class C5 (+/-1000V) (per AEC-Q100-011)	
<b>IC Latch-Up Test</b>		Class II Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

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## Revision History

Revision	Date	Notes/Changes
A	October 10, 2015	Initial release
Rev 1.1	March 25, 2016	Page 6 curve updated for Tin_delay explanation