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RF6559

4.0V TO 4.5V, 915MHZ ISM BAND TRANSMIT/RECEIVE MODULE

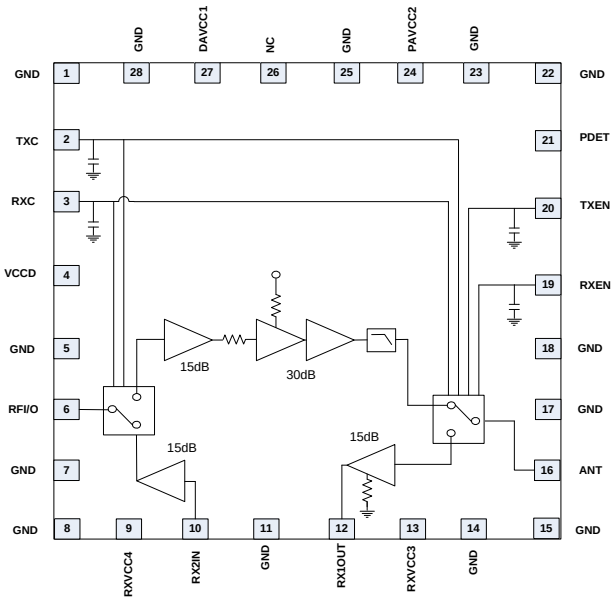
Package: LGA, 28-pin, 6mm x 6mm

Features

- Tx Output Power: 28dBm
- Tx Gain: 42dB
- Integrated Single Port Rx/Tx 50Ω Bi-directional Transceiver Interface
- LNA with Bypass Mode

Applications

- Wireless Automated Metering
- Wireless Alarm Systems
- Portable Battery Powered Equipment
- Smart Energy
- 868MHz/915MHz ISM Band Applications
- Single Chip RF Front End Module



Functional Block Diagram

Product Description

The RF6559 front end module is intended for use in 915MHz AMR solutions. The RF6559 addresses the need for aggressive size reduction for a typical 915MHz AMR front end design and greatly reduces the number of components outside the RF6559 thus minimizing the footprint and assembly cost of the overall solution. The RF6559 contains an integrated three stage power amplifier which provides 42dB of Gain and typical Power output of 28dBm. The RF6559 allows for Tx/Rx on a single antenna via the 2 integrated SPDT switches. Tx filtering, built in power detector and a two stage LNA which provides a typical 32dB of gain round out the inside of this module. All the functionality ofthe RF6559 is packaged in a 28-pin, 6mm x 6mm laminate package with backside ground. Greatly minimizes next level board space and allows for simplified integration.

Ordering Information

RF6559	ISM Band Transmit/Receive Module
RF6559SB	5-Piece Bag
RF6559SR	Standard 100-Piece Reel
RF6559TR13	Standard 2500-Piece reel
RF6559PCK-410	Fully Assembled Evaluation Board and 5-Piece Bag

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Battery Voltage	5.25	V
RF Input Power	-8	dBm
Operating Temperature	-40 to +105	°C
Storage Temperature	-40 to +150	°C
ESD, HBM (All Pins)	750	V
ESD, CDM (All Pins)	750	V
MSL	MSL 3	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Specifications					
Frequency	868	902 to 928		MHz	
RF Port Impedance		50		Ω	
Operating Voltage	4.0	4.2	4.5	V	
Module Leakage Current		1.64		μA	
Tx High Power Mode					
Input Power	-16	-10	-8	dBm	
PSA	27		30	dBm	P_{SAT}
Operating Output Power (+85°C to +105°C)	26			dBm	P_{SAT}
Large Signal Gain	38	42		dB	
Input Return Loss	7	8		dB	
Operating Current		340	385	mA	
P_{DET} Voltage Range	1		3	V	
P_{DET} Power Range	20		30	dBm	
P_{DET} Gradient		TBD			
P_{DET} Tempature Variation		TBD			
Stability	10:1				
Rx Mode					
Gain	28	32	35	dB	
Current	6	8	20	mA	
NF		1.8	2.2	dB	
Input IP3	-18	-11		dBm	
Input P1dB	-23	-20		dBm	
Input Return Loss	3.5	5		dB	
Output Return Loss	10	12		dB	
Antenna Switch Section					
Isolation	20	36		dB	Any used port to any unused port
2Fo Harmonic		-43	-5	dBc	
3Fo Harmonic		-50	-45	dBc	
4Fo Harmonic		-53	-45	dBc	
5Fo Harmonic		-43	-40	dBc	
6Fo to 10Fo Harmonic		-46	-45	dBc	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Switch Section					
Isolation	20			dB	
Return Loss (Rx)	10	15		dB	
Return Loss (Tx)	10	15		dB	
Logic Circuit and Power Supply					
V_{CC_DIG}	4.0	4.2	4.5	V	Digital Supply Voltage
I_{CC_DIG}; Rx Mode		5	8	mA	
I_{CC_DIG}; Tx Mode		7	12	mA	
Control Logic: High	2.7	4.0	4.3	V	
Control Logic: Low		0.2	0.3	V	
Control Logic: High Current TXC and RXC		0.1	0.5	µA	
Control Logic: RXEN		20	100	µA	
Control Logic: TXEN		140	500	µA	
Control Logic: Low Current		0.1	1	µA	TXC, RXC, RX Enable, TX Enable

Operating Mode	Logic Table				Typical Current Draw (mA)			
	TXC	RXC	TXEN	RXEN	Total	TX	RX	Digital
Tx	High	Low	High	Low	337	330	0.00064	7
Rx	Low	High	Low	High	17	0.0005	12	5
All Off	Low	Low	Low	Low	0.00164	0.0005	0.00064	0.0005

NOTES:
*Switch Control Logic High = Min 2.7V to Max 4.3V
*Switch Control Logic Low = Min 0.0V to Max 0.3V

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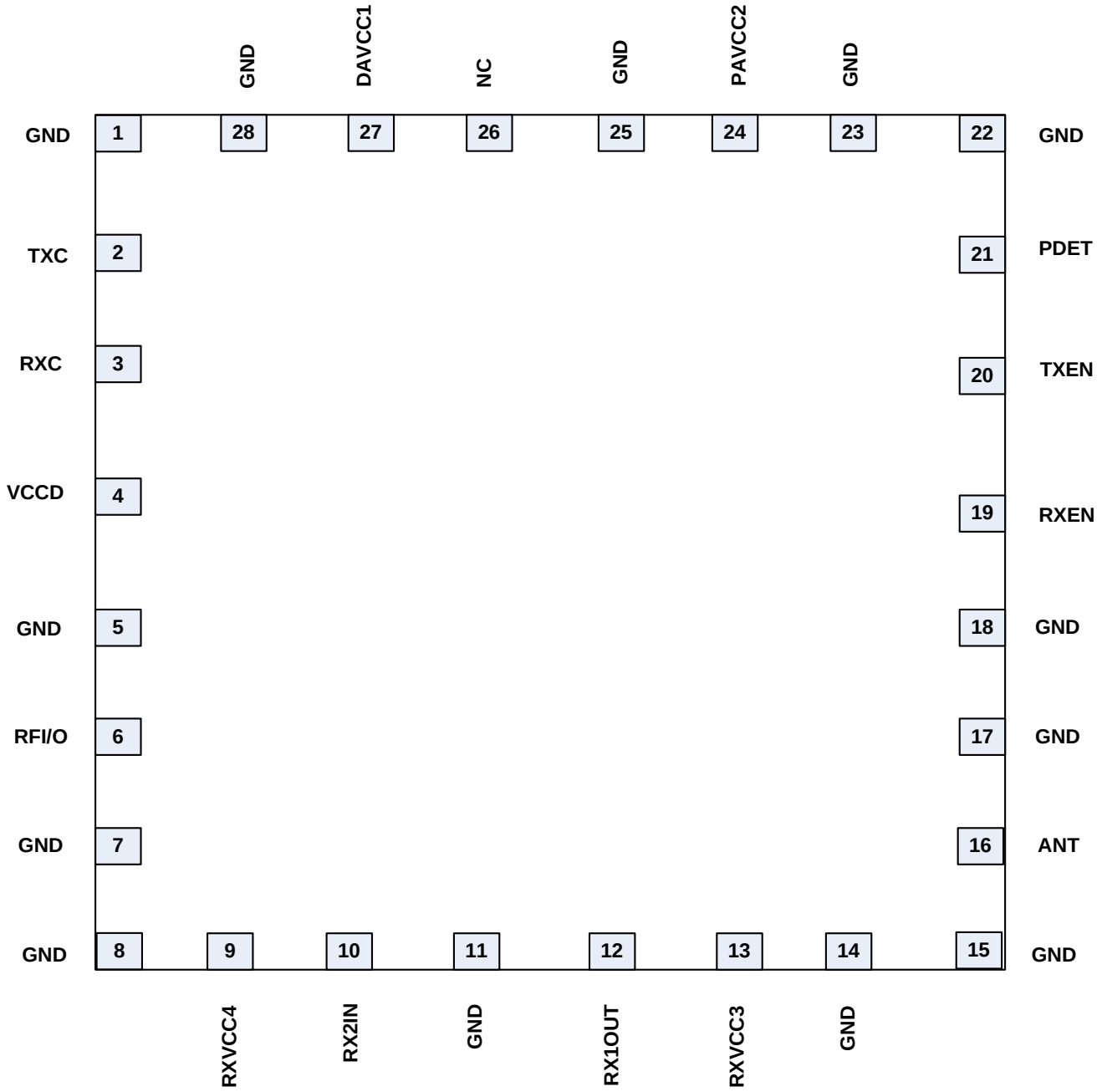
Pin Out



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Pin Names and Descriptions

Pin	Name	Description
1	GND	Corner Ground
2	TXC	Tx Switch Control Input
3	RXC	Rx Switch Control Input
4	VCCD	Digital Reference Voltage Input
5	GND	Ground
6	RFI/O	Module RF Tx Input / Rx Output, DC Blocked
7	GND	Ground
8	GND	Corner Ground
9	RXVCC4	LNA 2nd Stage Battery Bias
10	RX2IN	LNA 2nd Stage RF Input
11	GND	Ground
12	RX1OUT	LNA 1st Stage RF Output
13	RXVCC3	LNA 1st Stage Battery Bias
14	GND	Ground
15	GND	Corner Ground
16	ANT	Antenna RF Output/Input, DC Blocked
17	GND	Ground
18	GND	Ground
19	RXEN	Enable Voltage Input for Receive Channel
20	TXEN	Enable Voltage Input for Transmit Channel
21	PDET	PA Power Detected Voltage Output
22	GND	Corner Ground
23	GND	Ground
24	PAVCC2	Battery Bias Input for Final PA Stage
25	GND	Ground
26	NC	No Connect
27	DAVCC1	Battery Bias Input for Driver Stage
28	GND	Ground
29	GND	Center Ground Flag

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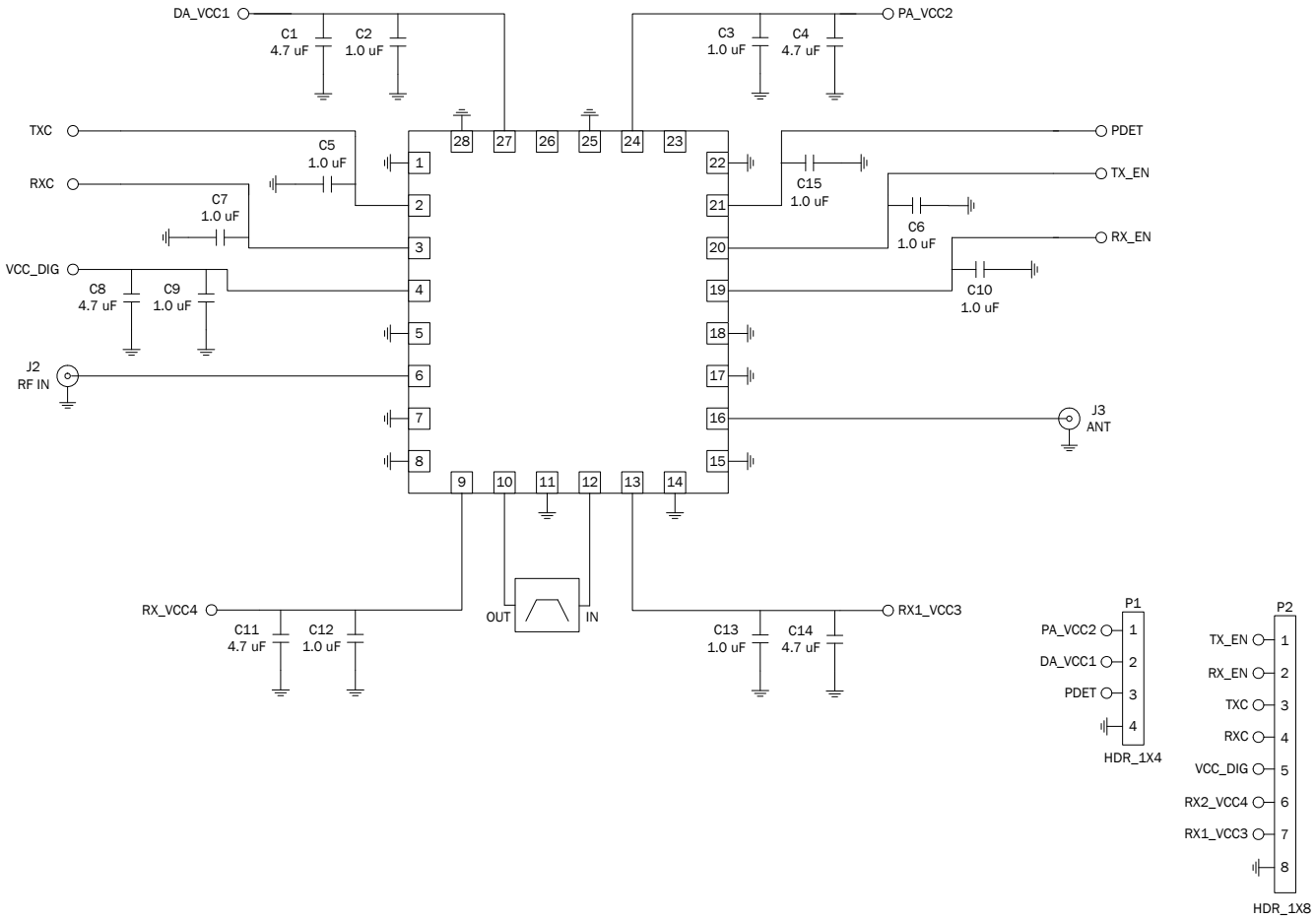
Evaluation Board Schematic



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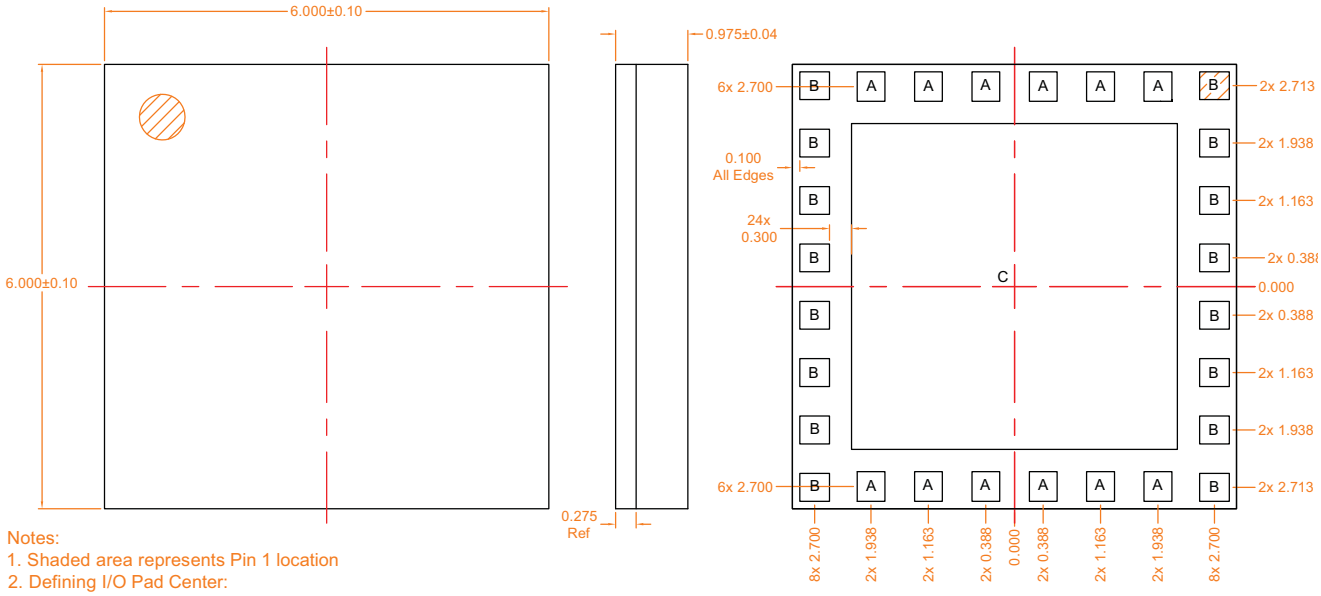
Package Drawing
28-pin, 6mm x 6mm



Notes:
1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:
   To define center of the I/O pad opening, draw a right triangle in one corner of the I/O pad
   Then take the center of the hypotenuse to determine center of I/O pad

A = 0.375 x 0.400 mm
B = 0.400 x 0.375 mm
C = 4.400 x 4.400 mm

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PCB Design Requirements

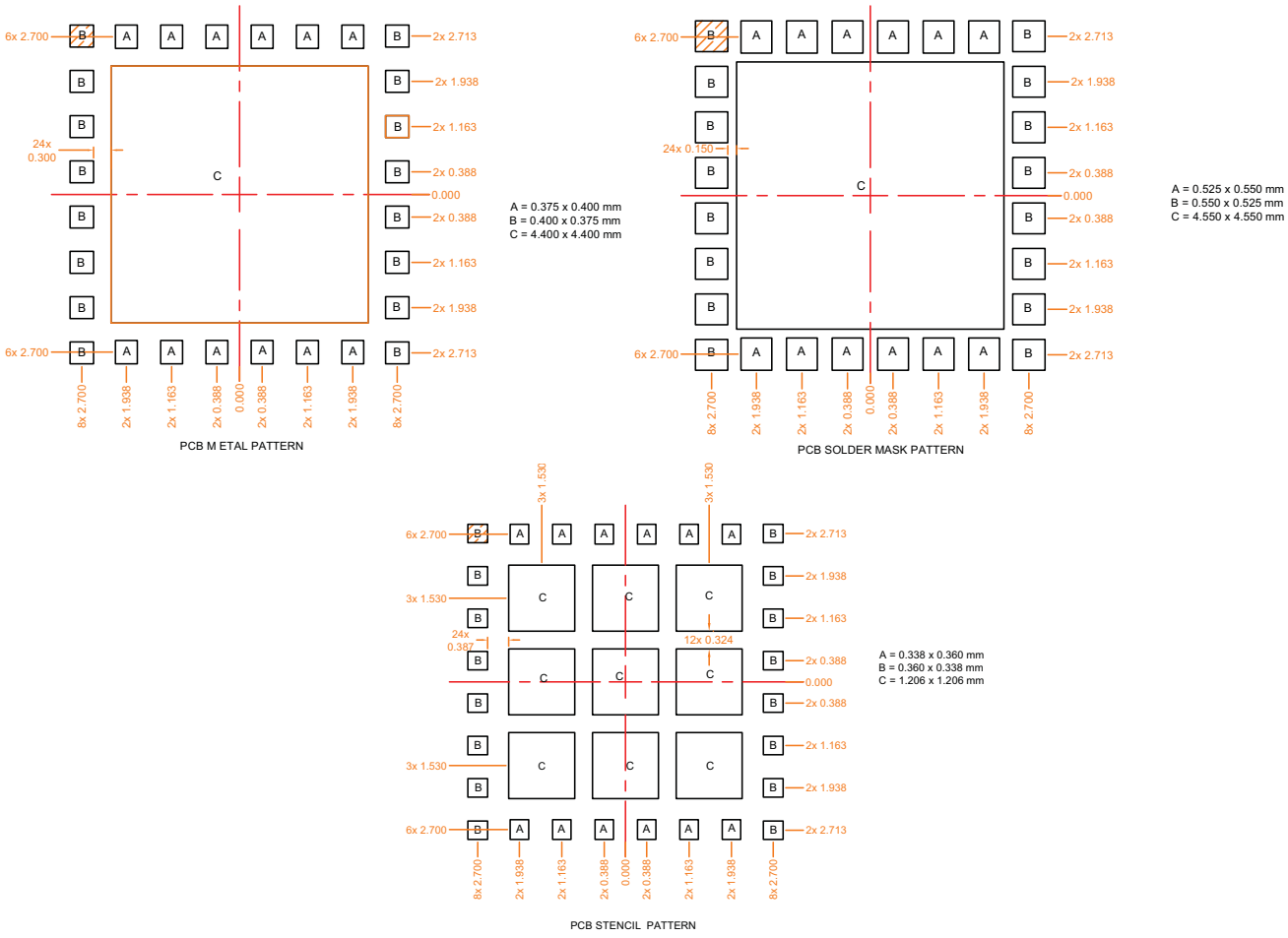
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



Notes:
Shaded area represents PIN 1.

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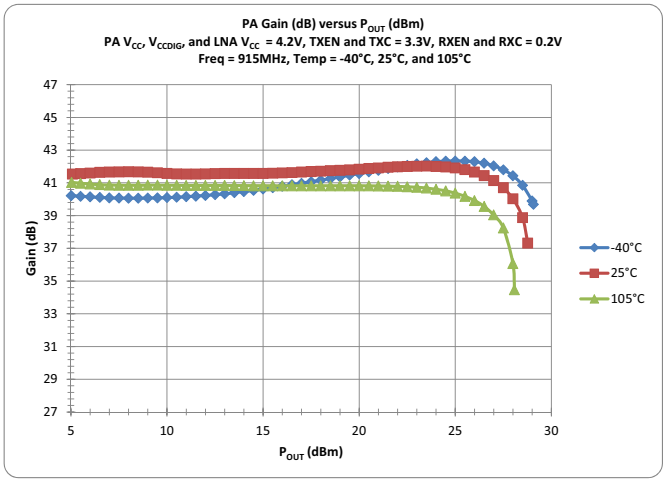
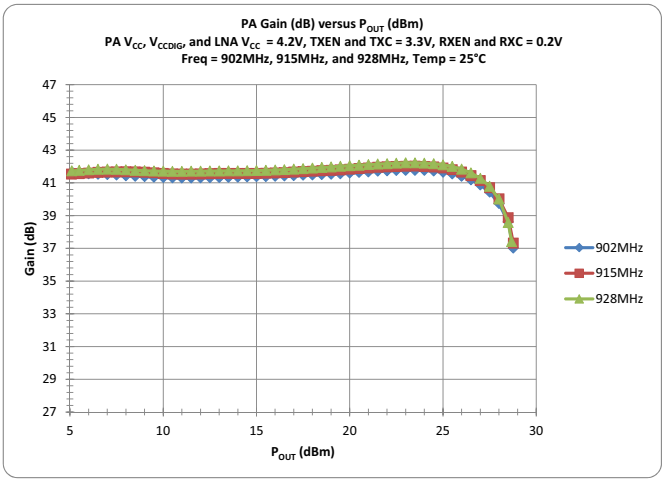
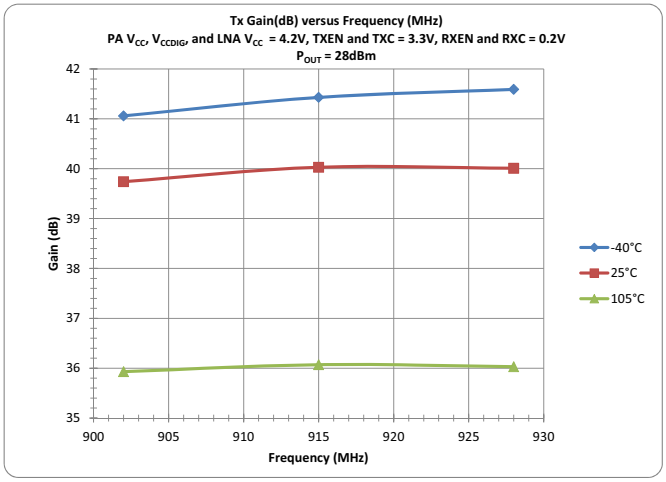
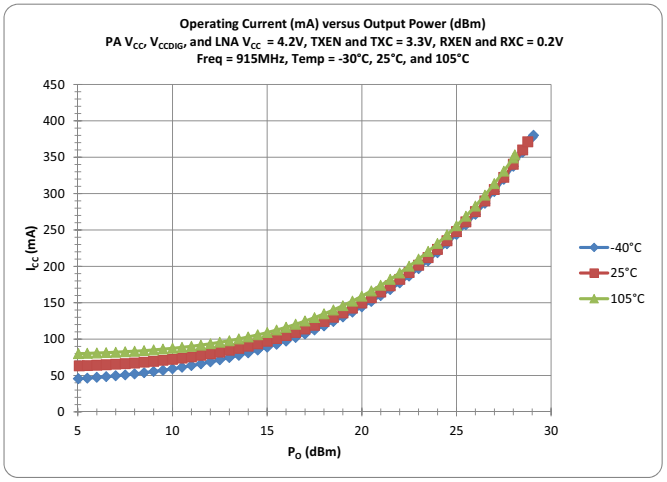
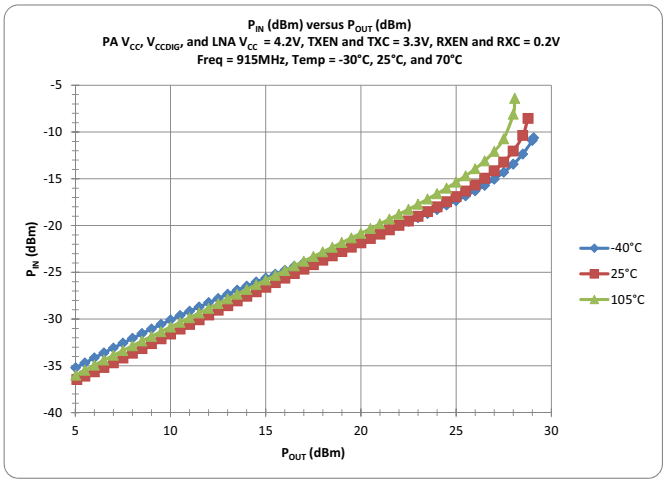
Typical Performance

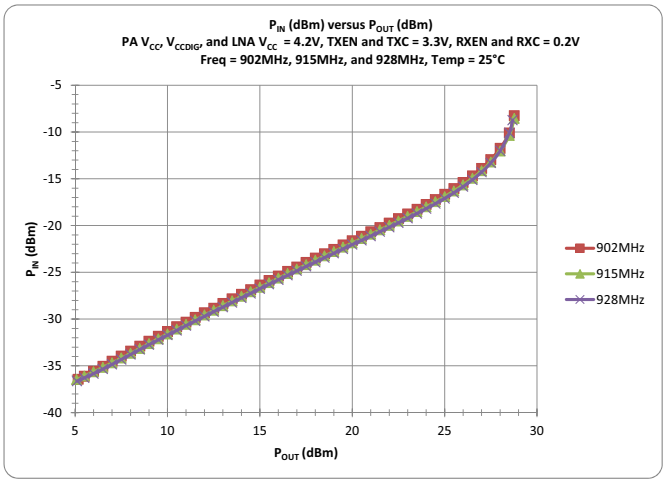




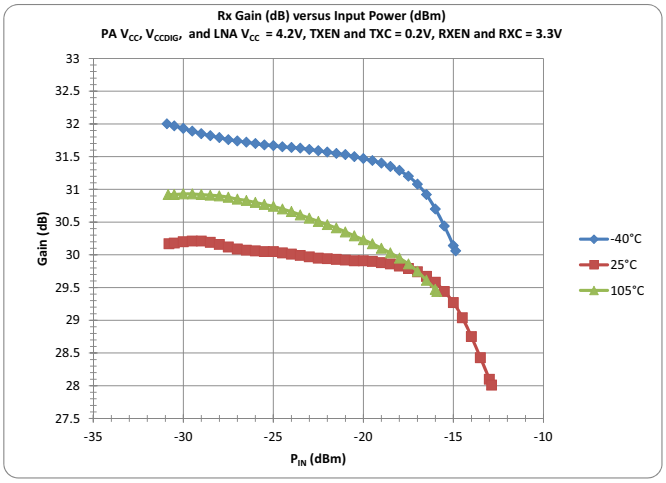


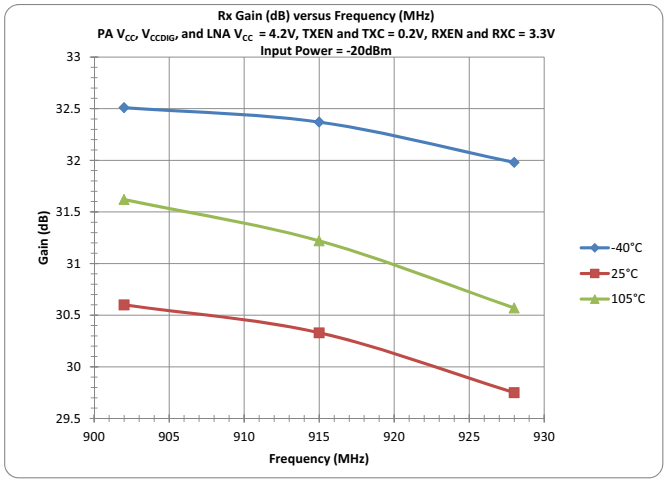


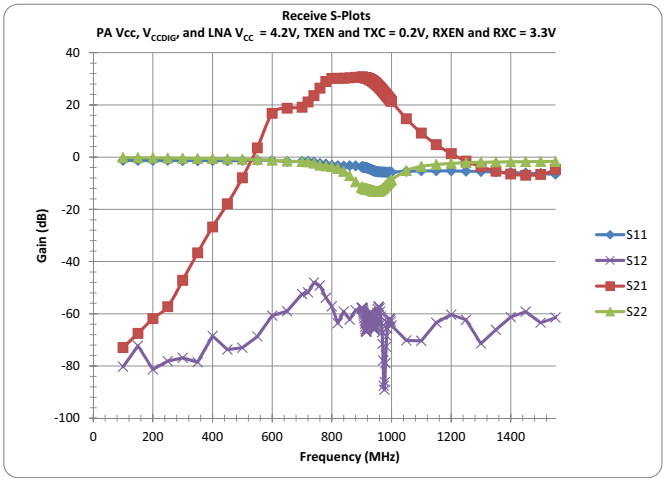


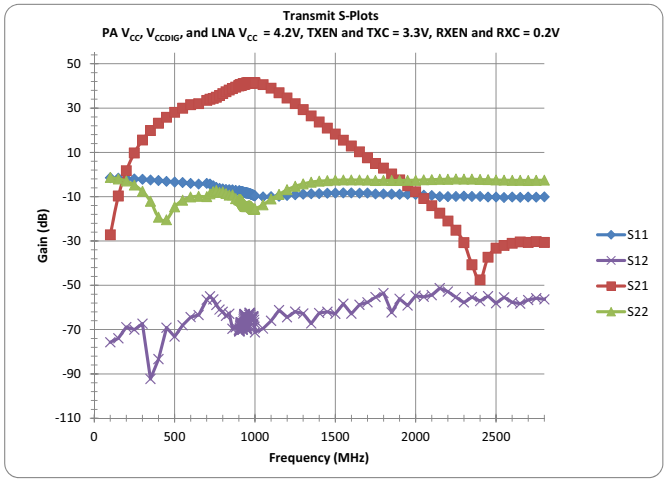


Typical Performance









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