10-Bit, SDTV Video Decoder with Differential Inputs

Data Sheet

ADV7182A

FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit ADC, 4× oversampling per channel for CVBS, S-Video mode, and YPrPb
- 4 analog video input channels with on-chip antialiasing filter
- Video input support for CVBS (composite), S-Video (Y/C), and YPrPb (component)
- Fully differential, pseudo differential, and single-ended CVBS video input support
- NTSC/PAL/SECAM autodetection
- Up to 4 V common-mode input range solution
- Excellent common-mode rejection capability
- 5-line adaptive comb filters and CTI/DNR video enhancement
- Integrated AGC with adaptive peak white mode
- Fast switch capability
- ACE
- Downdither (8 bits to 6 bits)
- Rovi copy protection detection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, or field synchronization
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode available
- 2-wire serial MPU interface (I^2C compatible)
- Single 1.8 V supply possible
- −40°C to +105°C automotive temperature grade
- −40°C to +85°C industrial qualified temperature grade
- 32-lead, 5 mm × 5 mm, RoHS compliant LFCSP
- Qualified for automotive applications

APPLICATIONS

- Advanced driver assistance
- Automotive infotainment
- DVRs for video security
- Media players

GENERAL DESCRIPTION

The ADV7182A[1] has the same pinout and is software compatible with the ADV7182.

The ADV7182A is a versatile, one chip, multiformat video decoder that automatically detects standard analog baseband video signals and converts them into YCbCr 4:2:2 component video data streams.

The analog input of the ADV7182A features a single, 10-bit analog-to-digital converter (ADC) and an on-chip differential to single-ended converter to accommodate direct connection of differential, pseudo differential, or single-ended CVBS without the need for external amplifier circuitry.

The standard definition processor (SDP) on the ADV7182A automatically detects NTSC, PAL, and SECAM standards in the form of CVBS (composite), S-Video (Y/C), and YPrPb (component). The analog video is converted into a 4:2:2 component video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard. External synchronization timing signals are also available.

The ADV7182A is provided in a space-saving, LFCSP, surface-mount, RoHS compliant package. It is offered in an automotive grade rated over the −40°C to +105°C temperature range, as well as a −40°C to +85°C industrial temperature range, making the device ideal for automotive, industrial, and consumer applications.

The ADV7182A must be configured in accordance with the I^2C writes provided in the evaluation board script files available at www.analog.com/ADV7182A.

[1] Protected by U.S. Patent 5,784,120.

Rev. 0

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REVISION HISTORY

9/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

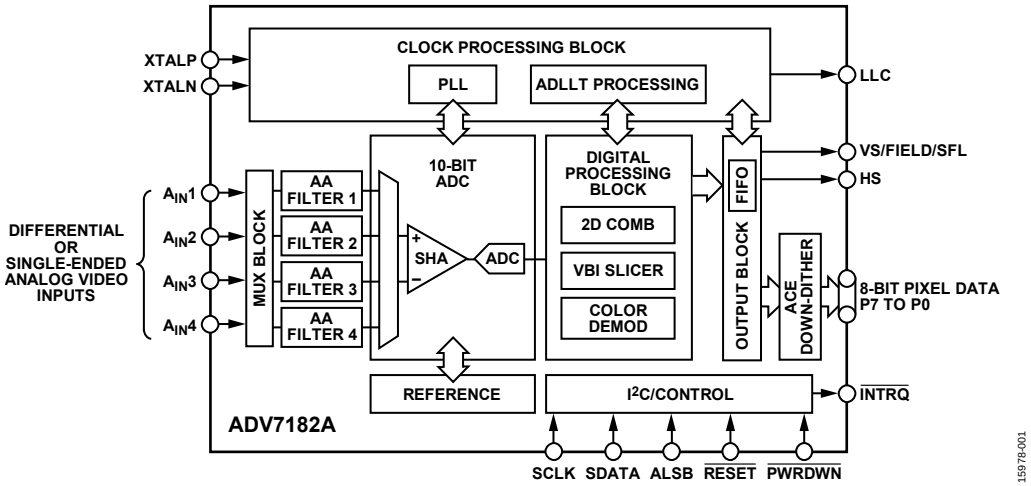

Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}					
D_{VDDIO} = 3.3 V			2			V
D_{VDDIO} = 1.8 V			1.2			V
Input Low Voltage	V_{IL}					
D_{VDDIO} = 3.3 V					0.8	V
D_{VDDIO} = 1.8 V					0.4	V
Crystal Inputs						
V_{IH}			1.2			V
V_{IL}					0.4	V
Input Leakage Current	I_{IN}		−10		+10	µA
SDATA, SCLK			−10		+15	µA
$\overline{\text{PWRDWN}}$, ALSB			−10		+48	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}					
D_{VDDIO} = 3.3 V		I_{SOURCE} = 0.4 mA	2.4			V
D_{VDDIO} = 1.8 V		I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage	V_{OL}					
D_{VDDIO} = 3.3 V		I_{SINK} = 3.2 mA			0.4	V
D_{VDDIO} = 1.8 V		I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2]						
Digital Input/Output Power Supply	D_{VDDIO}		1.62	3.3	3.63	V
Phase-Locked Loop (PLL) Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
Digital Input/Output Supply Current	I_{DVDDIO}			3		mA
PLL Supply Current	I_{PVDD}			12		mA
Analog Supply Current	I_{AVDD}	Single-ended CVBS input		47		mA
		Differential CVBS input		69		mA
		Single-ended CVBS fast switch		47		mA
		Differential CVBS fast switch		69		mA
		S-Video input		60		mA
		YPrPb input		75		mA
Digital Supply Current	I_{DVDD}	Single-ended CVBS input		60		mA
		Differential CVBS input		66		mA
		Single-ended CVBS fast switch		60		mA
		Differential CVBS fast switch		66		mA
		S-Video input		60		mA
		YPrPb input		60		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DOWN PERFORMANCE[1]						
Digital Input/Output Supply Power-Down Current						
PLL Supply Power-Down Current	I_{DVDDIO}			73		µA
Analog Supply Power-Down Current	I_{PVDD}			38		µA
Digital Supply Power-Down Current	I_{AVDD}			0.15		µA
Total Power Dissipation in Power-Down Mode	I_{DVDD}			368		µA
				1		mW
CRYSTAL OSCILLATOR[1]						
Transconductance	g_M			30		mA/V

[1] Guaranteed by characterization.
[2] Typical current consumption values are recorded with nominal voltage supply levels and an SMPTEBAR test pattern.

VIDEO SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulate five step		0.9		Degrees
Differential Gain	DG	CVBS input, modulate five step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five step		2.0		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp		57		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection[2]	CMR			75		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±1.3		kHz
Color Lock In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed[3]				100		Lines
Fast Switch Speed[4]				100		ms
LUMA SPECIFICATIONS		CVBS, 1 V input				
Luma Brightness Accuracy				1		%
Luma Contrast Accuracy				1		%

[1] These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.
[2] The CMR of this circuit design is critically dependent on the external resistor matching on its inputs. This measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] Autodetection switch speed is the time it takes the ADV7182A to detect the video format present at its input, for example, PAL I or NTSC M.
[4] Fast switch speed is the time it takes the ADV7182A to switch from one single-ended or differential analog input to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

TIMING SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.63636		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width						
High	t_1		0.6			µs
Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDATA Setup Time	t_5		100			ns
SCLK and SDATA Rise Times	t_6				300	ns
SCLK and SDATA Fall Times	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
$\overline{\text{RESET}}$ FEATURE						
$\overline{\text{RESET}}$ Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{ACCESS} = t_{10} - t_{11}$)			3.8	ns
	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 + t_{12}$)			6.9	ns

Timing Diagrams

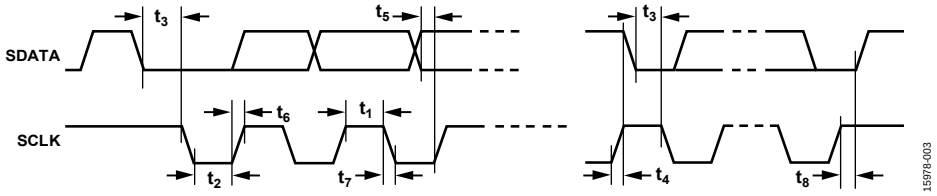

Figure 2. I²C Timing Diagram

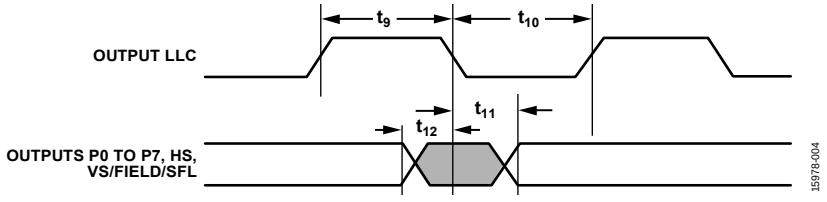

Figure 3. Pixel Port and Control Output Timing Diagram

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V; D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp					
Source Current			0.32		mA
Sink Current			0.32		mA
Fine Clamp					
Source Current			7		µA
Sink Current			7		µA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Rating
A_{VDD} to GND	2.2 V
D_{VDD} to GND	2.2 V
P_{VDD} to GND	2.2 V
D_{VDDIO} to GND	4 V
P_{VDD} to D_{VDD}	−0.9 V to +0.9 V
A_{VDD} to D_{VDD}	−0.9 V to +0.9 V
Digital Inputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	GND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to Ground	GND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	JEDEC J-STD-020

[1] The absolute maximum ratings assume that DGND pins and the exposed pad of the ADV7182A are connected together to a common ground plane (GND); this is part of the recommended layout scheme. See the PCB Layout Recommendations section for more information. The absolute maximum ratings are stated in relation to this common ground plane.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure as per JEDEC JESD51. ψ_{JT} is the junction to top thermal characterization parameter measured on a standard test board, as per JEDEC JESD51, allowing the heat generated in the ADV7182A die to flow normally along preferred thermal conduction paths that more closely represent the thermal flows in a typical application board.

Table 6. Thermal Resistance

Package	θ_{JA}	ψ_{JT}	Unit
CP-32-12[1]	39.6	0.86	°C/W

[1] JEDEC JESD51 2s2p 4-layer PCB with two signal layers and two buried solid ground planes (GND), and with via nine thermal vias connecting the exposed pad to the ground plane (GND).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

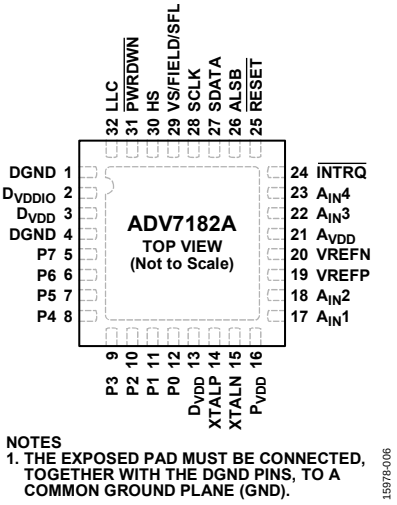

Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital Input/Output Supply Voltage (1.8 V to 3.3 V).
3, 13	D_{VDD}	Power	Digital Supply Voltage (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Port.
14	XTALP	Output	Output Pin for the Crystal Oscillator Amplifier. Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7182A. The crystal used with the ADV7182A must be a fundamental crystal.
15	XTALN	Input	Input Pin for the Crystal Oscillator Amplifier. The crystal used with the ADV7182A must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7182A, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Supply Voltage (1.8 V).
17, 18, 22, 23	$A_{IN}1$ to $A_{IN}4$	Input	Analog Video Input Channels.
19	VREFP	Output	Positive Internal Voltage Reference Output.
20	VREFN	Output	Negative Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Supply Voltage (1.8 V).
24	$\overline{\text{INTRQ}}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
25	$\overline{\text{RESET}}$	Input	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7182A circuitry.
26	ALSB	Input	Address Least Significant Bit. This pin selects the I^2C address for the ADV7182A. For ALSB set to Logic 0, the address selected for a write is 0x40; for ALSB set to Logic 1, the address selected is 0x42.
27	SDATA	Input/ output	I^2C Port Serial Data Input/Output Pin.
28	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
29	VS/FIELD/SFL	Output	Vertical Synchronization Output Signal (VS)/Field Synchronization Output Signal (FIELD)/ Subcarrier Frequency Lock (SFL). This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc., digital video encoder.
30	HS	Output	Horizontal Synchronization Output Signal.
31	$\overline{\text{PWRDWN}}$	Input	Power-Down. A logic low on this pin places the ADV7182A in power-down mode.
32	LLC	Output	Line Locked Clock for Output Pixel Data. This pin is nominally 27 MHz but varies up or down according to the video line length.
	EPAD (EP)		Exposed Ground Pad. The exposed pad must be connected, together with the DGND pins, to a common ground plane (GND).

THEORY OF OPERATION

The ADV7182A is a versatile, multiformat video decoder that automatically detects standard analog baseband video signals and converts them into a YCbCr 4:2:2 component video data stream. The ADV7182A supports video signals compatible with worldwide NTSC, PAL, and SECAM standards.

The analog front end (AFE) of the ADV7182A features a 4-channel input mux, a differential to single-ended converter, and a single 10-bit ADC. The analog video inputs accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources, making the ADV7182A ideal for automotive, industrial, and consumer applications.

The ADV7182A converts these analog video formats into a digital 8-bit ITU-R BT.656 video stream. External HS, VS, and FIELD signals provide timing references for liquid crystal display (LCD) controllers and other video application specific integrated circuits (ASICs).

The digital video output stream of the ADV7182A interfaces easily to a wide range of mobile video processors, MPEG encoders, codecs, and Analog Devices digital video encoders, such as the ADV7391.

The ADV7182A is programmed via a 2-wire, serial bidirectional port (I^2C compatible) and can communicate with other devices using the hardware interrupt pin.

The ADV7182A is fabricated in a low power, 1.8 V CMOS process. The device is provided in a space-saving, LFCSP, surface-mount, RoHS compliant package. The ADV7182A is available in an automotive grade rated over the −40°C to +105°C temperature range, making the ADV7182A ideal for automotive applications. The ADV7182A is also available in a −40°C to +85°C temperature range, making it ideal for consumer or industrial applications.

ANALOG FRONT END (AFE)

The ADV7182A AFE is comprised of a 4-channel input mux, a differential to single-ended converter with clamp circuitry, a set of four antialiasing filters, and a single 10-bit ADC.

The 4-channel input mux enables multiple composite video signals to be applied to the ADV7182A and is software controlled.

The next stage in the AFE features the differential to single-ended converter and the clamp circuitry. The incorporation of a differential front end allows differential video to be connected directly to the ADV7182A. The differential front end enables small and large signal noise rejection, improved electromagnetic interference (EMI), and the ability to absorb ground bounce. The architecture can support true differential, pseudo differential, and single-ended signals.

In conjunction with an external resistor divider, the ADV7182A provides a common-mode input range of 4 V, facilitating in the removal of large signal, common-mode transients present on both video inputs. CMR values of up to 80 dB can be achieved without the need for external amplifier circuitry.

The external resistor divider is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 23). Current and voltage clamps in the circuit attempt to ensure that the video signal remains within the range on the ADC.

The single 10-bit ADC digitizes the analog video before it is applied to the SDP. Table 8 shows the three ADC clocking rates determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, S-Video, and YPrPb modes.

Table 8. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
S-Video (Y/C)[2]	114	4×
YPrPb[2]	172	4×

[1] Based on a 28.63636 MHz clock input to the ADV7182A.
[2] See INSEL[4:0] in Table 96 for writes needed to set S-Video (Y/C) and YPrPb modes.

STANDARD DEFINITION PROCESSOR

The SDP in the ADV7182A is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include PAL B/PAL D/PAL I/PAL G/PAL H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/NTSC J, NTSC 4.43, and SECAM B/SECAM D/SECAM G/SECAM K/SECAM L. The ADV7182A can automatically detect the video standard and process it accordingly.

The ADV7182A features a five-line, superadaptive, 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts the processing mode according to the video standard and signal quality without requiring user intervention. Video user controls, such as brightness, contrast, saturation, and hue, are also available in the ADV7182A.

The ADV7182A implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7182A to track and decode poor quality video sources, such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7182A contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7182A features an automatic gain control (AGC) algorithm to ensure that the optimum luma gain is selected as the input video varies in brightness.

Adaptive contrast enhancement (ACE) is an algorithm that automatically varies the contrast level applied across an image to enhance the picture detail visible. This automatic variation enables the contrast in the dark areas of an image to be increased without saturating the bright areas, which is particularly useful in automotive applications where it can be important to be able to clearly discern objects in shaded areas.

Downdithering from eight bits to six bits enables ease of design for standard LCD panels.

The SDP can handle a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world standard teletext (WST). Data is transmitted via the 8-bit video output port as ancillary data packets (ANC).

The ADV7182A is fully Rovi™ (formerly Macrovision® and now rebranded as TiVo upon acquisition of the same) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The SDP is fully robust to all Rovi signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7182A is guaranteed by production testing.

The optimal power-up sequence for the ADV7182A is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}).

When powering up the ADV7182A, follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7182A.

SIMPLIFIED POWER-UP SEQUENCE

The simplified power-up sequence is guaranteed by characterization.

Alternatively, the ADV7182A can be powered up by asserting all supplies and the $\overline{\text{PWRDWN}}$ pin simultaneously. During this operation, the $\overline{\text{RESET}}$ pin must remain low. After the supplies and $\overline{\text{PWRDWN}}$ are fully asserted, wait at least 5 ms before bringing the $\overline{\text{RESET}}$ pin high. After the $\overline{\text{RESET}}$ pin is fully asserted, wait an additional 5 ms before initiating I^2C communication with the ADV7182A.

While the supplies are being established, take care to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7182A supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY

It is possible to power all the supplies (D_{VDD}, P_{VDD}, A_{VDD}, and D_{VDDIO}) to 1.8 V. In this case, apply the power-up sequences as described in the Optimal Power-Up Sequence section and the Simplified Power-Up Sequence section. The only change is that D_{VDDIO} is powered up to 1.8 V instead of 3.3 V.

In this setup,

- Power up the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin to 1.8 V instead of 3.3 V.
- Set the drive strengths of the digital outputs of the ADV7182A to the maximum setting (see the Global Pin Control section).
- Connect any pull-up resistors connected to pins on the ADV7182A (such as the SCLK pin and the SDATA pin) to 1.8 V and not 3.3 V.

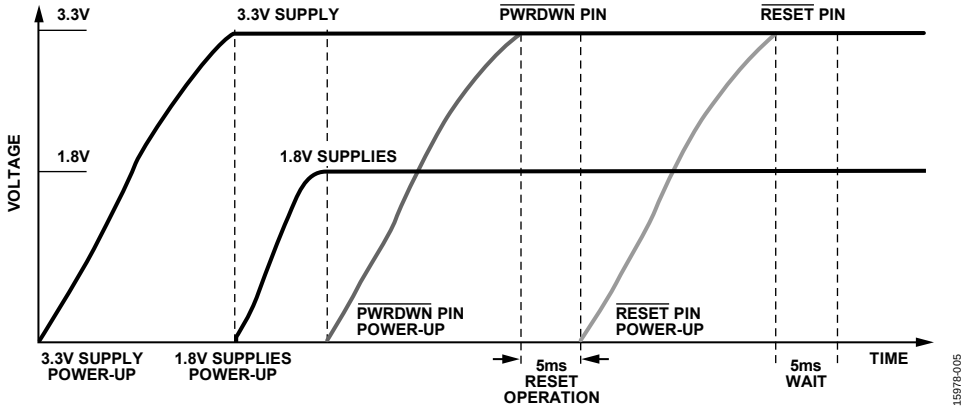

Figure 5. Recommended Power-Up Sequence

CRYSTAL OSCILLATOR DESIGN

The ADV7182A requires a stable and accurate clock source to guarantee operation. This clock is typically provided by a crystal resonator (XTAL), but can also be provided by a clock oscillator.

The required circuitry for an XTAL is shown in Figure 50. A damping resistor (R_{DAMP}) is required on the output of the ADV7182A XTAL amplifier (XTALP). The purpose of this damping resistor is to limit the current flowing through the XTAL and to limit the voltage across the XTAL amplifier. To define the appropriate value of the damping resistor, R_{DAMP} (see the Typical Circuit Connection section), consult the accompanying calculator tool (visit the design resources section at www.analog.com/ADV7182A to download).

The other components in the XTAL circuit must be chosen carefully; for example, incorrectly selected load capacitors may result in an offset to the crystal oscillation frequency. For more information on such considerations, refer to the AN-1260 Application Note, *Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers*. After the XTAL circuit is defined, it is recommended to consult the XTAL vendor to ensure that the design operates with a sufficient margin across all conditions.

The evaluation of the ADV7182A was completed using an XTAL with typical characteristics, as described in Table 9.

Table 9. Reference XTAL Characteristics

Characteristic	Value	Unit
Package	3.2 × 2.5 × 0.8	mm
Nominal Frequency	28.63636	MHz
Mode of Oscillation	Fundamental	Not applicable
Frequency Calibration (at 25°C)	±20	ppm
Frequency Temperature Stability Tolerance	±50	ppm
Operating Temperature Range	−40 to +125	°C
Maximum Equivalent Series Resistance	25	Ω
Load Capacitance	12	pF
Drive Level	200	µW
Maximum Shunt Capacitance	5	pF
Aging per Year	±3	ppm

The values in Table 9 are provided for reference only. It is recommended to characterize the operation of the XTAL circuit thoroughly across the operating temperature range of the application, in conjunction with the XTAL vendor, prior to releasing any new design.

INPUT NETWORKS

This section describes the input networks (external resistor and capacitor circuits) to be placed on the analog video input pins ($A_{IN}x$) of the ADV7182A. Different input networks are required for different analog input video formats.

SINGLE-ENDED INPUT NETWORK

Use the input network described in Figure 6 on each $A_{IN}x$ input pin of the ADV7182A when any of the following video input formats are used: single-ended CVBS, YC (S-Video), or YPrPb.

It is recommended that the input network circuit shown in Figure 6 be placed as close as possible to the $A_{IN}x$ pins of the ADV7182A.

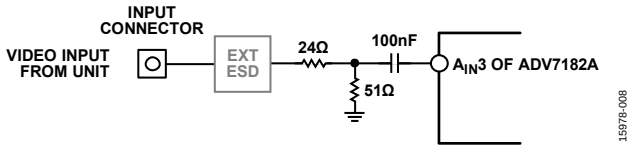

Figure 6. Input Single-Ended Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. In addition, these resistors create a resistor divider with a 0.68 gain that attenuates the amplitude of the inputted analog video and scales the input to the ADC range of the ADV7182A. This allows the ADV7182A to have an input range of up to 1.47 V p-p.

Note that amplifiers within the ADV7182A restore the amplitude of the input signal so that signal-to-noise (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog input pins of the ADV7182A.

The clamping circuitry within the ADV7182A restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7182A. See the Clamp Operation section for more information.

DIFFERENTIAL INPUT NETWORK

Use the input network shown in Figure 7 when differential CVBS video is input on the $A_{IN}x$ input pins of the ADV7182A.

It is recommended that the input network circuit shown in Figure 7 be placed as close as possible to the $A_{IN}x$ pins of the ADV7182A.

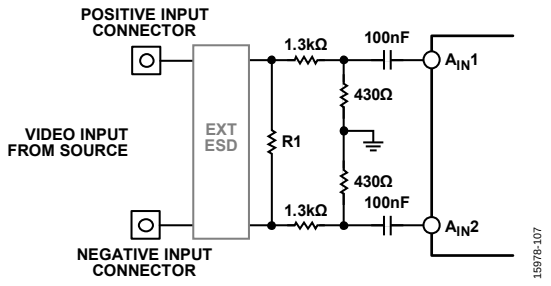

Figure 7. Input Differential Network

Differential video transmission involves transmitting two complementary CVBS signals and has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection.
- Improved EMI performance.
- Ability to absorb ground bounce.

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75 Ω is recommended for R1. For a fully differential CVBS input, a value of 150 Ω is recommended for R1.

The 1.3 kΩ and 430 Ω resistors provide a resistor divider with a 0.25 gain, resulting in an attenuation of the inputted analog video but also an increase in the input common-mode range of the ADV7182A of up to 4 V p-p.

Note that amplifiers within the ADV7182A restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog video input pins of the ADV7182A.

The clamping circuitry within the ADV7182A restores the dc bias of the optimized level before it is fed into the ADC of the ADV7182A. See the Clamp Operation section for further information.

The combination of the 1.3 kΩ and 430 Ω resistors and the 100 nF ac coupling capacitor limits current flow into the ADV7182A during short to battery (STB) events. See the Short to Battery (STB) Protection section.

To achieve optimal performance, closely match the 1.3 kΩ and 430 Ω resistors; that is, all the 1.3 kΩ and 430 Ω resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

SHORT TO BATTERY (STB) PROTECTION

In differential mode, the ADV7182A is protected against STB events by the external 100 nF ac coupling capacitors (see Figure 7). The external input network resistors are sized to be large enough to reduce the current flow during a STB event, but to be small enough not to effect the operation of the ADV7182A.

Choose the power rating of the input network resistors to withstand the high voltages of STB events. Similarly, choose the breakdown voltage of the AC coupling capacitors to be robust to STB events.

The R1 resistor is protected because no current or limited current flows through it during an STB event.

ANALOG FRONT END

INPUT CONFIGURATION

The following two steps are crucial for configuring the ADV7182A to correctly decode the input video.

1. Use INSEL[4:0] to configure the routing and format decoding (CVBS, S-Video, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. Using the INSEL[4:0] selection, configure the SDP block, which decodes the digital data, to process the CVBS, S-Video or YPrPb format.

INSEL[4:0], Input Control—Address 0x00, Bits[4:0]

The INSEL bits allow the user to select the input format. They also configure the SDP core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format.

INSEL[4:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 10). This allows the user to route the various video signal types to the decoder and select them using INSEL[4:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 10. INSEL[4:0]

INSEL[4:0]	Video Format	Analog Input
00000	CVBS	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$
01000	S-Video (Y/C)	Y input on $A_{IN}1$ C input on $A_{IN}2$
01001	S-Video (Y/C)	Y input on $A_{IN}3$ C input on $A_{IN}4$
01100	YPrPb	Y input on $A_{IN}1$ Pb input on $A_{IN}2$ Pr input on $A_{IN}3$
01110	Differential CVBS	Positive on $A_{IN}1$ Negative on $A_{IN}2$
01111	Differential CVBS	Positive on $A_{IN}3$ Negative on $A_{IN}4$

ANALOG INPUT MUXING

The ADV7182A has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder.

A maximum of four CVBS inputs can be connected to and decoded by the ADV7182A. As shown in the Pin Configuration and Function Description section, these analog input pins lie in close proximity to one another, which requires careful design of the PCB layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended that any unused analog input pins be connected to AGND to act as a shield.

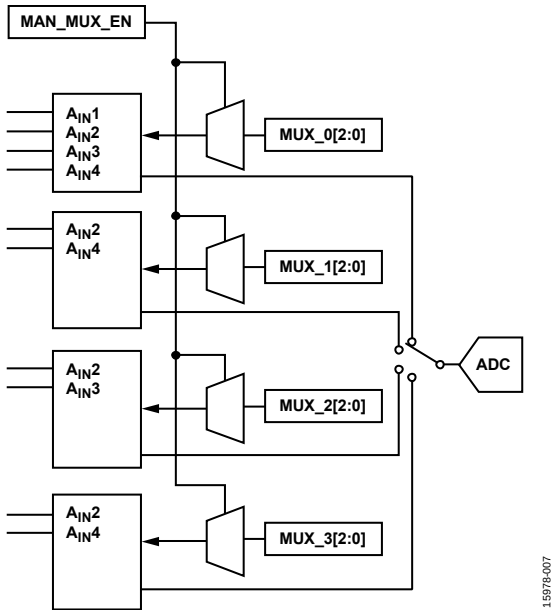

Figure 8. Manual Muxing

MAN_MUX_EN, Manual Input Muxing Enable—Address 0xC4, Bit 7

To configure the ADV7182A analog muxing section, the user must select the analog input $A_{IN}1$ to $A_{IN}8$ that is to be processed by the ADC. MAN_MUX_EN must be set to 1 to enable the following muxing blocks:

- MUX_0[2:0], ADC mux configuration (Address 0xC3, Bits[2:0])
- MUX_1[2:0], ADC mux configuration (Address 0xC3, Bits[6:4])
- MUX_2[2:0], ADC mux configuration (Address 0xC4, Bits[2:0])
- MUX_3[2:0], ADC mux configuration (Address 0x60, Bits[2:0])

The four mux sections are controlled by the signal buses, MUX_0/MUX_1/MUX_2/MUX_3[2:0]. Table 11 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX_0. For example, in an S-Video input configuration, connect MUX_0 to the Y channel and MUX_1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers must be powered down (see the description of Register 0x3A in Table 96).

ANTIALIASING FILTERS

The ADV7182A has optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 9). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 10 and Figure 11 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.

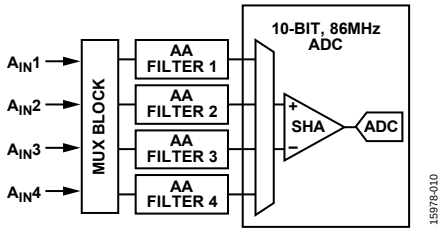

Figure 9. Antialias Filter Configuration

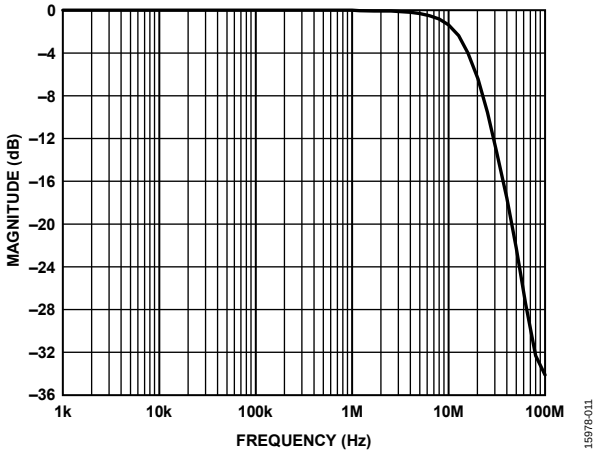

Figure 10. Antialiasing Filter Magnitude Response

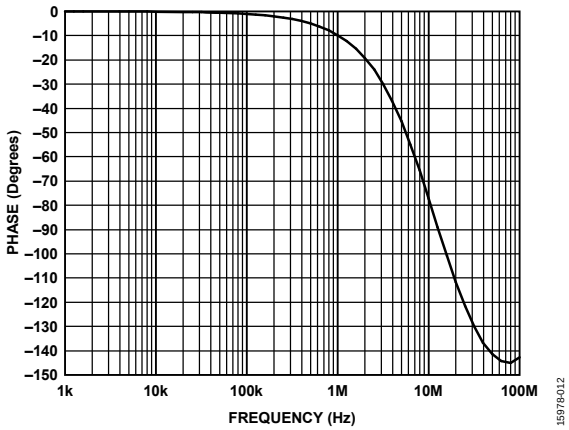

Figure 11. Antialiasing Filter Phase Response

AA_FILT_MAN_OVR, Antialiasing Filter Override—Address 0xF3, Bit 4

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

AA_FILT_EN[3:0], Antialiasing Filter Enable—Address 0xF3, Bits[3:0]

These bits allow the user to enable or disable the antialiasing filters on each of the four input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

AA_FILT_EN[0], Antialiasing Filter Enable—Address 0xF3, Bit 0

When AA_FILT_EN[0] is 0, AA Filter 1 is disabled. When AA_FILT_EN[0] is 1, AA Filter 1 is enabled.

AA_FILT_EN[1], Antialiasing Filter Enable—Address 0xF3, Bit 1

When AA_FILT_EN[1] is 0, AA Filter 2 is disabled. When AA_FILT_EN[1] is 1, AA Filter 2 is enabled.

AA_FILT_EN[2], Antialiasing Filter Enable—Address 0xF3, Bit 2

When AA_FILT_EN[2] is 0, AA Filter 3 is disabled. When AA_FILT_EN[2] is 1, AA Filter 3 is enabled.

AA_FILT_EN[3], Antialiasing Filter Enable—Address 0xF3, Bit 3

When AA_FILT_EN[3] is 0, AA Filter 4 is disabled. When AA_FILT_EN[3] is 1, AA Filter 4 is enabled.

Table 11. Manual Mux Settings for ADC (MAN_MUX_EN Must be Set to 1)[1, 2, 3, 4]

MUX_0[2:0]	ADC Connected To	MUX_1[2:0]	ADC Connected To	MUX_2[2:0]	ADC Connected To	MUX_3[2:0]	ADC Connected To
000	No connect	000	No connect	000	No connect	000	No connect
001	$A_{IN}1$	001	No connect	001	No connect	001	No connect
010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$	010	$A_{IN}2$
011	$A_{IN}3$	011	No connect	011	$A_{IN}3$	011	No connect
100	$A_{IN}4$	100	$A_{IN}4$	100	No connect	100	$A_{IN}4$

[1] CVBS can only be processed by MUX_0.
[2] Differential CVBS can only be processed by MUX_0 (positive channel) and MUX_3 (negative channel).
[3] Y/C can only be processed by MUX_0 and MUX_1.
[4] YPrPb can only be processed by MUX_0, MUX_1, and MUX_2.

GLOBAL CONTROL REGISTERS

Register control bits described in this section affect the entire chip.

POWER SAVING MODES

Power-Down

PWRDWN—Address 0x0F, Bit 5

The ADV7182A can be placed into a chip wide, power-down mode by setting the PWRDWN bit or by using the $\overline{\text{PWRDWN}}$ pin. The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I^2C interface is unaffected and remains operational in power-down mode.

When PWRDWN is 0, the chip is operational. When PWRDWN is 1 (default), the ADV7182A is in a chip-wide, power-down mode.

RESET CONTROL

Reset, Chip Reset—Address 0x0F, Bit 7

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7182A, issues a full chip reset. All I^2C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified and keep the last written value. These bits are marked as having a reset value of x in the register tables (see Table 96 and Table 98). After the reset sequence, the device immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the device returns to the default for its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.

The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the I2C Interface section).

When the reset bit is 0 (default), operation is normal. When the reset bit is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Tristate Output Drivers

TOD—Address 0x03, Bit 6

This bit allows the user to tristate the output drivers of the ADV7182A.

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL) can be forced active via the TIM_OE bit. For more information on tristate control, see the Tristate LLC Driver section and the Timing Signals Output Enable section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TOD is 0, the output drivers are enabled. When TOD is 1 (default), the output drivers are tristated.

Tristate LLC Driver

TRI_LLC—Address 0x1D, Bit 7

This bit allows the output drivers for the LLC pin of the ADV7182A to be tristated. For more information on tristate control, refer to the Tristate Output Drivers section and the Timing Signals Output Enable section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TRI_LLC is 0, the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled). When TRI_LLC is 1 (default), the LLC pin drivers are tristated.

Timing Signals Output Enable

TIM_OE—Address 0x04, Bit 3

Regard the TIM_OE bit as an addition to the TOD bit. Setting this bit high forces the output drivers for HS and VS/FIELD/SFL into the active state (that is, driving state), even if the TOD bit is set. If TIM_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator, which may be the case if only the timing signals are extracted from an incoming signal or if the device is in freerun mode, where a separate chip can output a company logo, for example.

For more information on tristate control, see the Tristate Output Drivers section and the Tristate LLC Driver section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TIM_OE is 0 (default), HS and VS/FIELD/SFL are tristated according to the TOD bit. When TIM_OE is 1, HS and VS/FIELD/SFL are always forced active.

VS/FIELD/SFL Sync Mux Selection

FLD_OUT_SEL[2:0]—Address 0x6B, Bits[2:0]

The FLD_OUT_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the Tristate Output Drivers section and the Tristate LLC Driver section.

Table 12. FLD_OUT_SEL Function

FLD_OUT_SEL[2:0]	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information.
001	The VS/FIELD/SFL pin outputs vertical sync information.
010 (default)	The VS/FIELD/SFL pin outputs field sync information.
011	The VS/FIELD/SFL pin outputs DE information.
100	The VS/FIELD/SFL pin outputs SFL information.

HS Sync Mux Selection

HS_OUT_SEL[2:0]—Address 0x6A, Bits[2:0]

The HS_OUT_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, DE, or SFL information.

Note that the HS pin must be active for this selection to occur (see the Tristate Output Drivers section and the Tristate LLC Driver section).

Table 13. HS_OUT_SEL Function

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs DE information.
100	The HS pin outputs SFL information.

Drive Strength Selection (Data)

DR_STR[1:0]—Address 0xF4, Bits[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the drive strength for the pixel output pins (P[7:0]) and the timing pins (HS and VS/FIELD/SFL).

For more information on tristate control, see the Tristate Output Drivers section and the Tristate LLC Driver section.

Table 14. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

DR_STR_C[1:0]—Address 0xF4, Bits[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Data) section.

Table 15. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (I^2C)

DR_STR_S[1:0]—Address 0xF4, Bits[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the I^2C signal output drivers. This affects the drive strength for the SDA and SCL pins.

Table 16. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN—Address 0x04, Bit 1

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7182A core to an encoder in a decoder/encoder back to back arrangement.

When the EN_SFL_PIN is 0 (default), the SFL output is disabled. When EN_SFL_PIN is 1, the SFL information is presented on the SFL pin.

GLOBAL STATUS REGISTERS

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7182A. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV7182A.

IDENTIFICATION REGISTER

IDENT[7:0]—Address 0x11, Bits[7:0]

This is the register identification of the ADV7182A revision. Table 17 describes the various versions of the ADV7182A.

Table 17. IDENT[7:0] CODE

IDENT[7:0]	Description
0x40	Prerelease silicon
0x41	Released silicon

STATUS 1 REGISTER

Status 1[7:0]—Address 0x10, Bits[7:0]

This read only register provides information about the internal status of the ADV7182A.

See the CIL[2:0], Count in to Lock—Address 0x51, Bits[2:0] section and the COL[2:0], Count Out of Lock (COL)—Address 0x51, Bits[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable—Address 0x51, Bit 7 section.

See the Autodetection of SD Modes section for a description of the AD_RESULT bits.

Table 18. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read)
2	FSC_LOCK	f_{SC} locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2 REGISTER

Status 2[7:0]—Address 0x12, Bits[7:0]

Table 19. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Rovi color striping
1	MVCS T3	Rovi color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV PS DET	Detected Rovi pseudo sync pulses
3	MV AGC DET	Detected Rovi AGC pulses
4	LL NSTD	Line length is nonstandard
5	FSC NSTD	f_{SC} frequency is nonstandard
6	Reserved	Reserved
7	Reserved	Reserved

STATUS 3 REGISTER

Status 3[7:0]—Address 0x13, Bits[7:0]

Table 20. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	Reserved	Reserved
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved
4	FREE_RUN_ACT	Flags if the ADV7182A entered freerun mode (see the Freerun Operation section)
5	STD FLD LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

AUTODETECTION RESULT

AD_RESULT[2:0]—Address 0x10, Bits[6:4]

The AD_RESULT[2:0] bits report back on the findings from the ADV7182A autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure the autodetection block.

Table 21. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

VIDEO PROCESSOR

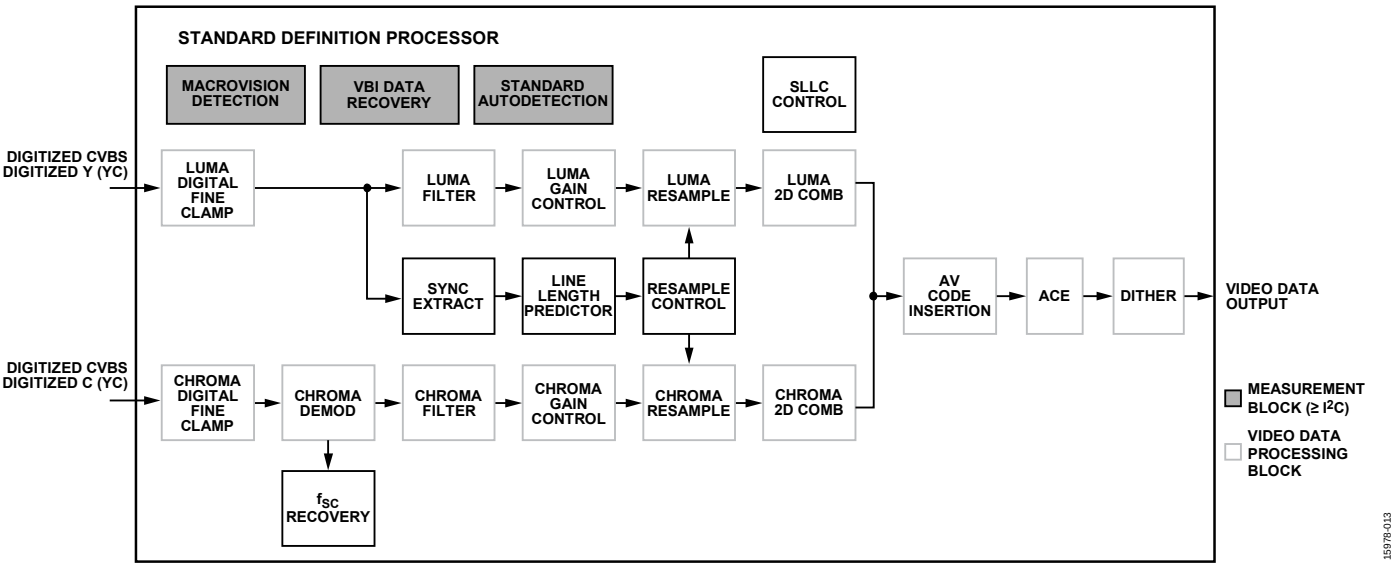

Figure 12. Block Diagram of Video Processor

Figure 12 shows a block diagram of the ADV7182A video processor. The ADV7182A can handle standard definition (SD) video in CVBS, Y/C, and YPrPb formats. The video processor features luminance and chrominance paths. If the input video is a composite type (CVBS), CVBS is supplied to both processing paths.

STANDARD DEFINITION (SD) LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct line length errors and dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted as per ITU-R BT.656.

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is performed to correct static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, superadaptive comb filter provides high quality Y/C separation if the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted as per ITU-R BT.656.

ACE AND DITHER PROCESSING BLOCKS

The ACE block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail (see the Adaptive Contrast Enhancement section).

When enabled, the dither block converts the digital output of the ADV7182A from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV7182A to communicate with some LCD panels (see the Dither Function section).

SYNC PROCESSING

The ADV7182A extracts syncs embedded in the analog input video signal. There is currently no support for external HS/VS inputs. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm uses a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this information then drives the digital resampling section to ensure that the ADV7182A outputs 720 active pixels per line.

The sync processing on the ADV7182A also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSYNC processor. This block provides extra filtering of the detected VSYNC signals to improve vertical lock.
- HSYNC processor. The HSYNC processor filters incoming HSYNCS signals corrupted by noise, providing much improved performance for video signals with a stable time base but poor SNR.

VERTICAL BLANK INTERVAL (VBI) DATA RECOVERY

The ADV7182A can retrieve the following information from the input video:

- Wide screen signaling (WSS).
- Copy generation management system (CGMS).
- Closed captioning (CCAP).
- Rovi protection presence.
- Teletext.

The ADV7182A is also capable of automatically detecting the incoming video standard with respect to color subcarrier frequency, field rate, and line rate.

The ADV7182A can configure itself to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x02, Bits[7:4]) allow the user to force the digital core into a specific video standard; this is not necessary under normal circumstances. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Autodetection of SD Modes

To guide the autodetect system of the ADV7182A, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x02[7:4]

Table 22. VID_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

AD_SEC525_EN, SECAM 525 Autodetect Enable—Address 0x07, Bit 7

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM modulated color component. Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM modulated color component.

AD_SECAM_EN, SECAM Autodetect Enable—Address 0x07, Bit 6

Setting AD_SECAM_EN to 0 (default) disables the autodetection of SECAM. Setting AD_SECAM_EN to 1 enables the detection of SECAM.

AD_N443_EN, NTSC 4.43 Autodetect Enable—Address 0x07, Bit 5

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier. Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, PAL 60 Autodetect Enable—Address 0x07, Bit 4

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate. Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, PAL N Autodetect Enable—Address 0x07, Bit 3

Setting AD_PALN_EN to 0 (default) disables the detection of the PAL N standard. Setting AD_PALN_EN to 1 enables the detection of the PAL N standard.

AD_PALM_EN, PAL M Autodetect Enable—Address 0x07, Bit 2

Setting AD_PALM_EN to 0 (default) disables the autodetection of PAL M. Setting AD_PALM_EN to 1 enables the detection of PAL M.

AD_NTSC_EN, NTSC Autodetect Enable—Address 0x07, Bit 1

Setting AD_NTSC_EN to 0 (default) disables the detection of standard NTSC. Setting AD_NTSC_EN to 1 enables the detection of standard NTSC.

AD_PAL_EN, PAL B/PAL D/PAL I/PAL G/PAL H Autodetect Enable—Address 0x07, Bit 0

Setting AD_PAL_EN to 0 (default) disables the detection of standard PAL. Setting AD_PAL_EN to 1 enables the detection of standard PAL.

SFL_INV, Subcarrier Frequency Lock Inversion—Address 0x41, Bit 6

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. This control solves some compatibility issues with video encoders, as well as solving two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

The second problem is to accommodate a design change using newer Analog Devices encoders, such as the ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179. The older encoders used the SFL (genlock telegram) bit directly, whereas the newer encoders invert the bit prior to using because the inversion compensates for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the newer video encoders (ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179), the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For the older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back to back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL_INV to 0 (default) makes the device SFL compatible with newer video encoders such as the ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179.

Setting SFL_INV to 1 makes the device SFL compatible with the older video encoders.

Lock Related Controls

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1[7:0]—Address 0x10, Bits[7:0] section). Figure 13 shows the signal flow and the controls available to influence the way the lock status information is generated.

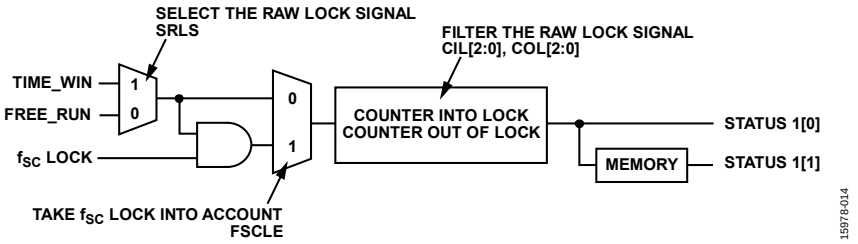

Figure 13. Lock Related Signal Path

SRLS, Select Raw Lock Signal—Address 0x51, Bit 6

Using the SRLS bit, the user can choose between two sources for determining the lock status per Bits[1:0] in the Status 1 register (see Figure 13):

- The TIME_WIN signal is based on a line to line evaluation of the horizontal synchronization pulse of the incoming video and reacts quickly.
- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE_RUN signal; that is, the signal evaluates the properties of the incoming video over several fields.

Setting SRLS to 1 selects the TIME_WIN signal; that is, the signal evaluates the horizontal synchronization pulse of the incoming video on a line to line basis.

FSCLE, f_{SC} Lock Enable—Address 0x51, Bit 7

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7182A in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is 0 (default), the overall lock status is dependent only on horizontal sync lock. When FSCLE is 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

CIL[2:0], Count in to Lock—Address 0x51, Bits[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Bits[1:0] in the Status 1 register. The bit counts the value in lines of video.

Table 23. CIL Function

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COL[2:0], Count Out of Lock (COL)—Address 0x51, Bits[5:3]

COL[2:0] determines the number of consecutive lines for which the out of lock condition must be true before the system switches into the unlocked state and reports this via Bits[1:0] in the Status 1 register. COL[2:0] counts the value in lines of video.

Table 24. COL Function

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROL REGISTERS

The color control registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Contrast Adjust—Address 0x08, Bits[7:0]

This register allows the user to control contrast adjustment of the picture.

Table 25. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0], SD Saturation Cb Channel—Address 0xE3, Bits[7:0]

This register allows the user to control the gain of the blue chroma (Cb) channel only, which in turn adjusts the saturation of the picture.

Table 26. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0], SD Saturation Red Chroma (Cr) Channel—Address 0xE4, Bits[7:0]

This register allows the user to control the gain of the red chroma (Cr) channel only, which in turn adjusts the saturation of the picture.

Table 27. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cr channel = −42 dB
0xFF	Gain on Cr channel = +6 dB

SD_OFF_Cb[7:0], SD Offset Cb Channel—Address 0xE1, Bits[7:0]

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register (Address 0x0B).

Table 28. SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 mV offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0], SD Offset Cr Channel—Address 0xE2, Bits[7:0]

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 29. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 mV offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0], Brightness Adjust—Address 0x0A, Bits[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 30. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = −30 IRE

HUE[7:0], Hue Adjust—Address 0x0B, Bits[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 31. HUE Function

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0], Default Value Y—Address 0x0C, Bits[7:2]

When the ADV7182A loses lock on the incoming video signal or when there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF_VAL_AUTO_EN bit is 1 and the ADV7182A lost lock to the input video signal, this is the intended mode of operation (automatic mode).
- If the DEF_VAL_EN bit is 1, regardless of the lock status of the video decoder, this is a forced mode that is useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = [DEF_Y[5:0], 0, 0].

For DEF_Y[5:0], 0x0D (blue) is the default value for Y. Register 0x0C has a default value of 0x36.

DEF_C[7:0], Default Value C—Address 0x0D, Bits[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7182A cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7182A for the chroma side is Cr[4:0] = [DEF_C[7:4]] and Cb[4:0] = [DEF_C[3:0]].

For DEF_C[7:0], 0x7C (blue) is the default value for Cr and Cb.

FREERUN OPERATION

Freerun mode provides the user with a stable clock and predictable data if the input signal cannot be decoded; for example, if input video is not present.

The ADV7182A automatically enters freerun mode if the input signal cannot be decoded. The user can prevent this operation by setting the DEF_VAL_AUTO_EN to 0. When the DEF_VAL_AUTO_EN bit is 0, the ADV7182A outputs noise if it cannot decode the input video. It is recommended that the user keep DEF_VAL_AUTO_EN set to 1.

The user can force freerun mode by setting the DEF_VAL_EN bit to 1. This can be a useful tool in debugging system level issues.

The VID_SEL[3:0] bits can be used to force the video standard output in freerun mode (see the Video Standard Selection section).

The user can also specify which data is output in freerun mode with the FREE_RUN_PAT_SEL bits. The following test patterns can be set using this function:

- Single color
- Color bars
- Luma ramp
- Boundary box

Single Color Test Pattern

In single color test pattern mode, the ADV7182A can be set to output the default luma and chroma data stored in DEF_Y and DEF_C (see the Color Control Registers section).

Color Bars Test Pattern

In color bars test pattern mode, the ADV7182A outputs the 100% color bars pattern.

Luma Ramp Test Pattern

In luma ramp test pattern mode, the ADV7182A outputs a series of vertical bars. Each vertical bar is progressively brighter than the vertical bar to its left.

Boundary Box Test Pattern

In boundary box test pattern mode, the ADV7182A outputs a black screen with a 1-pixel depth white border (see Figure 14).

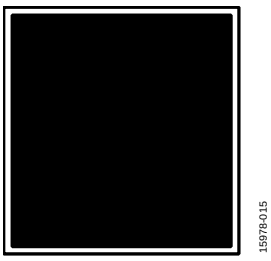

Figure 14. Boundary Box Freerun Test Pattern

DEF_VAL_AUTO_EN, Default Value Automatic Enable—Address 0x0C, Bit 1

This bit enables the ADV7182A to enter freerun mode if it cannot decode the video signal that has been input.

Table 32. DEF_VAL_AUTO_EN Function

DEF_VAL_AUTO_EN	Description
0	The ADV7182A outputs noise if it loses lock with the inputted video signal.
1 (default)	The ADV7182A enters freerun mode if it loses lock with the inputted video signal.

DEF_VAL_EN, Default Value Enable—Address 0x0C, Bit 0

This bit forces freerun mode.

Table 33. DEF_VAL_EN Function

DEF_VAL_EN	Description
0 (default)	Do not force freerun mode (that is, freerun mode dependent on DEF_VAL_AUTO_EN)
1	Force freerun mode

FREE_RUN_PAT_SEL[2:0], Free Run Pattern Select—Address 0x14, Bits[2:0]

This function selects what data is output in freerun mode.

Table 34. FREE_FUN_PAT_SEL Function

FREE_RUN_PAT_SEL	Description
000 (default)	Single color set by the DEF_C and DEF_Y controls; see the Color Control Registers section.
001	100% color bars.
010	Luma ramp. Note that, to display properly, set the DEF_C register to 0x88. See the Color Control Registers section.
101	Boundary box.

VS_COAST_MODE[1:0]—Address 0xF9, Bits[3:2]

If no video source is connected, then this function can set the video output standard during freerun mode.

If a valid input video source is connected to the ADV7182A and freerun mode is forced, the VS_COAST_MODE bits are ignored. The freerun standard is the same as the valid inputted video standard.

Table 35. VS_COAST_MODE Function

VS_COAST_MODE	Description
00 (default)	The ADV7182A outputs in the same standard as it did before it entered freerun mode. If no valid standard was output before entering freerun mode, the ADV7182A outputs a 576i, 50 Hz signal in freerun mode.
01	Outputs a 576i 50 Hz signal in freerun mode.
10	Outputs a 480i 60 Hz signal in freerun mode.
11	Reserved.

CLAMP OPERATION

The input video is ac-coupled into the ADV7182A, which protects the ADV7182A from STB events. However, the dc value of the input video must be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7182A in both single-ended and differential modes. This section also discusses the different ways a user can configure clamp operation behavior.

Single-Ended CVBS Clamp Operation

The ADV7182A uses a combination of current sources and a digital processing block for clamping, as shown in Figure 15. The analog processing channel shown in Figure 15 is replicated four times inside the IC. Whereas only a single channel is required for a single-ended CVBS signal, two independent channels are required for Y/C (SVHS) type signals, and three independent channels are required to allow component signals (YPrPb) to be processed.

The clamping is divided into two sections:

- Clamping before the ADC (analog domain): current sources and voltage sources.
- Clamping after the ADC (digital domain): digital processing block.

The primary task of the analog clamping circuits is to ensure that the video signal stays within the valid 1.0 V ADC input window so that the analog-to-digital conversion can take place. The current sources in Figure 15 correct the dc level of the ac-coupled input video signal before it is fed into the ADC. The digitized data from the ADC is then fed into the video processor. The digital fine clamp block within the video processor corrects any remaining variation in the dc level. The video processor also sends clamp control signals to the current sources. This feedback loop fine tunes the current clamp operation and compensates for any noise on the inputted video signal. This maintains the dc level of the video signal during normal operation.

Differential CVBS Clamping Operation

The differential clamping operation works in a similar manner to the single-ended clamping operation (see Single-Ended CVBS Clamp Operation section). In differential mode, a coarse clamp pulls the positive and negative video input to a common-mode voltage, V_{CML} (see Figure 16). The feedback loop between the current clamps and the video processor fine tune this coarse dc offset and make the clamping robust to noise on the video input.

Note that the current clamps are controlled within a feedback loop between the AFE and the video processor, and the coarse clamps are not.

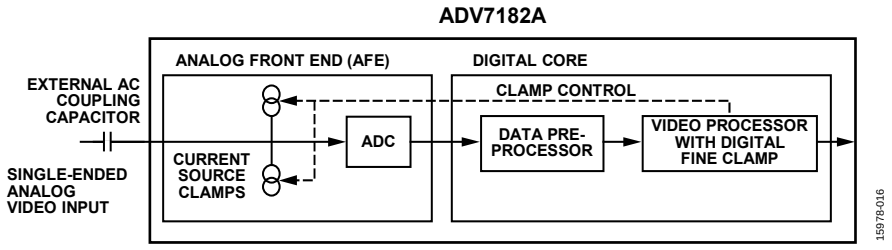

Figure 15. Single-Ended Clamping Overview

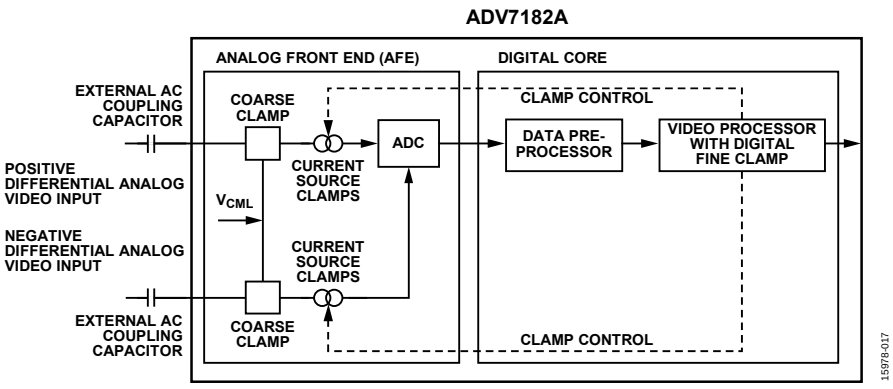

Figure 16. Differential Clamping Overview

Clamp Operation Controls

The following sections describe the I²C signals that can be used to influence the behavior of the clamping block.

CCLEN, Current Clamp Enable—Address 0x14, Bit 4

The current clamp enable bit allows the user to switch off all the current sources in the AFE simultaneously which is useful if the incoming analog video signal is clamped externally.

When CCLEN is 0, the current sources are switched off. When CCLEN is 1 (default), the current sources are enabled.

DCT[1:0], Digital Clamp Timing—Address 0x15, Bits[6:5]

The clamp timing register determines the time constant of the digital fine clamp circuitry. Note that the digital fine clamp reacts quickly because it immediately corrects any residual dc level error for the active line. The time constant from the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 36. DCT Function

DCT[1:0]	Description
00 (default)	Slow; time constant (TC) = 1 sec
01	Medium; TC = 0.5 sec
10	Fast; TC = 0.1 sec
11	Determined by ADV7182A, depending on the input video parameters

DCFE, Digital Clamp Freeze Enable—Address 0x15, Bit 4

This bit allows the user to freeze the digital clamp loop at any time to perform manual clamping. The user can disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is set to 0 (default), the digital clamp is operational. When DCFE is 1, the digital clamp loop is frozen.

LUMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

The ADV7182A receives video at a rate of 28.6363 MHz. (In the case of 4× oversampled video, the ADC samples at 57.27 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the ADV7182A is always 28.6363 MHz.) ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter (YAA) decimates the oversampled video using a high quality linear phase, low-pass filter that preserves the luma signal while, at the same time, attenuating out of band components. The luma antialias filter (YAA) has a fixed response.

The luma shaping filter (YSH) block is a programmable low-pass filter with a wide variety of responses. It can be used to reduce selectively the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. If the video is low-pass filtered, a follow on video compression stage can work more efficiently.

The ADV7182A has two responses for the shaping filter: one that is used for good quality composite, component, and SVHS type sources; and a second for nonstandard CVBS signals.

The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.

The digital resampling filter block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 18 through Figure 21 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. Y/C separation must aim for best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV7182A. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (f_{SC}). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship may be disturbed, and the comb filters may not be able to remove all crosstalk artifacts in the best fashion without the assistance of the shaping filter block.

An automatic mode is provided that allows the ADV7182A to evaluate the quality of the incoming video signal and select the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has the following control bits.

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (depending on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality composite (CVBS), component (YPrPb), and SVHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources (because they can be successfully

combed) as well as for luma components of YPrPb and Y/C sources (because they do not need to be combed). For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 17.

YSFM[4:0], Y Shaping Filter Mode—Address 0x17, Bits[4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter selection is based on other register selections, such as detected video standard, as well as properties extracted from the incoming video itself, such as quality and time base stability. The automatic selection always selects the widest possible bandwidth for the video input encountered (see Table 37).

The Y shaping filter mode operates as follows:

- If the YSFM settings specify a filter (that is, YSFM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wideband filters are used.

WYSFMOVR, Wideband Y Shaping Filter Override—Address 0x18, Bit 7

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information on luma shaping filters, see the Y Shaping Filter section and the flowchart shown in Figure 17.

When WYSFMOVR is set to 0, the shaping filter for good quality video signals is selected automatically. When WYSFMOVR is set to 1 (default), it enables manual override via WYSFM[4:0].

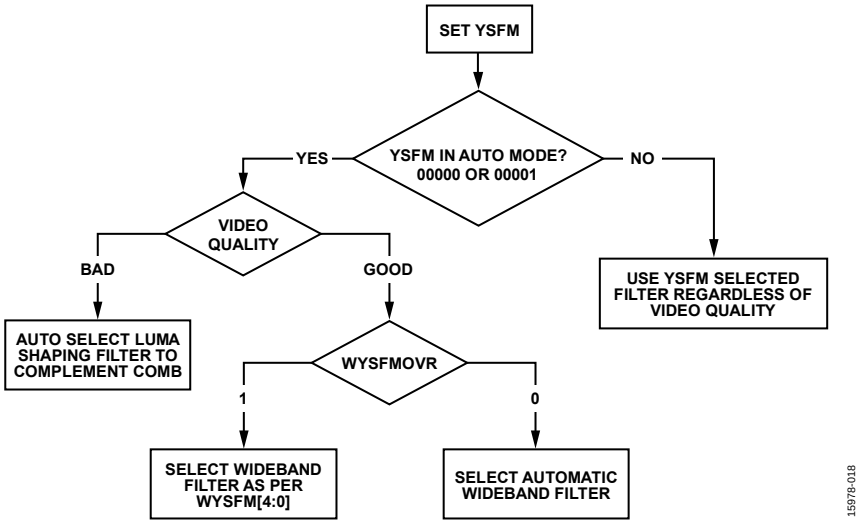

Figure 17. YSFM and WYSFM Control Flowchart

Table 37. YSFM Function

YSFM[4:0]	Description
00000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
00001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011	SVHS 18 (CCIR 601)
10100	PAL NN1
10101	PAL NN2
10110	PAL NN3
10111	PAL WN1
11000	PAL WN2
11001	NTSC NN1
11010	NTSC NN2
11011	NTSC NN3
11100	NTSC WN1
11101	NTSC WN2
11110	NTSC WN3
11111	Reserved

WYSFM[4:0], Wideband Y Shaping Filter Mode—Address 0x18, Bits[4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, for example, CVBS with stable time base, luma component of YPrPb, and luma component of Y/C. The WYSFM bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 38. WYSFM Function

WYSFM[4:0]	Description
00000	Reserved, do not use
00001	Reserved, do not use
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011 (default)	SVHS 18 (CCIR 601)
10100 to 11111	Reserved, do not use

Figure 18 show the SVHS 1 (narrowest) to SVHS 18 (widest) shaping filter settings. Figure 20 shows the PAL notch filter responses. The NTSC notch filter responses are shown in Figure 21.

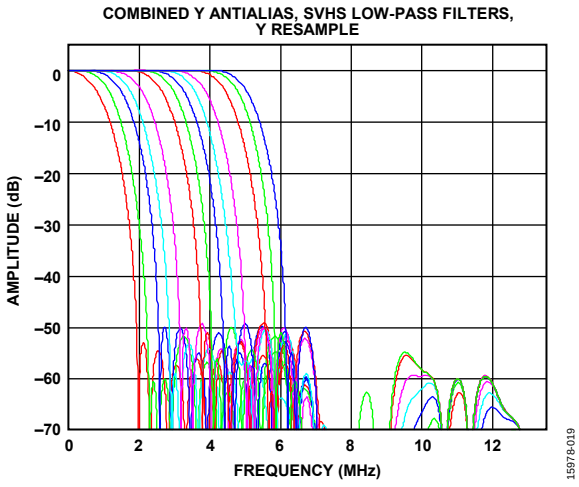

Figure 18. Y SVHS Combined Responses

CHROMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters as follows (the data format at this point is CVBS for CVBS inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats):

- Chroma antialias filter (CAA). The ADV7182A oversamples the CVBS by a factor of 4. A decimating filter (CAA) preserves the active video band and removes any out of band components. The CAA filter has a fixed response.
- Chroma shaping filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

Figure 22 shows the overall response of all filters together.

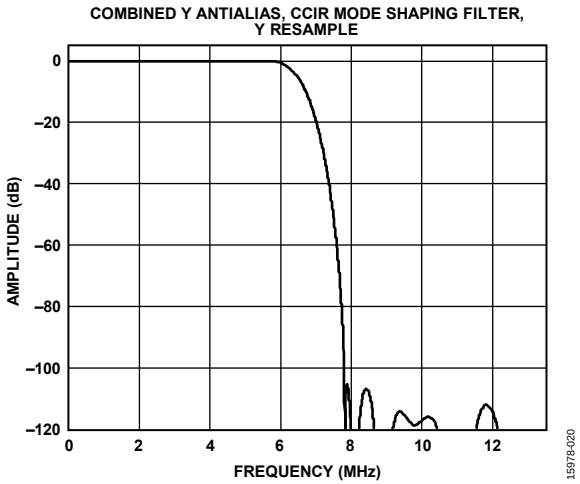

Figure 19. Combined Y Antialias, CCIR Mode Shaping Filter

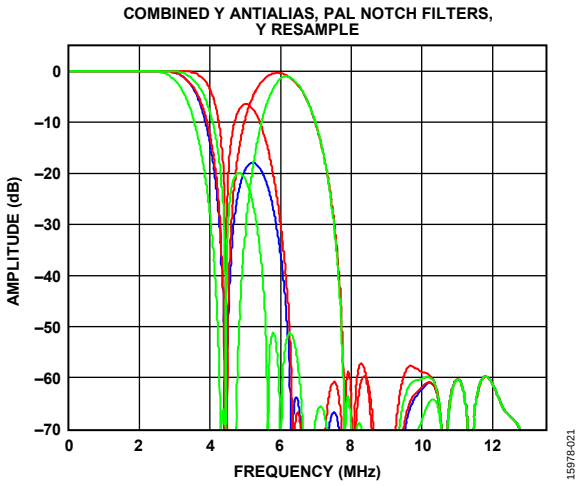

Figure 20. Combined Y Antialias, PAL Notch Filters

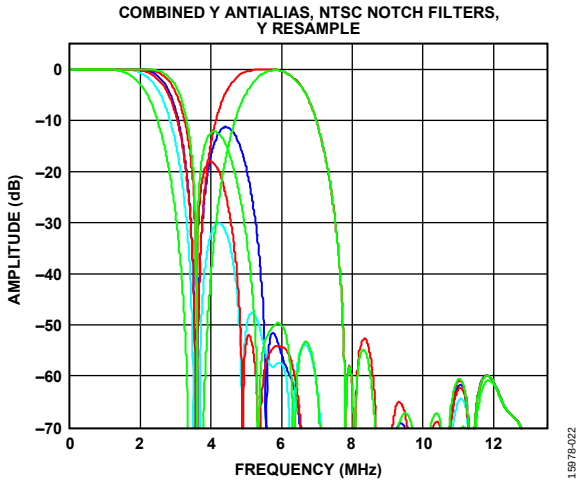

Figure 21. Combined Y Antialias Filter, NTSC Notch Filters

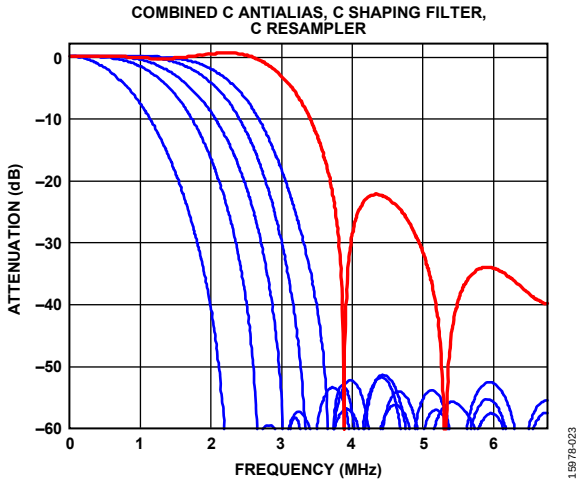

Figure 22. Chroma Shaping Filter Responses

CSFM[2:0], C Shaping Filter Mode—Address 0x17, Bits[7:5]

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see the 000 and 001 settings in Table 39).

Table 39. CSFM Function

CSFM[2:0]	Description
000 (default)	Autoselection 1.5 MHz bandwidth
001	Autoselection 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

Figure 22 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode (shown in red).

GAIN OPERATION

The gain control within the ADV7182A is performed on a purely digital basis. The input ADC supports a 10-bit range mapped into a 1.0 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

Advantages of this architecture over the commonly used programmable gain amplifier (PGA) before the ADC include the fact that the gain is completely independent of supply, temperature, and process variations.

As shown in Figure 25, the ADV7182A can decode a video signal as long as it fits into the ADC window. The components for this decoding are the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

Figure 23 and Figure 24 show the typical voltage divider networks required to keep the input video signal within the allowed range of the ADC, 0 V to 1 V. Place the circuit in Figure 23 before all the single-ended analog inputs to the ADV7182A, and place the circuit in Figure 24 before all the differential inputs to the ADV7182A.

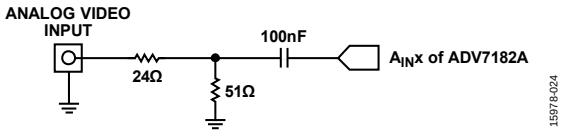

Figure 23. Single-Ended Input Voltage Divider Network

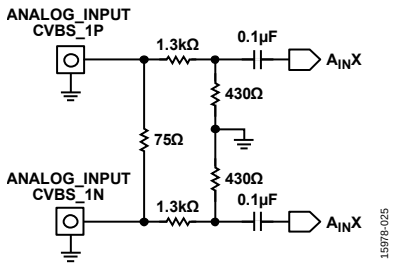

Figure 24. Differential Input Voltage Divider Network

The minimum supported amplitude of the input video is determined by the ability of the ADV7182A to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are separate gain control units for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are shown in Table 40.

Table 40. AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color burst amplitude taken from luma path
	Peak white	Dependent on color burst amplitude taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color burst amplitude taken from luma path
	Peak white	Dependent on color burst amplitude
YPrPb	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops, which causes the loops to stop updating and the AGC determined gain at the time of the freeze to stay active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual function manual gain registers, LG[11:0] luma gain and CG[11:0] chroma gain, in the Luma Gain section and the Chroma Gain section.

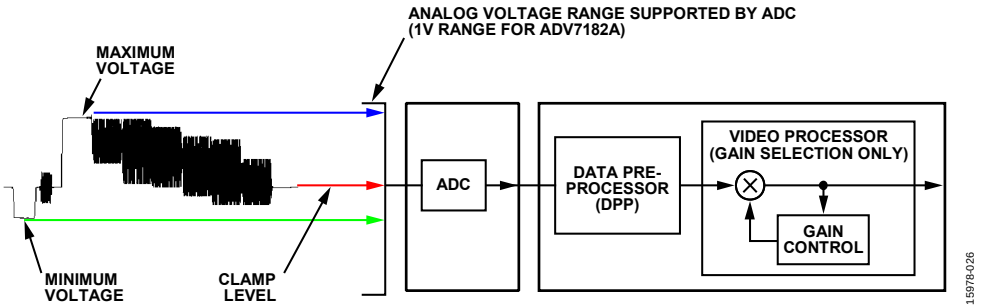

Figure 25. Gain Control Overview

Luma Gain

LAGC[2:0], Luma Automatic Gain Control—Address 0x2C, Bits[6:4]

The luma automatic gain control mode bits select the operating mode for the gain control in the luma path.

Table 41. LAGC Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip), peak white algorithm off
010 (default)	AGC (blank level to sync tip), peak white algorithm on
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0], Luma Automatic Gain Timing—Address 0x2F, Bits[7:6]

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. This register has an effect only if the LAGC[2:0] register is set to 001 or 010 (automatic gain control modes).

If peak white AGC is enabled and active (see the Status 1[7:0]—Address 0x10, Bits[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the device leaves peak white AGC, LAGT becomes relevant again.

Table 42. LAGT Function

LAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11 (default)	Adaptive

LG[11:0], Luma Gain—Address 0x2F[3:0] and Address 0x30[7:0]; LMG[11:0], Luma Manual Gain—Address 0x2F, Bits[3:0], Address 0x30, Bits[7:0]

Luma gain[11:0] is a dual function register. If all these bits are written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the LAGC[2:0] bits, the value is one of the following:

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to either of the automatic modes)

Table 43. LG/LMG Function

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = x	Write	Manual gain for luma path
LG[11:0] = x	Read	Actual used gain

$$Luma\ Gain \approx \frac{LMG[11:0]}{Luma\ Calibration\ Factor} \quad (1)$$

where *LMG[11:0]* is a decimal value between 1024 and 4095.

Calculation of the Luma Calibration Factor

Use the following procedure to calculate the luma calibration factor:

1. Using a video source, set the content to a gray field and apply as a standard CVBS signal to the CVBS input of the board.
2. Using an oscilloscope, measure the signal at the CVBS input to ensure that its sync depth, color burst, and luma are at the standard levels.
3. Connect the output parallel pixel bus of the ADV7182A to a backend system that has unity gain and monitor the output voltage.
4. Measure the luma level correctly from the black level. Turn off the luma AGC and manually change the value of the luma manual gain control register, LMG[11:0], until the output luma level matches the input measured in Step 2.

This value, in decimal, is the luma calibration factor.

BETACAM, Enable Betacam Levels—Address 0x01, Bit 5

If YPrPb data is routed through the ADV7182A, the automatic gain control modes can target different video input levels, as outlined in Table 47. The BETACAM bit is valid only if the input mode is YPrPb (component). The BETACAM bit sets the target value for AGC operation.

See the MAN_MUX_EN, Manual Input Muxing Enable—Address 0xC4, Bit 7 section for information on how component video (YPrPb) can be routed through the ADV7182A. See the Video Standard Selection section to select the various standards; for example, with and without pedestal.

The AGC algorithms adjust the levels based on the setting of the BETACAM bit (see Table 46).

PW_UPD, Peak White Update—Address 0x2B, Bit 0

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, see the LAGC[2:0], Luma Automatic Gain Control—Address 0x2C, Bits[6:4] section.

Setting PW_UPD to 0 updates the gain once per video line.

Setting PW_UPD to 1 (default) updates the gain once per field.

Chroma Gain

CAGC[1:0], Chroma Automatic Gain Control—Address 0x2C, Bits[1:0]

The two bits of the color automatic gain control mode select the basic mode of operation for the automatic gain control in the chroma path.

Table 44. CAGC Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Use Luma gain for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

CAGT[1:0], Chroma Automatic Gain Timing—Address 0x2D, Bits[7:6]

The chroma automatic gain timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register has an effect only if the CAGC[1:0] bits are set to 10 (automatic gain).

Table 45. CAGT Function

CAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Reserved
11 (default)	Adaptive

Table 46. BETACAM Function

BETACAM	Description
0 (default)	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects MII. Selecting PAL without pedestal selects SMPTE. Selecting NTSC with pedestal selects MII. Selecting NTSC without pedestal selects SMPTE.
1	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects BETACAM. Selecting PAL without pedestal selects BETACAM variant. Selecting NTSC with pedestal selects BETACAM. Selecting NTSC without pedestal selects BETACAM variant.

Table 47. BETACAM Levels

Name	BETACAM (mV)	BETACAM Variant (mV)	SMPTE (mV)	MII (mV)
Y	0 to +714 (including 7.5% pedestal)	0 to +714	0 to +700	0 to +700 (including 7.5% pedestal)
Pb and Pr	−467 to +467	−505 to +505	−350 to +350	−324 to +324
Sync Depth	+286	+286	+300	+300

CG[11:0], Chroma Gain—Address 0x2D, Bits[3:0], Address 0x2E, Bits[7:0]; CMG[11:0], Chroma Manual Gain—Address 0x2D, Bits[3:0], Address 0x2E, Bits[7:0]

Chroma gain[11:0] is a dual function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] function is switched to manual fixed gain. See Equation 2 for calculating a desired gain.
If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this gain value is either

- The chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
- The chroma automatic gain value (CAGC[1:0] set to either of the automatic modes).

Table 48. CG/CMG Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma\ Gain \approx \frac{CMG[11:0]_{Decimal}}{Chroma\ Calibration\ Factor} \quad (2)$$

where *Chroma Calibration Factor* is a decimal value between 0 and 4095.

Calculation of Chroma Calibration Factor

Take the following steps to calculate the chroma calibration factor:

1. Apply a CVBS signal with the color bars/SMPTE bars test pattern content directly to the measurement equipment.
2. Ensure correct termination of 75 Ω on the measurement equipment. Measure chroma output levels.
3. Reconnect the source to the CVBS input of the ADV7182A system that has a back end gain of 1. Repeat the measurement of chroma levels.
4. Turn off the chroma AGC and manually change the chroma gain control register, CMG[11:0], until the chroma level matches that measured directly from the source.

This value, in decimal, is the chroma calibration factor.

CKE, Color Kill Enable—Address 0x2B, Bit 6

The color kill enable bit allows the optional color kill function to be switched on or off.

For QAM-based video standards (PAL and NTSC), as well as FM-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled and the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Set CKE to 0 to disable color kill. Set CKE to 1 (default) to enable color kill.

CKILLTHR[2:0], Color Kill Threshold—Address 0x3D, Bits[6:4]

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM-based (NTSC and PAL) or FM-modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For the 000, 001, 010, and 011 settings, chroma demodulation inside the ADV7182A may not work satisfactorily for poor input video signals.

Table 49. CKILLTHR Function

	Description	
CKILLTHR[2:0]	**NTSC, PAL**	**SECAM**
000	Kill at <0.5%	No color kill
001	Kill at <1.5%	Kill at <5%
010 (default)	Kill at <2.5%	Kill at <7%
011	Kill at <4%	Kill at <8%
100	Kill at <8.5%	Kill at <9.5%
101	Kill at <16%	Kill at <15%
110	Kill at <32%	Kill at <32%
111	Reserved for Analog Devices internal use only; do not select	Reserved for Analog Devices internal use only; do not select

CHROMA TRANSIENT IMPROVEMENT (CTI)

The signal bandwidth allocated for chroma is typically much smaller than that for luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, may lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 26). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than that of the chroma component. The color edge is not sharp, and in the worst case it can be blurred over several pixels.

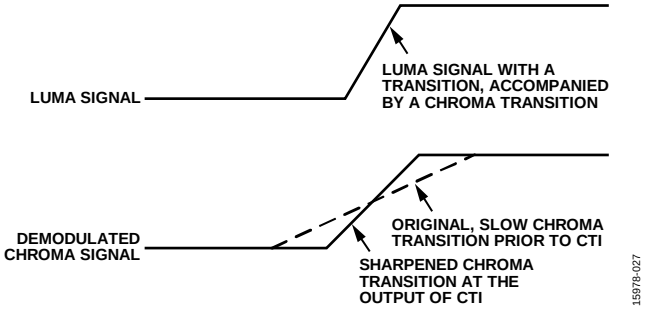

Figure 26. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to create steeper chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure that noise is not emphasized. Care was taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that have severe chroma bandwidth limitations. For these types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN, Chroma Transient Improvement (CTI) Enable—Address 0x4D, Bit 0

Set CTI_EN to 0 to disable the CTI block.

Set CTI_EN to 1 (default) to enable the CTI block.

CTI_AB_EN, Chroma Transient Improvement Alpha Blend Enable—Address 0x4D, Bit 1

The CTI_AB_EN bit enables an alpha blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI_EN bit.

Set CTI_AB_EN to 0 to disable the CTI alpha blender.

Set CTI_AB_EN to 1 (default) to enable the CTI alpha-blend mixing function.

CTI_AB[1:0], Chroma Transient Improvement Alpha Blend—Address 0x4D, Bits[3:2]

The CTI_AB[1:0] controls the behavior of alpha-blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become active, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture; however, it may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 50. CTI_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 (default)	Smoothest mixing between sharpened and original chroma signal

CTI_C_TH[7:0], CTI Chroma Threshold—Address 0x4E, Bits[7:0]

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition must be if it is going to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI_C_TH[7:0] is 0x08.

DIGITAL NOISE REDUCTION (DNR) AND LUMA PEAKING FILTER

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise and that their removal, therefore, improves picture quality. The two DNR blocks in the ADV7182A are the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 27.

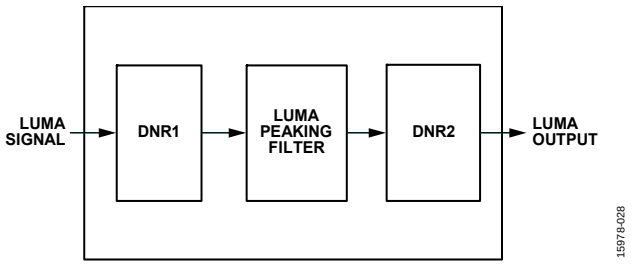

Figure 27. DNR and Peaking Block Diagram

DNR_EN, Digital Noise Reduction Enable—Address 0x4D, Bit 5

The DNR_EN bit enables the DNR block or bypasses it.

Table 51. DNR_EN Function

Setting	Description
0	Bypasses the DNR block (disable)
1 (default)	Enables the DNR block

DNR_TH[7:0], DNR Noise Threshold 1—Address 0x50, Bits[7:0]

The DNR1 block is positioned before the luma peaking block. The DNR_TH[7:0] value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 52. DNR_TH[7:0] Function

Setting	Description
0x08 (default)	Threshold for maximum luma edges to be interpreted as noise

PEAKING_GAIN[7:0], Luma Peaking Gain—Address 0xFB, Bits[7:0]

This filter can be manually enabled. The user can select to boost or to attenuate the midregion of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the luma data unaltered. A lower value attenuates the signal, and a higher value gains the luma signal. A plot of the responses of the filter is shown in Figure 28.

Table 53. PEAKING_GAIN[7:0] Function

Setting	Description
0x40 (default)	0 dB response

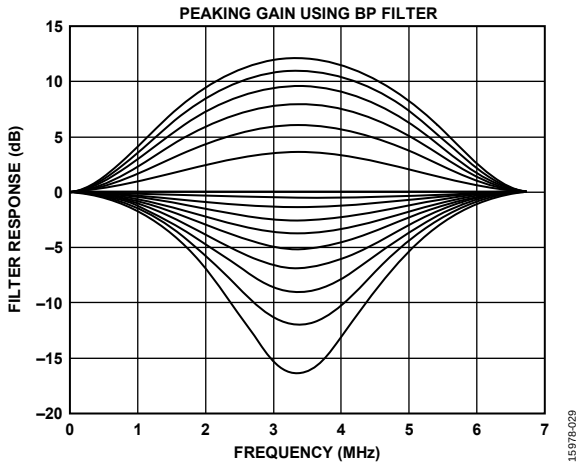

Figure 28. Peaking Filter Responses

DNR_TH2[7:0], DNR Noise Threshold 2—Address 0xFC, Bits[7:0]

The DNR2 block is positioned after the luma peaking block and, therefore, affects the gained luma signal. It operates in the same way as the DNR1 block; however, there is an independent threshold control, DNR_TH2[7:0], for this block. This value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH2[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 54. DNR_TH2[7:0] Function

Setting	Description
0x04 (default)	Threshold for maximum luma edges to be interpreted as noise

COMB FILTERS

The comb filters of the ADV7182A can automatically handle video of all types, standards, and levels of quality. The NTSC and PAL configuration registers allow the user to customize the comb filter operation depending on which video standard is detected (by autodetection) or selected (by manual programming).

NTSC Comb Filter Settings

The NTSC comb filter settings are used for NTSC M/NTSC J CVBS inputs.

NSFSEL[1:0], Split Filter Selection, NTSC—Address 0x19, Bits[3:2]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection results in better performance on diagonal lines but more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Table 55. NSFSEL Function

NSFSEL[1:0]	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

CTAPSN[1:0], Chroma Comb Taps, NTSC—Address 0x38, Bits[7:6]

Table 56. CTAPSN Function

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts three lines to two lines
10 (default)	NTSC chroma comb adapts five lines to three lines
11	NTSC chroma comb adapts five lines to four lines

CCMN[2:0], Chroma Comb Mode, NTSC—Address 0x38, Bits[5:3]

Table 57. CCMN Function

CCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Three-line adaptive chroma comb for CTAPSN = 01 Four-line adaptive chroma comb for CTAPSN = 10 Five-line adaptive chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMN[2:0], Luma Comb Mode, NTSC—Address 0x38, Bits[2:0]

Table 58. YCMN Function

YCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed luma comb two-line (two taps)
110	Fixed luma comb (all lines of line memory)	Fixed luma comb three-line (three taps)
111	Fixed luma comb (bottom lines of line memory)	Fixed luma comb two-line (two taps)

PAL Comb Filter Settings

The PAL comb filter settings are used for PAL B/PAL G/PAL H/PAL I/PAL D, PAL M, PAL Combination N, PAL 60, and NTSC 4.43 CVBS inputs.

PSFSEL[1:0], Split Filter Selection, PAL—Address 0x19, Bits[1:0]

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 59. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

CTAPSP[1:0], Chroma Comb Taps, PAL—Address 0x39, Bits[7:6]

Table 60. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use
01	PAL chroma comb adapts five lines (three taps) to three lines (two taps); cancels cross luma only
10	PAL chroma comb adapts five lines (five taps) to three lines (three taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts five lines (five taps) to four lines (four taps); cancels cross luma and hue error well

CCMP[2:0], Chroma Comb Mode, PAL—Address 0x39, Bits[5:3]

Table 61. CCMP Function

CCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMP[2:0], Luma Comb Mode, PAL—Address 0x39, Bits[2:0]

Table 62. YCMP Function

YCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive five lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed three lines (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed five lines (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed three lines (two taps) luma comb

IF FILTER COMPENSATION

IFFILTSEL[2:0], IF Filter Select—Address 0xF8, Bits[2:0]

The IFFILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input, as observed on tuner outputs. Figure 29 and Figure 30 show IF filter compensation for NTSC and PAL, respectively.

The options for this feature are as follows:

- Bypass mode.
- NTSC, consisting of three filter characteristics.
- PAL, consisting of three filter characteristics.

See Table 96 for programming details.

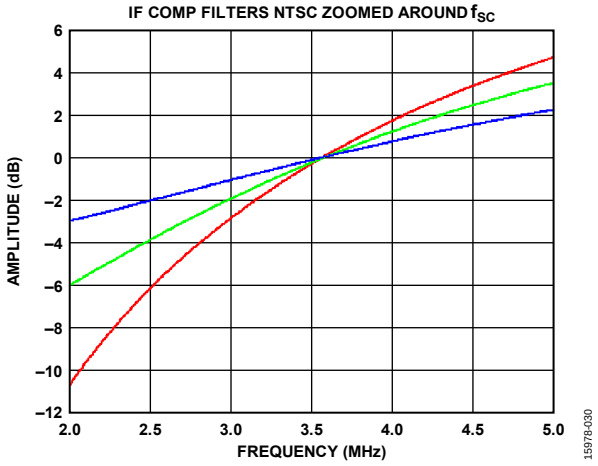

Figure 29. NTSC IF Filter Compensation

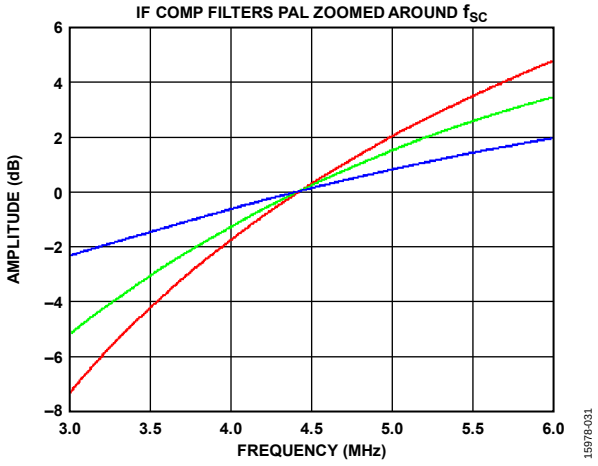

Figure 30. PAL IF Filter Compensation

ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The ADV7182A can increase the contrast of an image depending on the content of the picture, allowing bright areas to be made brighter and dark areas to be made darker. The optional ACE feature enables the contrast within dark areas to be increased without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

The ACE feature works by sampling the chroma and luma levels in the inputted image. This information is then histogrammed, and the resulting correction is applied to the entire image. This correction is performed in a nonlinear fashion so that more correction can be applied to dark areas if required.

For normal use, the luma and chroma gain controls can be used; however, in automotive applications, where dark areas may need to be further enhanced, also use the gamma gain controls.

The reaction time of the ACE function can be set using the ACE_RESPONSE_SPEED[7:4] bits (see Table 97). The corrected image is faded over the original image using alpha blending, giving a gradual change in contrast with scene changes. The ACE_RESPONSE_SPEED[7:4] bits determine the duration of the transition from the original to the corrected image. A larger value for these bits results in a faster transition time; however, a smaller value gives more stability to rapid scene changes.

The ACE_CHROMA_MAX[7:4] bits are used to set a maximum value that clips the chroma gain, regardless of the ACE_CHROMA_GAIN[3:0] settings.

The ACE_GAMMA_GAIN[3:0] bits are particularly useful in automotive applications because they allow dramatic image enhancement in dark regions by stretching the contrast of pixels at the low (dark) values of the image histogram. The luma and chroma gain controls are normally used; however, use the ACE_GAMMA_GAIN[3:0] bits when further stretching of the contrast in the dark areas of an image is required.

ACE_ENABLE, User Sub Map 2—Address 0x80, Bit 7

This bit enables ACE.

Table 63. ACE_ENABLE Function

ACE_ENABLE	Description
0 (default)	Disable ACE
1	Enable ACE

ACE_LUMA_GAIN[4:0], User Sub Map 2—Address 0x83, Bits[4:0]

Thes bits provide a control to set the autocontrast level for the luma channel when ACE_ENABLE is 1.

Table 64. ACE_LUMA_GAIN Function

ACE_LUMA_GAIN[4:0]	Description
00000	Set ACE luma autocontrast level to minimum value
01101 (default)	Set ACE luma autocontrast level to default value
11111	Set ACE luma autocontrast level to maximum value

ACE_RESPONSE_SPEED[3:0], User Sub Map 2—Address 0x85, Bits[7:4]

These bits set the reaction time of the ACE function.

Table 65. ACE_RESPONSE_SPEED Function

ACE_ RESPONSE_SPEED[3:0]	Description
0000	Set speed of ACE response to slowest value
1111 (default)	Set speed of ACE response to fastest value

ACE_CHROMA_GAIN[3:0], User Sub Map 2—Address 0x84, Bits[3:0]

This control sets the color saturation level for the color channels when ACE_ENABLE is 1.

Table 66. ACE_CHROMA_GAIN Function

ACE_CHROMA_GAIN[3:0]	Description
0000	Set ACE color auto-saturation level to minimum value
1000 (default)	Set ACE color auto-saturation level to default value
1111	Set ACE color auto-saturation level to maximum value

ACE_CHROMA_MAX[3:0], User Sub Map 2—Address 0x84, Bits[7:4]

This control sets a maximum threshold value that clips the chroma gain, regardless of the ACE_CHROMA_GAIN[3:0] settings.

Table 67. ACE_CHROMA_MAX Function

ACE_CHROMA_MAX[3:0]	Description
0000	Set maximum threshold for ACE color autosaturation level to minimum value
1000 (default)	Set maximum threshold for ACE color autosaturation level to default value
1111	Set maximum threshold for ACE color autosaturation level to maximum value

ACE_GAMMA_GAIN[3:0], User Sub Map 2—Address 0x85, Bits[3:0]

This control provides further contrast enhancement to the luma and chroma gain controls and is particularly effective in the darker areas of an image.

Table 68. ACE_GAMMA_GAIN[3:0] Function

ACE_GAMMA_GAIN[3:0]	Description
0000	Set further contrast enhancement to minimum value
1000 (default)	Set further contrast enhancements to default value
1111	Set further contrast enhancement to maximum value

DITHER FUNCTION

The dither function converts the digital output of the ADV7182A from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV7182A to communicate with some LCD panels. The dither function is turned off by default. It is activated by the BR_DITHER_MODE bit.

BR_DITHER_MODE, User Sub Map 2—Address 0x92, Bit 0

Table 69. BR_DITHER_MODE Function

BR_DITHER_MODE	Description
0 (default)	8-bit to 6-bit downdither disabled
1	8-bit to 6-bit downdither enabled

AV CODE INSERTION AND CONTROLS

This section describes the I²C-based controls that affect the following:

- Insertion of AV codes into the data stream.
- Data blanking during the VBI.
- The range of data values permitted in the output data stream.
- The relative delay of luma vs. chroma signals.

BT.656-4, ITU-R BT.656-3/ITU-R BT.656-4 Enable—Address 0x04, Bit 7

Between Revision 3 and Revision 4 of the ITU-R BT.656 standards, the ITU changed the toggling position for the V bit within the SAV EAV codes for NTSC. The ITU-R BT.656-4 standard bit allows the user to select an output mode that is compliant with either the ITU-R BT.656-3 standard or ITU-R BT.656-4 standard. For further information, visit the International Telecommunication Union website.

Note that the standard change affects only NTSC and has no bearing on PAL.

When ITU-R BT.656-4 is set to 0 (default), the ITU-R BT.656-3 specification is used. The V bit goes low at EAV of Line 10 and Line 273.

When ITU-R BT.656-4 is 1, the ITU-R BT.656-4 specification is used. The V bit goes low at EAV of Line 20 and Line 283.

VBI_EN, Vertical Blanking Interval Data Enable—Address 0x03, Bit 7

The VBI enable bit allows data such as intercast and closed caption data to be passed through the luma channel of the decoder with a minimal amount of filtering. All data for Line 1 to Line 21 is passed through and available at the output port. The ADV7182A does not blank the luma data and automatically switches all filters along the luma datapath into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

See the BL_C_VBI, Blank Chroma During VBI—Address 0x04, Bit 2 section for information on the chroma path.

When VBI_EN is set to 0 (default), all video lines are filtered/scaled.

When VBI_EN is 1, only the active video region is filtered/scaled.

BL_C_VBI, Blank Chroma During VBI—Address 0x04, Bit 2

Setting BL_C_VBI to 1 blanks the Cr and Cb values of all VBI lines so that any data that may arrive during VBI is not decoded as color and is output through Cr and Cb. As a result, it is possible to send VBI lines into the decoder and then output them through an encoder again, undistorted. Without this blanking, any color that is incorrectly decoded is encoded by the video encoder, thus distorting the VBI lines.

Setting BL_C_VBI to 0 decodes and outputs color during VBI.

Setting BL_C_VBI to 1 (default) blanks Cr and Cb values during VBI.

Range, Range Selection—Address 0x04, Bit 0

AV codes (as per ITU-R BT.656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and, therefore, are not to be used for active video. Additionally, the ITU specifies that the nominal range for video must be restricted to values between 16 and 235 for luma and 16 and 240 for chroma.

The range bit allows the user to limit the range of values output by the ADV7182A to the recommended value range. In any case, it ensures that the reserved values of 255d (0xFF) and 00d (0x00) are not presented on the output pins, unless they are part of an AV code header.

Table 70. Range Function

Range	Description
0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240
1 (default)	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254

AUTO_PDC_EN, Automatic Programmed Delay Control—Address 0x27, Bit 6

Enabling AUTO_PDC_EN activates a function within the ADV7182A that automatically programs the LTA[1:0] and CTA[2:0] registers to have the chroma and luma data match delays for all modes of operation. If AUTO_PDC_EN is 1, the LTA[1:0] and CTA[2:0] manual registers are not used. If the automatic mode is disabled (by setting the AUTO_PDC_EN bit

to 0), the values programmed into the LTA[1:0] and CTA[2:0] registers become active.

When AUTO_PDC_EN is set to 0, the ADV7182A uses the LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. See the LTA[1:0], Luma Timing Adjust—Address 0x27, Bits[1:0] section and the CTA[2:0], Chroma Timing Adjust—Address 0x27, Bits[5:3] section.

When AUTO_PDC_EN is 1 (default), the ADV7182A automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

LTA[1:0], Luma Timing Adjust—Address 0x27, Bits[1:0]

The luma timing adjust bits allow the user to specify a timing difference between chroma and luma samples.

There is a functionality overlap with the CTA[2:0] register. For manual programming, use the following default values:

- CVBS input LTA[1:0] = 00
- Y/C input LTA[1:0] = 01
- YPrPb input LTA[1:0] = 01

Table 71. LTA Function

LTA[1:0]	Description
00 (default)	No delay
01	Luma one clock (37 ns) late
10	Luma two clock (74 ns) early
11	Luma one clock (37 ns) early

CTA[2:0], Chroma Timing Adjust—Address 0x27, Bits[5:3]

The chroma timing adjust register allows the user to specify a timing difference between chroma and luma samples, which can be used to compensate for external filter group delay differences in the luma vs. chroma path and to allow a different number of pipeline delays while processing the video downstream. Review this functionality together with the LTA[1:0] bits.

The chroma can be delayed or advanced only in chroma pixel steps. One chroma pixel step is equal to two luma pixels. The programmable delay occurs after demodulation, where delay cannot be made by luma pixel steps.

For manual programming, use the following default values:

- CVBS input CTA[2:0] = 011
- Y/C input CTA[2:0] = 101
- YPrPb input CTA[2:0] = 110

Table 72. CTA Function

CTA[2:0]	Description
000	Reserved
001	Chroma + two pixels (early)
010	Chroma + one pixel (early)
011 (default)	No delay
100	Chroma – one pixel (late)
101	Chroma – two pixels (late)
110	Chroma – three pixels (late)
111	Reserved

SYNCHRONIZATION OUTPUT SIGNALS

HSYNC Configuration

The following controls allow the user to configure the behavior of the HSYNC output signal only:

- Beginning of HSYNC signal via HSB[10:0]
- End of HSYNC signal via HSE[10:0]
- Polarity of HSYNC using PHS

The HSYNC signal can be output on the VS/FIELD/SFL pin or the HS pin (see the Global Pin Control section.)

The HSYNC begin (HSB) and HSYNC end (HSE) registers allow the user to freely position the HSYNC signal within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HSYNC. Using both values, the user can program both the position and length of the HSYNC output signal.

HSB[10:0], HSYNC Begin—Address 0x34, Bits[6:4], Address 0x35, Bits[7:0]

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 31). HSB is set to 00000000010b, which is two LLC clock cycles from count [0].

The default value of HSB[10:0] is 0x02, indicating that the HSYNC pulse starts two pixels after the falling edge of HSYNC.

HSE[10:0], HSYNC End—Address 0x34, Bits[2:0], Address 0x36, Bits[7:0]

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 31). HSE is set to 00000000000b, which is 0 LLC clock cycles from count [0].

The default value of HSE[10:0] is 00, indicating that the HSYNC pulse ends 0 pixels after the falling edge of HSYNC.

For example,

- To shift the HSYNC toward active video by 20 LLCs, add 20 LLCs to both HSB and HSE, that is, HSB[10:0] = [00000010110], HSE[10:0] = [00000010100].
- To shift the HSYNC away from active video by 20 LLCs, add 1696 LLCs to both HSB and HSE (for NTSC), that is, HSB[10:0] = [11010100010], HSE[10:0] = [11010100000]. Therefore, 1696 is derived from the NTSC total number of pixels, 1716.
- To move 20 LLCs away from active video, subtract 20 from 1716 and add the result in binary to both HSB[10:0] and HSE[10:0].

PHS, HSYNC Polarity—Address 0x37, Bit 7

The polarity of the HSYNC signal can be inverted using the PHS bit. When PHS is 0 (default), HSYNC is active low. When PHS is 1, HSYNC is active high.

Table 73. HS Timing Parameters

	Characteristic				
Standard	HS Begin Adjust, HSB[10:0] (Default)	HS End Adjust, HSE[10:0] (Default)	HS to Active Video, LLC Clock Cycles, C in Figure 31 (Default)	Active Video Samples/ Line, D in Figure 31	Total LLC Clock Cycles, E in Figure 31
NTSC	00000000010b	00000000000b	272	720Y + 720C = 1440	1716
PAL	00000000010b	00000000000b	284	720Y + 720C = 1440	1728

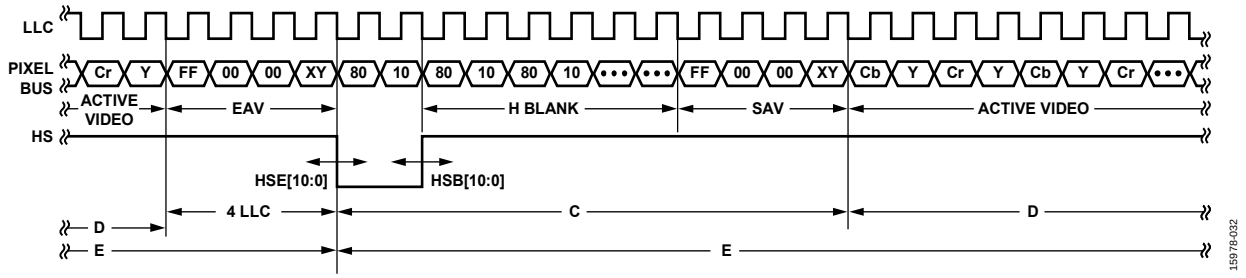

Figure 31. HSYNC Timing

VSYNC and FIELD Configuration

The following controls allow the user to configure the behavior of the VSYNC and FIELD output signals, as well as the generation of embedded AV codes. Note that the VSYNC and FIELD signals can be output on the VS/FIELD/SFL pin or the HS pin (see the Global Pin Control section).

NEWAVMODE, New AV Mode—Address 0x31, Bit 4

When NEWAVMODE is 0, EAV/SAV codes are generated to suit Analog Devices encoders. No adjustments are possible.

When NEWAVMODE is 1 (default), it enables the manual position of the VSYNC, FIELD, and AV codes using Register 0x32 to Register 0x33 and Register 0xE5 to Register 0xEA. The default register settings are CCIR656 (BT.565-4) compliant (see Figure 32 and Figure 33 for NTSC; see Figure 37 and Figure 38 for PAL).

HVSTIM, Horizontal VSYNC Timing—Address 0x31, Bit 3

The HVSTIM bit allows the user to select where the VSYNC signal is asserted within a line of video. Some interface circuitry may require VSYNC to go low while HSYNC is low.

When HVSTIM is 0 (default), the start of the line is relative to HSE. When HVSTIM is 1, the start of the line is relative to HSB.

VSBHO, VSYNC Begin Horizontal Position Odd—Address 0x32, Bit 7

The VSBHO and VSBHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HSYNC is high or low.

When VSBHO is 0 (default), the VSYNC signal goes high in the middle of a line of video (odd field). When VSBHO is 1, the VSYNC signal changes state at the start of a line (odd field).

VSBHE, VSYNC Begin Horizontal Position Even—Address 0x32, Bit 6

The VSBHO and VSBHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HS is high or low.

When VSBHE is 0 (default), the VSYNC signal goes high in the middle of a line of video (even field). When VSBHE is 1, the VSYNC signal changes state at the start of a line (even field).

VSEHO, VSYNC End Horizontal Position Odd—Address 0x33, Bit 7

The VSEHO and VSEHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HSYNC is high or low.

When VSEHO is 0 (default), the VSYNC signal goes low (inactive) in the middle of a line of video (odd field). When VSEHO is 1, the VSYNC signal changes state at the start of a line (odd field).

VSEHE, VSYNC End Horizontal Position Even—Address 0x33, Bit 6

The VSEHO and VSEHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HS is high or low.

When VSEHE is 0 (default), the VSYNC signal goes low (inactive) in the middle of a line of video (even field). When VSEHE is 1, the VSYNC signal changes state at the start of a line (even field).

PVS, VSYNC Polarity—Address 0x37, Bit 5

The polarity of the VSYNC signal can be inverted using the PVS bit.

When PVS is 0 (default), VSYNC is active high. When PVS is 1, VSYNC is active low.

PF, FIELD Polarity—Address 0x37, Bit 3

The FIELD pin can be inverted using the PHS bit.

When PHS is 0 (default), FIELD pin is active high. When PHS is 1, FIELD pin is active low.

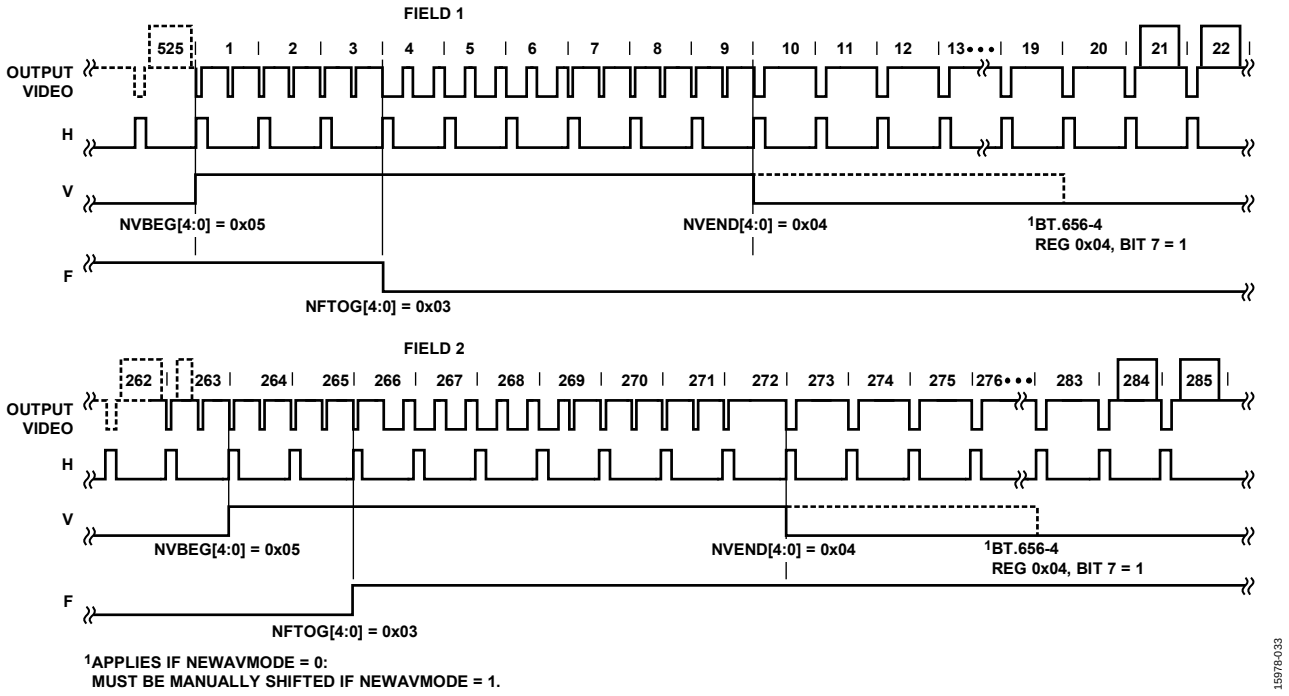

Figure 32. NTSC Default, ITU-R BT.656 (Polarity of H, V, and F Embedded in Data)

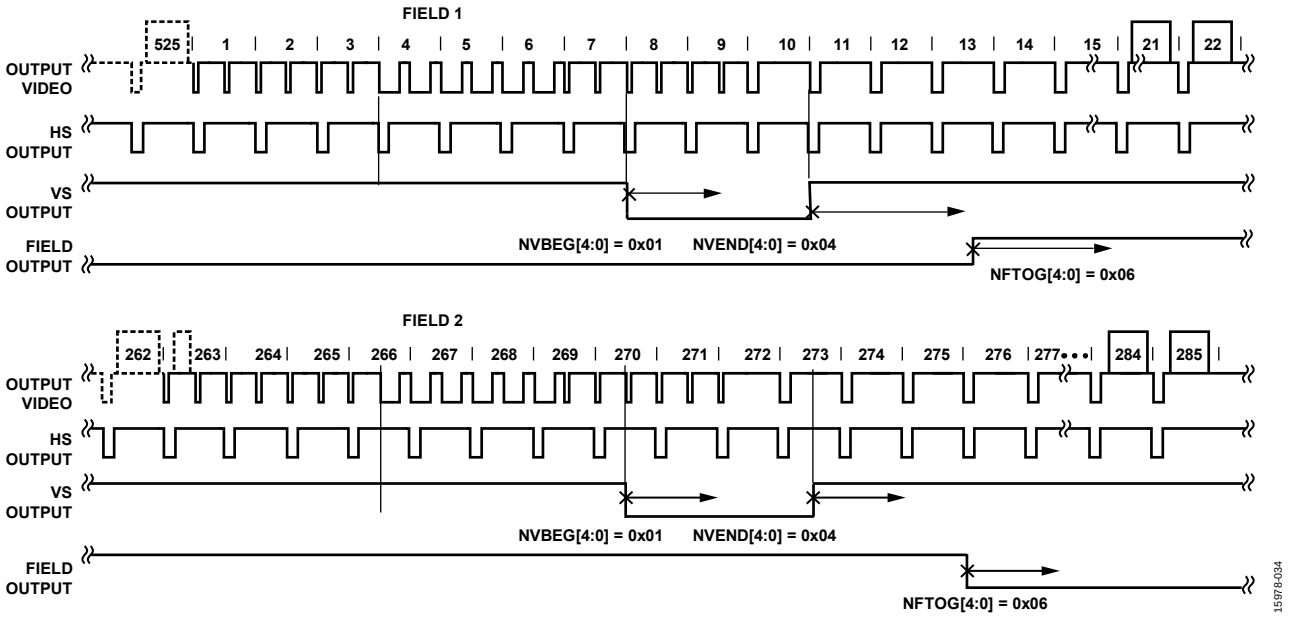

Figure 33. NTSC Typical VS/FIELD Positions

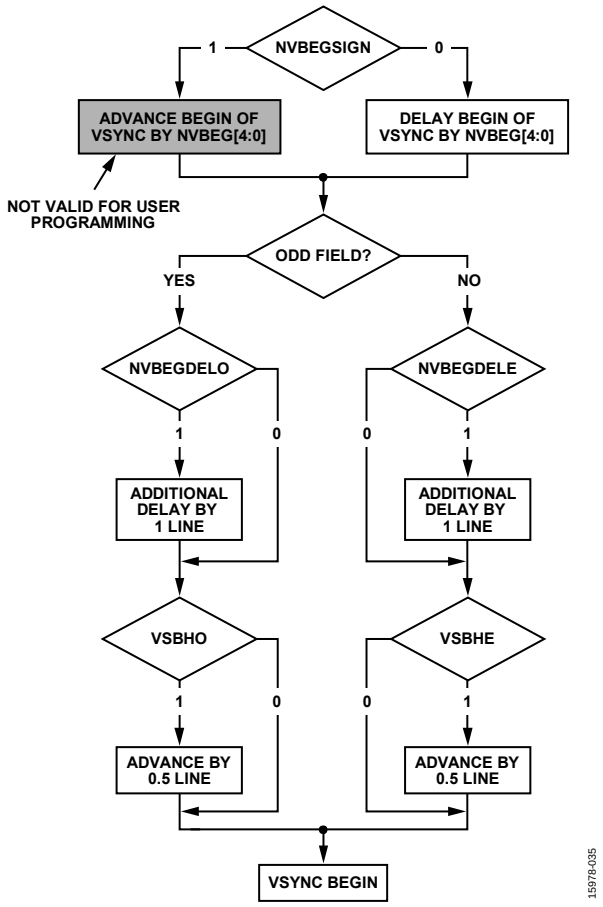

Figure 34. NTSC VSYNC Begin

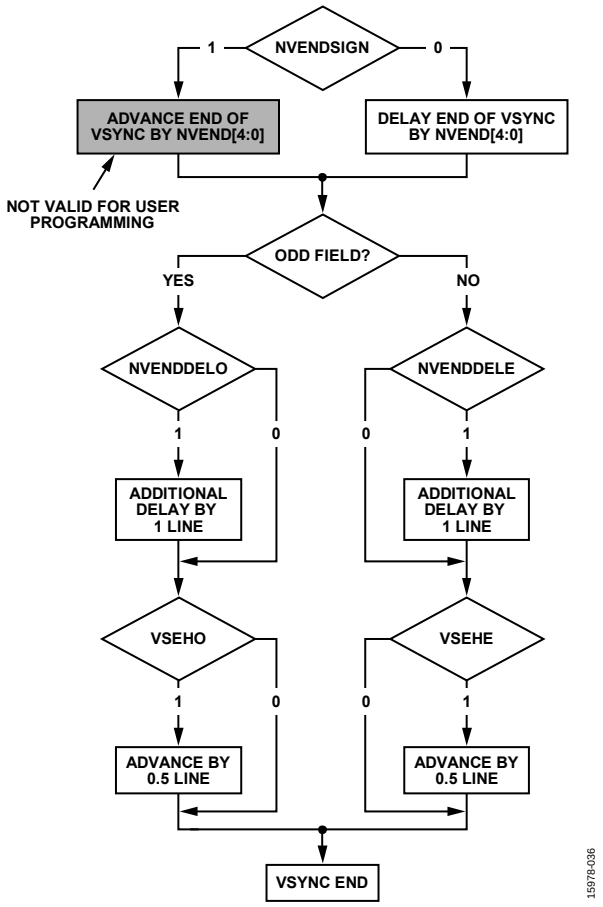

Figure 35. NTSC VSYNC End

NVBEGDELO, NTSC VSYNC Begin Delay on Odd Field—Address 0xE5, Bit 7

When NVBEGDELO is 0 (default), there is no delay.

Setting NVBEGDELO to 1 delays VSYNC going high by one line relative to NVBEG (odd field).

NVBEGDELE, NTSC VSYNC Begin Delay on Even Field—Address 0xE5, Bit 6

When NVBEGDELE is 0 (default), there is no delay.

Setting NVBEGDELE to 1 delays VSYNC going high by one line relative to NVBEG (even field).

NVBEGSIGN, NTSC VSYNC Begin Sign—Address 0xE5, Bit 5

Setting NVBEGSIGN to 0 delays the start of VSYNC; sets to low when manual programming.

Setting NVBEGSIGN to 1 (default) advances the start of VSYNC; however, it is not suitable for user programming.

NVBEG[4:0], NTSC VSYNC Begin—Address 0xE5, Bits[4:0]

The default value of NVBEG is 00101, indicating the NTSC VSYNC begin position. For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

NVENDDELO, NTSC VSYNC End Delay on Odd Field—Address 0xE6, Bit 7

When NVENDDELO is 0 (default), there is no delay.

Setting NVENDDELO to 1 delays VSYNC going low by one line relative to NVEND (odd field).

NVENDDELE, NTSC VSYNC End Delay on Even Field—Address 0xE6, Bit 6

When NVENDDELE is 0 (default), there is no delay.

Setting NVENDDELE to 1 delays VSYNC going low by a line relative to NVEND (even field).

NVENDSIGN, NTSC VSYNC End Sign—Address 0xE6, Bit 5

Setting NVENDSIGN to 0 (default) delays the end of VSYNC; sets to low when manual programming.

Setting NVENDSIGN to 1 advances the end of VSYNC; however, it is not suitable for user programming.

NVEND[4:0], NTSC VSYNC End—Address 0xE6, Bits[4:0]

The default value of NVEND is 00100, indicating the NTSC VSYNC end position.

For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

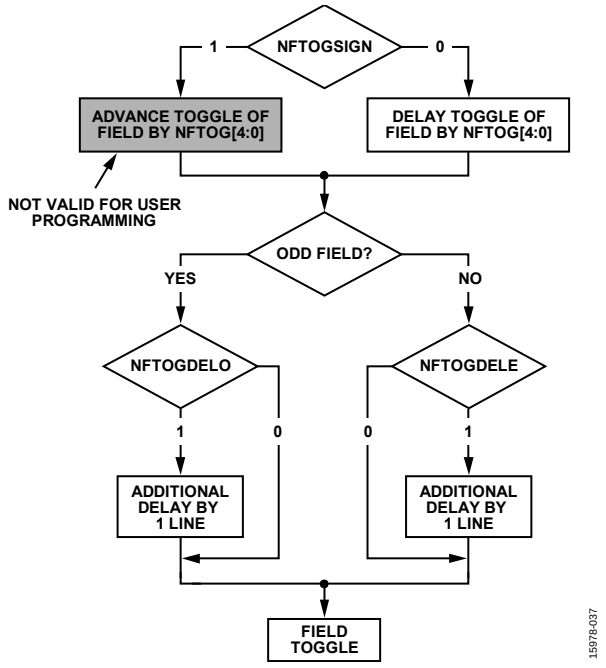

Figure 36. NTSC FIELD Toggle

NFTOGDELO, NTSC FIELD Toggle Delay on Odd Field—Address 0xE7, Bit 7

When NFTOGDELO is 0 (default), there is no delay.

Setting NFTOGDELO to 1 delays the FIELD toggle/transition by one line relative to NFTOG (odd field).

NFTOGDELE, NTSC FIELD Toggle Delay on Even Field—Address 0xE7, Bit 6

When NFTOGDELE is 0, there is no delay.

Setting NFTOGDELE to 1 (default) delays the FIELD toggle/transition by one line relative to NFTOG (even field).

NFTOGSIGN, NTSC FIELD Toggle Sign—Address 0xE7, Bit 5

Setting NFTOGSIGN to 0 delays the FIELD toggle/transition; sets to low when manual programming.

Setting NFTOGSIGN to 1 (default) advances the FIELD toggle/transition; however, it is not suitable for user programming.

NFTOG[4:0], NTSC FIELD Toggle—Address 0xE7, Bits[4:0]

The default value of NFTOG is 00011, indicating the NTSC field toggle position.

For all NTSC/PAL field timing controls, both the F bit in the AV code and the field signal are modified.

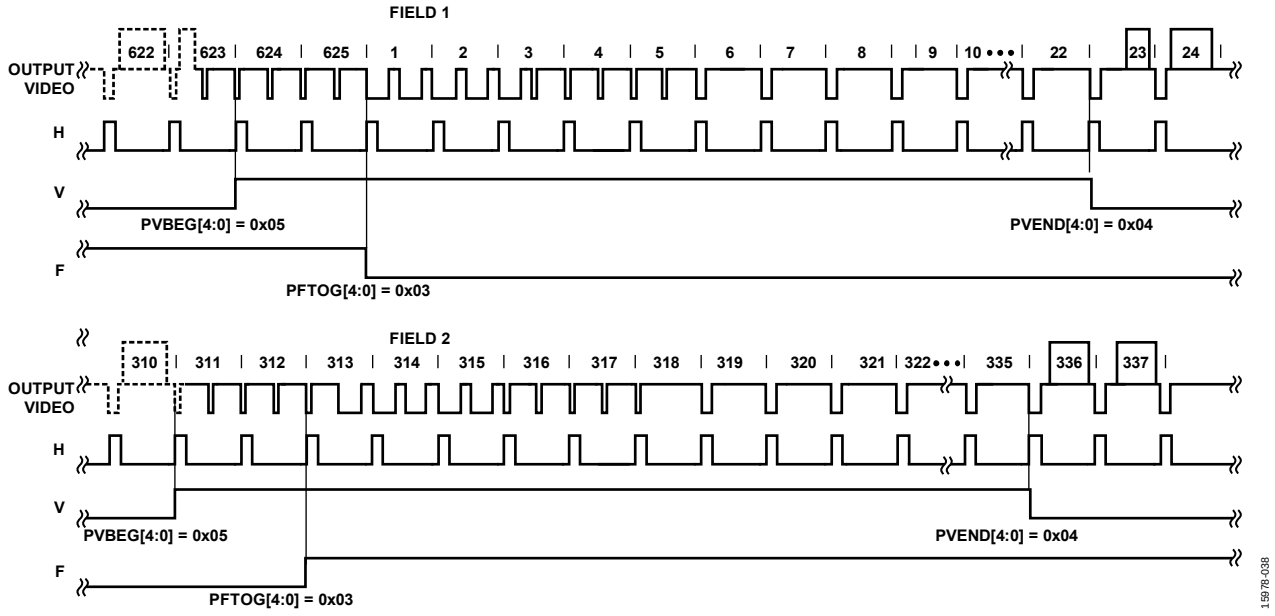

Figure 37. PAL Default, ITU-R BT.656 (Polarity of H, V, and F Embedded in Data)

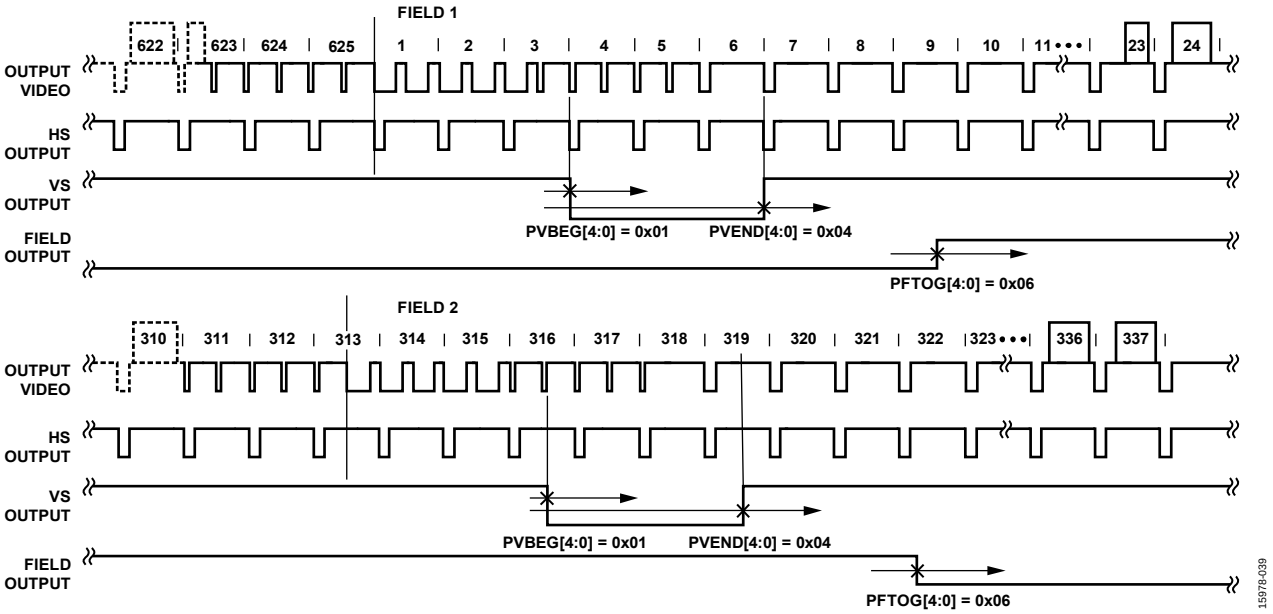

Figure 38. PAL Typical VS/FIELD Positions

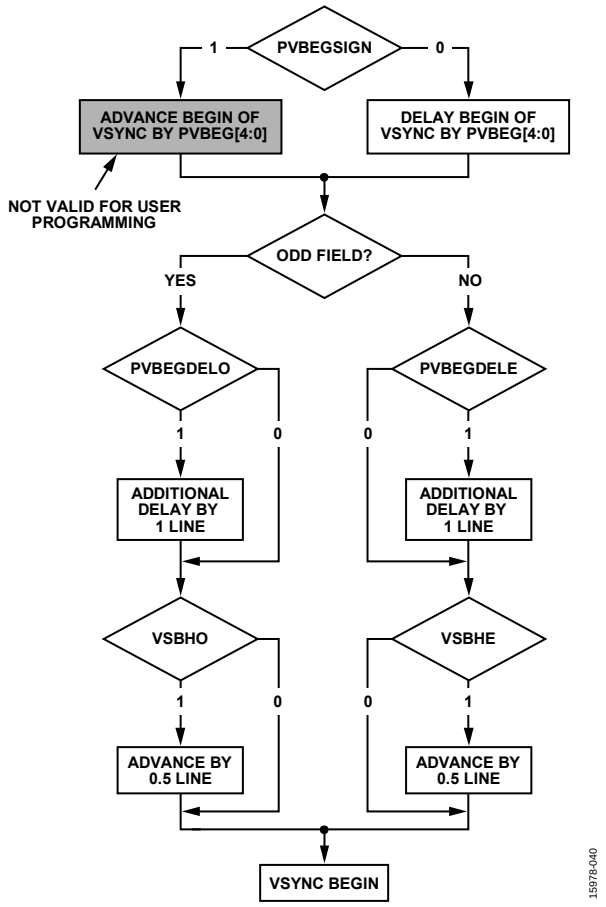

Figure 39. PAL VSYNC Begin

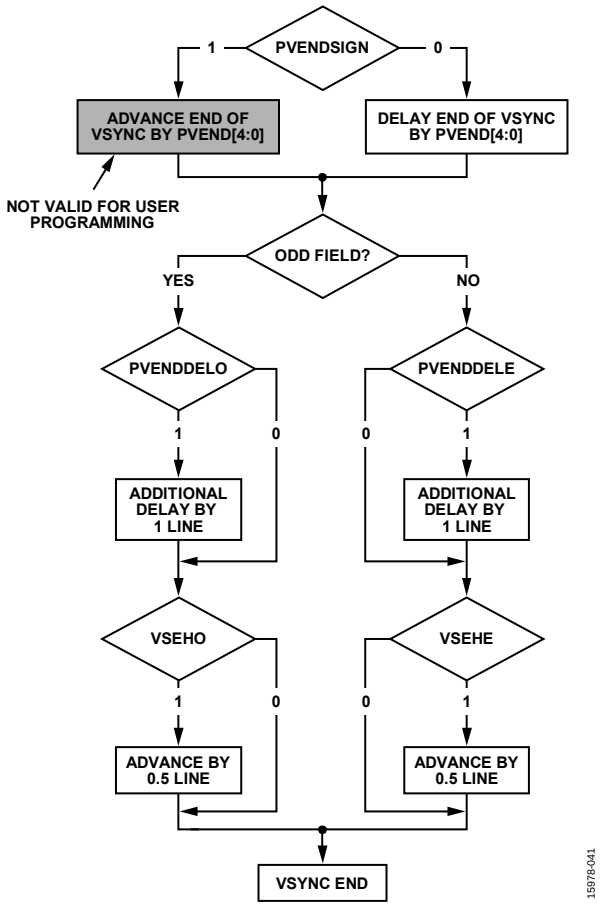

Figure 40. PAL VSYNC End

PVBEGDELO, PAL VSYNC Begin Delay on Odd Field—Address 0xE8, Bit 7

When PVBEGDELO is 0 (default), there is no delay.

Setting PVBEGDELO to 1 delays VSYNC going high by one line relative to PVBEG (odd field).

PVBEGDELE, PAL VSYNC Begin Delay on Even Field—Address 0xE8, Bit 6

When PVBEGDELE is 0, there is no delay.

Setting PVBEGDELE to 1 (default) delays VSYNC going high by one line relative to PVBEG (even field).

PVBEGSIGN, PAL VSYNC Begin Sign—Address 0xE8, Bit 5

Setting PVBEGSIGN to 0 delays the beginning of VSYNC; this bit is set low during manual programming.

Setting PVBEGSIGN to 1 (default) advances the beginning of VSYNC; however, it is not suitable for user programming.

PVBEG[4:0], PAL VSYNC Begin—Address 0xE8, Bits[4:0]

The default value of PVBEG is 00101, indicating the PAL VSYNC begin position. For all NTSC/PAL VSYNC timing controls, the V bit in the AV code and the VSYNC signal are modified.

PVENDDELO, PAL VSYNC End Delay on Odd Field—Address 0xE9, Bit 7

When PVENDDELO is 0 (default), there is no delay.

Setting PVENDDELO to 1 delays VSYNC going low by one line relative to PVEND (odd field).

PVENDDELE, PAL VSYNC End Delay on Even Field—Address 0xE9, Bit 6

When PVENDDELE is 0 (default), there is no delay.

Setting PVENDDELE to 1 delays VSYNC going low by one line relative to PVEND (even field).

PVENDSIGN, PAL VSYNC End Sign—Address 0xE9, Bit 5

Setting PVENDSIGN to 0 (default) delays the end of VSYNC; this bit is set low during manual programming.

Setting PVENDSIGN to 1 advances the end of VSYNC; however, it is not suitable for user programming.

PVEND[4:0], PAL VSYNC End—Address 0xE9, Bits[4:0]

The default value of PVEND is 10100, indicating the PAL VSYNC end position.

For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

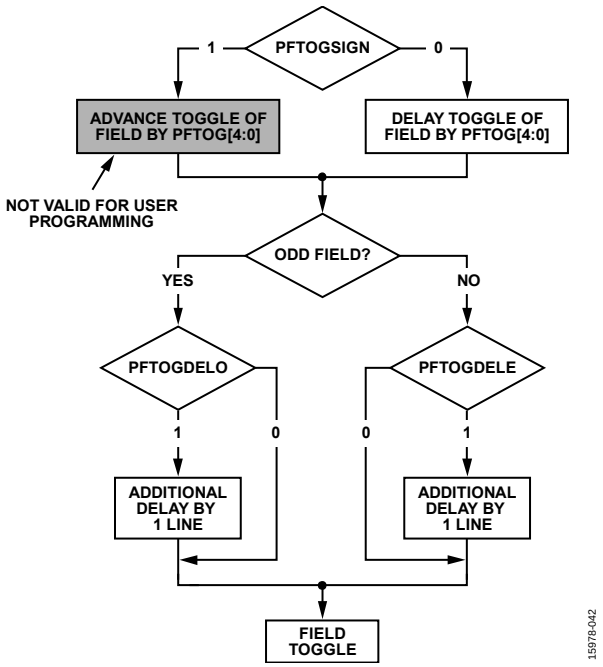

Figure 41. PAL FIELD Toggle

PFTOGDELO, PAL FIELD Toggle Delay on Odd Field—Address 0xEA, Bit 7

When PFTOGDELO is 0 (default), there is no delay.

Setting PFTOGDELO to 1 delays the FIELD toggle/transition by one line relative to PFTOG (odd field).

PFTOGDELE, PAL FIELD Toggle Delay on Even Field—Address 0xEA, Bit 6

When PFTOGDELE is 0, there is no delay.

Setting PFTOGDELE to 1 (default) delays the FIELD toggle/transition by one line relative to PFTOG (even field).

PFTOGSIGN, PAL FIELD Toggle Sign—Address 0xEA, Bit 5

Setting PFTOGSIGN to 0 delays the field transition and set to low when manual programming.

Setting PFTOGSIGN to 1 (default) advances the field transition; however, it is not suitable for user programming.

PFTOG, PAL FIELD Toggle—Address 0xEA, Bits[4:0]

The default value of PFTOG is 00011, indicating the PAL field toggle position.

For all NTSC/PAL field timing controls, the F bit in the AV code and the FIELD signal are modified.

SYNC PROCESSING

The ADV7182A has two additional sync processing blocks that postprocess the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the ENHSPLL and ENVSPROC I²C bits.

ENHSPLL, Enable HSYNC Processor—Address 0x01, Bit 6

The HSYNC processor filters incoming HSYNCs that are corrupted by noise, providing improved performance for video signals with stable time bases but poor SNR.

Setting ENHSPLL to 0 disables the HSYNC processor.

Setting ENHSPLL to 1 (default) enables the HSYNC processor.

ENVSPROC, Enable VSYNC Processor—Address 0x01, Bit 3

This block provides extra filtering of the detected VSYNCs to improve vertical lock.

Setting ENVSPROC to 0 disables the VSYNC processor.

Setting ENVSPROC to 1 (default) enables the VSYNC processor.

VBI DATA DECODE

The VBI data processor (VDP) on the ADV7182A can slice both low bandwidth standards and high bandwidth standards such as teletext.

The VDP is capable of slicing multiple VBI data standards on SD video. It decodes the VBI data on the incoming CVBS and Y/C or YUV data. The decoded results are available as ancillary data in output 656 data stream. For low data rate VBI standards like CC/WSS/CGMS, the decoded data bytes can be read from the I²C registers.

The VBI data standards that can be decoded by the VDP are listed in Table 74 and Table 75.

Table 74. PAL

Feature	Standard
Teletext System A, Teletext System C, or Teletext System D	ITU-R BT.653
Teletext System B/Teletext System WST	ITU-R BT.653
Wide Screen Signaling (WSS)	ITU-R BT.1119-1/ ETSI EN.300294
Closed Captioning (CCAP)	Not applicable

Table 75. NTSC

Feature	Standard
Teletext System B and Teletext System D	ITU-R BT.653
Teletext System C/Teletext System NABTS	ITU-R BT.653/ EIA-516
Copy Generation Management System (CGMS)	EIA-J CPR-1204/ IEC 61880
Closed Captioning (CCAP)	EIA-608

The VBI data standard that the VDP decodes on a particular line of incoming video is set by default as described in Table 76. This setting can be overridden manually and any VBI data can be decoded on any line. The details of manual programming are described in Table 77.

VDP Default Configuration

The VDP can decode different VBI data standards on a line to line basis. The various standards supported by default on different lines of VBI are explained in Table 76.

VDP Manual Configuration

MAN_LINE_PGM, Enable Manual Line Programming of VBI Standards—Address 0x64, Bit 7, Interrupt/VDP Map

The user can configure the VDP to decode different standards on a line to line basis through manual line programming. For this, set the MAN_LINE_PGM bit. The user must write into all the line programming registers, VBI_DATA_Px_Ny and VBI_DATA_Px (see Register 0x64 to Register 0x77 in Table 98).

When MAN_LINE_PGM is set to 0 (default), the VDP decodes default standards on lines, as shown in Table 76.

When MAN_LINE_PGM is set to 1, the VBI standards to be decoded are manually programmed.

VBI_DATA_Px_Ny[3:0], VBI_DATA_Px[3:0], VBI Standard to be Decoded on Line x for PAL, Line Y for NTSC—Address 0x64 to Address 0x77, Interrupt/VDP Map

These are related 4-bit clusters in Register 0x64 to Register 0x77 of the interrupt/VDP map details (see Table 95). These 4-bit, line programming registers, VBI_DATA_Px_Ny and VBI_DATA_Px, identify the VBI data standard that is decoded on Line x in PAL mode or on Line Y in NTSC mode. The different types of VBI standards decoded by VBI_DATA_Px_Ny and VBI_DATA_Px are shown in Table 77. Note that the X or Y value depends on whether the ADV7182A is in PAL or NTSC mode.

Table 76. Default Standards on Lines for PAL and NTSC

PAL—625/50				NTSC—525/60			
Line No.	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**
6	WST	318	Reserved	23	Reserved	286	Reserved
7	WST	319	WST	24	Reserved	287	Reserved
8	WST	320	WST	25	Reserved	288	Reserved
9	WST	321	WST	10	NABTS	272	NABTS
10	WST	322	WST	11	NABTS	273	NABTS
11	WST	323	WST	12	NABTS	274	NABTS
12	WST	324	WST	13	NABTS	275	NABTS
13	WST	325	WST	14	Reserved	276	NABTS
14	WST	326	WST	15	NABTS	277	Reserved
15	WST	327	WST	16	Reserved	278	NABTS
16	Reserved	328	WST	17	NABTS	279	Reserved
17	Reserved	329	Reserved	18	NABTS	280	NABTS
18	Reserved	332	Reserved	19	NABTS	281	NABTS
19	Reserved	333	WST	20	CGMS	282	NABTS
20	WST	334	WST	21	CCAP	283	CGMS
21	WST	335	CCAP	22 + full odd field	NABTS	284	CCAP
22	CCAP	336	WST	Reserved	Reserved	285 + full even field	NABTS
23	WSS	337 + full even field	WST	Reserved	Reserved	Reserved	Reserved
24 + full odd field	WST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 77. VBI Data Standards for Manual Configuration

VBI_DATA_Px_Ny	PAL—625/50	NTSC—525/60
0000	Disable VDP	Disable VDP
0001	Teletext system identified by VDP_TTXT_TYPE	Teletext system identified by VDP_TTXT_TYPE
0010	Reserved	Reserved
0011	Reserved	Reserved
0100	WSS ITU-R BT.1119-1/ETSI.EN.300294	CGMS EIA-J CPR-1204/IEC 61880
0101	Reserved	Reserved
0110	Reserved	Reserved
0111	CCAP	CCAP EIA-608
1000 to 1111	Reserved	Reserved

Table 78.VBI Data Standards to be Decoded on Line Px (PAL) or Line Ny (NTSC)

Signal Name	Bit Location	Dec Address	Hex Address
VBI_DATA_P6_N23	VDP_LINE_00F[7:4]	101	0x65
VBI_DATA_P7_N24	VDP_LINE_010[7:4]	102	0x66
VBI_DATA_P8_N25	VDP_LINE_011[7:4]	103	0x67
VBI_DATA_P9	VDP_LINE_012[7:4]	104	0x68
VBI_DATA_P10	VDP_LINE_013[7:4]	105	0x69
VBI_DATA_P11	VDP_LINE_014[7:4]	106	0x6A
VBI_DATA_P12_N10	VDP_LINE_015[7:4]	107	0x6B
VBI_DATA_P13_N11	VDP_LINE_016[7:4]	108	0x6C
VBI_DATA_P14_N12	VDP_LINE_017[7:4]	109	0x6D
VBI_DATA_P15_N13	VDP_LINE_018[7:4]	110	0x6E
VBI_DATA_P16_N14	VDP_LINE_019[7:4]	111	0x6F
VBI_DATA_P17_N15	VDP_LINE_01A[7:4]	112	0x70
VBI_DATA_P18_N16	VDP_LINE_01B[7:4]	113	0x71
VBI_DATA_P19_N17	VDP_LINE_01C[7:4]	114	0x72
VBI_DATA_P20_N18	VDP_LINE_01D[7:4]	115	0x73
VBI_DATA_P21_N19	VDP_LINE_01E[7:4]	116	0x74
VBI_DATA_P22_N20	VDP_LINE_01F[7:4]	117	0x75
VBI_DATA_P23_N21	VDP_LINE_020[7:4]	118	0x76
VBI_DATA_P24_N22	VDP_LINE_021[7:4]	119	0x77
VBI_DATA_P318	VDP_LINE_00E[3:0]	100	0x64
VBI_DATA_P319_N286	VDP_LINE_00F[3:0]	101	0x65
VBI_DATA_P320_N287	VDP_LINE_010[3:0]	102	0x66
VBI_DATA_P321_N288	VDP_LINE_011[3:0]	103	0x67
VBI_DATA_P322	VDP_LINE_012[3:0]	104	0x68
VBI_DATA_P323	VDP_LINE_013[3:0]	105	0x69
VBI_DATA_P324_N272	VDP_LINE_014[3:0]	106	0x6A
VBI_DATA_P325_N273	VDP_LINE_015[3:0]	107	0x6B
VBI_DATA_P326_N274	VDP_LINE_016[3:0]	108	0x6C
VBI_DATA_P327_N275	VDP_LINE_017[3:0]	109	0x6D
VBI_DATA_P328_N276	VDP_LINE_018[3:0]	110	0x6E
VBI_DATA_P329_N277	VDP_LINE_019[3:0]	111	0x6F
VBI_DATA_P330_N278	VDP_LINE_01A[3:0]	112	0x70
VBI_DATA_P331_N279	VDP_LINE_01B[3:0]	113	0x71
VBI_DATA_P332_N280	VDP_LINE_01C[3:0]	114	0x72
VBI_DATA_P333_N281	VDP_LINE_01D[3:0]	115	0x73
VBI_DATA_P334_N282	VDP_LINE_01E[3:0]	116	0x74
VBI_DATA_P335_N283	VDP_LINE_01F[3:0]	117	0x75
VBI_DATA_P336_N284	VDP_LINE_020[3:0]	118	0x76
VBI_DATA_P337_N285	VDP_LINE_021[3:0]	119	0x77

Full field detection (lines other than VBI lines) of any standard can also be enabled by writing to the VBI_DATA_P24_N22[3:0] and VBI_DATA_P337_N285[3:0] bits. So, if VBI_DATA_P24_N22[3:0] is programmed with any teletext standard, teletext is decoded off for the entire odd field. The corresponding register for the even field is VBI_DATA_P337_N285[3:0].

For teletext system identification, VDP assumes that if teletext is present in a video channel, all the teletext lines comply with a single standard system. Therefore, the line programming using the VBI_DATA_Px_Ny and VBI_DATA_Px registers identifies whether the data in line is teletext; the actual standard is identified by the VDP_TTXT_TYPE_MAN bit.

To program the VDP_TTXT_TYPE_MAN bit, the VDP_TTXT_TYPE_MAN_ENABLE bit must be set to 1.

VDP_TTXT_TYPE_MAN_ENABLE, Enable Manual Selection of Teletext Type—Address 0x60, Bit 2, Interrupt/VDP Map

Setting VDP_TTXT_TYPE_MAN_ENABLE to 0 (default), disables manual programming of the teletext type.

Setting VDP_TTXT_TYPE_MAN_ENABLE to 1 enables manual programming of the teletext type.

VDP_TTXT_TYPE_MAN[1:0], Specify the Teletext Type—Address 0x60, Bits[1:0], Interrupt/VDP Map

These bits specify the teletext type to be decoded. These bits are functional only if VDP_TTXT_TYPE_MAN_ENABLE is set to 1.

Table 79. VDP_TTXT_TYPE_MAN Function

VDP_TTXT_TYPE_MAN[1:0]	625/50 (PAL)	525/60 (NTSC)
00 (default)	Teletext-ITU-BT.653-625/50-A	Reserved
01	Teletext-ITU-BT.653-625/50-B (WST)	Teletext-ITU-BT.653-525/60-B
10	Teletext-ITU-BT.653-625/50-C	Teletext-ITU-BT.653-525/60-C or EIA516 (NABTS)
11	Teletext-ITU-BT.653-625/50-D	Teletext-ITU-BT.653-525/60-D

VDP Ancillary Data Output

Reading the data back via I²C may not be feasible for VBI data standards with high data rates (for example, teletext). An alternative is to place the sliced data in a packet in the line blanking of the digital output CCIR656 stream. This is available for all standards sliced by the VDP module.

When data is sliced on a given line, the corresponding ancillary data packet is placed immediately after the next EAV code that occurs at the output (that is, data sliced from multiple lines are not buffered up and then emitted in a burst). Note that, due to the vertical delay through the comb filters, the line number on which the packet is placed differs from the line number on which the data is sliced.

The user can enable or disable the insertion of VDP results that are decoded into the 656 ancillary streams by using the ADF_ENABLE bit.

ADF_ENABLE, Enable Ancillary Data Output Through 656 Stream—Address 0x62, Bit 7, User Sub Map 2

Setting ADF_ENABLE to 0 (default) disables the insertion of VBI decoded data into the ancillary 656 stream.

Setting ADF_ENABLE to 1 enables the insertion of VBI decoded data into the ancillary 656 stream.

The user can select the data identification word (DID) and the secondary data identification word (SDID) through programming the ADF_DID[4:0] and ADF_SDID[5:0] bits, respectively.

ADF_DID[4:0], User-Specified Data ID Word in Ancillary Data—Address 0x62, Bits[4:0], Interrupt/VDP Map

These bits select the data ID word to be inserted into the ancillary data stream with the data decoded by the VDP.

The default value of ADF_DID[4:0] is 10101.

ADF_SDID[5:0], User-Specified Secondary Data ID Word in Ancillary Data—Address 0x63, Bits[5:0], Interrupt/VDP Map

These bits select the secondary data ID word to be inserted in the ancillary data stream with the data decoded by the VDP.

The default value of ADF_SDID[5:0] is 101010.

DUPLICATE_ADF, Enable Duplication/Spreading of Ancillary Data over Y and C Buses—Address 0x63, Bit 7, Interrupt/VDP Map

This bit determines whether the ancillary data is duplicated over both Y and C buses, or if the data packets are spread between the two channels.

When DUPLICATE_ADF to 0 (default) is set, the ancillary data packet is spread across the Y and C data streams.

When DUPLICATE_ADF to 1 is set, the ancillary data packet is duplicated on the Y and C data streams.

ADF_MODE[1:0], Determine the Ancillary Data Output Mode—Address 0x62, Bits[6:5], Interrupt/VDP Map

These bits determine whether the ancillary data output mode is in byte mode or nibble mode.

Table 80. ADF_MODE

ADF_MODE[1:0]	Description
00 (default)	Nibble mode
01	Byte mode, no code restrictions
10	Byte mode, but 0x00 and 0xFF prevented (0x00 replaced by 0x01, 0xFF replaced by 0xFE)
11	Reserved

The ancillary data packet sequence is explained in Table 81 and Table 82. The nibble output mode is the default mode of output from the ancillary stream when ancillary stream output is enabled. This format is in compliance with ITU-R BT.1364. The following abbreviations are used in Table 81 and Table 82:

- EP—even parity for Bit B8 to Bit B2. The EP of the parity bit is set so that an even number of 1s are in Bit B8 to Bit B2, including the parity bit, B8.
- CS—checksum word. The CS word is used to increase confidence of the integrity of the ancillary data packet from the DID, SDID, and dc through user data-words (UDWs). The CS word consists of 10 bits that include a 9-bit calculated value and B9 as the inverse of B8. The checksum value B8 to B0 is equal to the nine LSBs of the sum of the nine LSBs of the DID, SDID, and dc, and all UDWs in the packet. Prior to the start of the checksum count cycle, all checksum and carry bits are preset to 0. Any carry resulting from the checksum count cycle is ignored.
- $\overline{EP}$—the MSB, B9, is the inverse of EP, which ensures that restricted Code 0x00 and Code 0xFF do not occur.
- LINE_NUMBER[9:0]—the line number of the line that immediately precedes the ancillary data packet. The line number is from the numbering system in ITU-R BT.470. The line number runs from 1 to 625 in a 625-line system and from 1 to 263 in a 525-line system. Note that, due to the vertical delay through the comb filters, the line number on which the packet is output differs from the line number on which the VBI data was sliced.
- Data count—the data count specifies the number of UDWs in the ancillary stream for the standard. The total number of user data-words is four times the data count. Padding words can be introduced to make the total number of UDWs divisible by 4.

Table 81. Ancillary Data in Nibble Output Format

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{EP}$	EP	0	I²C_DID6_2[4:0]					0	0	DID (data identification word)
4	$\overline{EP}$	EP	I²C_SDID7_2[5:0]						0	0	SDID (secondary data identification word)
5	$\overline{EP}$	EP	0	DC[4:0]					0	0	Data count
6	$\overline{EP}$	EP	Padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 (User Data-Word 1)
7	$\overline{EP}$	EP	0	LINE_NUMBER[9:5]					0	0	ID1 (User Data-Word 2)
8	$\overline{EP}$	EP	EVEN_FIELD	LINE_NUMBER[4:0]					0	0	ID2 (User Data-Word 3)
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 (User Data-Word 4)
10	$\overline{EP}$	EP	0	0	VBI_WORD_1[7:4]				0	0	ID4 (User Data-Word 5)
11	$\overline{EP}$	EP	0	0	VBI_WORD_1[3:0]				0	0	ID5 (User Data-Word 6)
12	$\overline{EP}$	EP	0	0	VBI_WORD_2[7:4]				0	0	ID6 (User Data-Word 7)
13	$\overline{EP}$	EP	0	0	VBI_WORD_2[3:0]				0	0	ID7 (User Data-Word 8)
14	$\overline{EP}$	EP	0	0	VBI_WORD_3[7:4]				0	0	ID8 (User Data-Word 9)
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word
n – 3	1	0	0	0	0	0	0	0	0	0	
n – 2	1	0	0	0	0	0	0	0	0	0	
n – 1	$\overline{B8}$	Checksum (CS)							0	0	CS (checksum word)

Table 82. Ancillary Data in Byte Output Format[1]

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{EP}$	EP	0	I^2C_DID6_2[4:0]					0	0	DID
4	$\overline{EP}$	EP	I^2C_SDID7_2[5:0]						0	0	SDID
5	$\overline{EP}$	EP	0	DC[4:0]					0	0	Data count
6	$\overline{EP}$	EP	Padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 (User Data-Word 1)
7	$\overline{EP}$	EP	0	LINE_NUMBER[9:5]					0	0	ID1 (User Data-Word 2)
8	$\overline{EP}$	EP	EVEN_FIELD	LINE_NUMBER[4:0]					0	0	ID2 (User Data-Word 3)
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 (User Data-Word 4)
10	VBI_WORD_1[7:0]								0	0	ID4 (User Data-Word 5)
11	VBI_WORD_2[7:0]								0	0	ID5 (User Data-Word 6)
12	VBI_WORD_3[7:0]								0	0	ID6 (User Data-Word 7)
13	VBI_WORD_4[7:0]								0	0	ID7 (User Data-Word 8)
14	VBI_WORD_5[7:0]								0	0	ID8 (User Data-Word 9)
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word
n – 3	1	0	0	0	0	0	0	0	0	0	
n – 2	1	0	0	0	0	0	0	0	0	0	
n – 1	$\overline{B8}$	Checksum							0	0	CS (checksum word)

[1] This mode does not fully comply with ITU-R BT.1364.

Structure of VBI Words in the Ancillary Data Stream

Each VBI data standard is split into a clock run in (CRI), a framing code (FC), and a number of data bytes (n). The data packet in the ancillary stream includes only the FC and data bytes. Table 83 shows the format of VBI_WORD_x in the ancillary data stream.

Table 83. Structure of VBI Data-Words in the Ancillary Stream

Ancillary Data Byte No.	Byte Type	Description
VBI_WORD_1	FC0	Framing Code[23:16]
VBI_WORD_2	FC1	Framing Code[15:8]
VBI_WORD_3	FC2	Framing Code[7:0]
VBI_WORD_4	DB1	First data byte
…	…	…
VBI_WORD_N + 3	DBn	Last (n^{th}) data byte

VDP Framing Code

The length of the actual framing code depends on the VBI data standard. For uniformity, the length of the framing code reported in the ancillary data stream is always 24 bits. For standards with a smaller framing code length, the extra LSB bits are set to 0. The valid length of the framing code can be decoded from the VBI_DATA_STD bits available in ID0 (UDW 1). The framing code is always reported in the inverse transmission order.

Table 84 shows the framing code and its valid length for VBI data standards supported by VDP.

Example

For teletext (B-WST), the framing code byte is 11100100 (0xE4), with bits shown in the order of transmission. VBI_WORD_1 = 0x27, VBI_WORD_2 = 0x00, and VBI_WORD_3 = 0x00 translated into UDWs in the ancillary data stream for nibble mode are as follows:

- UDW5[5:2] = 0010
- UDW6[5:2] = 0111
- UDW7[5:2] = 0000 (undefined bits set to 0)
- UDW8[5:2] = 0000 (undefined bits set to 0)
- UDW9[5:2] = 0000 (undefined bits set to 0)
- UDW10[5:2] = 0000 (undefined bits set to 0)

For byte mode,

- UDW5[9:2] = 0010_0111
- UDW6[9:2] = 0000_0000 (undefined bits set to 0)
- UDW7[9:2] = 0000_0000 (undefined bits set to 0)

Data Bytes

VBI_WORD_4 to VBI_WORD_N + 3 contain the data-words decoded by the VDP in the transmission order. The position of bits in bytes is in the inverse transmission order.

For example, closed captioning has two user data bytes, as shown in Table 89.

The data bytes in the ancillary data stream are as follows:

- VBI_WORD_4 = Byte 1[7:0]
- VBI_WORD_5 = Byte 2[7:0]

The number of VBI_WORDS for each VBI data standard and the total number of UDWs in the ancillary data stream is shown in Table 85.

Table 84. Framing Code Sequence for Different VBI Standards

VBI Standard	Length in Bits	Error Free Framing Code Bits (in Order of Transmission)	Error Free Framing Code Reported by VDP (in Reverse Order of Transmission)
TTXT_SYSTEM_A (PAL)	8	11100111	11100111
TTXT_SYSTEM_B (PAL)	8	11100100	00100111
TTXT_SYSTEM_B (NTSC)	8	11100100	00100111
TTXT_SYSTEM_C (PAL and NTSC)	8	11100111	11100111
TTXT_SYSTEM_D (PAL and NTSC)	8	11100101	10100111
WSS (PAL)	24	000111100011110000011111	111110000011110001111000
CCAP (NTSC and PAL)	3	001	100
CGMS (NTSC)	1	0	0

Table 85. Total User Data-Words for Different VBI Standards[1]

VBI Standard	ADF Mode	Framing Code UDWs	VBI Data-Words	No. of Padding Words	Total UDWs
TTXT_SYSTEM_A (PAL)	00 (nibble mode)	6	74	0	84
	01, 10 (byte mode)	3	37	0	44
TTXT_SYSTEM_B (PAL)	00 (nibble mode)	6	84	2	96
	01, 10 (byte mode)	3	42	3	52
TTXT_SYSTEM_B (NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
TTXT_SYSTEM_C (PAL and NTSC)	00 (nibble mode)	6	66	0	76
	01, 10 (byte mode)	3	33	2	42
TTXT_SYSTEM_D (PAL and NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
WSS (PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
CCAP (NTSC and PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
CGMS (NTSC)	00 (nibble mode)	6	6	0	16
	01, 10 (byte mode)	3	3 + 3	2	12

[1] The first four UDWs are always the ID.

I²C Interface

Dedicated I²C readback registers are available for CCAP, CGMS, and WSS. Because teletext is a high data rate standard, data extraction is supported only through the ancillary data packet.

User Interface for I²C Readback Registers

The VDP decodes all enabled VBI data standards in real-time. Because the I²C access speed is much lower than the decoded rate, when the registers are accessed, they may be updated with data from the next line. To avoid this updating, VDP has a self clearing clear bit and an available (AVL) status bit accompanying all I²C readback registers.

The user must clear the I²C readback register by writing a high to the clear bit. This resets the state of the available bit to low and indicates that the data in the associated readback registers is not valid. After the VDP decodes the next line of the corresponding VBI data, the decoded data is placed into the I²C readback register, and the available bit is set to high to indicate that valid data is now available.

Though the VDP decodes this VBI data in subsequent lines, if present, the decoded data is not updated to the readback registers until the clear bit is set high again. However, this data is available through the 656 ancillary data packets.

The clear and available bits are in the VDP_STATUS_CLEAR register (Register 0x78, interrupt/VDP map, write only) and the VDP_STATUS register (Register 0x78, interrupt/VDP map, read only), respectively.

VDP—Content-Based Data Update

For certain standards, such as WSS and CGMS, the information content in the signal transmitted remains the same over numerous lines, and the user may want to be notified only when there is a change in the information content or loss of the information content. The user must enable content-based updating for the required standard through the WSS_CGMS_CB_CHANGE bit. This bit shows the availability of WSS and CGMS information only when its content has changed.

Content-based updating also applies to lines with lost data. Therefore, for standards such as CGMS and WSS, if no data arrives in the next four lines programmed, the corresponding available bit in the VDP_STATUS register is set high, and the content in the I²C registers for that standard is set to 0. The user must write high to the corresponding clear bit so that when a valid line is decoded after some time, the decoded results are available in the I²C registers, with the available status bit set high.

If content-based updating is enabled, the available bit is set high (assuming the clear bit was written) in the following cases:

- The data contents changed.
- Data is being decoded and four lines with no data are detected.
- No data is being decoded, and new data is now being decoded.

WSS_CGMS_CB_CHANGE, Enable Content-Based Updating for WSS/CGMS—Address 0x9C, Bit 4, Interrupt/VDP Map

Setting WSS_CGMS_CB_CHANGE to 0 disables content-based updating.

Setting WSS_CGMS_CB_CHANGE to 1 (default) enables content-based updating.

VDP—Interrupt-Based Reading of VDP I²C Registers

Some VDP status bits are also linked to the interrupt request controller so that the user does not have to poll the available status bit. The user can configure the video decoder to trigger an interrupt request on the $\overline{\text{INTRQ}}$ pin in response to the valid data available in the I²C registers. This function is available for the CGMS or WSS data types. The user can either trigger an interrupt request each time sliced data is available, or trigger an interrupt request only when the sliced data changes. This selection is made via the WSS_CGMS_CB_ CHANGE bit.

The sequence for the interrupt-based reading of the VDP I²C data registers is as follows for the CCAP standard:

1. The user unmasks the CCAP interrupt mask bit (Register 0x50, Bit 0, interrupt/VDP map = 1). CCAP data occurs on the incoming video. VDP slices CCAP data and places it into the VDP readback registers.
2. The VDP CCAP available bit, VDP_CCAPD_Q, goes high, and the VDP module signals to the interrupt controller to stimulate an interrupt request (for CCAP in this case).
3. The user reads the interrupt status bits (interrupt/VDP map) and sees that new CCAP data is available (Register 0x4E, Bit 0, interrupt/VDP map = 1).
4. The user writes 1 to the CCAP interrupt clear bit (Register 0x4F, Bit 0, interrupt/VDP map = 1) in the interrupt I²C space (this is a self clearing bit). This write clears the interrupt on the $\overline{\text{INTRQ}}$ pin but does not have an effect in the VDP I²C area.
5. The user reads the CCAP data from the VDP I²C area.
6. The user writes to Bit CC_CLEAR in the VDP_STATUS_ CLEAR register, (Register 0x78, Bit 0, User Sub Map 2 = 1) to signify that the CCAP data has been read (and, therefore, the VDP CCAP can be updated at the next occurrence of CCAP).
7. The user goes back to Step 2.

Interrupt Mask Register Details

The following bits set the interrupt mask on the signal from the VDP VBI data slicer.

VDP_CCAPD_MSK—Address 0x50, Bit 0, Interrupt/ VDP Map

Setting VDP_CCAPD_MSK to 0 (default) masks (disables) the interrupt on the VDP_CCAPD_Q signal.

Setting VDP_CCAPD_MSK to 1 unmasks (enables) the interrupt on the VDP_CCAPD_Q signal.

VDP_CGMS_WSS_CHNGD_MSK—Address 0x50, Bit 2, Interrupt/VDP Map

Setting VDP_CGMS_WSS_CHNGD_MSK to 0 (default) masks (disables) the interrupt on the VDP_CGMS_WSS_ CHNGD_Q signal.

Setting VDP_CGMS_WSS_CHNGD_MSK to 1 unmasks (enables) the interrupt on the VDP_CGMS_WSS_CHNGD_Q signal.

Interrupt Status Register Details

The following read only bits contain data detection information from the VDP module since the status bit was last cleared or unmasked.

VDP_CCAPD_Q—Address 0x4E, Bit 0, Interrupt/VDP Map

When VDP_CCAPD_Q is 0 (default), CCAP data is not detected. When VDP_CCAPD_Q is 1, CCAP data is detected.

VDP_CGMS_WSS_CHNGD_Q—Address 0x4E, Bit 2, Interrupt/VDP Map

When VDP_CGMS_WSS_CHNGD_Q is 0 (default), CGMS or WSS data is not detected.

VDP_CGMS_WSS_CHNGD_Q is also 0 if the CGMS or WSS data state has not changed since it was last cleared (see the Interrupt Status Clear Register Details section).

When VDP_CGMS_WSS_CHNGD_Q is 1, CGM or WSS data is detected.

Interrupt Status Clear Register Details

It is not necessary to write 0 to these write only bits because they automatically reset after being set to 1 (self clearing).

VDP_CCAPD_CLR—Address 0x4F, Bit 0, Interrupt/VDP Map

Setting VDP_CCAPD_CLR to 1 clears the VDP_CCAP_Q bit.

VDP_CGMS_WSS_CHNGD_CLR, Address 0x4F[2], Interrupt/VDP Map

Setting VDP_CGMS_WSS_CHNGD_CLR to 1 clears the VDP_CGMS_WSS_CHNGD_Q bit.

I²C READBACK REGISTERS

Teletext

Because teletext is a high data rate standard, the decoded bytes are available only as ancillary data. However, a TTXT_AVL bit is provided in I²C so that the user can check whether the VDP has detected teletext. Note that the TTXT_AVL bit is a plain status bit and does not use the protocol discussed in the I2C Interface section. When teletext is detected, the TTXT_AVL bit goes high and remains high until cleared by the TTXT_CLEAR bit.

TTXT_AVL, Teletext Detected Status—Address 0x78, Bit 7, Interrupt/VDP Map, Read Only

When TTXT_AVL is 0, teletext is not detected.

When TTXT_AVL is 1, teletext is detected.

TTXT_CLEAR, Teletext Clear—Address 0x78, Bit 7, Interrupt/VDP Map, Write Only

Setting TTXT_CLEAR to 1 clears the TTXT_AVL bit.

WST Packet Decoding

For WST only, the VDP decodes the magazine and row address of teletext packets and further decodes the 8 × 4 hamming coded words of the packet. This feature can be disabled using the WST_PKT_DECODE_DISABLE bit (Bit 3, Register 0x60, user sub map). This feature is valid for WST only.

WST_PKT_DECODE_DISABLE, Disable Hamming Decoding of Bytes in WST—Address 0x60, Bit 3, Interrupt/VDP Map

Setting WST_PKT_DECODE_DISABLE to 0 enables hamming decoding of WST packets.

Setting WST_PKT_DECODE_DISABLE to 1 (default) disables hamming decoding of WST packets.

For hamming coded bytes, the dehammed nibbles are output along with some error information from the hamming decoder as follows:

- Input hamming coded byte: {D3, P3, D2, P2, D1, P1, D0, P0} (bits in decoded order)
- Output dehammed byte: {E1, E0, 0, 0, D3', D2', D1', D0'} (Di' – corrected bits, Ei error information).

Table 86. Error Bits in the Dehammed Output Byte

E[1:0]	Error Information
00	No errors detected
01	Error in P4
10	Double error[1]
11	Single error found and corrected

[1] The hamming decoder cannot correct for two decoding errors.

Table 87 describes the WST packets that are decoded.

Table 87. WST Packet Description

Packet	Byte	Description
Header Packet (X/00)	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Page number—Dehammed Byte 6
	4th	Page number—Dehammed Byte 7
	5th to 10th	Control bytes—Dehammed Byte 8 to Byte 13
	11th to 42nd	Raw data bytes
Text Packets (X/01 to X/25)	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd to 42nd	Raw data bytes
8/30 (Format 1) Packet Design Code = 0000 or 0001 UTC	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Design code—Dehammed Byte 6
	4th to 10th	Dehammed initial teletext page, Byte 7 to Byte 12
	11th to 23rd	UTC bytes—Dehammed Byte 13 to Byte 25
	24th to 42nd	Raw status bytes
8/30 (Format 2) Packet Design Code = 0010 or 0011 Program Delivery Control (PDC)	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Design code—Dehammed Byte 6
	4th to 10th	Dehammed initial teletext page, Byte 7 to Byte 12
	11th to 23rd	PDC bytes—Dehammed Byte 13 to Byte 25
	24th to 42nd	Raw status bytes
X/26, X/27, X/28, X/29, X/30, X/31[1]	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Design code—Dehammed Byte 6
	4th to 42nd	Raw data bytes

[1] For X/26, X/28, and X/29, further decoding requires 24 × 18 hamming decoding (this is not currently supported).

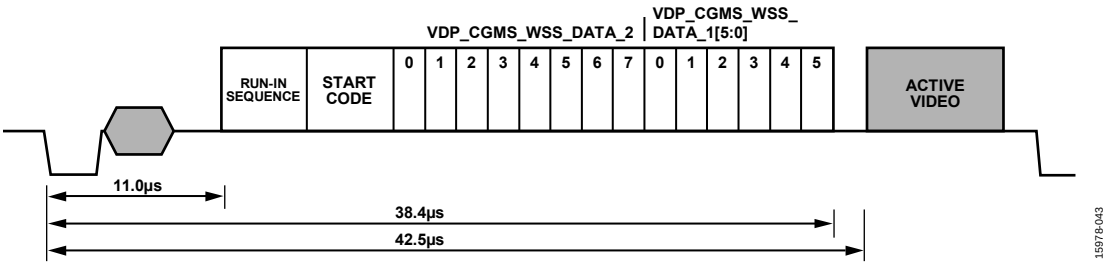

Figure 42. WSS Waveform

CGMS and WSS

The CGMS and WSS data packets convey the same type of information for different video standards. WSS is for PAL and CGMS is for NTSC; therefore, the CGMS and WSS readback registers are shared. WSS is biphase coded; the VDP performs a biphase decoding to produce the 14 raw WSS bits in the CGMS/WSS readback I²C registers and to set the CGMS_WSS_AVL bit.

CGMS_WSS_CLEAR, CGMS/WSS Clear—Address 0x78, Bit 2, Interrupt/VDP Map, Write Only, Self Clearing

Setting CGMS_WSS_CLEAR to 0 does not reinitialize the CGMS/WSS readback registers. Setting CGMS_WSS_CLEAR to 1 reinitializes the CGMS/WSS readback registers.

CGMS_WSS_AVL, CGMS/WSS Available—Address 0x78, Bit 2, User Sub Map, Read Only

When CGMS_WSS_AVL is 0, CGMS/WSS is not detected. When CGMS_WSS_AVL is 1, CGMS/WSS is detected.

VDP_CGMS_WSS_DATA_0[3:0]—Address 0x7D, Bits[3:0]; VDP_CGMS_WSS_DATA_1[7:0]—Address 0x7E, Bits[7:0]; VDP_CGMS_WSS_DATA_2, Bits[7:0], Address 0x7F, Bits[7:0]; Interrupt/VDP Map, Read Only

These bits hold the decoded CGMS or WSS data. See Figure 42 and Figure 43 for the I²C to WSS and I²C to CGMS bit mapping, respectively.

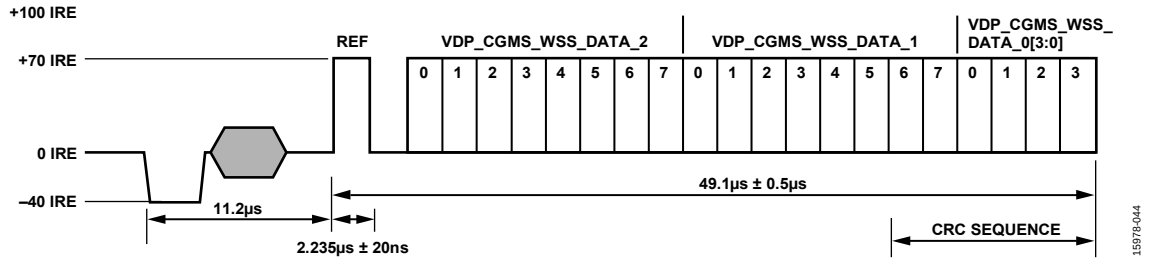

Figure 43. CGMS Waveform

Table 88. CGMS Readback Registers[1]

Signal Name	Register Location	Dec	Hex
CGMS_WSS_DATA_0[3:0]	VDP_CGMS_WSS_DATA_0[3:0]	125	0x7D
CGMS_WSS_DATA_1[7:0]	VDP_CGMS_WSS_DATA_1[7:0]	126	0x7E
CGMS_WSS_DATA_2[7:0]	VDP_CGMS_WSS_DATA_2[7:0]	127	0x7F

[1] These registers are readback registers; the default value does not apply.

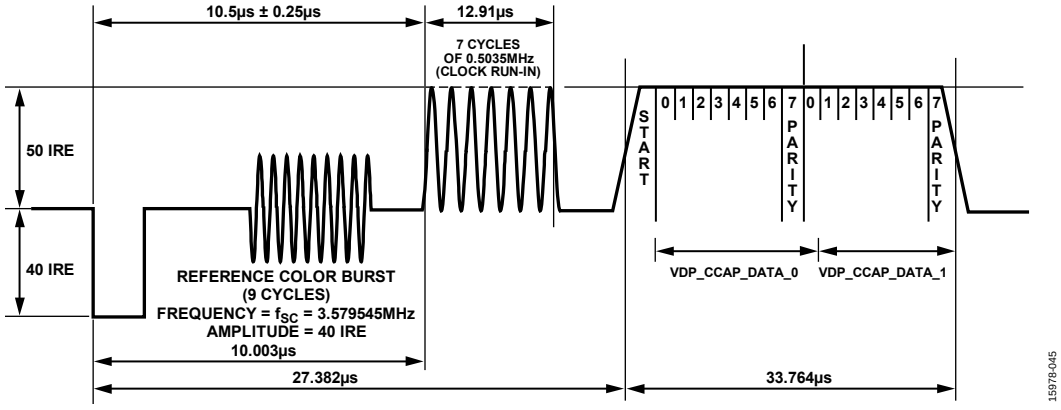

Figure 44. CCAP Waveform and Decoded Data Correlation

Table 89. CCAP Readback Registers[1]

Signal Name	Register Location	Dec	Hex
CCAP_BYTE_1[7:0]	VDP_CCAP_DATA_0[7:0]	121	0x79
CCAP_BYTE_2[7:0]	VDP_CCAP_DATA_1[7:0]	122	0x7A

[1] These registers are readback registers; the default value does not apply.

CCAP

Two bytes of decoded closed caption data are available in the I²C registers. The field information of the decoded CCAP data can be obtained from the CC_EVEN_FIELD bit (Register 0x78).

CC_CLEAR, Closed Caption Clear—Address 0x78, Bit 0, Interrupt/VDP Map, Write Only, Self Clearing

Setting CC_CLEAR to 0 does not reinitializes the CCAP readback registers.

Setting CC_CLEAR to 1 reinitializes the CCAP readback registers.

CC_AVL, Closed Caption Available—Address 0x78, Bit 0, Interrupt/VDP Map, Read Only

When CC_AVL is 0, closed captioning is not detected.

When CC_AVL is 1, closed captioning is detected.

CC_EVEN_FIELD—Address 0x78, Bit 1, Interrupt/VDP Map, Read Only

Identifies the field from which the CCAP data was decoded.

When CC_EVEN_FIELD is 0, closed captioning is detected from an odd field.

When CC_EVEN_FIELD is 1, closed captioning is detected from an even field.

VDP_CCAP_DATA_0—Address 0x79, Bits[7:0], Interrupt/VDP Map, Read Only

Decoded Byte 1 of CCAP data.

VDP_CCAP_DATA_1—Address 0x7A, Bits[7:0], Interrupt/VDP Map, Read Only

Decoded Byte 2 of CCAP data.

Letterbox Detection

Incoming video signals can conform to different aspect ratios (16:9 wide screen or 4:3 standard). For certain transmissions in the widescreen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from the digitally decoded bits that WSS contains.

In the absence of a WSS sequence, letterbox detection can be used to find widescreen signals. The detection algorithm examines the active video content of lines at the start and end of a field. If black lines are detected, this may indicate that the currently shown picture is in widescreen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold, and a decision is made as to whether or not a particular line is black. The required threshold value depends on the type of input signal; some control is provided via LB_TH[4:0].

Detection at the Start of a Field

The ADV7182A expects a section of at least six consecutive black lines of video at the top of a field. After these lines are detected, LB_LCT[7:0] reports the number of black lines that were actually found. By default, the ADV7182A starts looking for these black lines in synchronization with the beginning of active video; for example, immediately after the last VBI video line. LB_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line by line basis. The detection window closes in the middle of the field.

Detection at the End of a Field

The ADV7182A expects at least six continuous lines of black video at the bottom of a field before reporting the number of lines actually found via the LB_LCB[7:0] value. The activity window for letterbox detection (end of field) starts in the middle of an active field. Its end is programmable via LB_EL[3:0].

Detection at the Midrange

Some transmissions of widescreen video include subtitles within the lower black box. If the ADV7182A finds at least two black lines followed by some more nonblack video, for example, the subtitle followed by the remainder of the bottom black block, it reports a midcount via LB_LCM[7:0]. If no subtitles are found, LB_LCM[7:0] reports the same number as LB_LCB[7:0].

There is a two-field delay in reporting any line count parameter.

There is no letterbox detected bit. Read the LB_LCT[7:0] and LB_LCB[7:0] register values to determine whether the letterbox-type video is present in the software.

LB_LCT[7:0], Letterbox Line Count Top—Address 0x9B, Bits[7:0]; LB_LCM[7:0], Letterbox Line Count Mid—Address 0x9C, Bits[7:0]; LB_LCB[7:0], Letterbox Line Count Bottom—Address 0x9D, Bits[7:0]

Table 90. LB_LCx Access Information

Signal Name	Address
LB_LCT[7:0]	0x9B
LB_LCM[7:0]	0x9C
LB_LCB[7:0]	0x9D

LB_TH[4:0], Letterbox Threshold Control—Address 0xDC, Bits[4:0]

Table 91. LB_TH Function

LB_TH[4:0]	Description
01100 (default)	Default threshold for detection of black lines
01101 to 10000	Increase threshold (need larger active video content before identifying nonblack lines)
00000 to 01011	Decrease threshold (even small noise levels can cause the detection of nonblack lines)

LB_SL[3:0], Letterbox Start Line—Address 0xDD, Bits[7:4]

The LB_SL[3:0] bits are set at 1100 by default. For an NTSC signal, this window is from Line 31 to Line 294.

By changing the bits to 0100, the detection window starts on Line 23 and ends on Line 286.

LB_EL[3:0], Letterbox End Line—Address 0xDD, Bits[3:0]

The LB_EL[3:0] bits are set at 1100 by default. This means that the letterbox window ends with the last active video line. For an NTSC signal, this window is from Line 261 to Line 524.

By changing the bits to 1101, the detection window starts on Line 262 and ends on Line 255.

ITU-R BT.656 Tx CONFIGURATION

The ADV7182A receives analog video and outputs digital video according to the ITU-R BT.656 specification. The ADV7182A outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins and has a line locked clock (LLC) pin and two synchronization pins (HS and VS/FIELD/SFL).

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output is used to clock the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

The two synchronization pins (HS and VS/FIELD/SFL) output a variety of synchronization signals such as horizontal sync, vertical sync, field sync, and color subcarrier frequency lock (SFL) sync. The majority of these synchronization signals are already embedded in the video data. Therefore, the use of the synchronization pins is optional.

The following registers can be used to configure the ITU-R BT.656 output from the ADV7182A. See the Global Control Registers section for further registers that can be used to configure the output from the ADV7182A.

SWPC, Swap Pixel Cr/Cb—Address 0x27, Bit 7

This bit allows Cr and Cb samples to be swapped.

When SWPC is 0 (default), no swapping is allowed. When SWPC is 1, the Cr and Cb values can be swapped.

Polarity LLC Pin

PCLK—Address 0x37, Bit 0

The polarity of the clock that leaves the ADV7182A via the LLC pin can be inverted using the PCLK bit. Changing the polarity of the LLC clock output may be necessary to meet the setup and hold time expectations of follow-on chips. When PCLK is 0, the LLC output polarity is inverted. When PCLK is 1 (default), the LLC output polarity is normal (see the Timing Specifications section.)

LLC_PAD_SEL[2:0] LLC Output Selection—Address 0x8F, Bits[6:4]

The following I^2C write allows the user to select between LLC (nominally at 27 MHz) and LLC (nominally at 13.5 MHz).

When LLC_PAD_SEL is 000, the output is nominally 27 MHz LLC on the LLC pin (default).

When LLC_PAD_SEL is 101, the output is nominally 13.5 MHz LLC on the LLC pin.

BT.565-4, ITU-R BT.565-3/ITU-R BT.565-4 Enable—Address 0x04, Bit 7

Between Revision 3 and Revision 4 of the ITU-R BT.656 standards, the toggling position for the V bit within the SAV EAV codes for NTSC has changed. Note that the standard change affects only NTSC and has no bearing on PAL. For further information, visit the International Telecommunication Union website.

The BT.656-4 bit allows the user to select an output mode that is compliant with either the ITU-R BT.656-3 standard or ITU-R BT.656-4 standard.

When the BT.656-4 bit is set to 0 (default), the ITU-R BT.656-3 specification is used. The V bit goes low at EAV of Line 10 and Line 273.

When ITU-R BT.656-4 is 1, the ITU-R BT.656-4 specification is used. The V bit goes low at EAV of Line 20 and Line 283.

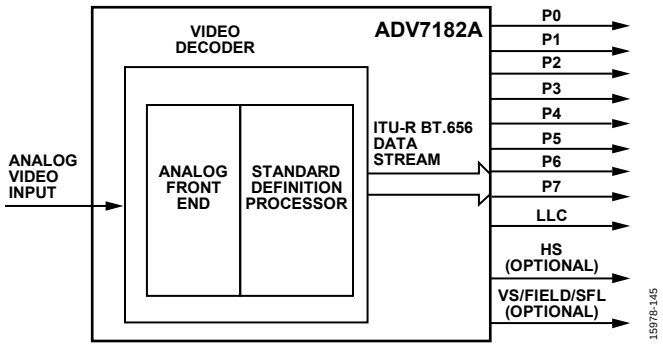

Figure 45. ITU-R BT.656 Output Stage of the ADV7182A

I²C INTERFACE

The ADV7182A supports a 2-wire (I²C-compatible) serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7182A and the system I²C master controller. Each slave device is recognized by a unique address. The ADV7182A I²C port allows the user to set up and configure the decoder and to read back the captured VBI data. The ADV7182A has four possible slave addresses for both read and write operations, depending on the logic level of the ALSB pin. The four unique addresses are shown in Table 92. The ADV7182A ALSB pin controls Bit 1 of the slave address. By altering the ALSB, it is possible to control two ADV7182As in an application without the conflict of using the same slave address. The LSB (Bit 0) sets either a read or write operation. Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

Table 92. I²C Address for ADV7182A

		Slave Address	
ALSB	**R/$\overline{W}$**	**Hexadecimal**	**Binary**
0	0 (read)	0x40	0b'0100 0000
0	1 (write)	0x41	0b'0100 0001
1	0 (read)	0x42	0b'01000010
1	1 (write)	0x43	0b'0100 0011

To control the device on the bus, a specific protocol must be followed. First, the master initiates a data transfer by establishing a start condition, which is defined by a high to low transition on SDATA while SCLK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7182A acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has subaddresses to enable access to the internal registers. It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one by one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued, the ADV7182A does not issue an acknowledge and returns to the idle condition.

In auto-increment mode, if the user exceeds the highest subaddress, the following action is taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the ADV7182A, and the device returns to the idle condition.

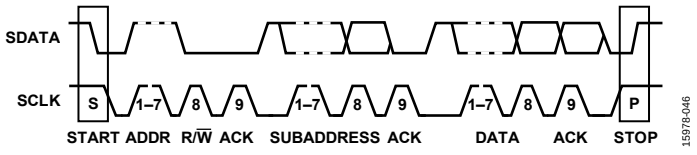

Figure 46. Bus Data Transfer

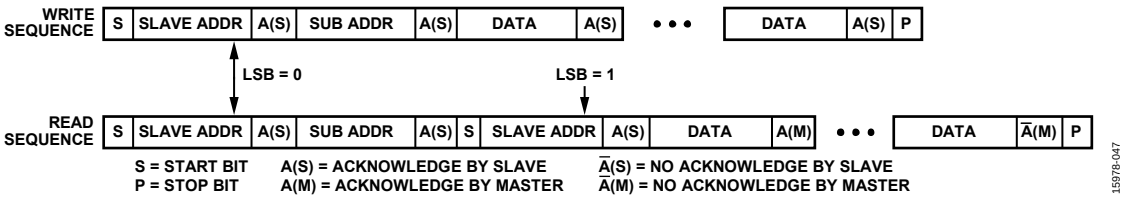

Figure 47. Read and Write Sequence

REGISTER ACCESS

The MPU can write to or read from all of the ADV7182A registers except the subaddress register, which is write only. The subaddress register determines which register the next read or write operation accesses. All communications with the device through the bus start with an access to the subaddress register. A read/write operation is then performed from or to the target address, which increments to the next address until a stop command on the bus is performed. Note that only the registers listed in the I2C Register Maps section are supported.

REGISTER PROGRAMMING

The following sections describe the configuration for each register. The communication register is an 8-bit, write only register. After the device is accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place.

SUB_USR_EN—Address 0x0E, Bits[6:5]

The ADV7182A has three I²C maps. The main register map (see Table 93) is the map that is available by default. The other two maps are accessed using the SUB_USR_EN bit (Address 0x0E). When programming of these maps is completed, it is necessary to write to the SUB_USR_EN bit to return to the main register map (see Table 93).

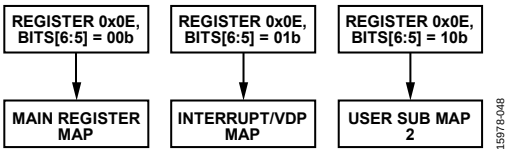

Figure 48. Register Access—Main Register Map, Interrupt/VDP Map, and User Sub Map 2

Register Select (SR7 to SR0)

These bits are set up to point to the required starting address.

I²C SEQUENCER

An I²C sequencer is used when a parameter exceeds eight bits and is, therefore, distributed over two or more I²C registers, for example, HSB[10:0].

When such a parameter is changed using two or more I²C write operations, the parameter can hold an invalid value for the time between the first I²C being completed and the last I²C being completed. In other words, the top bits of the parameter may hold the new value while the remaining bits of the parameter still hold the previous value.

To avoid this problem, the I²C sequencer holds the updated bits of the parameter in local memory, and all bits of the parameter are updated together once the last register write operation has completed.

The correct operation of the I²C sequencer relies on the following conditions:

- All I²C registers for the parameter in question must be written to in order of ascending addresses. For example, for HSB[10:0], write to Address 0x34 first, followed by 0x35, and so on.
- No other I²C can take place between the two (or more) I²C writes for the sequence. For example, for HSB[10:0], write to Address 0x34 first, immediately followed by 0x35, and so on.

I²C REGISTER MAPS

To access all the registers listed in Table 93, SUB_USR_EN in Register Address 0x0E must be programmed to 00b. All read only registers are left blank.

Table 93. Main Register Map Details

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
0	00	Input control	RW				INSEL[4]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]	00001110	0E
1	01	Video Selection 1	RW		ENHSPLL	BETACAM		ENVSPROC				11001000	C8
2	02	Video Selection 2	RW	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]					00000100	04
3	03	Output control	RW	VBI_EN	TOD							01001100	4C
4	04	Extended output control	RW	BT.656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	Range	00110101	35
5	05	Reserved											
6	06	Reserved											
7	07	Autodetect enable	RW	AD_ SEC525_EN	AD_SECAM_ EN	AD_N443_ EN	AD_P60_EN	AD_PALN_EN	AD_PALM_ EN	AD_NTSC_ EN	AD_PAL_ EN	01111111	7F
8	08	Contrast	RW	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]	10000000	80
9	09	Reserved											
10	0A	Brightness adjust	RW	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]	00000000	00
11	0B	Hue adjust	RW	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]	00000000	00
12	0C	Default Value Y	RW	DEF_Y[5]	DEF_Y[4]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_VAL_ AUTO_EN	DEF_VAL_ EN	00110110	36
13	0D	Default Value C	RW	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]	01111100	7C
14	0E	ADI Control 1	RW		SUB_USR_ EN[1]	SUB_USR_ EN[0]						00000000	00
15	0F	Power management	RW	Reset		PWRDWN						00100000	20
16	10	Status 1	R	COL_KILL	AD_ RESULT[2]	AD_ RESULT[1]	AD_ RESULT[0]	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK		
17	11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]	00011100	1C
18	12	Status 2	R			FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET		
19	13	Status 3	R	PAL_SW_ LOCK	Interlaced	STD FLD LEN	FREE_RUN_ ACT	Reserved	SD_OP_ 50Hz	Reserved	INST_ HLOCK		
20	14	Analog clamp control	RW				CCLEN		FREE_RUN_ PAT_SEL.2	FREE_RUN_ PAT_SEL.1	FREE_ RUN_ PAT_SEL.0	00010000	10
21	15	Digital Clamp Control 1	RW		DCT[1]	DCT[0]	DCFE					0000xxxx	00
22	16	Reserved											
23	17	Shaping Filter Control 1	RW	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]	00000001	01
24	18	Shaping Filter Control 2	RW	WYSFMOVR			WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]	10010011	93
25	19	Comb filter control	RW					NSFSEL[1]	NSFSEL[0]	PSFSEL[1]	PSFSEL[0]	11110001	F1
29	1D	ADI Control 2	RW	TRI_LLC								11000xxx	C0
39	27	Pixel delay control	RW	SWPC	AUTO_PDC_ EN	CTA[2]	CTA[1]	CTA[0]		LTA[1]	LTA[0]	01011000	58
43	2B	Misc gain control	RW		CKE						PW_UPD	11100001	E1
44	2C	AGC mode control	RW		LAGC[2]	LAGC[1]	LAGC[0]			CAGC[1]	CAGC[0]	10101110	AE
45	2D	Chroma Gain Control 1	W	CAGT[1]	CAGT[0]			CMG[11]	CMG[10]	CMG[9]	CMG[8]	11110100	F4
45	2D	Chroma Gain 1	R					CG[11]	CG[10]	CG[9]	CG[8]		

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
46	2E	Chroma Gain Control 2	W	CMG[7]	CMG[6]	CMG[5]	CMG[4]	CMG[3]	CMG[2]	CMG[1]	CMG[0]	00000000	00
46	2E	Chroma Gain 2	R	CG[7]	CG[6]	CG[5]	CG[4]	CG[3]	CG[2]	CG[1]	CG[0]		
47	2F	Luma Gain Control 1	W	LAGT[1]	LAGT[0]			LMG[11]	LMG[10]	LMG[9]	LMG[8]	1111xxxx	F0
47	2F	Luma Gain 1	R					LG[11]	LG[10]	LG[9]	LG[8]		
48	30	Luma Gain Control 2	W	LMG[7]	LMG[6]	LMG[5]	LMG[4]	LMG[3]	LMG[2]	LMG[1]	LMG[0]	xxxxxxxx	00
48	30	Luma Gain 2	R	LG[7]	LG[6]	LG[5]	LG[4]	LG[3]	LG[2]	LG[1]	LG[0]		
49	31	VS/FIELD Control 1	RW				NEWAVMODE	HVSTIM				00000010	02
50	32	VS/FIELD Control 2	RW	VSBHO	VSBHE							01000001	41
51	33	VS/FIELD Control 3	RW	VSEHO	VSEHE							10000100	84
52	34	HS Position Control 1	RW		HSB[10]	HSB[9]	HSB[8]		HSE[10]	HSE[9]	HSE[8]	00000000	00
53	35	HS Position Control 2	RW	HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]	00000010	02
54	36	HS Position Control 3	RW	HSE[7]	HSE[6]	HSE[5]	HSE[4]	HSE[3]	HSE[2]	HSE[1]	HSE[0]	00000000	00
55	37	Polarity	RW	PHS		PVS		PF			PCLK	00010001	09
56	38	NTSC comb control	RW	CTAPSN[1]	CTAPSN[0]	CCMN[2]	CCMN[1]	CCMN[0]	YCMN[2]	YCMN[1]	YCMN[0]	10000000	80
57	39	PAL comb control	RW	CTAPSP[1]	CTAPSP[0]	CCMP[2]	CCMP[1]	CCMP[0]	YCMP[2]	YCMP[1]	YCMP[0]	11000000	C0
58	3A	ADC control	RW					PWRDWN_ MUX_0	PWRDWN_ MUX_1	PWRDWN_ MUX_2	MUX power-down override	00000000	00
61	3D	Manual window control	RW		CKILLTHR[2]	CKILLTHR[1]	CKILLTHR[0]					00100010	22
65	41	Resample control	RW		SFL_INV							00000001	01
77	4D	CTI DNR Control 1	RW			DNR_EN		CTI_AB[1]	CTI_AB[0]	CTI_AB_EN	CTI_EN	11101111	EF
78	4E	CTI DNR Control 2	RW	CTI_C_ TH[7]	CTI_C_TH[6]	CTI_C_ TH[5]	CTI_C_TH[4]	CTI_C_TH[3]	CTI_C_ TH[2]	CTI_C_ TH[1]	CTI_C_TH[0]	00001000	08
80	50	DNR Noise Threshold 1	RW	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]	00001000	08
81	51	Lock count	RW	FSCLE	SRLS	COL[2]	COL[1]	COL[0]	CIL[2]	CIL[1]	CIL[0]	00100100	24
96	60	ADC Switch 3	RW						MUX_3[2]	MUX_3[1]	MUX_3[0]	00010000	10
106	6A	Output Sync Select 1	RW						HS_OUT_ SEL[2]	HS_OUT_ SEL[1]	HS_OUT_ SEL[0]	00000000	00
107	6B	Output Sync Select 2	RW		FLD_OUT_ SEL[2]	FLD_OUT_ SEL[1]	FLD_OUT_ SEL[0]					00010010	12
143	8F	Freerun Line Length 1	W		LLC_PAD_ SEL[2]	LLC_PAD_ SEL[1]	LLC_PAD_ SEL[0]					00000000	00
153	99	CCAP1	R	CCAP1[7]	CCAP1[6]	CCAP1[5]	CCAP1[4]	CCAP1[3]	CCAP1[2]	CCAP1[1]	CCAP1[0]		
154	9A	CCAP2	R	CCAP2[7]	CCAP2[6]	CCAP2[5]	CCAP2[4]	CCAP2[3]	CCAP2[2]	CCAP2[1]	CCAP2[0]		
155	9B	Letterbox 1	R	LB_LCT[7]	LB_LCT[6]	LB_LCT[5]	LB_LCT[4]	LB_LCT[3]	LB_LCT[2]	LB_LCT[1]	LB_LCT[0]		
156	9C	Letterbox 2	R	LB_LCM[7]	LB_LCM[6]	LB_LCM[5]	LB_LCM[4]	LB_LCM[3]	LB_LCM[2]	LB_LCM[1]	LB_LCM[0]		
157	9D	Letterbox 3	R	LB_LCB[7]	LB_LCB[6]	LB_LCB[5]	LB_LCB[4]	LB_LCB[3]	LB_LCB[2]	LB_LCB[1]	LB_LCB[0]		
178	B2	CRC enable	W						CRC_ ENABLE			00011100	1C
195	C3	ADC Switch 1	RW		MUX_1[2]	MUX_1[1]	MUX_1[0]		MUX_0[2]	MUX_0[1]	MUX_0[0]	xxxxxxxx	00
196	C4	ADC Switch 2	RW	MAN_ MUX_EN					MUX_2[2]	MUX_2[1]	MUX_2[0]	0xxxxxxx	00
220	DC	Letterbox Control 1	RW				LB_TH[4]	LB_TH[3]	LB_TH[2]	LB_TH[1]	LB_TH[0]	10101100	AC

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
221	DD	Letterbox Control 2	RW	LB_SL[3]	LB_SL[2]	LB_SL[1]	LB_SL[0]	LB_EL[3]	LB_EL[2]	LB_EL[1]	LB_EL[0]	01001100	4C
222	DE	ST Noise Readback 1	R					ST_NOISE_ VLD	ST_ NOISE[10]	ST_ NOISE[9]	ST_NOISE[8]		
223	DF	ST Noise Readback 2	R	ST_ NOISE[7]	ST_NOISE[6]	ST_ NOISE[5]	ST_NOISE[4]	ST_NOISE[3]	ST_ NOISE[2]	ST_ NOISE[1]	ST_ NOISE[0]		
225	E1	SD offset Cb channel	RW	SD_OFF_ Cb[7]	SD_OFF_ Cb[6]	SD_OFF_ Cb[5]	SD_OFF_ Cb[4]	SD_OFF_ Cb[3]	SD_OFF_ Cb[2]	SD_OFF_ Cb[1]	SD_OFF_ Cb[0]	10000000	80
226	E2	SD offset Cr channel	RW	SD_OFF_ Cr[7]	SD_OFF_ Cr[6]	SD_OFF_ Cr[5]	SD_OFF_Cr[4]	SD_OFF_Cr[3]	SD_OFF_ Cr[2]	SD_OFF_ Cr[1]	SD_OFF_ Cr[0]	10000000	80
227	E3	SD saturation Cb channel	RW	SD_SAT_ Cb[7]	SD_SAT_Cb[6]	SD_SAT_ Cb[5]	SD_SAT_Cb[4]	SD_SAT_Cb[3]	SD_SAT_ Cb[2]	SD_SAT_ Cb[1]	SD_SAT_ Cb[0]	10000000	80
228	E4	SD saturation Cr channel	RW	SD_SAT_ Cr[7]	SD_SAT_Cr[6]	SD_SAT_ Cr[5]	SD_SAT_Cr[4]	SD_SAT_Cr[3]	SD_SAT_ Cr[2]	SD_SAT_ Cr[1]	SD_SAT_ Cr[0]	10000000	80
229	E5	NTSC V bit begin	RW	NVBEG-DELO	NVBEG-DELE	NVBEGSIGN	NVBEG[4]	NVBEG[3]	NVBEG[2]	NVBEG[1]	NVBEG[0]	00100101	25
230	E6	NTSC V bit end	RW	NVEND-DELO	NVENDDELE	NVEND-SIGN	NVEND[4]	NVEND[3]	NVEND[2]	NVEND[1]	NVEND[0]	00000100	04
231	E7	NTSC F bit toggle	RW	NFTOG-DELO	NFTOGDELE	NFTOGSIGN	NFTOG[4]	NFTOG[3]	NFTOG[2]	NFTOG[1]	NFTOG[0]	01100011	63
232	E8	PAL V bit begin	RW	PVBEG-DELO	PVBEGDELE	PVBEGSIGN	PVBEG[4]	PVBEG[3]	PVBEG[2]	PVBEG[1]	PVBEG[0]	01100101	65
233	E9	PAL V bit end	RW	PVEND-DELO	PVENDDELE	PVENDSIGN	PVEND[4]	PVEND[3]	PVEND[2]	PVEND[1]	PVEND[0]	00010100	14
234	EA	PAL F bit toggle	RW	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG[4]	PFTOG[3]	PFTOG[2]	PFTOG[1]	PFTOG[0]	01100011	63
235	EB	VBLANK Control 1	RW	NVBIOL-CM[1]	NVBIOLCM[0]	NVBIELCM[1]	NVBIELCM[0]	PVBIOLCM[1]	PVBIOL-CM[0]	PVBIEL-CM[1]	PVBIEL-CM[0]	01010101	55
236	EC	VBLANK Control 2	RW	NVBIO-CCM[1]	NVBIOCCM[0]	NVBIE-CCM[1]	NVBIECCM[0]	PVBIOCCM[1]	PVBIO-CCM[0]	PVBIE-CCM[1]	PVBIE-CCM[0]	01010101	55
243	F3	AFE_ CONTROL 1	RW				AA_FILT_ MAN_OVR	AA_FILT_ EN[3]	AA_FILT_ EN[2]	AA_FILT_ EN[1]	AA_FILT_ EN[0]	00000000	00
244	F4	Drive strength	RW	GLITCH_ FILT_BYP		DR_STR[1]	DR_STR[0]	DR_STR_C[1]	DR_STR_ C[0]	DR_STR_ S[1]	DR_STR_ S[0]	0x010101	15
248	F8	IF comp control	RW						IFFILTSEL[2]	IFFILTSEL[1]	IFFILTSEL[0]	00000000	00
249	F9	VS mode control	RW					VS_COAST_ MODE[1]	VS_COAST_ MODE[0]	EXTEND_ VS_MIN_ FREQ	EXTEND_ VS_MAX_ FREQ	00000011	03
251	FB	Peaking gain	RW	PEAKING_ GAIN[7]	PEAKING_ GAIN[6]	PEAKING_ GAIN[5]	PEAKING_ GAIN[4]	PEAKING_ GAIN[3]	PEAKING_ GAIN[2]	PEAKING_ GAIN[1]	PEAKING_ GAIN[0]	01000000	40
252	FC	DNR Noise Threshold 2	RW	DNR_ TH2[7]	DNR_TH2[6]	DNR_ TH2[5]	DNR_TH2[4]	DNR_TH2[3]	DNR_ TH2[2]	DNR_ TH2[1]	DNR_ TH2[0]	00000100	04

To access the registers listed in Table 94, the SUB_USR_EN bit in Register Address 0x0E must be programmed to 10b. All read only registers are left blank.

Table 94. User Sub Map 2 Register Map Details

Address		Register										Reset	
Dec	Hex	Name	RW	7	6	5	4	3	2	1	0	Value	Hex
128	80	ACE Control 1	RW	ACE_ ENABLE								00000000	00
131	83	ACE Control 4	RW				ACE_ LUMA_ GAIN[4]	ACE_LUMA_ GAIN [3]	ACE_ LUMA_ GAIN[2]	ACE_ LUMA_ GAIN[1]	ACE_ LUMA_ GAIN[0]	00001101	0D
132	84	ACE Control 5	RW	ACE_CHR OMA_ MAX[3]	ACE_ CHROMA_ MAX[2]	ACE_ CHROMA_ MAX[1]	ACE_ CHROMA_ MAX[0]	ACE_ CHROMA_ GAIN[3]	ACE_ CHROMA_ GAIN[2]	ACE_ CHROMA_ GAIN[1]	ACE_ CHROMA_ GAIN[0]	10001000	88
133	85	ACE Control 6	RW	ACE_ RES- PONSE_ SPEED[3]	ACE_ RESPONSE_ SPEED[2]	ACE_ RESPONSE_ SPEED[2]	ACE_ RESPONSE_ SPEED[1]	ACE_ GAMMA_ GAIN[3]	ACE_ GAMMA_ GAIN[2]	ACE_ GAMMA_ GAIN[1]	ACE_ GAMMA_ GAIN[0]	11111000	F8
146	92	Dither control	RW								BR_ DITHER_ MODE	00000000	00
217	D9	Min Max 0	RW	MIN_ THRESH_ Y[7]	MIN_ THRESH_ Y[6]	MIN_ THRESH_Y[5]	MIN_ THRESH_ Y[4]	MIN_ THRESH_Y[3]	MIN_ THRESH_Y[2]	MIN_ THRESH_ Y[1]	MIN_ THRESH_ Y[0]	00000000	00
218	DA	Min Max 1	RW	MAX_ THRESH_ Y[7]	MAX_ THRESH_ Y[6]	MAX_ THRESH_Y[5]	MAX_ THRESH_ Y[4]	MAX_ THRESH_Y[3]	MAX_ THRESH_Y[2]	MAX_ THRESH_ Y[1]	MAX_ THRESH_ Y[0]	11111111	FF
219	DB	Min Max 2	RW	MIN_ THRESH_ C[7]	MIN_ THRESH_ C[6]	MIN_ THRESH_C[5]	MIN_ THRESH_ C[4]	MIN_ THRESH_C[3]	MIN_ THRESH_C[2]	MIN_ THRESH_ C[1]	MIN_ THRESH_ C[0]	00000000	00
220	DC	Min Max 3	RW	MAX_ THRESH_ C[7]	MAX_ THRESH_ C[6]	MAX_ THRESH_C[5]	MAX_ THRESH_ C[4]	MAX_ THRESH_C[3]	MAX_ THRESH_C[2]	MAX_ THRESH_ C[1]	MAX_ THRESH_ C[0]	11111111	FF
221	DD	Min Max 4	RW	MIN_ SAMPLES _ALL- OWED_ Y[3]	MIN_ SAMPLES_ ALLOWED_ Y[2]	MIN_ SAMPLES_ ALLOWED_ Y[1]	MIN_SAMP LES_ ALLOWED_ Y[0]	MAX_ SAMPLES_ ALLOWED_ Y[3]	MAX_ SAMPLES_ ALLOWED_ Y[2]	MAX_ SAMPLES_ ALLOWED_ Y[1]	MAX_ SAMPLES_ ALLOWED_ Y[0]	11001100	CC
222	DE	Min Max 5	RW	MIN_ SAMPLES_ ALL- OWED_ C[3]	MIN_ SAMPLES_ ALLOWED_ C[2]	MIN_ SAMPLES_ ALLOWED_ C[1]	MIN_ SAMPLES_ ALLOWED_ C[0]	MAX_ SAMPLES_ ALLOWED_ C[3]	MAX_ SAMPLES_ ALLOWED_ C[2]	MAX_ SAMPLES_ ALLOWED_ C[1]	MAX_ SAMPLES_ ALLOWED_ C[0]	11001100	CC
224	E0	FL control	RW								FL_ENABLE	00000000	00
225	E1	Y Average 0	RW	LINE_ START[8]	LINE_ START[7]	LINE_ START[6]	LINE_ START[5]	LINE_ START[4]	LINE_ START[3]	LINE_ START[2]	LINE_ START[1]	0001001	11
226	E2	Y Average 1	RW	LINE_ END[8]	LINE_ END[7]	LINE_END[6]	LINE_ END[5]	LINE_END[4]	LINE_END[3]	LINE_ END[2]	LINE_ END[1]	10001000	88
227	E3	Y Average 2	RW	SAMPLE_ START[9]	SAMPLE_ START[8]	SAMPLE_ START[7]	SAMPLE_ START[6]	SAMPLE_ START[5]	SAMPLE_ START[4]	SAMPLE_ START[3]	SAMPLE_ START[2]	00010111	1B
228	E4	Y Average 3	RW	SAMPLE_ END[9]	SAMPLE_ END[8]	SAMPLE_ END[7]	SAMPLE_ END[6]	SAMPLE_ END[5]	SAMPLE_ END[4]	SAMPLE_ END[3]	SAMPLE_ END[2]	11010111	D7
229	E5	Y Average 4	RW	SAMPLE_ END[1]	SAMPLE_ END[0]	SAMPLE_ START[1]	SAMPLE_ START[0]			LINE_ END[0]	LINE_ START[0]	00100011	23
230	E6	Y Average 5	RW				Y_AVG_ TIME_ CONST[2]	Y_AVG_TIME_ CONST[1]	Y_AVG_ TIME_ CONST[0]	Y_AVG_ FILT_EN	CAPTURE_ VALUE	00010000	10
231	E7	Y average data MSB	R	Y_AVER- AGE[9]	Y_AVER- AGE[8]	Y_AVER- AGE[7]	Y_AVER- AGE[6]	Y_AVERAGE[5]	Y_AVER- AGE[4]	Y_AVER- AGE[3]	Y_AVER- AGE[2]		
232	E8	Y average data LSB	R							Y_AVER- AGE[1]	Y_AVER- AGE[0]		

To access the registers listed in Table 95, the SUB_USR_EN bit in Register Address 0x0E must be programmed to 01b. All read only registers are left blank.

Table 95. Interrupt/VDP Map Details[1]

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
64	40	Interrupt Configuration 1	RW	INTRQ_ DUR_SEL[1]	INTRQ_ DUR_SEL[0]	MV_INTRQ_ SEL[1]	MV_INTRQ_ SEL[0]		MPU_STIM_ INTRQ	INTRQ_OP_ SEL[1]	INTRQ_OP_ SEL[0]	0001x000	10
66	42	Interrupt Status 1	R		MV_PS_CS_ Q	SD_FR_ CHNG_Q				SD_ UNLOCK_Q	SD_LOCK_Q		
67	43	Interrupt Clear 1	W		MV_PS_CS_ CLR	SD_FR_ CHNG_CLR				SD_ UNLOCK_ CLR	SD_LOCK_ CLR	x0000000	00
68	44	Interrupt Mask 1	RW		MV_PS_CS_ MSKB[2]	SD_FR_ CHNG_ MSKB[2]				SD_ UNLOCK_ MSKB[2]	SD_LOCK_ MSKB[2]	x0000000	00
69	45	Raw Status 2	R	MPU_STIM_ INTRQ		CHX_MIN_ MAX_INTRQ	EVEN_FIELD				CCAPD		
70	46	Interrupt Status 2	R	MPU_STIM_ INTRQ_Q			SD_FIELD_ CHNGD_Q				CCAPD_Q		
71	47	Interrupt Clear 2	W	MPU_STIM_ INTRQ_CLR		CHX_MIN_ MAX_ INTRQ_CLR	SD_FIELD_ CHNGD_ CLR				CCAPD_CLR	0xx00000	00
72	48	Interrupt Mask 2	RW	MPU_STIM_ INTRQ_ MSKB[2]		CHX_MIN_ MAX_INTRQ _MSKB[2]	SD_FIELD_ CHNGD_ MSKB[2]				CCAPD_ MSKB[2]	0xx00000	00
73	49	Raw Status 3	R				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_ 50Hz		
74	4A	Interrupt Status 3	R			PAL_SW_ LK_CHNG_Q	SCM_LOCK_ CHNG_Q	SD_AD_ CHNG_Q	SD_H_ LOCK_ CHNG_Q	SD_V_ LOCK_ CHNG_Q	SD_OP_ CHNG_Q		
75	4B	Interrupt Clear 3	W			PAL_SW_ LK_CHNG_ CLR	SCM_LOCK_ CHNG_CLR	SD_AD_ CHNG_ CLR	SD_H_ LOCK_ CHNG_CLR	SD_V_ LOCK_ CHNG_CLR	SD_OP_ CHNG_ CLR	xx000000	00
76	4C	Interrupt Mask 3	RW			PAL_SW_ LK_CHNG_ MSKB[2]	SCM_LOCK_ CHNG_ MSKB[2]	SD_AD_ CHNG_ MSKB[2]	SD_H_ LOCK_ CHNG_ MSKB[2]	SD_V_ LOCK_ CHNG_ MSKB[2]	SD_OP_ CHNG_ MSKB[2]	xx000000	00
78	4E	Interrupt Status 4	R						VDP_CGMS_ WSS_ CHNGD_Q		VDP_ CCAPD_Q		
79	4F	Interrupt Clear 4	W						VDP_CGMS_ WSS_ CHNGD_ CLR		VDP_ CCAPD_CLR	00x0x0x0	00
80	50	Interrupt Mask 4	RW						VDP_CGMS_ WSS_ CHNGD_ MSKB[2]		VDP_ CCAPD_ MSKB[2]	00x0x0x0	00
81	51	Interrupt Latch 0	R			Y_ CHANNEL_ MIN_ VIOLATION	Y_ CHANNEL_ MAX_ VIOLATION	CB_ CHANNEL_ MIN_ VIOLATION	CB_ CHANNEL_ MAX_ VIOLATION	CR_ CHANNEL_ MIN_ VIOLATION	CR_ CHANNEL_ MAX_ VIOLATION		
96	60	VDP_CONFIG_1	RW					WST_PKT_ DECODE_ DISABLE	VDP_TTXT_ TYPE_MAN_ ENABLE	VDP_TTXT_ TYPE_ MAN[1]	VDP_TTXT_ TYPE_ MAN[0]	10001000	88
98	62	VDP_ADF_ CONFIG_1	RW	ADF_ ENABLE	ADF_ MODE[1]	ADF_ MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]	00010101	15
99	63	VDP_ADF_ CONFIG_2	RW	DUPLICATE_ ADF		ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]	0x101010	2A
100	64	VDP_LINE_00E	RW	MAN_LINE_ PGM				VBI_DATA_ P318[3]	VBI_DATA_ P318[2]	VBI_DATA_ P318[1]	VBI_DATA_ P318[0]	0xxx0000	00
101	65	VDP_LINE_00F	RW	VBI_DATA_ P6_N23[3]	VBI_DATA_ P6_N23[2]	VBI_DATA_ P6_N23[1]	VBI_DATA_ P6_N23[0]	VBI_DATA_ P319_ N286[3]	VBI_DATA_ P319_ N286[2]	VBI_DATA_ P319_ N286[1]	VBI_DATA_ P319_ N286[0]	00000000	00

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
102	66	VDP_LINE_010	RW	VBI_DATA_P7_N24[3]	VBI_DATA_P7_N24[2]	VBI_DATA_P7_N24[1]	VBI_DATA_P7_N24[0]	VBI_DATA_P320_N287[3]	VBI_DATA_P320_N287[2]	VBI_DATA_P320_N287[1]	VBI_DATA_P320_N287[0]	00000000	00
103	67	VDP_LINE_011	RW	VBI_DATA_P8_N25[3]	VBI_DATA_P8_N25[2]	VBI_DATA_P8_N25[1]	VBI_DATA_P8_N25[0]	VBI_DATA_P321_N288[3]	VBI_DATA_P321_N288[2]	VBI_DATA_P321_N288[1]	VBI_DATA_P321_N288[0]	00000000	00
104	68	VDP_LINE_012	RW	VBI_DATA_P9[3]	VBI_DATA_P9[2]	VBI_DATA_P9[1]	VBI_DATA_P9[0]	VBI_DATA_P322[3]	VBI_DATA_P322[2]	VBI_DATA_P322[1]	VBI_DATA_P322[0]	00000000	00
105	69	VDP_LINE_013	RW	VBI_DATA_P10[3]	VBI_DATA_P10[2]	VBI_DATA_P10[1]	VBI_DATA_P10[0]	VBI_DATA_P323[3]	VBI_DATA_P323[2]	VBI_DATA_P323[1]	VBI_DATA_P323[0]	00000000	00
106	6A	VDP_LINE_014	RW	VBI_DATA_P11[3]	VBI_DATA_P11[2]	VBI_DATA_P11[1]	VBI_DATA_P11[0]	VBI_DATA_P324_N272[3]	VBI_DATA_P324_N272[2]	VBI_DATA_P324_N272[1]	VBI_DATA_P324_N272[0]	00000000	00
107	6B	VDP_LINE_015	RW	VBI_DATA_P12_N10[3]	VBI_DATA_P12_N10[2]	VBI_DATA_P12_N10[1]	VBI_DATA_P12_N10[0]	VBI_DATA_P325_N273[3]	VBI_DATA_P325_N273[2]	VBI_DATA_P325_N273[1]	VBI_DATA_P325_N273[0]	00000000	00
108	6C	VDP_LINE_016	RW	VBI_DATA_P13_N11[3]	VBI_DATA_P13_N11[2]	VBI_DATA_P13_N11[1]	VBI_DATA_P13_N11[0]	VBI_DATA_P326_N274[3]	VBI_DATA_P326_N274[2]	VBI_DATA_P326_N274[1]	VBI_DATA_P326_N274[0]	00000000	00
109	6D	VDP_LINE_017	RW	VBI_DATA_P14_N12[3]	VBI_DATA_P14_N12[2]	VBI_DATA_P14_N12[1]	VBI_DATA_P14_N12[0]	VBI_DATA_P327_N275[3]	VBI_DATA_P327_N275[2]	VBI_DATA_P327_N275[1]	VBI_DATA_P327_N275[0]	00000000	00
110	6E	VDP_LINE_018	RW	VBI_DATA_P15_N13[3]	VBI_DATA_P15_N13[2]	VBI_DATA_P15_N13[1]	VBI_DATA_P15_N13[0]	VBI_DATA_P328_N276[3]	VBI_DATA_P328_N276[2]	VBI_DATA_P328_N276[1]	VBI_DATA_P328_N276[0]	00000000	00
111	6F	VDP_LINE_019	RW	VBI_DATA_P16_N14[3]	VBI_DATA_P16_N14[2]	VBI_DATA_P16_N14[1]	VBI_DATA_P16_N14[0]	VBI_DATA_P329_N277[3]	VBI_DATA_P329_N277[2]	VBI_DATA_P329_N277[1]	VBI_DATA_P329_N277[0]	00000000	00
112	70	VDP_LINE_01A	RW	VBI_DATA_P17_N15[3]	VBI_DATA_P17_N15[2]	VBI_DATA_P17_N15[1]	VBI_DATA_P17_N15[0]	VBI_DATA_P330_N278[3]	VBI_DATA_P330_N278[2]	VBI_DATA_P330_N278[1]	VBI_DATA_P330_N278[0]	00000000	00
113	71	VDP_LINE_01B	RW	VBI_DATA_P18_N16[3]	VBI_DATA_P18_N16[2]	VBI_DATA_P18_N16[1]	VBI_DATA_P18_N16[0]	VBI_DATA_P331_N279[3]	VBI_DATA_P331_N279[2]	VBI_DATA_P331_N279[1]	VBI_DATA_P331_N279[0]	00000000	00
114	72	VDP_LINE_01C	RW	VBI_DATA_P19_N17[3]	VBI_DATA_P19_N17[2]	VBI_DATA_P19_N17[1]	VBI_DATA_P19_N17[0]	VBI_DATA_P332_N280[3]	VBI_DATA_P332_N280[2]	VBI_DATA_P332_N280[1]	VBI_DATA_P332_N280[0]	00000000	00
115	73	VDP_LINE_01D	RW	VBI_DATA_P20_N18[3]	VBI_DATA_P20_N18[2]	VBI_DATA_P20_N18[1]	VBI_DATA_P20_N18[0]	VBI_DATA_P333_N281[3]	VBI_DATA_P333_N281[2]	VBI_DATA_P333_N281[1]	VBI_DATA_P333_N281[0]	00000000	00
116	74	VDP_LINE_01E	RW	VBI_DATA_P21_N19[3]	VBI_DATA_P21_N19[2]	VBI_DATA_P21_N19[1]	VBI_DATA_P21_N19[0]	VBI_DATA_P334_N282[3]	VBI_DATA_P334_N282[2]	VBI_DATA_P334_N282[1]	VBI_DATA_P334_N282[0]	00000000	00
117	75	VDP_LINE_01F	RW	VBI_DATA_P22_N20[3]	VBI_DATA_P22_N20[2]	VBI_DATA_P22_N20[1]	VBI_DATA_P22_N20[0]	VBI_DATA_P335_N283[3]	VBI_DATA_P335_N283[2]	VBI_DATA_P335_N283[1]	VBI_DATA_P335_N283[0]	00000000	00
118	76	VDP_LINE_020	RW	VBI_DATA_P23_N21[3]	VBI_DATA_P23_N21[2]	VBI_DATA_P23_N21[1]	VBI_DATA_P23_N21[0]	VBI_DATA_P336_N284[3]	VBI_DATA_P336_N284[2]	VBI_DATA_P336_N284[1]	VBI_DATA_P336_N284[0]	00000000	00
119	77	VDP_LINE_021	RW	VBI_DATA_P24_N22[3]	VBI_DATA_P24_N22[2]	VBI_DATA_P24_N22[1]	VBI_DATA_P24_N22[0]	VBI_DATA_P337_N285[3]	VBI_DATA_P337_N285[2]	VBI_DATA_P337_N285[1]	VBI_DATA_P337_N285[0]	00000000	00
120	78	VDP_STATUS	R	TTXT_AVL					CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL		
120	78	VDP_STATUS_CLEAR	W						CGMS_WSS_CLEAR		CC_CLEAR	00000000	00
121	79	VDP_CCAP_DATA_0	R	CCAP_BYTE_1[7]	CCAP_BYTE_1[6]	CCAP_BYTE_1[5]	CCAP_BYTE_1[4]	CCAP_BYTE_1[3]	CCAP_BYTE_1[2]	CCAP_BYTE_1[1]	CCAP_BYTE_1[0]		
122	7A	VDP_CCAP_DATA_1	R	CCAP_BYTE_2[7]	CCAP_BYTE_2[6]	CCAP_BYTE_2[5]	CCAP_BYTE_2[4]	CCAP_BYTE_2[3]	CCAP_BYTE_2[2]	CCAP_BYTE_2[1]	CCAP_BYTE_2[0]		
125	7D	VDP_CGMS_WSS_DATA_0	R					CGMS_CRC[5]	CGMS_CRC[4]	CGMS_CRC[3]	CGMS_CRC[2]		
126	7E	VDP_CGMS_WSS_DATA_1	R	CGMS_CRC[1]	CGMS_CRC[0]	CGMS_WSS[13]	CGMS_WSS[12]	CGMS_WSS[11]	CGMS_WSS[10]	CGMS_WSS[9]	CGMS_WSS[8]		

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	Hex
127	7F	VDP_CGMS_ WSS_DATA_2	R	CGMS_ WSS[7]	CGMS_ WSS[6]	CGMS_ WSS[5]	CGMS_ WSS[4]	CGMS_ WSS[3]	CGMS_ WSS[2]	CGMS_ WSS[1]	CGMS_ WSS[0]		
156	9C	VDP_OUTPUT_ SEL	RW				WSS_CGMS_ CB_CHANGE					00110000	30

[1] x in a reset value indicates do not care.
[2] B at the end of the bit name equals an overbar for the whole bit name.

To access all the registers listed in Table 96, SUB_USR_EN in Register Address 0x0E must be programmed to 00b. The gray shading is the default.

Table 96. Register Map Descriptions (Main Register Map)[1]

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x00	Input control	INSEL[4:0]; the INSEL bits allow the user to select an input channel and the input format				0	0	0	0	0	CVBS input on $A_{IN}1$	
						0	0	0	0	1	CVBS input on $A_{IN}2$	
						0	0	0	1	0	CVBS input on $A_{IN}3$	
						0	0	0	1	1	CVBS input on $A_{IN}4$	
						0	1	0	0	0	Y input on $A_{IN}1$, C input on $A_{IN}2$	
						0	1	0	0	1	Y input on $A_{IN}3$, C input on $A_{IN}4$	
						0	1	1	0	0	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	
						0	1	1	1	0	Differential positive on $A_{IN}1$, differential negative on $A_{IN}2$	
						0	1	1	1	1	Differential positive on $A_{IN}3$, differential negative on $A_{IN}4$	
0x01	Video Selection 1	Reserved						0	0	0	Sets to default	
		ENVSPROC					0				Disables VSYNC processor	
							1				Enables VSYNC processor	
		Reserved				0					Sets to default	
		BETACAM; enables BETACAM levels			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disables HSYNC processor	
				1							Enables HSYNC processor	
		Reserved	1								Sets to default	
0x02	Video Selection 2	Reserved					0	1	0	0	Set to default	
		VID_SEL[3:0]; the VID_SEL bits allow the user to select the input video standard	0	0	0	0					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC J (no pedestal), SECAM	
			0	0	0	1					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC M (pedestal), SECAM	
			0	0	1	0					Autodetects PAL N (pedestal), NTSC J (no pedestal), SECAM	
			0	0	1	1					Autodetects PAL N (pedestal), NTSC M (pedestal) SECAM	
			0	1	0	0					NTSC J	
			0	1	0	1					NTSC M	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL B/G/H/I/D	
			1	0	0	1					PAL N = PAL B/PAL G/PAL H/ PAL I/PAL D (with pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL Combination N	
			1	1	0	1					PAL Combination N (with pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x03	Output control	Reserved			0	0	1	1	0	0	Reserved	
		TOD; tristate output drivers; this bit allows the user to tristate the output drivers; pixel outputs, HS and VS/FIELD/SFL		0							Output drivers enabled	See the TIM_OE and TRI_LLC bits
				1							Output drivers tristated	
		VBI_EN; vertical blanking interval data enable; allows VBI data (Line 1 to Line 21) to be passed through with only a minimum amount of filtering performed	0								All lines filtered and scaled	
			1								Only active video region filtered	
0x04	Extended output control	Range; allows the user to select the range of output values; can be ITU-R BT.656 compliant or can fill the whole accessible number range								0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240	ITU-R BT.656
										1	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254	Extended range
		EN_SFL_PIN							0		Disables SFL output	SFL output enables encoder and decoder to be connected directly
									1		Outputs SFL information on the SFL pin	
		BL_C_VBI; blank chroma during VBI; if set, it enables data in the VBI region to be passed through the decoder undistorted						0			Decode and output color during VBI	during VBI
								1			Blank Cr and Cb values during VBI	
		TIM_OE; enables timing signals output					0				HS, VS, FIELD tristated	Controlled by TOD
							1				HS, VS, FIELD forced active	
		Reserved		0	1	1						
		BT.656-4; allows the user to select an output mode compatible with ITU-R BT.656-3/-4	0								ITU-R BT.656-3 compatible	
			1								ITU-R BT.656-4 compatible	
0x07	Autodetect enable	AD_PAL_EN; PAL B/PAL D/PAL I/PAL G/PAL H autodetect enable								0	Disables	
										1	Enables	
		AD_NTSC_EN; NTSC autodetect enable							0		Disables	
									1		Enables	
		AD_PALM_EN; PAL M autodetect enable						0			Disables	
								1			Enables	
		AD_PALN_EN; PAL N autodetect enable					0				Disables	
							1				Enables	
		AD_P60_EN; PAL 60 autodetect enable				0					Disables	
						1					Enables	
		AD_N443_EN; NTSC 4.43 autodetect enable			0						Disables	
					1						Enables	
		AD_SECAM_EN; SECAM autodetect enable		0							Disables	
				1							Enables	
		AD_SEC525_EN; SECAM 525 autodetect enable	0								Disables	
			1								Enables	
0x08	Contrast	CON[7:0]; contrast adjust; this is the user control for contrast adjustment	1	0	0	0	0	0	0	0	Luma gain = 1	0x00 gain = 0, 0x80 gain = 1, 0xFF gain = 2
0x0A	Brightness adjust	BRI[7:0]; this register controls the brightness of the video signal	0	0	0	0	0	0	0	0		0x00 = 0 IRE, 0x7F = +30 IRE, 0x80 = −30 IRE
0x0B	Hue adjust	HUE[7:0]; this register contains the value for the color hue adjustment	0	0	0	0	0	0	0	0		Hue range = −90° to +90°

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x0C	Default Value Y	DEF_VAL_EN; default value enable								0	Freerun mode dependent on DEF_VAL_AUTO_EN	
										1	Forces freerun mode on	
		DEF_VAL_AUTO_EN; default value automatic enable							0		Disables freerun mode	When lock is lost, freerun mode can be enabled to output stable timing, clock, and a set color
									1		Enables automatic freerun mode	
		DEF_Y[5:0]; default value is Y; this register holds the Y default value	0	0	1	1	0	1			Y[7:0] = {DEF_Y[5:0], 0, 0}	Default Y value output in freerun mode
0x0D	Default Value C	DEF_C[7:0]; default value is C; the Cr and Cb default values are defined in this register	0	1	1	1	1	1	0	0	Cr[3:0] = {DEF_C[7:4]}, Cb[3:0] = {DEF_C[3:0]}	Default Cb/Cr value output in freerun mode; default values give blue screen output
0x0E	ADI Control 1	Reserved				0	0	0	0	0	Sets as default	
		SUB_USR_EN[1:0]; enables user to access the interrupt/VDP map and User Sub Map 2		0	0						Accesses main register space	See Figure 48
				0	1						Accesses interrupt/VDP register space	
				1	0						Accesses User Sub Map 2	
		Reserved	0								Sets as default	
0x0F	Power management	Reserved							0	0	Sets to default	
		Reserved				0	0				Sets to default	
		PWRDWN; power-down places the decoder into a full power-down mode			0						System functional	
					1						Powered down	
		Reserved		0							Sets to default	
		Reset; chip reset, loads all I²C bits with default values	0								Normal operation	
			1								Starts reset sequence	Executing reset takes approximately 2 ms; this bit is self clearing
0x10	Status 1 (read only)	IN_LOCK								x	1 = in lock (now)	Provides info about the internal status of the decoder
		LOST_LOCK							x		1 = lost lock (since last read)	
		FSC_LOCK						x			1 = f_{SC} lock (now)	
		FOLLOW_PW					x				1 = peak white AGC mode active	
		AD_RESULT[2:0]; autodetection result reports the standard of the input video		0	0	0					NTSC M/NTSC J	Detected standard
				0	0	1					NTSC 4.43	
				0	1	0					PAL M	
				0	1	1					PAL 60	
				1	0	0					PAL B/PAL G/PAL H/PAL I/PAL D	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL	x								1 = color kill is active	Color kill
0x11	IDENT (read only)	IDENT[7:0]; provides ID on the revision of the device	0	1	0	0	0	0	0	1		Power-up value = 0x41
0x12	Status 2 (read only)	MVCS DET								x	MV color striping detected	1 = detected
		MVCS T3							x		MV color striping type	0 = Type 2, 1 = Type 3
		MV PS DET						x			MV pseudosync detected	1 = detected
		MV AGC DET					x				MV AGC pulses detected	1 = detected
		LL NSTD				x					Nonstandard line length	1 = detected
		FSC NSTD			x						f_{SC} frequency nonstandard	1 = detected
		Reserved	x	x								

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x13	Status 3 (read only)	INST_HLOCK								x	1 = horizontal lock achieved	Unfiltered
		Reserved							x		Reserved	
		SD_OP_50Hz						0			SD 60 Hz detected	SD field rate detect
								1			SD 50 Hz detected	
		Reserved					x					
		FREE_RUN_ACT				x					1 = freerun mode active	
		STD FLD LEN			x						1 = field length standard	Correct field length found
		Interlaced		x							1 = interlaced video detected	Field sequence found
		PAL_SW_LOCK	x								1 = swinging burst detected	Reliable swinging burst sequence
0x14	Analog clamp control	FREE_RUN_PAT_SEL[2:0]						0	0	0	Single color set by DEF_C and DEF_Y; see the Color Control Registers section	
								0	0	1	100% color bars	
								0	1	0	Luma ramp	
								1	0	1	Boundary box	
		Reserved					0				Sets to default	
		CCLEN; current clamp enable allows the user to switch off the current sources in the analog front				0					Current sources switched off	
						1					Current sources enabled	
		Reserved	0	0	0						Sets to default	
0x15	Digital Clamp Control 1	Reserved					x	x	x	x	Sets to default	
		DCFE; digital clamp freeze enable				0					Digital clamp on	
						1					Digital clamp off	
		DCT[1:0]; digital clamp timing determines the time constant of the digital fine clamp circuitry		0	0						Slow (TC = 1 sec)	
				0	1						Medium (TC = 0.5 sec)	
				1	0						Fast (TC = 0.1 sec)	
				1	1						TC dependent on video	
		Reserved	0								Set to default	
0x17	Shaping Filter Control 1	YSFM[4:0]; selects Y shaping filter mode in CVBS only mode; allows the user to select a wide range of low-pass or notch filters; if either autowide or autonarrow mode is selected, the decoder selects the optimum Y filter, depending on the CVBS video source quality (good vs. poor)				0	0	0	0	0	Autowide notch for poor quality sources or wideband filter with comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality
						0	0	0	0	1	Autonarrow notch for poor quality sources or wideband filter with comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected, the decoder does not change filter modes; depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	PAL NN1	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN1	
						1	1	0	0	0	PAL WN2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	
		CSFM[2:0]: C shaping filter mode allows selection from a range of low-pass chrominance filters; if either auto mode is selected, the decoder selects the optimum C filter depending on the CVBS video source quality (good vs. bad); nonauto settings force a C filter for all standards and quality of CVBS video	0	0	0						Autoselection 1.5 MHz	Automatically selects a C filter based on video standard and quality
			0	0	1						Autoselection 2.17 MHz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wideband mode	
0x18	Shaping Filter Control 2	WYSFM[4:0]; wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPrPb, B/W input signals; it is also used when a good quality input CVBS signal is detected; for all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0]				0	0	0	0	0	Reserved, do not use	
						0	0	0	0	1	Reserved, do not use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved, do not use	
						~	~	~	~	~	Reserved, do not use	
						1	1	1	1	1	Reserved, do not use	
		Reserved		0	0						Set to default	
		WYSFMOVR; enables use of the automatic WYSFM filter	0								Autoselection of best filter	
			1								Manual select filter using WYSFM[4:0]	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x19	Comb filter control	PSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1						
0x1D	ADI Control 2	Reserved			0	0	0	x	x	x		
		Reserved		1								
		TRI_LLC; tristate LLC driver	0								LLC pin active	
			1								LLC pin tristated	
0x27	Pixel delay control	LTA[1:0]; luma timing adjust allows the user to specify a timing difference between chroma and luma samples							0	0	No delay	CVBS mode, LTA[1:0] = 00b, Y/C mode, LTA[1:0] = 01b, YPrPb mode, LTA[1:0] = 01b
									0	1	Luma one clock (37 ns) late	
									1	0	Luma two clocks (74 ns) early	
									1	1	Luma one clock (37 ns) early	
		Reserved						0			Sets to 0	
		CTA[2:0]; chroma timing adjust allows a specified timing difference between the luma and chroma samples			0	0	0				Reserved	CVBS mode CTA[2:0] = 011b, Y/C mode, CTA[2:0] = 101b, YPrPb mode, CTA[2:0] = 110b
					0	0	1				Chroma + two pixels (early)	
					0	1	0				Chroma + one pixel (early)	
					0	1	1				No delay	
					1	0	0				Chroma – one pixel (late)	
					1	0	1				Chroma – two pixels (late)	
					1	1	0				Chroma – three pixels (late)	
					1	1	1				Reserved	
		AUTO_PDC_EN; automatic programmed delay control. automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma	
				1							LTA and CTA values determined automatically	
		SWPC; allows the Cr and Cb samples to be swapped	0								No swapping	
			1								Swaps the Cr and Cb output samples	
0x2B	Misc gain control	PW_UPD; peak white update determines the rate of gain								0	Updates once per video line	Peak white must be enabled; see LAGC[2:0]
										1	Updates once per field	
		Reserved			1	0	0	0	0		Sets to default	
		CKE; color kill enable allows the color kill function to be switched on and off		0							Color kill disabled	For SECAM color kill, the threshold is set at 8%; see CKILLTHR[2:0]
				1							Color kill enabled	
		Reserved	1								Sets to default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x2C	AGC mode control	CAGC[1:0]; chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path							0	0	Manual fixed gain	Use CMG[11:0]
									0	1	Uses luma gain for chroma	
									1	0	Automatic gain	Based on color burst
									1	1	Freeze chroma gain	
		Reserved					1	1			Sets to 1	
		LAGC[2:0]; luma automatic gain control selects the mode of operation for the gain control in the luma path		0	0	0					Manual fixed gain	Uses LMG[11:0]
				0	0	1					AGC peak white algorithm off	Blank level to sync tip
				0	1	0					AGC peak white algorithm on	Blank level to sync tip
				0	1	1					Reserved	
				1	0	0					Reserved	
				1	0	1					Reserved	
				1	1	0					Reserved	
				1	1	1					Freeze gain	
		Reserved	1								Sets to 1	
0x2D	Chroma Gain Control 1, Chroma Gain 1 (CG)	CMG[11:8]/CG[11:8]; in manual mode, the chroma gain control can be used to program a desired manual chroma gain; in auto mode, it can be used to read back the current gain value					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates
		Reserved			1	1					Set to 1	Has an effect only if CAGC[1:0] is set to autogain (10)
		CAGT[1:0]; chroma automatic gain timing allows adjustment of the chroma AGC tracking speed	0	0							Slow (TC = 2 sec)	
			0	1							Medium (TC = 1 sec)	
			1	0							Reserved	
			1	1							Adaptive	
0x2E	Chroma Gain Control 2, Chroma Gain 2 (CG)	CMG[7:0]/CG[7:0]; chroma manual gain lower eight bits; see CMG[11:8]/CG[11:8] for description	0	0	0	0	0	0	0	0	CMG[11:0] = see the CMG section	Minimum value = 0d, maximum value = 4095d
0x2F	Luma Gain Control 1, Luma Gain 1 (LG)	LMG[11:8]/LG[11:8]; in manual mode, luma gain control can be used to program a desired manual luma gain; in auto mode, it can be used to read back the actual gain value used					x	x	x	x	LAGC[1:0] settings decide in which mode LMG[11:0] operates	
		Reserved			1	1					Sets to 1	
		LAGT[1:0]; luma automatic gain timing allows adjustment of the luma AGC tracking speed	0	0							Slow (TC = 2 sec)	Has an effect only if LAGC[1:0] is set to autogain (001, 010)
			0	1							Medium (TC = 1 sec)	
			1	0							Fast (TC = 0.2 sec)	
			1	1							Adaptive	
0x30	Luma Gain Control 2, Luma Gain 2 (LG)	LMG[7:0]/LG[7:0]; luma manual gain/ luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	x	x	x	x	x	x	x	x	LMG[7:0]/LG[7:0]; luma manual gain/luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	Minimum value = 1024d, Maximum value = 4095d
0x31	VS/FIELD Control 1	Reserved						0	1	0	Sets to default	
		HVSTIM; horizontal VSYNC timing; selects where within a line of video the VSYNC signal is asserted					0				Start of line relative to HSE	HSE = HSYNC end
							1				Start of line relative to HSB	HSB = HSYNC begin
		NEWAVMODE; sets the EAV/SAV mode				0					EAV/SAV codes generated to suit Analog Devices encoders	
						1					Manual VS/FIELD position controlled by the Register 0x32, Register 0x33, and Register 0xE5 to Register 0xEA	
		Reserved	0	0	0						Sets to default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x32	VS/FIELD Control 2	Reserved			0	0	0	0	0	1	Sets to default	NEWAVMODE bit must be set high
		VSBHE		0							VSYNC signal goes high in the middle of the line (even field)	
				1							VSYNC signal changes state at the start of the line (even field)	
		VSBHO	0								VSYNC signal goes high in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line (odd field)	
0x33	VS/FIELD Control 3	Reserved			0	0	0	1	0	0	Sets to default	
		VSEHE		0							VSYNC signal goes low in the middle of the line (even field)	NEWAVMODE bit must be set high
				1							VSYNC signal changes state at the start of the line (even field)	
		VSEHO	0								VSYNC signal goes low in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line odd field	
0x34	HS Position Control 1	HSE[10:8]; HSYNC end allows positioning of the HSYNC output within the video line						0	0	0	HSYNC output ends HSE[10:0] pixels after the falling edge of HSYNC	Using HSB and HSE, the position/length of the output HSYNC can be programmed
		Reserved					0				Sets to 0	
		HSB[10:8]; HSYNC begin allows positioning of the HSYNC output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSYNC	
		Reserved	0								Sets to 0	
0x35	HS Position Control 2	HSB[7:0]; see Address 0x34, using HSB[10:0] and HSE[10:0], users can program the position and length of the HSYNC output signal	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	HSE[7:0]; see Address 0x35 description	0	0	0	0	0	0	0	0		

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x37	Polarity	PCLK; sets polarity of LLC								0	Inverts polarity	
										1	Normal polarity as per the timing diagrams	
		Reserved						0	0		Set to 0	
		PF; sets the FIELD polarity					0					
							1					
		Reserved				0						
		PVS; sets the VSYNC polarity			0						Active high	
					1						Active low	
		Reserved		0							Sets to 0	
		PHS; sets HSYNC polarity	0		0						Active high	
			1		1						Active low	
0x38	NTSC comb control	YCMN[2:0]; luma comb mode, NTSC						0	0	0	Adaptive three-line, three-tap luma comb	
								1	0	0	Uses low-pass/notch filter	
								1	0	1	Fixed luma comb two-line (two taps)	Top lines of memory
								1	1	0	Fixed luma comb three-line (three taps)	All lines of memory
								1	1	1	Fixed luma comb two-line (two taps)	Bottom lines of memory
		CCMN[2:0]; chroma comb mode, NTSC			0	0	0				Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN= 10, five-line adaptive for CTAPSN = 11	
					1	0	0				Disables chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSN[1:0]; chroma comb taps, NTSC	0	0							Not used	
			0	1							Adapts three lines to two lines	
			1	0							Adapts five lines to three lines	
			1	1							Adapts five lines to four lines	
0x39	PAL comb control	YCMP[2:0]; luma comb mode, PAL						0	0	0	Adaptive five-line, three-tap luma comb	
								1	0	0	Use low-pass notch filter	
								1	0	1	Fixed luma comb (three-line)	Top lines of memory
								1	1	0	Fixed luma comb (five-line)	All lines of memory
								1	1	1	Fixed luma comb (three-line)	Bottom lines of memory

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
		CCMP[2:0]; chroma comb mode, PAL			0	0	0				Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN = 10, five-line adaptive for CTAPSN = 11	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSP[1:0]; chroma comb taps, PAL	0	0							Not used	
			0	1							Adapts five lines to three lines (two taps)	
			1	0							Adapts five lines to three lines (three taps)	
			1	1							Adapts five lines to four lines (four taps)	
0x3A	ADC control	Mux power-down override								0		No control over power-down for muxes and associated channel circuit
										1		Allows power-down of MUX_0/MUX_1/ MUX_2 and associated channel circuit; when INSEL[4:0] is used, unused channels are automatically powered down
		PWRDWN_MUX_2; enables power-down of MUX_2 and associated channel clamp and buffer							0		MUX_2 and associated channel in normal operation	
									1		Power down MUX_2 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_1; enables power-down of MUX_1 and associated channel clamp and buffer						0			MUX_1 and associated channel in normal operation	
								1			Power down MUX_1 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_0; enables power-down of MUX_0 and associated channel clamp and buffer					0				MUX_0 and associated channel in normal operation	
							1				Power down MUX_0 and associated channel operation	MUX PDN override = 1
		Reserved	0	0	0	0					Sets as default	
0x3D	Manual	Reserved					0	0	1	0	Sets to default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
		CKILLTHR[2:0]; color kill threshold		0	0	0					NTSC, PAL color kill at <0.5%, SECAM no color kill	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					NTSC, PAL color kill at <1.5%, SECAM color kill at <5%	
				0	1	0					NTSC, PAL color kill at <2.5%, SECAM color kill at <7%	
				0	1	1					NTSC, PAL color kill at <4%, SECAM color kill at <8%	
				1	0	0					NTSC, PAL color kill at <8.5%, SECAM color kill at <9.5%	
				1	0	1					NTSC, PAL color kill at <16%, SECAM color kill at <15%	
				1	1	0					NTSC, PAL color kill at <32%, SECAM color kill at <32%	
				1	1	1					Reserved	
		Reserved	0								Sets to default	
0x41	Resample control	Reserved			0	0	0	0	0	1	Sets to default	
		SFL_INV; controls the behavior of the PAL switch bit		0							SFL-compatible with newer video encoders	The newer video encoders are ADV7340, ADV7341, ADV7342, ADV7343, ADV7344, ADV7390, ADV7391, ADV7392, ADV7393, ADV7171, ADV7172, ADV7173, ADV7174, ADV7177, and ADV7179. ADV7194 is an example of an older encoder.
				1							SFL-compatible with older video encoders, such as the ADV7194.	
		Reserved	0								Set to default	
0x4D	CTI DNR Control 1	CTI_EN; CTI enable								0	Disables CTI	
										1	Enables CTI	
		CTI_AB_EN; enables the mixing of the transient improved chroma with the original signal							0		Disables CTI alpha blender	
									1		Enables CTI alpha blender	
		CTI_AB[1:0]; controls the behavior of the alpha-blend circuitry					0	0			Sharpest mixing between sharpened/original chroma signal	
							0	1			Sharp mixing between sharpened and original chroma signal	
							1	0			Smooth mixing between sharpened/original chroma signal	
							1	1			Smoothest mixing between sharpened and original chroma signal	
		Reserved				0					Sets to default	
		DNR_EN; enables or bypasses the DNR block			0						Bypasses the DNR block	
					1						Enables the DNR block	
		Reserved	1	1							Sets to default	
0x4E	CTI DNR Control 2	CTI_C_TH[7:0]; specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0		
0x50	DNR Noise Threshold 1	DNR_TH[7:0]; specifies the maximum luma edge that is interpreted as noise and is therefore blanked	0	0	0	0	1	0	0	0		

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x51	Lock count	CIL[2:0]; count into lock determines the number of lines the system must remain in lock before showing a locked status						0	0	0	One line of video	
								0	0	1	Two lines of video	
								0	1	0	Five lines of video	
								0	1	1	10 lines of video	
								1	0	0	100 lines of video	
								1	0	1	500 lines of video	
								1	1	0	1000 lines of video	
								1	1	1	100,000 lines of video	
		COL[2:0]; count out of lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status			0	0	0				One line of video	
					0	0	1				Two lines of video	
					0	1	0				Five lines of video	
					0	1	1				10 lines of video	
					1	0	0				100 lines of video	
					1	0	1				500 lines of video	
					1	1	0				1000 lines of video	
					1	1	1				100,000 lines of video	
		SRLS; select raw lock signal and selects the determination of the lock status		0							Over field with vertical info	
				1							Line to line evaluation	
		FSCLE; f_{SC} lock enable	0								Lock status set only by horizontal lock	
			1								Lock status set by horizontal lock and subcarrier lock	
0x60	ADC Switch 3	MUX_3[2:0]					0	0	0	0	No connect	
							0	0	0	1	No connect	
							0	0	1	0	$A_{IN}2$	
							0	0	1	1	No connect	
							0	1	0	0	$A_{IN}4$	
		Reserved	0	0	0	1	0					
0x6A	Output Sync Select 1	HS_OUT_SEL[2:0] selects which sync comes out on the HS pin						0	0	0	HSYNC	
								0	0	1	VSYNC	
								0	1	0	FIELD	
								0	1	1	DE	
								1	0	0	SFL	
		Reserved	0	0	0	0	0					
0x6B	Output Sync Select 2	FLD_OUT_SEL[2:0] selects which sync comes out on the VS/FIELD/SFL pin						0	0	0	HSYNC	
								0	0	1	VSYNC	
								0	1	0	FIELD	
								0	1	1	DE	
								1	0	0	SFL	
		Reserved	0	0	0	1	0				Set as default	
0x8F	Freerun Line Length 1	Reserved					0	0	0	0	Set as default	
		LLC_PAD_SEL[2:0]; enables manual selection of the clock for the LLC pin		0	0	0					LLC (nominal 27 MHz) selected out on LLC pin	
				1	0	1					LLC (nominal 13.5 MHz) selected out on LLC pin	
		Reserved	0								Sets to default	
0x99	CCAP1 (read only)	CCAP1[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP1[7] contains parity bit for Byte 0	
0x9A	CCAP2 (read only)	CCAP2[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP2[7] contains parity bit for Byte 0	
0x9B	Letterbox 1 (read only)	LB_LCT[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the top of active video	This feature examines the active video at the start and end of each field; it enables format detection even if the video is not accompanied
0x9C	Letterbox 2 (read only)	LB_LCM[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected in the middle half of active video if subtitles are detected	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x9D	Letterbox 3 (read only)	LB_LCB[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the bottom of active video	
0xB2	CRC enable (write only)	Reserved							0	0	Sets as default	
		CRC_ENABLE; enable CRC checksum decoded from FMS packet to validate CGMSD						0			Turns off CRC check	
								1			CGMSD goes high with valid checksum	
		Reserved	0	0	0	1	1				Sets as default	
0xC3	ADC Switch 1	MUX_0[2:0]; manual muxing control for MUX_0; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	$A_{IN}1$	
								0	1	0	$A_{IN}2$	
								0	1	1	$A_{IN}3$	
								1	0	0	$A_{IN}4$	
		Reserved					0					
		MUX_1[2:0]; manual muxing control for MUX_1; this setting controls which input is routed to the ADC for processing		0	0	0					No connect	
				0	0	1					No connect	
				0	1	0					$A_{IN}2$	
				0	1	1					No connect	
				1	0	0					$A_{IN}4$	
		Reserved	0									
0xC4	ADC Switch 2	MUX_2[2:0]; manual muxing control for MUX_2; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	No connect	
								0	1	0	$A_{IN}2$	
								0	1	1	$A_{IN}3$	
								1	0	0	No connect	
		Reserved		0	0	0	0					
		MAN_MUX_EN; enable manual setting of input signal muxing	0								Disables	This bit must be set to 1 for manual muxing
			1								Enables	
0xDC	Letterbox Control 1	LB_TH[4:0]; sets the threshold value that determines if a line is black				0	1	1	0	0	Default threshold for the detection of black lines 01101 to 10000—increase threshold, 00000 to 01011—decrease threshold	
		Reserved	1	0	1						Sets as default	
0xDD	Letterbox Control 2	LB_EL[3:0]; programs the end line of the activity window for LB detection (end of field)					1	1	0	0	LB detection ends with the last line of active video on a field, 1100b: 262/525	
		LB_SL[3:0]; programs the start line of the activity window for LB detection (start of field)	1	1	0	0					Letterbox detection aligned with the start of active video, 0100b: 23/286 NTSC	
0xDE	ST Noise Readback 1 (read only)	ST_NOISE[10:8]						x	x	x		ST noise[10:0] measures the noise on the horizontal sync tip of video source
		ST_NOISE_VLD					x				When = 1, ST_NOISE[10:0] is valid	
0xDF	ST Noise Readback 2 (read only)	ST_NOISE[7:0]	x	x	x	x	x	x	x	x		
0xE1	SD offset Cb channel	SD_OFF_Cb[7:0]; adjusts the hue by selecting the offset for the Cb channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cb channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cb channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cb channel	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xE2	SD offset Cr channel	SD_OFF_Cr[7:0]; adjusts the hue by selecting the offset for the Cr channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cr channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cr channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cr channel	
0xE3	SD saturation Cb channel	SD_SAT_Cb[7:0]; adjusts the saturation by affecting gain on the Cb channel	0	0	0	0	0	0	0	0	Gain on Cb channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB	
0xE4	SD saturation Cr channel	SD_SAT_Cr[7:0]; adjusts the saturation by affecting gain on the Cr channel	0	0	0	0	0	0	0	0	Gain on Cr channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cr channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cr channel = +6 dB	
0xE5	NTSC VSYNC begin	NVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	NTSC default (ITU-R BT.656)	
		NVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE; delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		NVBEGDELO; delay V bit going high by one line relative to NVBEG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE6	NTSC VSYNC end	NVEND[4:0]; number of lines after I_{COUNT} rollover to set V low				0	0	1	0	0	NTSC default (ITU-R BT.656)	
		NVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE; delay V bit going low by one line relative to NVEND (even field)		0							No delay	
				1							Additional delay by one line	
		NVENDDELO; delay V bit going low by one line relative to NVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xE7	NTSC FIELD toggle	NFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	NTSC default	
		NFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE; delay F transition by one line relative to NFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		NFTOGDELO; delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE8	PAL VSYNC begin	PVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	PAL default (ITU-R BT.656)	
		PVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE; delay V bit going high by one line relative to PVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		PVBEGDELO; delay V bit going high by one line relative to PVBEG (odd field)	0								No delay	
			1								Additional delay by one line	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0xE9	PAL VSYNC end	PVEND[4:0]; number of lines after I_{COUNT} rollover to set V low.				1	0	1	0	0	PAL default (ITU-R BT.656)	
		PVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE; delay V bit going low by one line relative to PVEND (even field)		0							No delay	
				1							Additional delay by one line	
		PVENDDELO; delay V bit going low by one line relative to PVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xEA	PAL FIELD toggle	PFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	PAL default (ITU-R BT.656)	
		PFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE; delay F transition by one line relative to PFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		PFTOGDELO; delay F transition by one line relative to PFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xEB	VBLANK Control 1	PVBIELCM[1:0]; PAL VBI even field line control							0	0	VBI ends one line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant (Line 336)	
									1	0	VBI ends one line later (Line 337)	
									1	1	VBI ends two lines later (Line 338)	
		PVBIOLCM[1:0]; PAL VBI odd field line control					0	0			VBI ends one line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on odd field in PAL
							0	1			ITU-R BT.470 compliant (Line 23)	
							1	0			VBI ends one line later (Line 24)	
							1	1			VBI ends two lines later (Line 25)	
		NVBIELCM[1:0]; NTSC VBI even field line control			0	0					VBI ends one line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on even field in NTSC
					0	1					ITU-R BT.470 compliant (Line 283)	
					1	0					VBI ends one line later (Line 284)	
					1	1					VBI ends two lines later (Line 285)	
		NVBIOLCM[1:0]; NTSC VBI odd field line control	0	0							VBI ends one line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant (Line 21)	
			1	0							VBI ends one line later (Line 22)	
			1	1							VBI ends two lines later (Line 23)	
0xEC	VBLANK Control 2	PVBIECCM[1:0]; PAL VBI even field color control							0	0	Color output beginning Line 335	Controls the position of first line that outputs color after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant color output beginning Line 336	
									1	0	Color output beginning Line 337	
									1	1	Color output beginning Line 338	
		PVBIOCCM[1:0]; PAL VBI odd field color control					0	0			Color output beginning Line 22	Controls the position of first line that outputs color after VBI on odd field in PAL
							0	1			ITU-R BT.470-compliant color output beginning Line 23	
							1	0			Color output beginning Line 24	
							1	1			Color output beginning Line 25	
		NVBIECCM[1:0]; NTSC VBI even field color control			0	0					Color output beginning Line 282	Controls the position of first line that outputs color after VBI on even field in NTSC
					0	1					ITU-R BT.470-compliant color output beginning Line 283	
					1	0					VBI ends one line later (Line 284)	
					1	1					Color output beginning Line 285	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
		NVBIOCCM[1:0]; NTSC VBI odd field color control	0	0							Color output beginning Line 20	Controls the position of first line that outputs color after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant color output beginning Line 21	
			1	0							Color output beginning Line 22	
			1	1							Color output beginning Line 23	
0xF3	AFE_ CONTROL 1	AA_FILT_EN[3:0] antialiasing filter enable								0	Antialiasing Filter 1 disabled	AA_FILT_MAN_OVR must be enabled to change settings defined by INSEL[4:0]
										1	Antialiasing Filter 1 enabled	
									0		Antialiasing Filter 2 disabled	
									1		Antialiasing Filter 2 enabled	
								0			Antialiasing Filter 3 disabled	
								1			Antialiasing Filter 3 enabled	
							0				Antialiasing Filter 4 enabled	
							1				Antialiasing Filter 4 enabled	
		AA_FILT_MAN_OVR; antialiasing filter override				0					Override disabled	
						1					Override enabled	
		Reserved	0	0	0							
0xF4	Drive strength	DR_STR_S[1:0]; selects the drive strength for the sync output signals							0	0	Low drive strength (1×)	
									0	1	Medium low drive strength (2×)	
									1	0	Medium high drive strength (3×)	
									1	1	High drive strength (4×)	
		DR_STR_C[1:0]; selects the drive strength for the clock output signal					0	0			Low drive strength (1×)	
							0	1			Medium low drive strength (2×)	
							1	0			Medium high drive strength (3×)	
							1	1			High drive strength (4×)	
		DR_STR[1:0]; selects the drive strength for the data output signals; can be increased or decreased for EMC or crosstalk reasons			0	0					Low drive strength (1×)	
					0	1					Medium low drive strength (2×)	
					1	0					Medium high drive strength (3×)	
					1	1					High drive strength (4×)	
		Reserved		x								
		GLITCH_FILT_BYP	0									
			1									
0xF8	IF comp control	IFFILTSEL[2:0]; IF filter selection for PAL and NTSC						0	0	0	Bypass mode	0 dB
											2 MHz NTSC filters	
								0	0	1	−3 dB	
								0	1	0	−6 dB	
								0	1	1	−10 dB	
								1	0	0	Reserved	
											3 MHz PAL filters	
								1	0	1	−2 dB	
								1	1	0	−5 dB	
								1	1	1	−7 dB	
		Reserved	0	0	0	0	0					
0xF9	VS mode control	EXTEND_VS_MAX_FREQ								0	Limits maximum VSYNC frequency to 66.25 Hz (475 lines/frame)	
										1	Limits maximum VSYNC frequency to 70.09 Hz (449 lines/frame)	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
		EXTEND_VS_MIN_FREQ							0		Limits minimum VSYNC frequency to 42.75 Hz (731 lines/frame)	
									1		Limits minimum VSYNC frequency to 39.51 Hz (791 lines/frame)	
		VS_COAST_MODE[1:0]					0	0			Autocoast mode	This value forces the video standard output during freerun mode
							0	1			576i 50 Hz coast mode	
							1	0			480i 60 Hz coast mode	
							1	1			Reserved	
		Reserved	0	0	0	0						
0xFB	Peaking gain	PEAKING_GAIN[7:0]	0	1	0	0	0	0	0	0	Increases/decreases the gain for high frequency portions of the video signal	
0xFC	DNR Noise Threshold 2	DNR_TH2[7:0]	0	0	0	0	0	1	0	0	Specifies the maximum luma edge that is interpreted as noise and therefore blanked	

[1] x indicates a bit that keeps the last written value.

To access the registers listed in Table 97, SUB_USR_EN in Register Address 0x0E must be programmed to 10b. The gray shading is the default.

Table 97. Register Map Descriptions User Sub Map 2

User Sub Map 2			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x80	ACE Control 1	Reserved		0	0	0	0	0	0	0	Reserved.	
		ACE_ENABLE	0								Disable ACE.	
			1								Enable ACE.	
0x83	ACE Control 4	ACE_LUMA_GAIN[4:0]				0	1	1	0	1	Set ACE luma autocontrast level to default value. 5b'00000 minimum value … 5b'11111 maximum value	When ACE_ ENABLE is set to 1
		Reserved	0	0	0							
0x84	ACE Control 5	ACE_CHROMA_GAIN[3:0]					1	0	0	0	Set ACE color auto-saturation level 4b'0000 minimum value … 4b'1111 maximum value	
		ACE_CHROMA_MAX[3:0]	1	0	0	0					Set maximum threshold for ACE color color saturation level 4b'0000 = minimum value … 4b'1111 = maximum value	
0x85	ACE Control 6	ACE_GAMMA_GAIN[3:0]					1	0	0	0	Set further contrast enhancement 4b'0000 = minimum value … 4b'1111 = maximum value	
		ACE_RESPONSE_SPEED[3:0]	1	1	1	1					Sets speed of ACE response 4b'0000 slowest value … 4b'1111 fastest value	
0x92	Dither control	BR_DITHER_MODE								0	8-bit to 6-bit downdither disabled	
										1	8-bit to 6-bit downdither enabled	
		Reserved	0	0	0	0	0	0	0			

User Sub Map 2			Bits (Shading Indicates Default State)									
Subaddress	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0xD9	Min Max 0	MIN_THRESH_Y[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming luma video signal.	
0xDA	Min Max 1	MAX_THRESH_Y[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming luma video signal.	
0xDB	Min Max 2	MIN_THRESH_C[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming chroma video signal.	
0xDC	Min Max 3	MAX_THRESH_C[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming chroma video signal.	
0xDD	Min Max 4	MAX_SAMPLES_ ALLOWED_Y[3:0]					1	1	0	0	Selects the number of maximum luma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ ALLOWED_Y[3:0]	1	1	0	0					Selects the number of minimum luma samples allowed in a given window before an interrupt is triggered.	
0xDE	Min Max 5	MAX_SAMPLES_ ALLOWED_C[3:0]					1	1	0	0	Selects the number of maximum chroma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ ALLOWED_C[3:0]	1	1	0	0					Selects the number of minimum chroma samples allowed in a given window before an interrupt is triggered.	
0xE0	FL Control	FL_ENABLE								0		
										1	Enables fast lock.	
		Reserved	0	0	0	0	0	0	0			
0xE1	Y Average 0	LINE_START[8:1]	0	0	0	1	0	0	0	1	Selects starting line for field averaging.	See Subaddress 0xE5 for least significant bits
0xE2	Y Average 1	LINE_END[8:1]	1	0	0	0	1	0	0	0	Selects end line for field averaging.	
0xE3	Y Average 2	SAMPLE_START[9:2]	0	0	0	1	0	1	1	1	Selects starting sample for line averaging.	
0xE4	Y Average 3	SAMPLE_END[9:2]	1	1	0	1	0	1	1	1	Selects end sample for line averaging.	
0xE5	Y Average 4	LINE_START[0]								1		
		LINE_END[0]							1			
		Reserved					0	0				
		SAMPLE_START[1:0]			1	0						
		SAMPLE_END[1:0]	0	0								
0xE6	Y Average 5	CAPTURE_VALUE								0	Trigger used to store the readback value.	
		Y_AVG_FILT_EN							0		Enable low pass filtering of the y_averaged signal.	
		Y_AVG_TIME_CONST[2:0]				1	0	0			Selects the filter cutoff to be used for filtering the y averaged data. 3'b1xx = least filtered. 3'b000 = next least. … 3'b011 = heavily filtered.	
		Reserved	0	0	0							
0xE7	Y Average Data MSB	Y_AVERAGE[9:2]	x	x	x	x	x	x	x	x	Contains the averaged video data.	Note these are read only registers
0xE8	Y Average Data LSB	Y_AVERAGE[1:0]							x	x		

To access the registers listed in Table 98, SUB_USR_EN in Register Address 0x0E must be programmed to 01b. The gray shading is the default.

Table 98. Interrupt/VDP Map Descriptions[1]

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x40	Interrupt Configuration 1	INTRQ_OP_SEL[1:0]; interrupt drive level select							0	0	Open drain	
									0	1	Drive low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INTRQ; manual interrupt set mode						0			Manual interrupt mode disabled	
								1			Manual interrupt mode enabled	
		Reserved					x				Not used	
		MV_INTRQ_SEL[1:0]; Rovi interrupt select			0	0					Reserved	
					0	1					Pseudo sync only	
					1	0					Color stripe only	
					1	1					Pseudo sync or color stripe	
		INTRQ_DUR_SEL[1:0]; interrupt duration select	0	0							Three XTAL periods	
			0	1							15 XTAL periods	
			1	0							63 XTAL periods	
			1	1							Active until cleared	
0x42	Interrupt Status 1 (read only)	SD_LOCK_Q								0	No change	These bits can be cleared or masked in Register 0x43 and Register 0x44, respectively
										1	SD input has caused the decoder to go from an unlocked state to a locked state	
		SD_UNLOCK_Q							0		No change	
									1		SD input has caused the decoder to go from a locked state to an unlocked state	
		Reserved				x	x	x				
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the freerun status	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync/color striping detected; see Register 0x40, MV_INTRQ_SEL[1:0], for selection	
		Reserved	x									
0x43	Interrupt Clear 1 (write only)	SD_LOCK_CLR								0	Do not clear	
										1	Clears SD_LOCK_Q bit	
		SD_UNLOCK_CLR							0		Do not clear	
									1		Clears SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		SD_FR_CHNG_CLR			0						Do not clear	
					1						Clears SD_FR_CHNG_Q bit	
		MV_PS_CS_CLR		0							Do not clear	
				1							Clears MV_PS_CS_Q bit	
		Reserved	x								Not used	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x44	Interrupt Mask 1 (read/write)	$\overline{\text{SD\_LOCK\_MSK}}$								0	Masks SD_LOCK_Q bit	
										1	Unmasks SD_LOCK_Q bit	
		$\overline{\text{SD\_UNLOCK\_MSK}}$							0		Masks SD_UNLOCK_Q bit	
									1		Unmasks SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		$\overline{\text{SD\_FR\_CHNG\_MSK}}$			0						Masks SD_FR_CHNG_Q bit	
					1						Unmasks SD_FR_CHNG_Q bit	
		$\overline{\text{MV\_PS\_CS\_MSK}}$		0							Masks MV_PS_CS_Q bit	
				1							Unmasks MV_PS_CS_Q bit	
		Reserved	x								Not used	
0x45	Raw Status 2 (read only)	CCAPD								0	No CCAPD data detected—VBI System 2	These bits are status bits only; they cannot be cleared or masked; Register 0x46 is used for this purpose
										1	CCAPD data detected—VBI System 2	
		Reserved					x	x	x			
		EVEN_FIELD				0					Current SD field is odd numbered	
						1					Current SD field is even numbered	
		CHX_MIN_MAX_INTRQ			0						If the input to the ADC is within the correct range this is 0	
					1						If the input to the ADC is outside the range this is set to 1. The range is set by User Sub Map 2	
		Reserved		x							Not used	
		MPU_STIM_INTRQ	0								MPU_STIM_INTRQ = 0	
			1								MPU_STIM_INTRQ = 1	
0x46	Interrupt Status 2 (read only)	CCAPD_Q								0	Closed captioning not detected in the input video signal—VBI System 2	These bits can be cleared or masked by Register 0x47 and Register 0x48, respectively; note that the interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Closed captioning data detected in the video input signal—VBI System 2	
		Reserved							x		Not used	
		Reserved					x	x			Not used	
		SD_FIELD_CHNGD_Q				0					SD signal has not changed field from odd to even or vice versa	
						1					SD signal has changed field from odd to even or vice versa	
		Reserved		x	x						Not used	
		MPU_STIM_INTRQ_Q	0								Manual interrupt not set	
			1								Manual interrupt set	
0x47	Interrupt Clear 2 (write only)	CCAPD_CLR								0	Do not clear—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Clears CCAPD_Q bit—VBI System 2	
		Reserved							x		Not used	
		Reserved					x	x				
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q bit	
		CHX_MIN_MAX_INTRQ_CLR			0						Do not clear	
					1						Clears CHX_MIN_MAX_INTRQ bit	
		Reserved		x							Not used	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
		MPU_STIM_INTRQ_CLR	0								Do not clear	
			1								Clears MPU_STIM_INTRQ_Q bit	
0x48	Interrupt Mask 2 (read/write)	$\overline{\text{CCAPD\_MSK}}$								0	Masks CCAPD_Q bit—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Unmasks CCAPD_Q bit—VBI System 2	
		Reserved							0		Not used	
		Reserved					0	0			Not used	
		$\overline{\text{SD\_FIELD\_CHNGD\_MSK}}$				0					Masks SD_FIELD_CHNGD_Q bit	
						1					Unmasks SD_FIELD_CHNGD_Q bit	
		$\overline{\text{CHX\_MIN\_MAX\_INTRQ\_MSKB}}$			0						Masks CHX_MIN_MAX_INTRQ bit	
					1						Unmasks CHX_MIN_MAX_INTRQ bit	
		Reserved		0							Not used	
		$\overline{\text{MPU\_STIM\_INTRQ\_MSK}}$	0								Masks MPU_STIM_INTRQ_Q bit	
			1								Unmasks MPU_STIM_INTRQ_Q bit	
0x49	Raw Status 3 (read only)	SD_OP_50Hz; SD 60 Hz/50 Hz frame rate at output								0	SD 60 Hz signal output	These bits are status bits only; they cannot be cleared or masked; Register 0x4A is used for this purpose
										1	SD 50 Hz signal output	
		SD_V_LOCK							0		SD vertical sync lock is not established	
									1		SD vertical sync lock established	
		SD_H_LOCK						0			SD horizontal sync lock is not established	
								1			SD horizontal sync lock established	
		Reserved					x				Not used	
		SCM_LOCK				0					SECAM lock is not established	
						1					SECAM lock established	
		Reserved	x	x	x						Not used	
0x4A	Interrupt Status 3 (read only)	SD_OP_CHNG_Q; SD 60 Hz/50 Hz frame rate at output								0	No change in SD signal standard detected at the output	These bits can be cleared and masked by Register 0x4B and Register 0x4C, respectively
										1	A change in SD signal standard is detected at the output	
		SD_V_LOCK_CHNG_Q							0		No change in SD VSYNC lock status	
									1		SD VSYNC lock status has changed	
		SD_H_LOCK_CHNG_Q						0			No change in HSYNC lock status	
								1			SD HSYNC lock status has changed	
		SD_AD_CHNG_Q; SD autodetect changed					0				No change in AD_RESULT[2:0] bits in Status 1 register	
							1				AD_RESULT[2:0] bits in Status 1 register have changed	
		SCM_LOCK_CHNG_Q; SECAM lock				0					No change in SECAM lock status	
						1					SECAM lock status has changed	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
		PAL_SW_LK_CHNG_Q			0						No change in PAL swinging burst lock status	
					1						PAL swinging burst lock status has changed	
		Reserved	x	x							Not used	
0x4B	Interrupt Clear 3 (write only)	SD_OP_CHNG_CLR								0	Do not clear	
										1	Clears SD_OP_CHNG_Q bit	
		SD_V_LOCK_CHNG_CLR							0		Do not clear	
									1		Clears SD_V_LOCK_CHNG_Q bit	
		SD_H_LOCK_CHNG_CLR						0			Do not clear	
								1			Clears SD_H_LOCK_CHNG_Q bit	
		SD_AD_CHNG_CLR					0				Do not clear	
							1				Clears SD_AD_CHNG_Q bit	
		SCM_LOCK_CHNG_CLR				0					Do not clear	
						1					Clears SCM_LOCK_CHNG_Q bit	
		PAL_SW_LK_CHNG_CLR			0						Do not clear	
					1						Clears PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	
0x4C	Interrupt Mask 3 (read/write)	$\overline{\text{SD\_OP\_CHNG\_MSK}}$								0	Masks SD_OP_CHNG_Q bit	
										1	Unmasks SD_OP_CHNG_Q bit	
		$\overline{\text{SD\_V\_LOCK\_CHNG\_MSK}}$							0		Masks SD_V_LOCK_CHNG_Q bit	
									1		Unmasks SD_V_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_H\_LOCK\_CHNG\_MSK}}$						0			Masks SD_H_LOCK_CHNG_Q bit	
								1			Unmasks SD_H_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_AD\_CHNG\_MSK}}$					0				Masks SD_AD_CHNG_Q bit	
							1				Unmasks SD_AD_CHNG_Q bit	
		$\overline{\text{SCM\_LOCK\_CHNG\_MSK}}$				0					Masks SCM_LOCK_CHNG_Q bit	
						1					Unmasks SCM_LOCK_CHNG_Q bit	
		$\overline{\text{PAL\_SW\_LK\_CHNG\_MSK}}$			0						Masks PAL_SW_LK_CHNG_Q bit	
					1						Unmasks PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x4E	Interrupt Status 4 (read only)	VDP_CCAPD_Q								0	Closed captioning not detected	These bits can be cleared and masked by Register 0x4F and Register 0x50, respectively; note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Closed captioning detected	
		Reserved							x			
		VDP_CGMS_WSS_CHNGD_Q; see Address 0x9C, Bit 4, of the user sub map to determine whether interrupt is issued for a change in detected data or for when data is detected, regardless of content						0			CGMS/WSS data is not changed/not available	
								1			CGMS/WSS data is changed/available	
		Reserved					x					
		Reserved				x						
		Reserved			x							
		Reserved		x								
		Reserved	x									
0x4F	Interrupt Clear 4 (write only)	VDP_CCAPD_CLR								0	Do not clear	In Register 0x4E, CCAP/CGMS/WSS data uses VDP data slicer
										1	Clears VDP_CCAPD_Q	
		Reserved							0			
		VDP_CGMS_WSS_CHNGD_CLR						0			Do not clear	
								1			Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0							Do not clear	
		Reserved	0									
		VDP_CCAPD_CLR								0	Do not clear	
0x50	Interrupt Mask 4	VDP_CCAPD_MSK								0	Masks VDP_CCAPD_Q	Note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Unmasks VDP_CCAPD_Q	
		Reserved							0			
		VDP_CGMS_WSS_CHNGD_MSK						0			Masks VDP_CGMS_WSS_CHNGD_Q	
								1			Unmasks VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0								
		Reserved	0									
0x51	Interrupt Latch 0 (read only)	CR_CHANNEL_MAX_VIOLATION								0	Cr value is below programmed maximum value	This register is cleared by CHX_MIN_MAX_INTRQ_CLR
										1	Cr value is above programmed maximum value	
		CR_CHANNEL_MIN_VIOLATION							0		Cr value is above programmed minimum value	
									1		Cr value is below programmed minimum value	
		CB_CHANNEL_MAX_VIOLATION						0			Cb value is below programmed maximum value	
								1			Cb value is above programmed maximum value	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
		CB_CHANNEL_MIN_VIOLATION					0				Cb value is above programmed minimum value	
							1				Cb value is below programmed minimum value	
		Y_CHANNEL_MAX_VIOLATION				0					Y value is below programmed maximum value	
						1					Y value is above programmed maximum value	
		Y_CHANNEL_MIN_VIOLATION			0						Y value is above programmed minimum value	
					1						Y value is below programmed minimum value	
		Reserved	0	0								

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x60	VDP_CONFIG_1	VDP_TTXT_TYPE_MAN[1:0]							0	0	PAL: Teletext-ITU-BT.653-625/50-A, NTSC: reserved	
									0	1	PAL: Teletext-ITU-BT.653-625/50-B (WST), NTSC: Teletext-ITU-BT.653-525/60-B	
									1	0	PAL: Teletext-ITU-BT.653-625/50-C, NTSC: Teletext-ITU-BT.653-525/60-C, or EIA516 (NABTS)	
									1	1	PAL: Teletext-ITU-BT.653-625/50-D, NTSC: Teletext-ITU-BT.653-525/60-D	
		VDP_TTXT_TYPE_MAN_ENABLE						0			User programming of teletext type disabled	
								1			User programming of teletext type enabled	
		WST_PKT_DECODE_DISABLE					0				Enables hamming decoding of WST packets	
							1				Disables hamming decoding of WST packets	
		Reserved	1	0	0	0						
0x62	VDP_ADF_CONFIG_1	ADF_DID[4:0]				1	0	1	0	1	User-specified DID sent in the ancillary data stream with VDP decoded data	
		ADF_MODE[1:0]		0	0						Nibble mode	Sets whether ancillary data output mode in byte mode or nibble mode
				0	1						Byte mode, no code restrictions	
				1	0						Byte mode with 0x00 and 0xFF prevented	
				1	1						Reserved	
		ADF_ENABLE	0								Disables insertion of VBI decoded data into ancillary 656 stream	
			1								Enables insertion of VBI decoded data into ancillary 656 stream	
0x63	VDP_ADF_CONFIG_2	ADF_SDID[5:0]			1	0	1	0	1	0	User-specified SDID sent in the ancillary data stream with VDP decoded data	
		Reserved		x								
		DUPLICATE_ADF	0								Ancillary data packet is spread across the Y and C data streams	
			1								Ancillary data packet is duplicated on the Y and C data streams	
0x64	VDP_LINE_00E	VBI_DATA_P318[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 318 (PAL), NTSC—not applicable	
		Reserved		0	0	0						
		MAN_LINE_PGM	0								Decode default standards on the lines indicated in Table 76	
			1								Manually program the VBI standard to be decoded on each line; see Table 77	If set to 1, all VBI_DATA_Px_Ny bits can be set as desired
0x65	VDP_LINE_00F	VBI_DATA_P319_N286[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 319 (PAL), Line 286 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P6_N23[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 6 (PAL), Line 23 (NTSC)	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x66	VDP_LINE_010	VBI_DATA_P320_N287[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 320 (PAL), Line 287 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 7 (PAL), Line 24 (NTSC)	
0x67	VDP_LINE_011	VBI_DATA_P321_N288[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 321 (PAL), Line 288 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 8 (PAL), Line 25 (NTSC)	
0x68	VDP_LINE_012	VBI_DATA_P322[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 322 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 9 (PAL), NTSC—not applicable	
0x69	VDP_LINE_013	VBI_DATA_P323[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 323 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 10 (PAL), NTSC—not applicable	
0x6A	VDP_LINE_014	VBI_DATA_P324_N272[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 324 (PAL), Line 272 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 11 (PAL); NTSC—not applicable	
0x6B	VDP_LINE_015	VBI_DATA_P325_N273[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 325 (PAL), Line 273 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 12 (PAL), Line 10 (NTSC)	
0x6C	VDP_LINE_016	VBI_DATA_P326_N274[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 326 (PAL), Line 274 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 13 (PAL), Line 11 (NTSC)	
0x6D	VDP_LINE_017	VBI_DATA_P327_N275[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 327 (PAL), Line 275 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 14 (PAL), Line 12 (NTSC)	
0x6E	VDP_LINE_018	VBI_DATA_P328_N276[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 328 (PAL), Line 276 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 15 (PAL), Line 13 (NTSC)	
0x6F	VDP_LINE_019	VBI_DATA_P329_N277[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 329 (PAL), Line 277 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 16 (PAL), Line 14 (NTSC)	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x70	VDP_LINE_01A	VBI_DATA_P330_N278[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 330 (PAL), Line 278 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 17 (PAL), Line 15 (NTSC)	
0x71	VDP_LINE_01B	VBI_DATA_P331_N279[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 331 (PAL), Line 279 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 18 (PAL), Line 16 (NTSC)	
0x72	VDP_LINE_01C	VBI_DATA_P332_N280[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 332 (PAL), Line 280 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 19 (PAL), Line 17 (NTSC)	
0x73	VDP_LINE_01D	VBI_DATA_P333_N281[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 333 (PAL), Line 281 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 20 (PAL), Line 18 (NTSC)	
0x74	VDP_LINE_01E	VBI_DATA_P334_N282[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 334 (PAL), Line 282 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 21 (PAL), Line 19 (NTSC)	
0x75	VDP_LINE_01F	VBI_DATA_P335_N283[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 335 (PAL), Line 283 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 22 (PAL), Line 20 (NTSC)	
0x76	VDP_LINE_020	VBI_DATA_P336_N284[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 336 (PAL), Line 284 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 23 (PAL), Line 21 (NTSC)	
0x77	VDP_LINE_021	VBI_DATA_P337_N285[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 337 (PAL), Line 285 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P24_N22[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 24 (PAL), Line 22 (NTSC)	

Interrupt/VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x78	VDP_STATUS (read only)	CC_AVL								0	Closed captioning not detected	CC_CLEAR resets the CC_AVL bit
										1	Closed captioning is detected	
		CC_EVEN_FIELD							0		Closed captioning decoded from odd field	
									1		Closed captioning decoded from even field	
		CGMS_WSS_AVL						0			CGMS/WSS is not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
								1			CGMS/WSS detected	
		Reserved		0	0	0	0					
		TTXT_AVL	0								Teletext not detected	TTXT_CLEAR resets the TTXT_AVL BIT
			1								Teletext detected	
	VDP_STATUS_CLEAR (write only)	CC_CLEAR								0	Does not reinitialize the CCAP readback registers	This is a self clearing bit
										1	Reinitializes the CCAP readback registers	
		Reserved							0			
		CGMS_WSS_CLEAR						0			Does not reinitialize the CGMS/WSS readback registers	This is a self clearing bit
								1			Reinitializes the CGMS/WSS readback registers	
		Reserved	0	0	0	0	0					
		TTXT_CLEAR	0								Does not reinitialize TTXT_AVL	This is a self clearing bit
			1								Reinitializes the TTXT_AVL register	
0x79	VDP_CCAP_DATA_0 (read only)	CCAP_BYTE_1[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 1 of CCAP	
0x7A	VDP_CCAP_DATA_1 (read only)	CCAP_BYTE_2[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 2 of CCAP	
0x7D	VDP_CGMS_WSS_DATA_0 (read only)	CGMS_CRC[5:2]					x	x	x	x	Decoded CRC sequence for CGMS	
		Reserved	0	0	0	0						
0x7E	VDP_CGMS_WSS_DATA_1 (read only)	CGMS_WSS[13:8]			x	x	x	x	x	x	Decoded CGMS/WSS data	
		CGMS_CRC[1:0]	x	x							Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_WSS_DATA_2 (read only)	CGMS_WSS[7:0]	x	x	x	x	x	x	x	x	Decoded CGMS/WSS data	
0x9C	VDP_OUTPUT_SEL	Reserved					0	0	0	0		
		WSS_CGMS_CB_CHANGE				0					Disable content-based updating of CGMS and WSS data	The available bit shows the availability of data only when its content has changed
						1					Enable content-based updating of CGMS and WSS data	
		Reserved	0	0	0							

[1] x indicates a bit that keeps the last written value.

PCB LAYOUT RECOMMENDATIONS

The ADV7182A is a high precision, high speed, mixed-signal device. To achieve the maximum performance from the device, it is important to have a well laid out PCB. The following is a guide for designing a board using the ADV7182A.

ANALOG INTERFACE INPUTS

Take care when routing the inputs on the PCB. Keep track lengths to a minimum and use 75 Ω trace impedances when possible because trace impedances other than 75 Ω increase the chance of reflections.

Place the resistor divider and ac coupling capacitor circuit described in the Input Networks section as close as possible to the A_{IN} pins of the ADV7182A. Place the resistor divider and ac coupling capacitor circuit on the same side of the PCB as the ADV7182A.

POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with 0.1 µF and 10 nF capacitors. The fundamental idea is to have a decoupling capacitor within about 0.5 cm of each power pin. In addition, avoid placing the capacitor on the opposite side of the PCB from the ADV7182A because doing so interposes inductive vias in the path. Locate the decoupling capacitors between the power plane and the power pin. Flow current from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. Placing a via underneath the 100 nF capacitor pads, down to the power plane, is the best approach (see Figure 49).

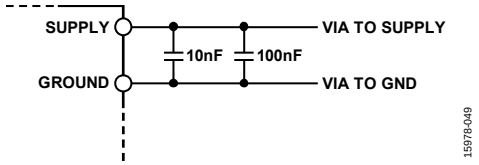

Figure 49. Recommended Power Supply Decoupling

It is important to ensure that the power supplies connected to the ADV7182A, P_{VDD} in particular, are well regulated and filtered. For optimum performance of the ADV7182A, it is recommended to isolate each supply and to use decoupling on each pin, located as physically close to the ADV7182A package as possible.

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least P_{VDD}, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended.

Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

VREFN AND VREFP

Place the circuit associated with the VREFN and VREFP pins as close as possible and on the same side of the PCB as the ADV7182A.

DIGITAL OUTPUTS (BOTH DATA AND CLOCKS)

The ADV7182A digital outputs are: $\overline{\text{INTRQ}}$, LLC, HS, VS/FIELD/SFL, and P0 to P7.

Minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7182A. If series resistors are used, place them as close as possible to the ADV7182A pins. However, try not to add vias or extra length to the output trace to place the resistors closer.

If possible, limit the capacitance that each of the digital outputs drives to less than 15 pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7182A, creating more digital noise on its power supplies.

The ADV7182A has an exposed metal pad on the bottom of the package. This paddle must be soldered to PCB ground for proper heat dissipation and for noise and mechanical strength benefits.

DIGITAL INPUTS

The digital inputs on the ADV7182A are designed to work with 1.8 V to 3.3 V signals and are not tolerant of 5 V signals. Extra components are needed if 5 V logic signals are required to be applied to the decoder.

TYPICAL CIRCUIT CONNECTION

Figure 50 provides an example of how to connect the ADV7182A. For a detailed schematic of the ADV7182A evaluation board, refer to the ADV7182A product page at www.analog.com/ADV7182A.

See the XTAL data sheet (from the XTAL vendor), the AN-1260 Application Note, and the calculator tool (visit the design resources section at www.analog.com/ADV7182A to download) for the correct values for C1, C2, and R_{DAMP}.

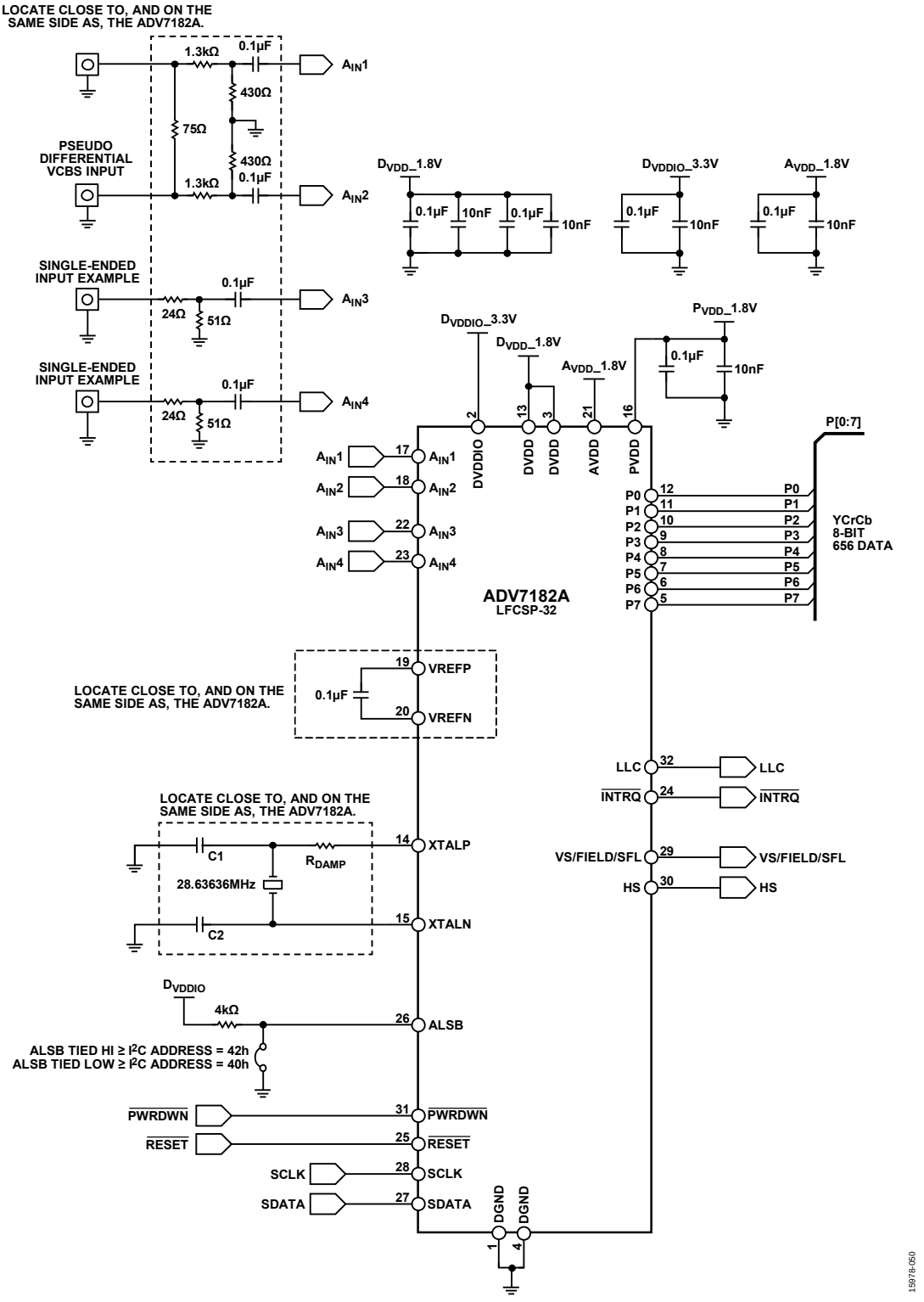

Figure 50. Typical Connection Diagram

OUTLINE DIMENSIONS

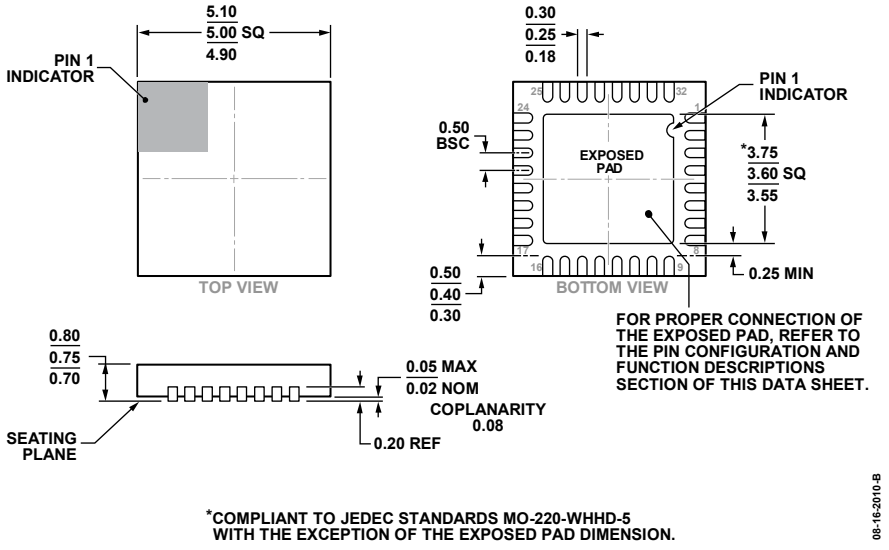

Figure 51. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7182AWBCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7182AWBCPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7182ABCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADV7182ABCPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EVAL-ADV7182AEBZ		Evaluation Board for the ADV7182A	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7182AW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).