

FEATURES

Nonreflective 50 Ω design

Low insertion loss: 1.5 dB at 4 GHz

High isolation: 50 dB at 4 GHz

High input linearity

0.1 dB compression (P0.1dB): 34 dBm typical

Third-order intercept (IP3): 57 dBm typical

High power handling at 85°C

33 dBm through path

27 dBm terminated path

ESD rating

3.5 kV HBM, Class 2

Single-supply or dual-supply operation

Optional internal negative voltage generator (NVG)

1.8 V logic-compatible control

4 mm \times 4 mm, 24-lead LFCSP

APPLICATIONS

Cellular/4G infrastructure

Wireless infrastructure

Mobile radios

Test equipment

GENERAL DESCRIPTION

The ADRF5250 is a general-purpose, single-pole, five-throw (SP5T), nonreflective switch manufactured using a silicon process. The ADRF5250 is available in a 4 mm \times 4 mm, 24-lead lead frame chip scale package (LFCSP) and provides high isolation and low insertion loss from 100 MHz to 6 GHz.

FUNCTIONAL BLOCK DIAGRAM

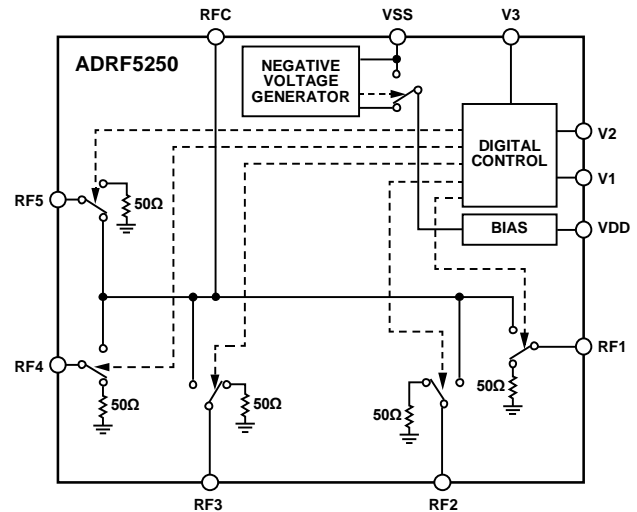


Figure 1.

The ADRF5250 incorporates a negative voltage generator to operate with a single positive supply voltage from 3.3 V to 5 V applied to the VDD pin when the VSS pin is connected to ground. The negative voltage generator can be disabled when an external negative supply voltage of -3.3 V is applied to the VSS pin. The ADRF5250 provides a 1.8 V logic-compatible, 3-pin control interface.

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REVISION HISTORY

6/2017—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_1 = V_2 = V_3 = 0\text{ V}/V_{DD}$, $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|----------------------------|--------------------|--|-----|-----|-----|---------------|
| FREQUENCY RANGE | f | | 0.1 | | 6 | GHz |
| INSERTION LOSS | | | | | | |
| Between RFC and RFx (On) | | 0.1 GHz to 2 GHz | | 1.3 | | dB |
| | | 2 GHz to 4 GHz | | 1.5 | | dB |
| | | 4 GHz to 6 GHz | | 1.8 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RFx (Off) | | 0.1 GHz to 2 GHz | | 55 | | dB |
| | | 2 GHz to 4 GHz | | 50 | | dB |
| | | 4 GHz to 6 GHz | | 46 | | dB |
| RETURN LOSS | | | | | | |
| RFC and RFx (On) | | 0.1 GHz to 2 GHz | | 15 | | dB |
| | | 2 GHz to 4 GHz | | 13 | | dB |
| | | 4 GHz to 6 GHz | | 13 | | dB |
| RFx (Off) | | 0.1 GHz to 2 GHz | | 17 | | dB |
| | | 2 GHz to 4 GHz | | 15 | | dB |
| | | 4 GHz to 6 GHz | | 8 | | dB |
| SWITCHING | | | | | | |
| Rise Time | t_{RISE} | 10% to 90% of radio frequency (RF) output | | 40 | | ns |
| Fall Time | t_{FALL} | 10% to 90% of RF output | | 80 | | ns |
| On and Off Time | t_{ON}, t_{OFF} | 50% of digital control voltage (V_1, V_2, V_3) to 90% of RF output | | 150 | | ns |
| Settling Time (RFx to RFx) | | | | | | |
| 0.1 dB | | 50% of V_1, V_2, V_3 to 0.1 dB of final RF output | | 400 | | ns |
| 0.05 dB | | 50% of V_1, V_2, V_3 to 0.05 dB of final RF output | | 500 | | ns |
| INPUT LINEARITY | | | | | | |
| 0.1 dB Compression | P0.1dB | | | 34 | | dB |
| Third-Order Intercept | IP3 | | | 57 | | dBm |
| SUPPLY CURRENT | | | | | | |
| Positive | I_{DD} | VDD, VSS pins NVG enabled ($V_{SS} = 0\text{ V}$) | | 360 | | μA |
| | | NVG disabled ($V_{SS} = -3.3\text{ V}$) | | 280 | | μA |
| Negative | I_{SS} | NVG disabled ($V_{SS} = -3.3\text{ V}$) | | -60 | | μA |
| DIGITAL CONTROL INPUTS | | | | | | |
| Voltage | | V1, V2, V3 pins | | | | |
| Low | V_{INL} | $V_{DD} = 3.3\text{ V}$ | 0 | | 0.8 | V |
| | | $V_{DD} = 5\text{ V}$ | 0 | | 1.2 | V |
| High | V_{INH} | $V_{DD} = 3.3\text{ V}$ | 1.3 | | 3.3 | V |
| | | $V_{DD} = 5\text{ V}$ | 1.6 | | 5 | V |
| Current | | | | | | |
| Low and High | I_{INL}, I_{INH} | $V_{DD} = 3.3\text{ V to }5\text{ V}$ | | <1 | | μA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-------------------------------------|-----------------|--|-------|-----|----------|-------------|
| RECOMMENDED OPERATING CONDITIONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | V_{DD} | | 3.0 | | 5.25 | V |
| Negative | V_{SS} | | -3.45 | | -3.15 | V |
| Digital Control Voltage | V_1, V_2, V_3 | | 0 | | V_{DD} | V |
| Maximum RF Input Power ¹ | P_{IN} | | | | | |
| $T_{CASE} = 105^{\circ}C$ | | Through path ($V_{DD} = 3.3V$ to $5V$) | | | 30 | dBm |
| | | Terminated path | | | 24 | dBm |
| | | Hot switching | | | 24 | dBm |
| $T_{CASE} = 85^{\circ}C$ | | Through path ($V_{DD} = 3.3V$ to $5V$) | | | 33 | dBm |
| | | Terminated path | | | 27 | dBm |
| | | Hot switching | | | 27 | dBm |
| Case Temperature | T_{CASE} | | -40 | | +105 | $^{\circ}C$ |

¹ Exposure to levels between the recommended operating conditions and the absolute maximum rating conditions for extended period may affect device reliability.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

| Parameter | Rating |
|--|----------------------------|
| Positive Supply Voltage (V_{DD}) | -0.3 V to +5.5 V |
| Negative Supply Voltage (V_{SS}) | -3.6 V to +0.3 V |
| Digital Control Input Voltage (V_1, V_2, V_3) | -0.3 V to $V_{DD} + 0.5$ V |
| RF Input Power | |
| Through Path | 35 dBm |
| Terminated Path | 34 dBm |
| All Off State, RFC as Input | 24 dBm |
| Hot Switching | |
| RFC as Input | |
| RFx to RFx | 32 dBm |
| All Off to RFx | 24 dBm |
| RFx as Input | |
| RFx to RFx | 34 dBm |
| All Off to RFx | 34 dBm |
| Temperature | |
| Junction, T_J | 135°C |
| Storage | -65°C to +150°C |
| Reflow (MSL3 Rating) | 260°C |
| Junction to Case Thermal Resistance, θ_{JC} | |
| Through Path | 90°C/W |
| Terminated Path | 100°C/W |
| ESD Sensitivity | |
| Human Body Model (HBM) | 3.5 kV (Class 2) |
| Field Induced Device Model (FICDM) | 1.25 kV (Class IV) |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

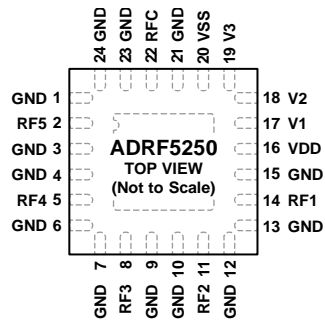
Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

155606-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|--|----------|--|
| 1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24 | GND | Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB). |
| 2 | RF5 | RF Throw Port 5. This pin is dc coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| 5 | RF4 | RF Throw Port 4. This pin is dc coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| 8 | RF3 | RF Throw Port 3. This pin is dc coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| 11 | RF2 | RF Throw Port 2. This pin is dc coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| 14 | RF1 | RF Throw Port 1. This pin is dc coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| 16 | VDD | Positive Supply Voltage. |
| 17 | V1 | Digital Input Voltage Applied to the Least Significant Bit (LSB) of Digital Interface for Controlling RF Path State. See Table 5. |
| 18 | V2 | Digital Input Voltage Applied to the Second Bit of Digital Interface for Controlling RF Path State. See Table 5. |
| 19 | V3 | Digital Input Voltage Applied to the Most Significant Bit (MSB) of Digital Interface for Controlling RF Path State. See Table 5. |
| 20 | VSS | Optional Negative Supply Voltage. This pin can be connected to ground to operate with the internal negative voltage generator. The internal negative voltage generator is disabled when this pin is connected to an external 3.3 V supply. |
| 22 | RFC | RF Common Port. This pin is dc-coupled and no dc blocking capacitor is necessary when the RF line potential is within 0 V dc. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB. |

INTERFACE SCHEMATICS

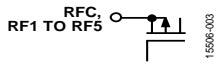


Figure 3. RF Pin Interface Schematic

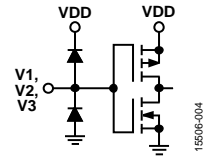


Figure 4. Digital Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

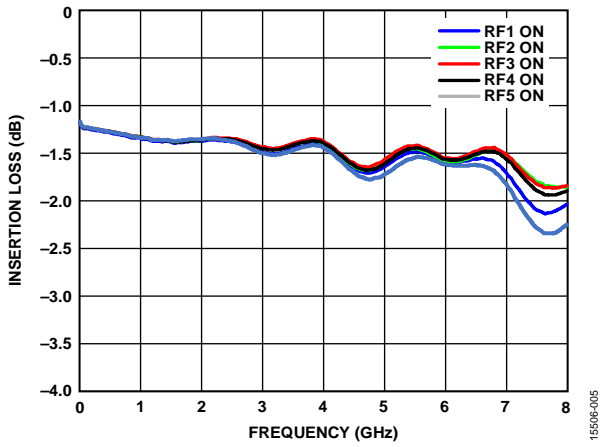


Figure 5. Insertion Loss on RF Paths at Room Temperature

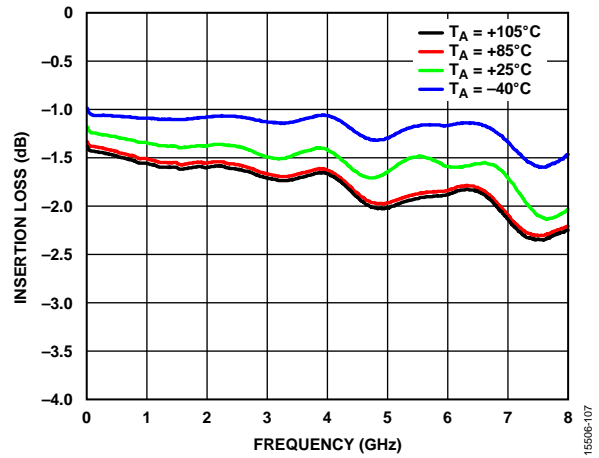


Figure 8. Insertion Loss on RF Paths over Temperature

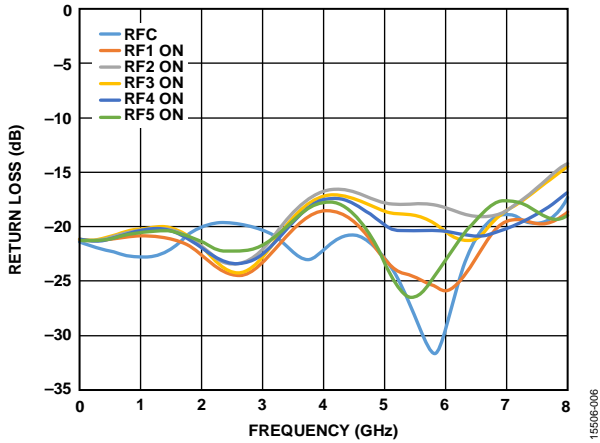


Figure 6. Return Loss on Selected RFx Ports and RFC

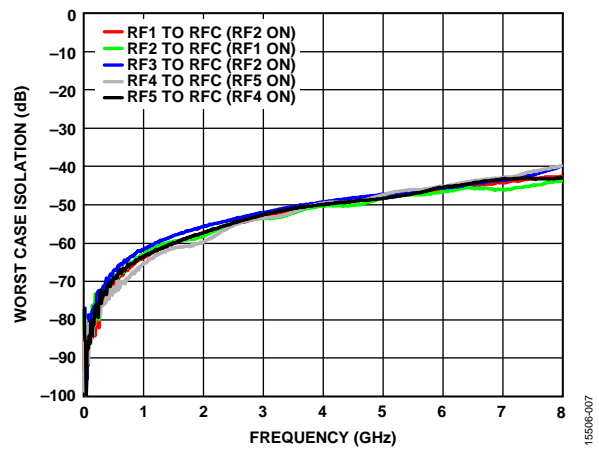


Figure 9. Worst Case Isolation on RF Paths

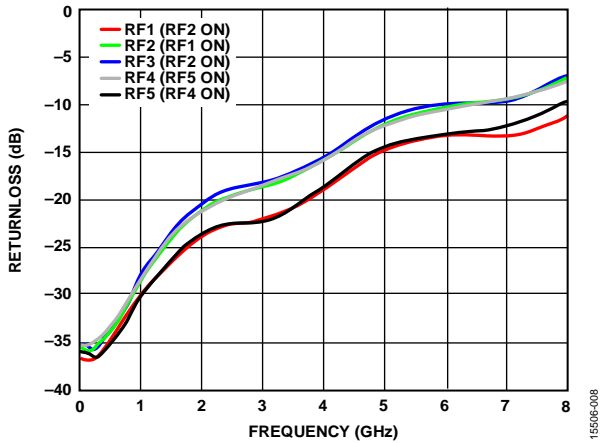


Figure 7. Return Loss on Terminated RFx Ports

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT (IP3)

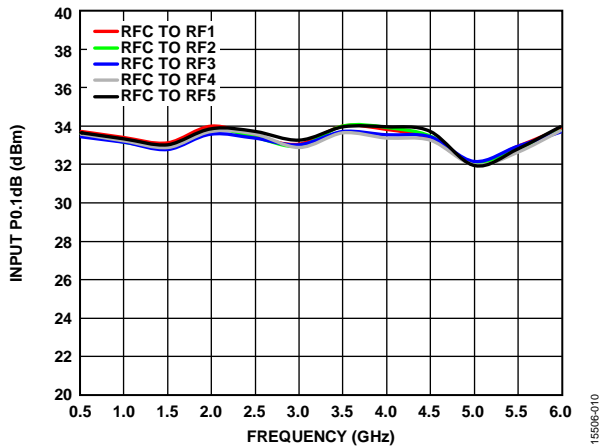


Figure 10. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency, V_{DD} = 3.3 V, V_{SS} = 0 V

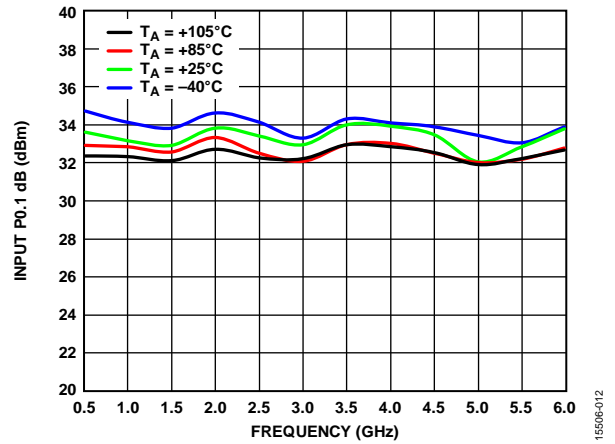


Figure 13. Input 0.1 dB Power Compression vs. Frequency over Temperature, V_{DD} = 3.3 V, V_{SS} = 0 V

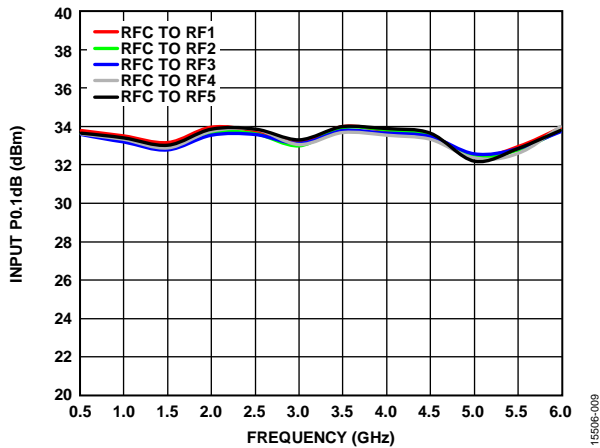


Figure 11. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency, V_{DD} = 5 V, V_{SS} = 0 V

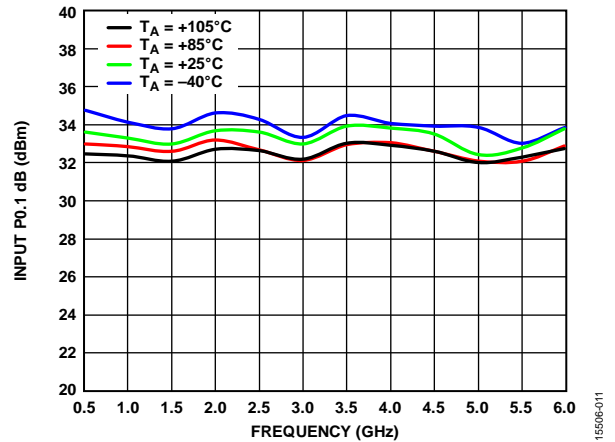


Figure 14. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature, V_{DD} = 5 V, V_{SS} = 0 V

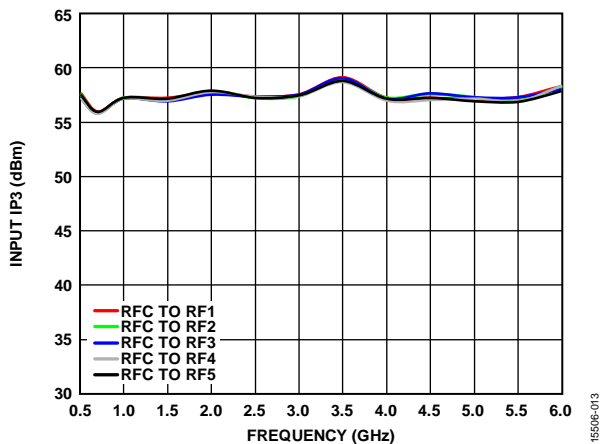


Figure 12. Input IP3 vs. Frequency, V_{DD} = 5 V, V_{SS} = 0 V

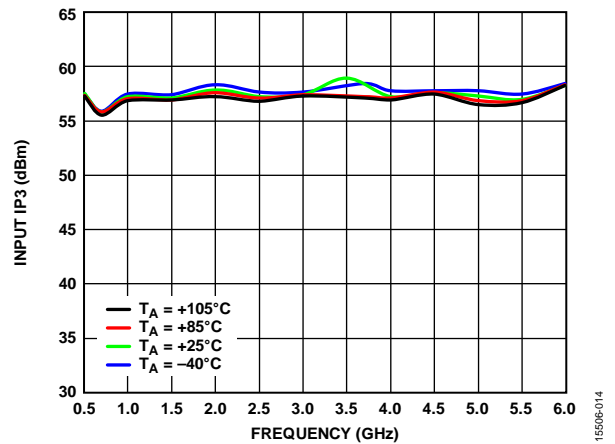


Figure 15. Input IP3 vs. Frequency over Temperature, V_{DD} = 5 V, V_{SS} = 0 V

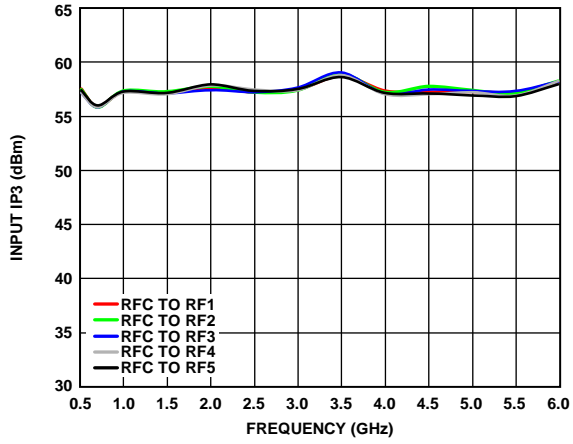


Figure 16. Input IP3 vs. Frequency, $V_{DD} = 3.3 V$, $V_{SS} = 0 V$

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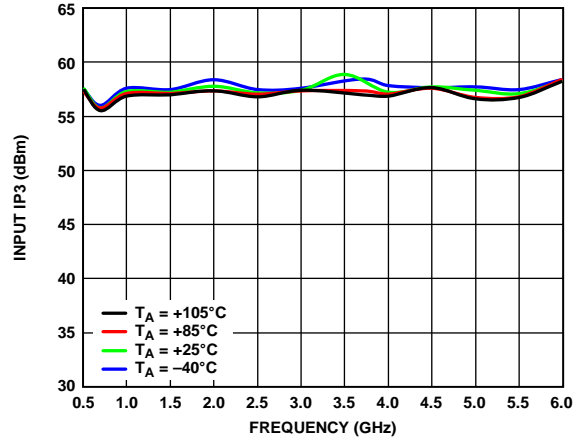


Figure 17. Input IP3 vs. Frequency over Temperature, $V_{DD} = 3.3 V$, $V_{SS} = 0 V$

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THEORY OF OPERATION

The ADRF5250 requires a positive supply voltage applied to the VDD pin and 0 V or -3.3 V supply voltage applied to the VSS pin. Bypass capacitors are recommended on the supply and digital control lines to minimize RF coupling. An incorporated negative supply generator is enabled or disabled depending on the applied V_{SS} supply voltage. Table 4 describes the operation mode of that negative supply generator.

Table 4. Negative Voltage Generator Operation Mode

| V_{SS} | Test Conditions/Comments |
|----------|---|
| 0 V | The incorporated negative voltage generator is enabled |
| -3.3 V | The incorporated negative voltage generator is disabled |

The ADRF5250 is internally matched to $50\ \Omega$ at the RF common port (RFC) and the RF throw ports (RF1 to RF5); therefore, no external matching components are required. All of the RF ports are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The design is bidirectional; the RF input signal can be applied to the RFC port while the RF throw port (RF1 to RF5) is output, or vice versa.

The ADRF5250 has a 3-bit, 1.8 V logic-compatible control interface that is controlled through the V1, V2, and V3 digital control voltage pins. A small bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation. The V1 and V3 test points correspond to the LSB and MSB of the digital control interface of the ADRF5250. The modes of the RF paths are determined as shown in Table 5.

When an RF path is on, the RF signal is conducted equally well in both directions between its throw port (RFx) and common port (RFC). Otherwise, each RFx path is terminated to an internal $50\ \Omega$ resistor that provides high loss between the insertion loss path and its throw ports.

Table 5. Control Voltage Truth Table

| V_3 | V_2 | V_1 | Mode |
|-------|-------|-------|---------|
| Low | Low | Low | All Off |
| Low | Low | High | RF1 on |
| Low | High | Low | RF2 on |
| Low | High | High | RF3 on |
| High | Low | Low | RF4 on |
| High | Low | High | RF5 on |
| High | High | Low | All off |
| High | High | High | All off |

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up VDD and VSS. The relative order is not important.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply an RF input signal.

APPLICATIONS INFORMATION

EVALUATION BOARD

Figure 18 and Figure 19 show the top and cross sectional views of the evaluation board, which uses 4-layer construction with a copper thickness of 0.5 oz (0.7 mil) and dielectric materials between each copper layer.

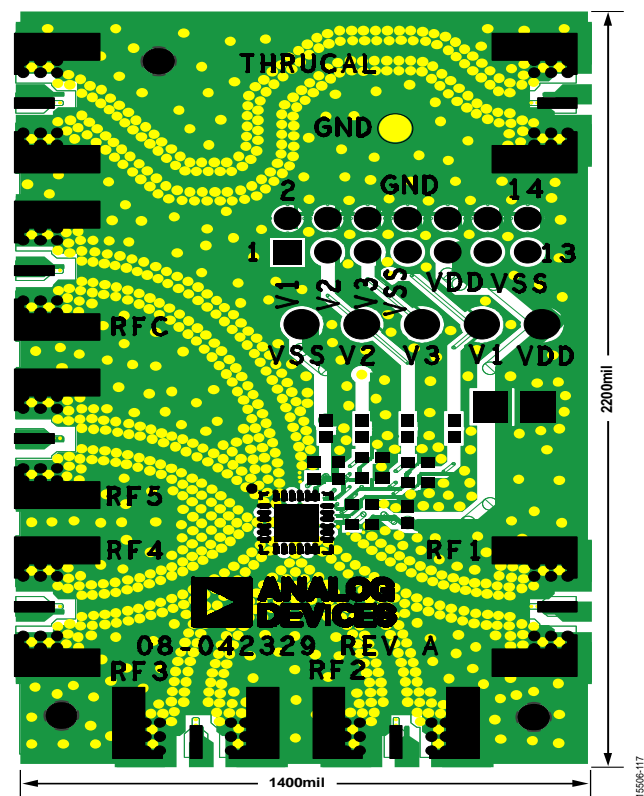


Figure 18. Evaluation Board Layout Top View



Figure 19. Evaluation Board Cross Sectional View

All RF traces are routed on Layer 2; the V1, V3, and VSS dc traces are routed on Layer 3; the V2 and VDD dc traces are routed on the top layer; and the other remaining layers are grounded planes that provide a solid ground for RF transmission lines. The top and bottom dielectric material are Rogers 4350B, offering low loss performance. The middle dielectric material is Rogers 4450F and is used to achieve an overall board thickness of 30 mil. The RF transmission lines were designed using a

coplanar waveguide (CPWG) model with a width of 8 mil and ground spacing of 10 mil for a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around the transmission lines and under the exposed pad of the package.

Figure 20 shows the actual ADRF5250 evaluation board with component placement. Two power supply ports are connected to the VDD and VSS test points, TP3 and TP5, and the ground reference is connected to the GND test point, TP6. On the digital control and VDD supply traces, bypass capacitors are used.

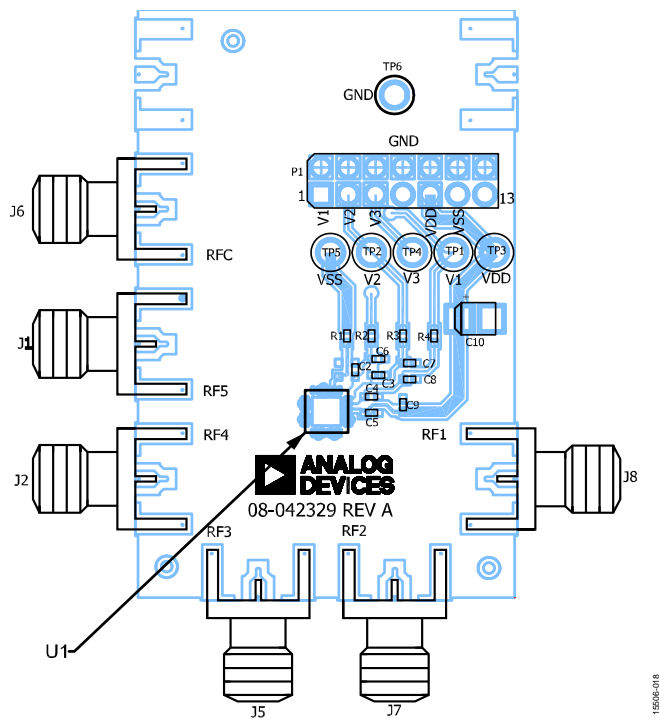


Figure 20. ADRF5250-EVALZ Evaluation Board

Three control ports are connected to the V1, V2, and V3 test points, TP1, TP2, and TP4, respectively. On each control trace, a resistor position is available to improve the isolation between the RF and control signals. The RF ports are connected to the RFC, RF1, RF2, RF3, RF4, and RF5 connectors (J6, J8, J7, J5, J2, and J1), which are end launch jack SMA RF connectors. A through transmission line that connects unpopulated RF connectors (J3 and J4) is also available to measure the loss of the PCB. Figure 22 and Table 6 show the evaluation board schematic and bill of materials, respectively.

The evaluation board shown in Figure 20 is available for order from the Analog Devices, Inc., website at www.analog.com.

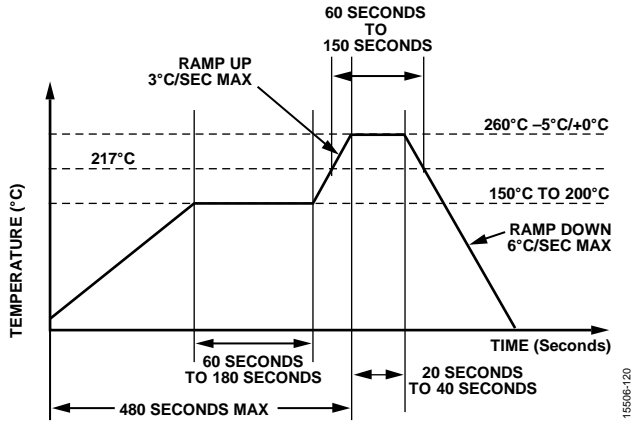


Figure 21. Pb-Free Reflow Solder Profile

Table 6. Bill of Materials for the ADRF5250-EVALZ Evaluation Board

| Item | Description |
|------------------|---|
| J1, J2, J5 to J8 | RF SMA connectors |
| TP1 to TP6 | DC bias test pins |
| C2 to C5 | 100 pF capacitors, 0402 package |
| C6 to C9 | 0.01 μF capacitor, 0402 package |
| C10 | 10 μF capacitor, tantalum package |
| 08-042239 | Evaluation PCB, Rogers 4350B circuit board material |

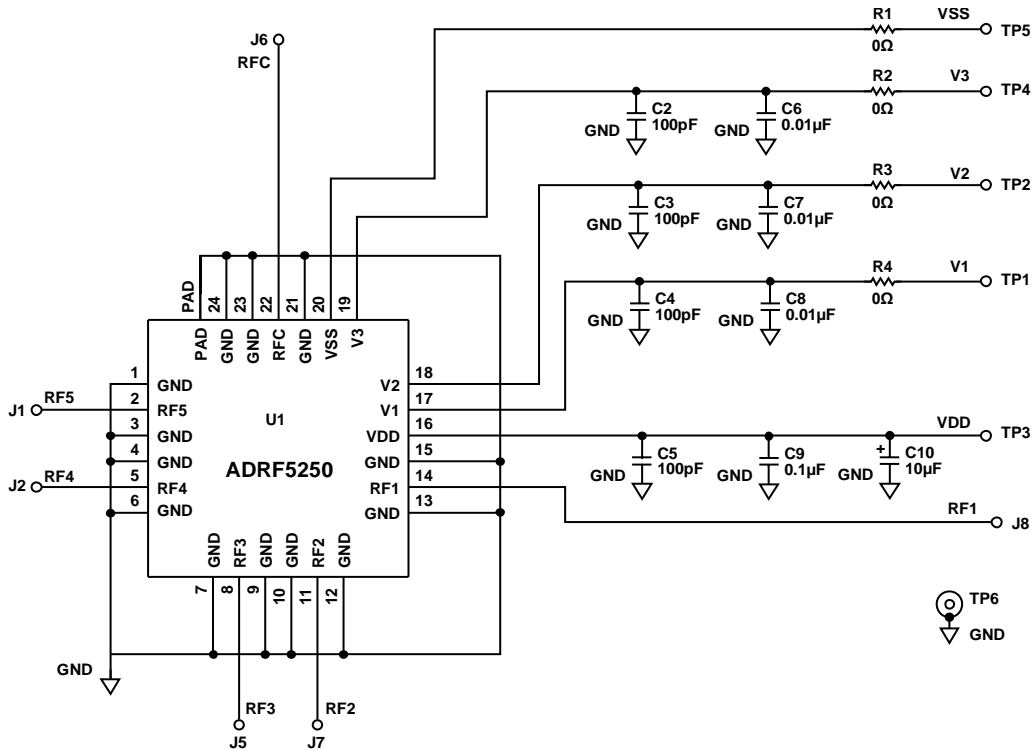
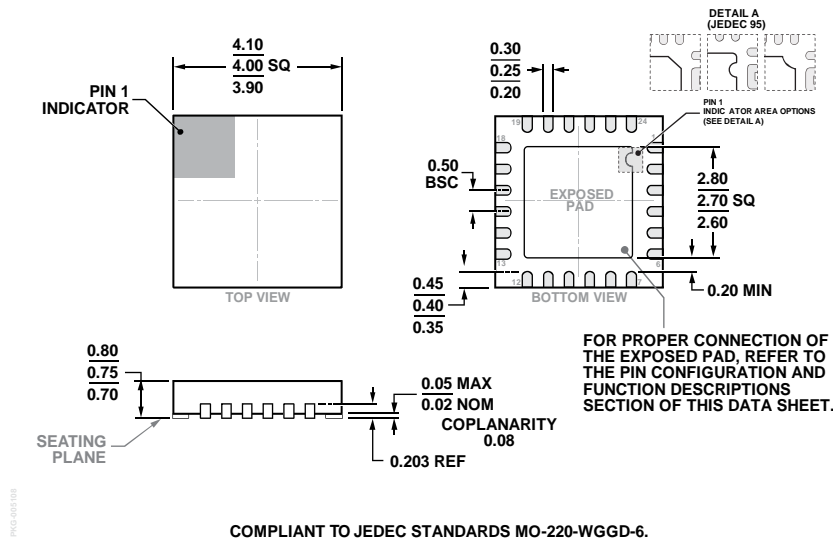


Figure 22. ADRF5250-EVALZ Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-6.
 Figure 23. 24-Lead Lead Frame Chip Scale Package [LFCSP]
 4 mm × 4 mm Body and 0.75 mm Package Height
 (CP-24-23)
 Dimensions shown in millimeters

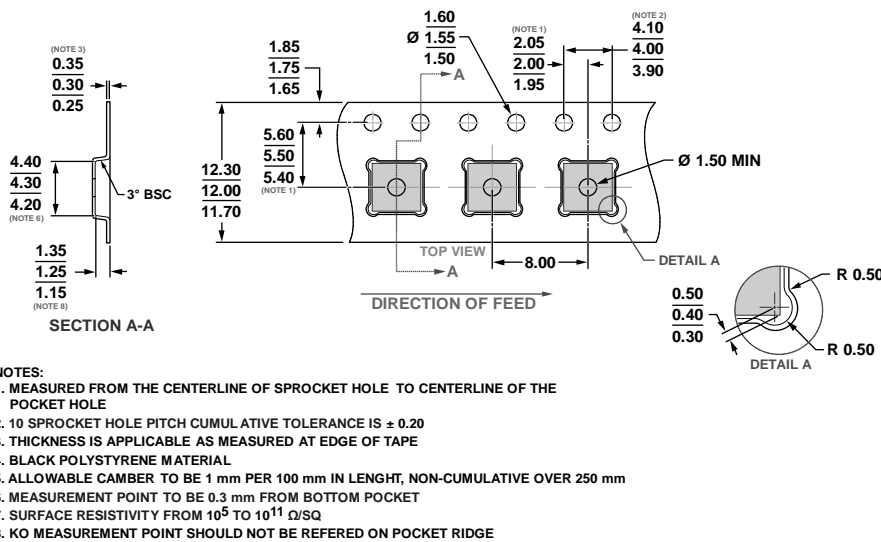


Figure 24. LFCSP Tape and Reel Outline Dimensions
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| ADRF5250BCPZ | -40°C to +105°C | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-23 |
| ADRF5250BCPZ-R7 | -40°C to +105°C | 24-Lead Lead Frame Chip Scale Package [LFCSP], 7" Tape and Reel | CP-24-23 |
| ADRF5250BCPZRL | -40°C to +105°C | 24-Lead Lead Frame Chip Scale Package [LFCSP], 13" Tape and Reel | CP-24-23 |
| ADRF5250-EVALZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

NOTES