



Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

General Description

The MAX398/MAX399 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100Ω), which is matched to within 6Ω between channels and remains flat over the specified analog signal range (11Ω max). They also offer low leakage over temperature (NO off-leakage current less than 2.5nA at $+85^\circ\text{C}$) and fast switching speeds (transition time less than 250ns). The MAX398 is an 8-channel device, and the MAX399 is a dual 4-channel device.

The MAX398/MAX399 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (less than 5pC) and guarantee electrostatic discharge protection (ESD) greater than 2000V .

These muxes operate with a single $+3\text{V}$ to $+15\text{V}$ supply or bipolar $\pm 3\text{V}$ to $\pm 8\text{V}$ supplies, while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. The MAX398/MAX399 are pin compatible with the industry-standard DG408, DG409, DG508A, and DG509A.

Applications

Sample-and-Hold Circuits
Automatic Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing
Low-Voltage Data-Acquisition Systems

Features

- ◆ Pin Compatible with Industry-Standard DG408/DG409/DG508A/DG509A
- ◆ Guaranteed On-Resistance Match Between Channels ($< 6\Omega$)
- ◆ Low On-Resistance ($< 100\Omega$)
- ◆ Guaranteed Flat On-Resistance over Signal Range ($< 11\Omega$)
- ◆ Guaranteed Low Charge Injection ($< 5\text{pC}$)
- ◆ NO Off-Leakage Current $< 1\text{nA}$ at $+85^\circ\text{C}$
- ◆ COM Off-Leakage Current $< 2.5\text{nA}$ at $+85^\circ\text{C}$
- ◆ ESD Protection $> 2000\text{V}$
- ◆ $+3\text{V}$ to $+15\text{V}$ Single-Supply Operation
 $\pm 3\text{V}$ to $\pm 8\text{V}$ Bipolar-Supply Operation
- ◆ Low Power Consumption ($< 300\mu\text{W}$)
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

Ordering Information

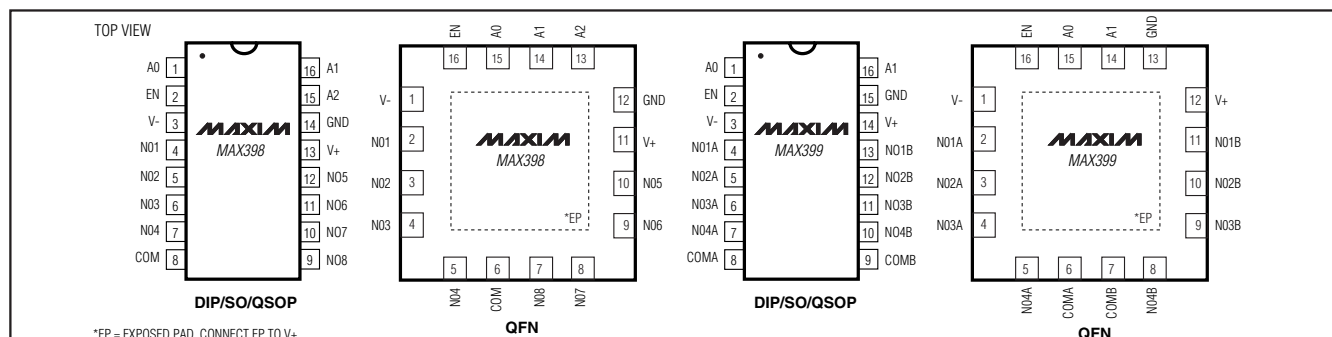
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX398CGE	0°C to $+70^\circ\text{C}$	16 QFN-EP*	G1655-3
MAX398CEE	0°C to $+70^\circ\text{C}$	16 QSOP	E16-1
MAX398CSE	0°C to $+70^\circ\text{C}$	16 Narrow	S16-1
MAX398CPE	0°C to $+70^\circ\text{C}$	16 Plastic	P16-1
MAX398C/D	0°C to $+70^\circ\text{C}$	Dice**	—
MAX398EGE	-40°C to $+85^\circ\text{C}$	16 QFN-EP*	G1655-3
MAX398EEE	-40°C to $+85^\circ\text{C}$	16 QSOP	E16-1
MAX398ESE	-40°C to $+85^\circ\text{C}$	16 Narrow	S16-1
MAX398EPE	-40°C to $+85^\circ\text{C}$	16 Plastic	P16-1
MAX398EJE	-40°C to $+85^\circ\text{C}$	16 CERDIP	J16-1
MAX398MJE	-55°C to $+125^\circ\text{C}$	16 CERDIP	J16-1

Ordering Information continued at end of data sheet.

*EP = Exposed pad.

**Contact factory for dice specifications.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+-0.3V to +17V

V-+0.3V to -17V

V+ to V--0.3V to +17V

Voltage into Any Terminal (Note 1).....(V- - 2V) to (V+ + 2V) or
30mA (whichever occurs first)

Current into Any Terminal30mA

Peak Current, Any Terminal

(pulsed at 1ms, 10% duty cycle max)40mA

Continuous Power Dissipation (T_A = +70°C)

QFN (derate 18.5mW/°C above +70°C)1484mW

QSOP (derate 8.3mW/°C above +70°C)667mW

Narrow SO (derate 8.7mW/°C above +70°C)696mW

Plastic DIP (derate 7.5mW/°C above +70°C)470mW

CERDIP (derate 10.0mW/°C above +70°C)900mW

Operating Temperature Ranges

MAX39_C_ _0°C to +70°C

MAX39_E_ _-40°C to +85°C

MAX39_MJE-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10s)+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V
Channel On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V		T _A = +25°C		60	100	Ω
				T _A = T _{MIN} to T _{MAX}			125	
R _{ON} Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V, V+ = 5V, V- = -5V		T _A = +25°C			6	Ω
				T _A = T _{MIN} to T _{MAX}			8	
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	I _{NO} = 1mA, V _{COM} = ±3V, V+ = 5V, V- = -5V		T _A = +25°C			11	Ω
				T _A = T _{MIN} to T _{MAX}			14	
NO Off-Leakage Current (Note 6)	I _{NO(OFF)}	V _{NO} = ±4.5V, V _{COM} = ∓4.5V, V+ = 5.5V, V- = -5.5V		T _A = +25°C		-0.1	+0.1	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-1.0	+1.0	
					M	-10	+10	
COM Off-Leakage Current (Note 6)	I _{COM(OFF)}	V _{COM} = ±4.5V, V _{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX398	T _A = +25°C		-0.2	+0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5	+2.5	
					M	-20	+20	
		V _{COM} = ±4.5V, V _{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX399	T _A = +25°C		-0.1	+0.1	
				T _A = T _{MIN} to T _{MAX}	C, E	-1.5	+1.5	
					M	-10	+10	
COM On-Leakage Current (Note 6)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NO} = ±4.5V	MAX398	T _A = +25°C		-0.4	+0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-5	+5	
					M	-40	+40	
		MAX399	T _A = +25°C		-0.2	+0.2		
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5	+2.5		
				M	-20	+20		

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V₊ = +5V ±10%, V₋ = -5V ±10%, GND = 0, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
DIGITAL LOGIC INPUT								
Logic-High Input Voltage	V _{AH} , V _{ENH}		T _A = T _{MIN} to T _{MAX}	2.4			V	
Logic-Low Input Voltage	V _{AL} , V _{ENL}		T _A = T _{MIN} to T _{MAX}		0.8		V	
Input Current with Input-Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V		-0.1		+0.1	μA	
Input Current with Input-Voltage Low	I _{AL} , I _{ENL}	V _A = V _{EN} = 0.8V		-0.1		+0.1	μA	
SUPPLY								
Power-Supply Range				±3		±8	V	
Positive Supply Current	I ₊	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V	T _A = +25°C	-1		+1	μA	
Negative Supply Current	I ₋	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V	T _A = T _{MIN} to T _{MAX}	-1		+1	μA	
Ground Current	I _{GND}	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V	T _A = +25°C	-1		+1	μA	
			T _A = T _{MIN} to T _{MAX}	-1		+1		
DYNAMIC								
Transition Time	t _{TRANS}	Figure 2				150	ns	
Break-Before-Make Interval	t _{OPEN}	Figure 4	T _A = +25°C	0		40	ns	
Enable Turn-On Time	t _{ON(EN)}	Figure 3	T _A = +25°C			60	150	ns
			T _A = T _{MIN} to T _{MAX}				250	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3	T _A = +25°C			40	150	ns
			T _A = T _{MIN} to T _{MAX}				200	
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0, R _S = 0Ω	T _A = +25°C			2	5	pC
Off-Isolation (Note 7)		V _{EN} = 0, R _L = 1kΩ, f = 100kHz	T _A = +25°C			-75		dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{P-P} , R _L = 1kΩ	T _A = +25°C			-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C			8		pF
NO Off-Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _D = 0V	T _A = +25°C			11		pF
COM Off-Capacitance	C _{COM(OFF)}	f = 1MHz, V _{EN} = V _D = 0V	MAX398 MAX399	T _A = +25°C		40		pF
							20	
COM On-Capacitance	C _{COM(ON)}	f = 1MHz, V _{EN} = V _D = 0V	MAX398 MAX399	T _A = +25°C		54		pF
							34	

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ELECTRICAL CHARACTERISTICS—Single +5V

(V+ = 5V ±10%, V- = 0, GND = 0, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		T _A = +25°C	150	225	Ω	
				T _A = T _{MIN} to T _{MAX}		280		
R _{ON} Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		T _A = +25°C		11	Ω	
				T _A = T _{MIN} to T _{MAX}		13		
On-Resistance Flatness	R _{FLAT}	I _{NO} = 1mA; V _{COM} = 3V, 2V, 1V; V+ = 5V		T _A = +25°C	10	18	Ω	
				T _A = T _{MIN} to T _{MAX}	15	22		
NO Off-Leakage Current (Note 8)	I _{NO} (OFF)	V _{NO} = 4.5V, V _{COM} = 0, V+ = 5.5V		T _A = +25°C	-0.1	+0.1	nA	
				T _A = T _{MIN} to T _{MAX}	C, E	-1.0		+1.0
					M	-10		+10
COM Off-Leakage Current (Note 8)	I _{COM} (OFF)	V _{COM} = 4.5V, V _{NO} = 0, V+ = 5.5V	MAX398	T _A = +25°C	-0.2	+0.2	nA	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		+2.5
					M	-20		+20
		V _{COM} = 4.5V, V _{NO} = 0, V+ = 5.5V	MAX399	T _A = +25°C	-0.1	+0.1		
				T _A = T _{MIN} to T _{MAX}	C, E	-1.5		+1.5
					M	-10		+10
COM On-Leakage Current (Note 8)	I _{COM} (ON)	V _{COM} = 4.5V, V _{NO} = 4.5V, V+ = 5.5V	MAX398	T _A = +25°C	-0.4	+0.4	nA	
				T _A = T _{MIN} to T _{MAX}	C, E	-5		+5
					M	-40		+40
		MAX399	T _A = +25°C	-0.2	+0.2			
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5	+2.5		
				M	-20	+20		
DIGITAL LOGIC INPUT								
Logic-High Input Voltage	V _{AH} , V _{ENH}			T _A = T _{MIN} to T _{MAX}	2.4		V	
Logic-Low Input Voltage	V _{AL} , V _{ENL}			T _A = T _{MIN} to T _{MAX}		0.8	V	
Input Current with Input-Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V			-0.1	+0.1	μA	
Input Current with Input-Voltage Low	I _{AL} , I _{ENL}	V _A = 0 V _{EN} = 0.8V			-0.1	+0.1	μA	
SUPPLY								
Power-Supply Range					3	15	V	
Positive Supply Current	I+	V _{EN} = V _A = 0, V+; V+ = 5.5V; V- = 0			-1.0	+1.0	μA	
Negative Supply Current	I-	V _{EN} = V _A = 0V, V+; V+ = 5.5V; V- = 0			-1.0	+1.0	μA	
IGND Supply Current	IGND	V _{EN} = V+, 0; V _A = 0; V+ = 5.5V; V- = 0		T _A = +25°C	-1.0	+1.0	μA	
				T _A = T _{MIN} to T _{MAX}	-1.0	+1.0		

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ELECTRICAL CHARACTERISTICS—Single +5V (continued)

(V₊ = 5V ±10%, V₋ = 0, GND = 0, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Transition Time	t _{TRANS}	V _{NO} = 3V		90	245	ns
Break-Before-Make Interval	t _{OPEN}	T _A = +25°C	10	40		ns
Enable Turn-On Time	t _{ON(EN)}	T _A = +25°C		90	200	ns
		T _A = T _{MIN} to T _{MAX}			275	
Enable Turn-Off Time	t _{OFF(EN)}	T _A = +25°C		50	125	ns
		T _A = T _{MIN} to T _{MAX}			200	
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0, R _S = 0Ω, T _A = +25°C		1.5	5	pC

ELECTRICAL CHARACTERISTICS—Single +3V

(V₊ = 3V ±10%, V₋ = 0, GND = 0, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V _{ANALOG}	(Note 3)		V-		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 1.5V, V+ = 3V	T _A = +25°C	230	375	Ω	
			T _A = T _{MIN} to T _{MAX}		425		
DYNAMIC							
Transition Time (Note 3)	t _{TRANS}	Figure 2, V _{IN} = 2.4V, V _{N01} = 1.5V, V _{N08} = 0	T _A = +25°C	230	575	ns	
Enable Turn-On Time (Note 3)	t _{ON(EN)}	Figure 3, V _{INH} = 2.4V, V _{INL} = 0, V _{N01} = 1.5V	T _A = +25°C	200	500	ns	
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}	Figure 3, V _{INH} = 2.4V, V _{INL} = 0, V _{N01} = 1.5V	T _A = +25°C	75	400	ns	
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0, R _S = 0Ω	T _A = +25°C	1	5	pC	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = R_{ONMAX} - R_{ONMIN}.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0 and 0 to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

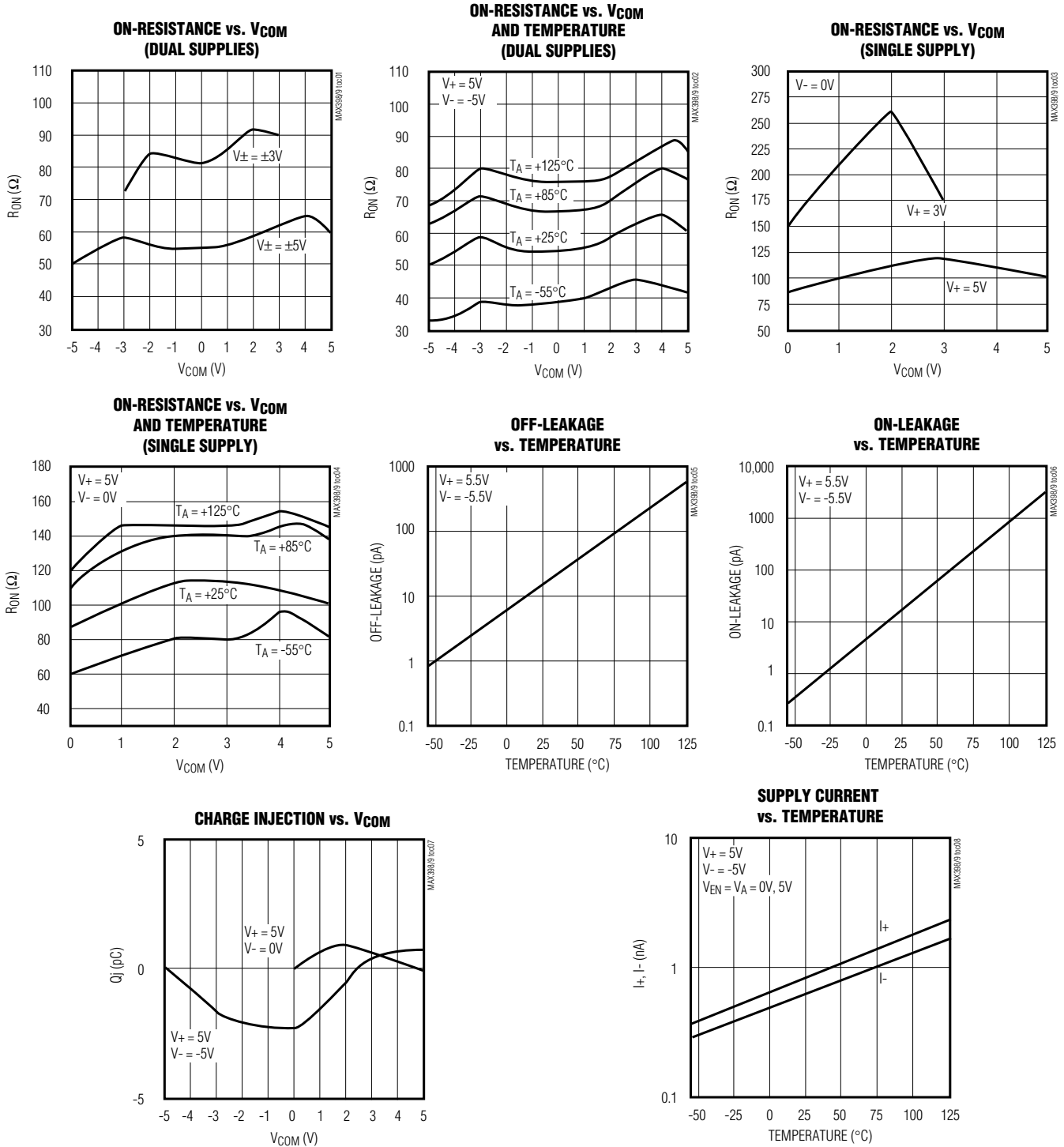
Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off-isolation = 20log V_{COM} / V_{NO}, V_{COM} = output, V_{NO} = input to off switch.

Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Pin Description

PIN				NAME	FUNCTION
MAX398		MAX399			
QSOP/DIP/ SO	QFN	QSOP/DIP/ SO	QFN		
1, 15, 16	15, 14, 13	—	—	A0, A2, A1	Address Inputs
—	—	1, 16	15, 14	A0, A1	Address Inputs
2	16	2	16	EN	Enable
3	1	3	1	V-	Negative-Supply Voltage Input
4–7	2–5	—	—	N01–N04	Analog Inputs—Bidirectional
—	—	4–7	2–5	N01A–N04A	Analog Inputs—Bidirectional
8	6	—	—	COM	Analog Output—Bidirectional
—	—	8, 9	6, 7	COMA, COMB	Analog Outputs—Bidirectional
9–12	7–10	—	—	N08–N05	Analog Inputs—Bidirectional
–	–	10–13	8–11	N04B–N01B	Analog Inputs—Bidirectional
13	11	14	12	V+	Positive-Supply Voltage Input
14	12	15	13	GND	Ground
—	EP	—	EP	EP	Exposed Pad. Connect to V+.

MAX398/MAX399

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

Using supply voltages less than $\pm 5V$ reduces the analog signal range. The MAX398/MAX399 muxes operate with $\pm 3V$ to $\pm 8V$ bipolar supplies or with a $+3V$ to $+15V$ single supply. Connect V_- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as $+10V$ and $-5V$. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 3V$, $\pm 5V$, $+3V$, and $+5V$ supplies. (Switching times increase by a factor of two or more for operation at $+5V$.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, then V_- , followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes ($D1$, $D2$) in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V_+ and one diode drop

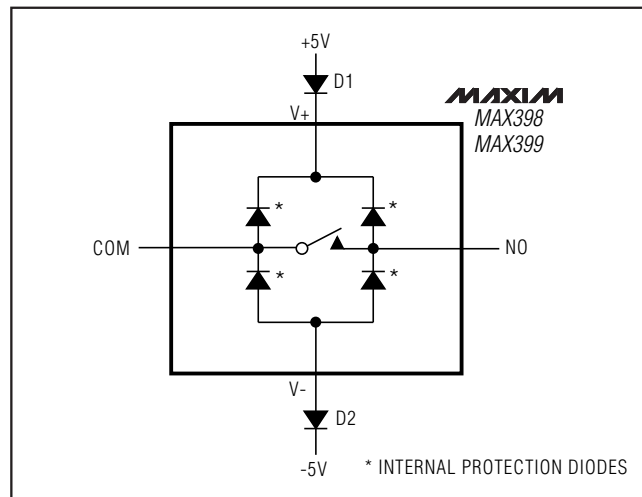


Figure 1. Overvoltage Protection Using External Blocking Diodes

above V_- , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_+ and V_- should not exceed $17V$. These protection diodes are not recommended when using a single supply.

Test Circuits/Timing Diagrams

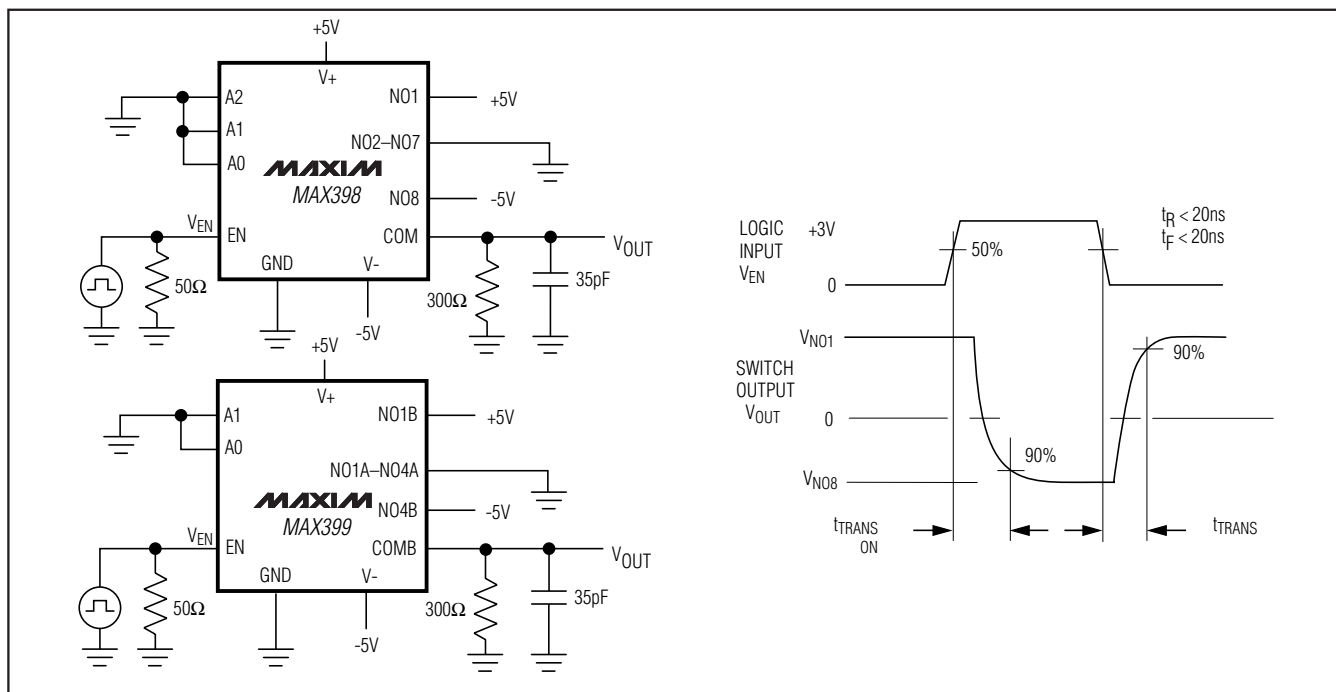


Figure 2. Transition Time

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Test Circuits/Timing Diagrams (continued)

MAX398/MAX399

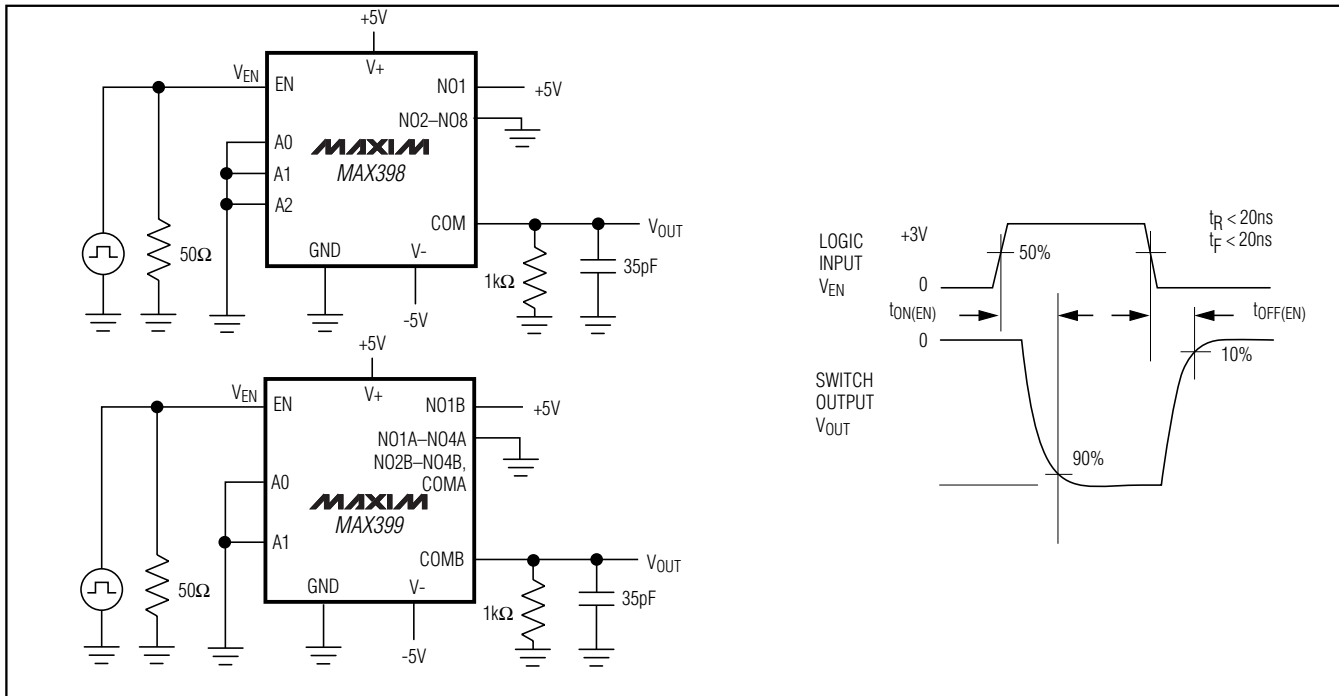


Figure 3. Enable Switching Time

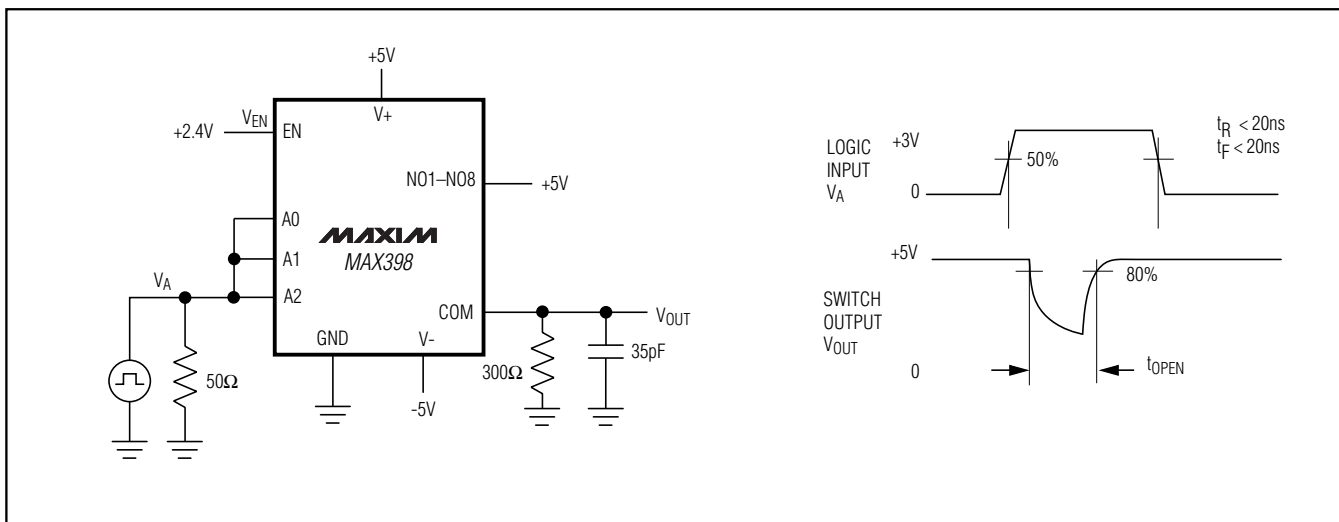


Figure 4. Break-Before-Make Interval

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Test Circuits/Timing Diagrams (continued)

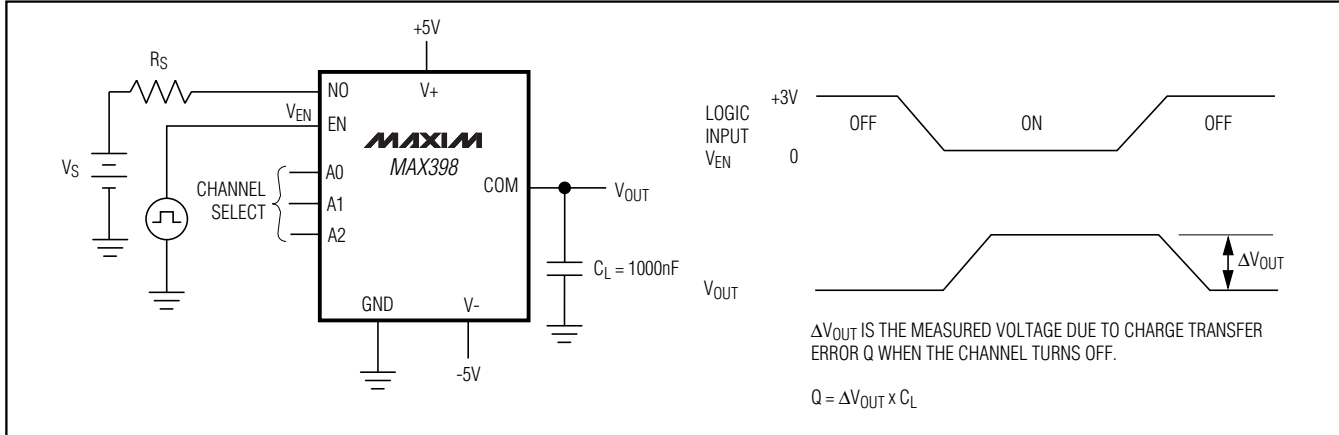


Figure 5. Charge Injection

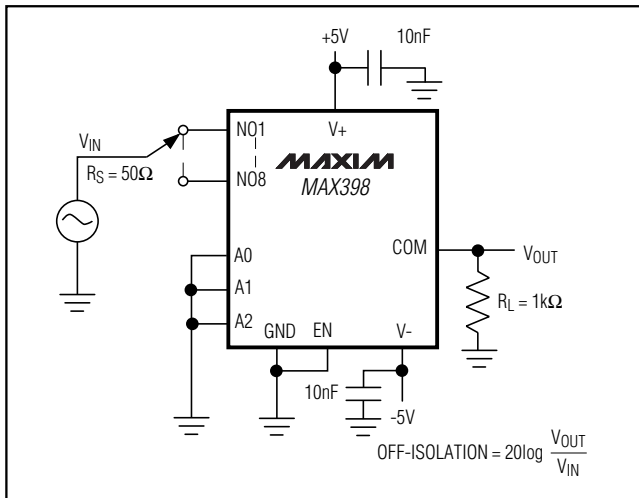


Figure 6. Off-Isolation

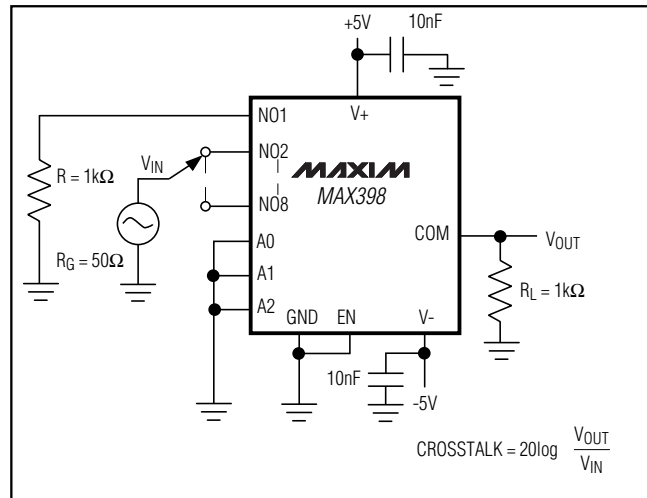


Figure 7. Crosstalk

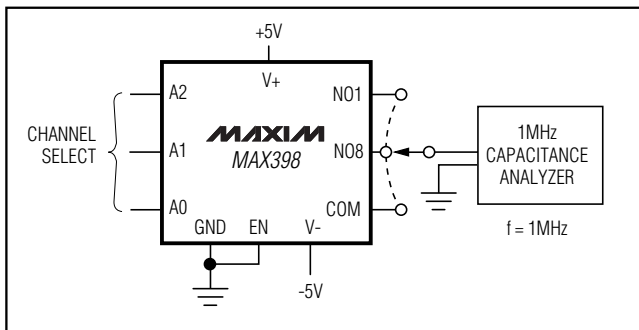


Figure 8. NO/COM Capacitance

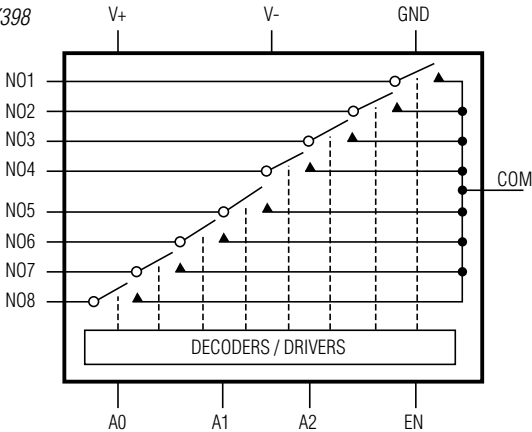
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Functional Diagrams/Truth Tables

MAX398/MAX399

MAXIM

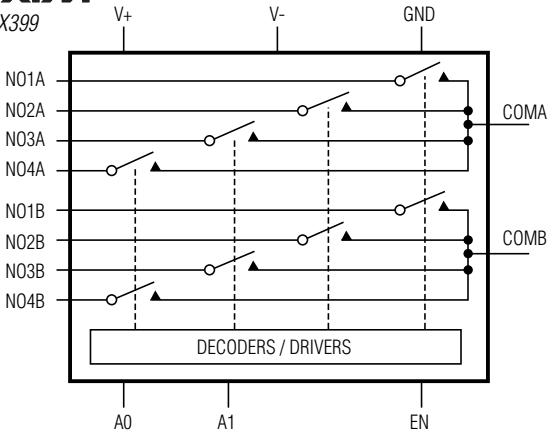
MAX398



MAX398				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAXIM

MAX399



MAX399			
A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8\text{ V}$, LOGIC "1" $V_{AH} \geq +2.4\text{ V}$

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX399CGE	0°C to +70°C	16 QFN-EP*	G1655-3
MAX399CEE	0°C to +70°C	16 QSOP	E16-1
MAX399CSE	0°C to +70°C	16 Narrow	S16-1
MAX399CPE	0°C to +70°C	16 Plastic	P16-1
MAX399C/D	0°C to +70°C	Dice**	—
MAX399EGE	-40°C to +85°C	16 QFN-EP*	G1655-3
MAX399EEE	-40°C to +85°C	16 QSOP	E16-1
MAX399ESE	-40°C to +85°C	16 Narrow	S16-1
MAX399EPE	-40°C to +85°C	16 Plastic	P16-1
MAX399EJE	-40°C to +85°C	16 CERDIP†	J16-1
MAX399MJE	-55°C to +125°C	16 CERDIP†	J16-1

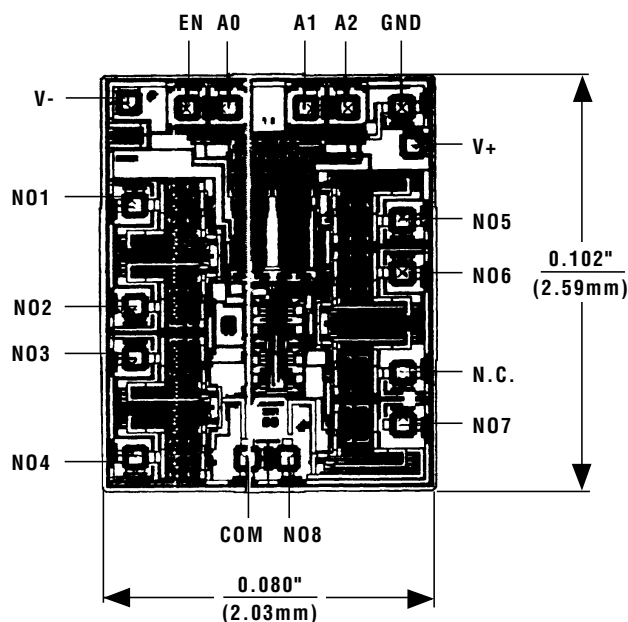
*EP = Exposed pad.

**Contact factory for dice specifications.

†Contact factory for package availability.

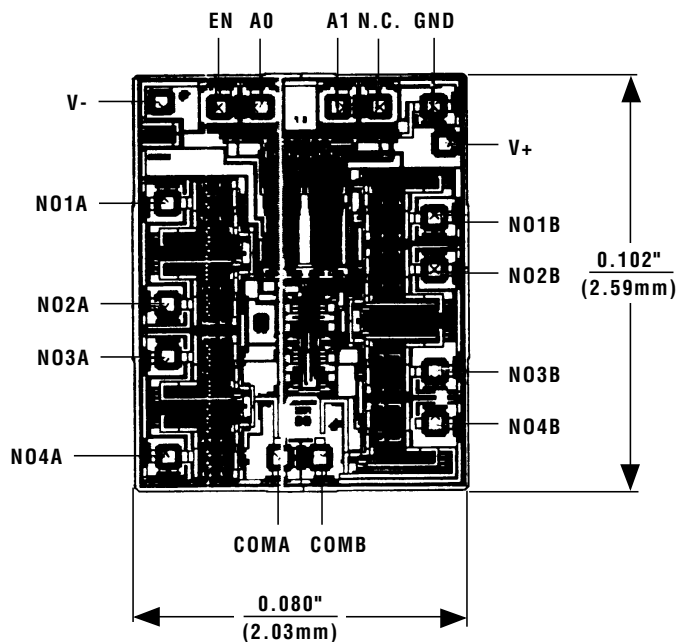
Chip Topographies

MAX398



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+

MAX399

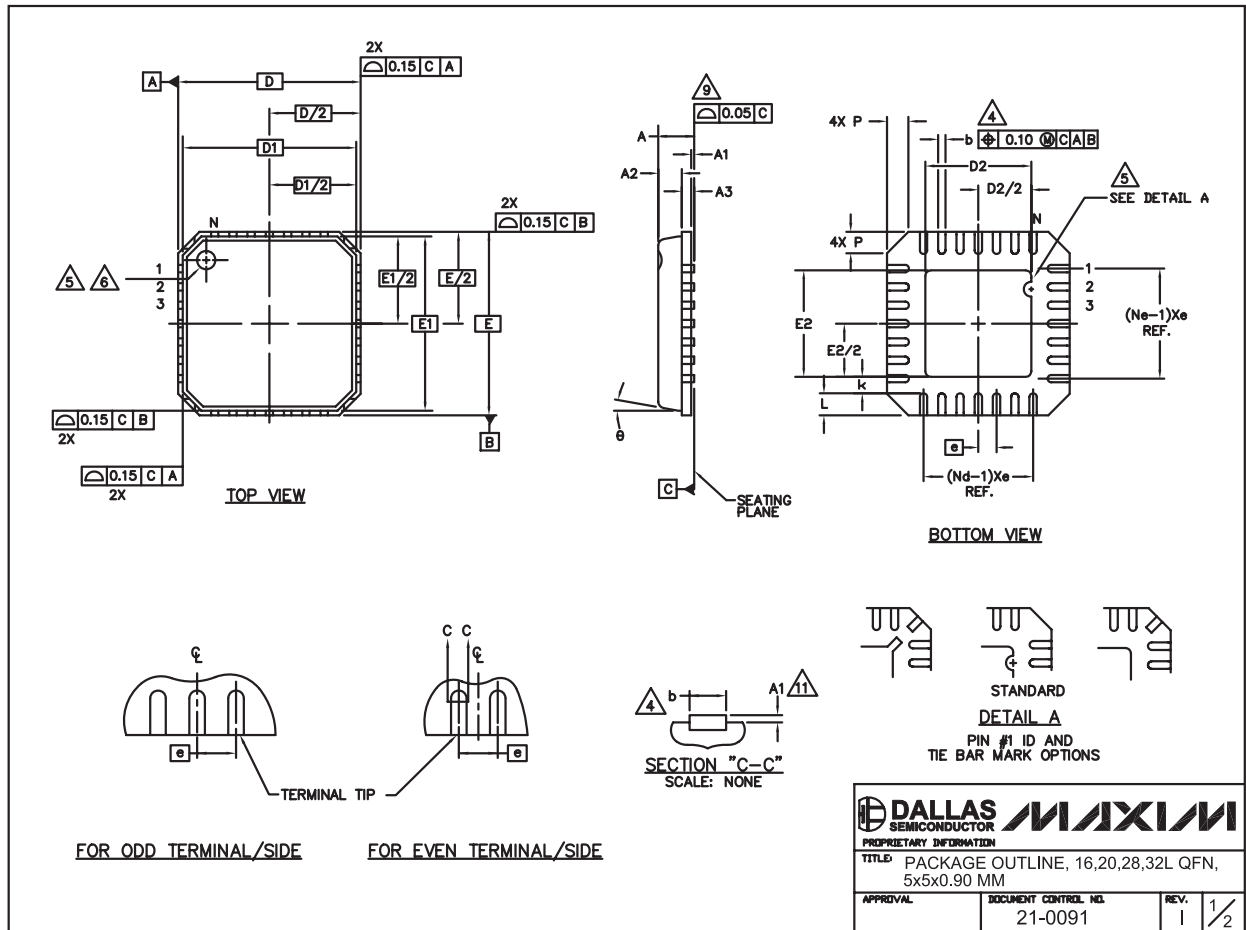


TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
g	0"		12"	0"		12"	0"		12"	0"		12"

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

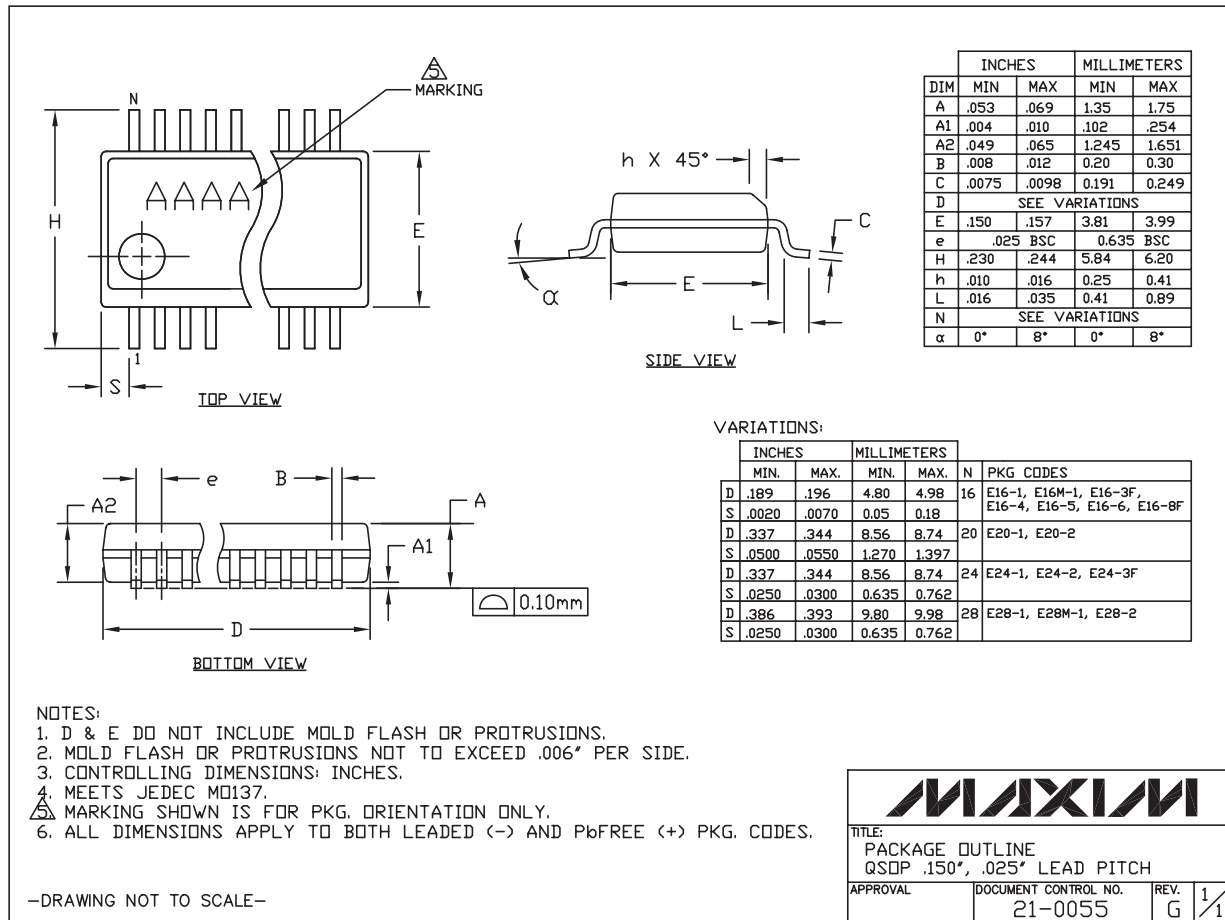
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. — 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0091	1	2/2

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



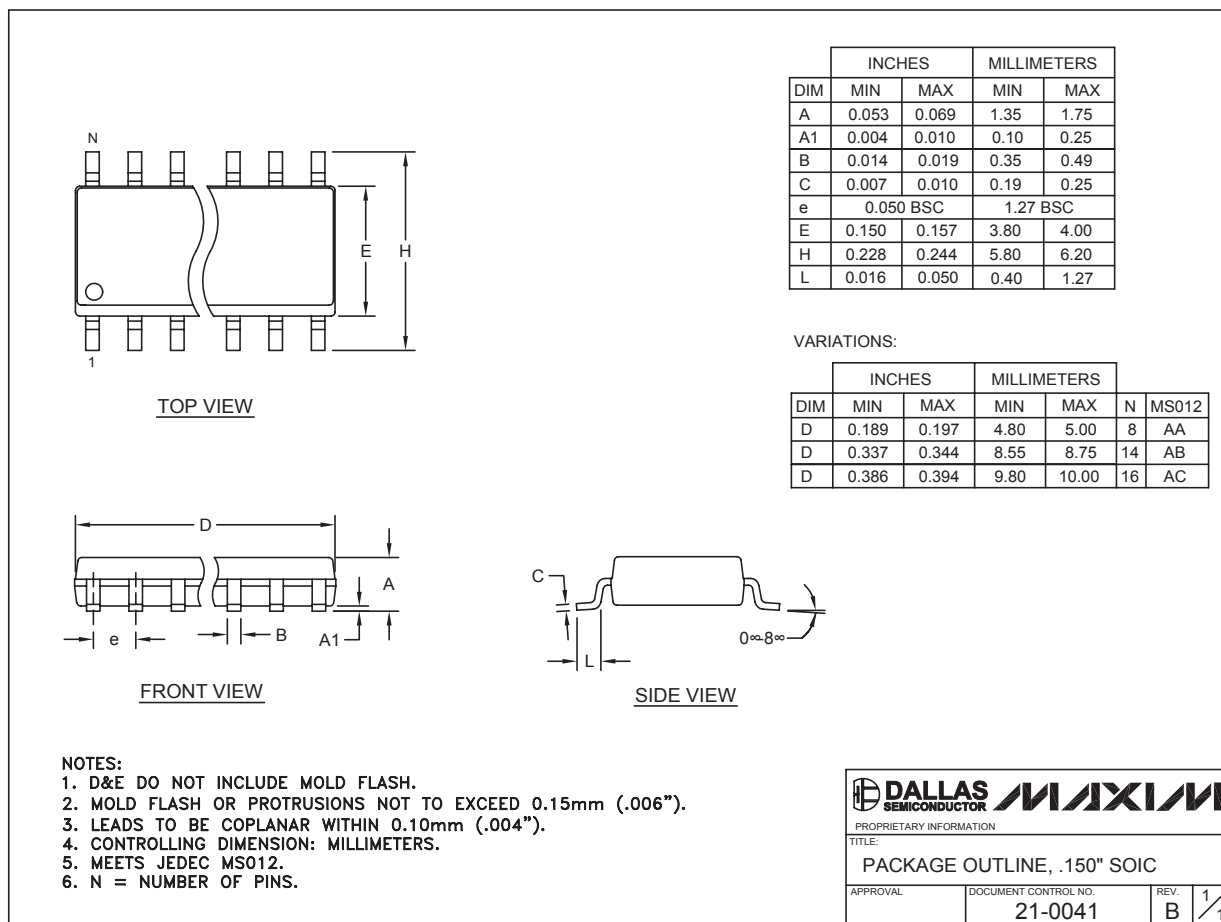
QSOPEPS

MAX398/MAX399

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

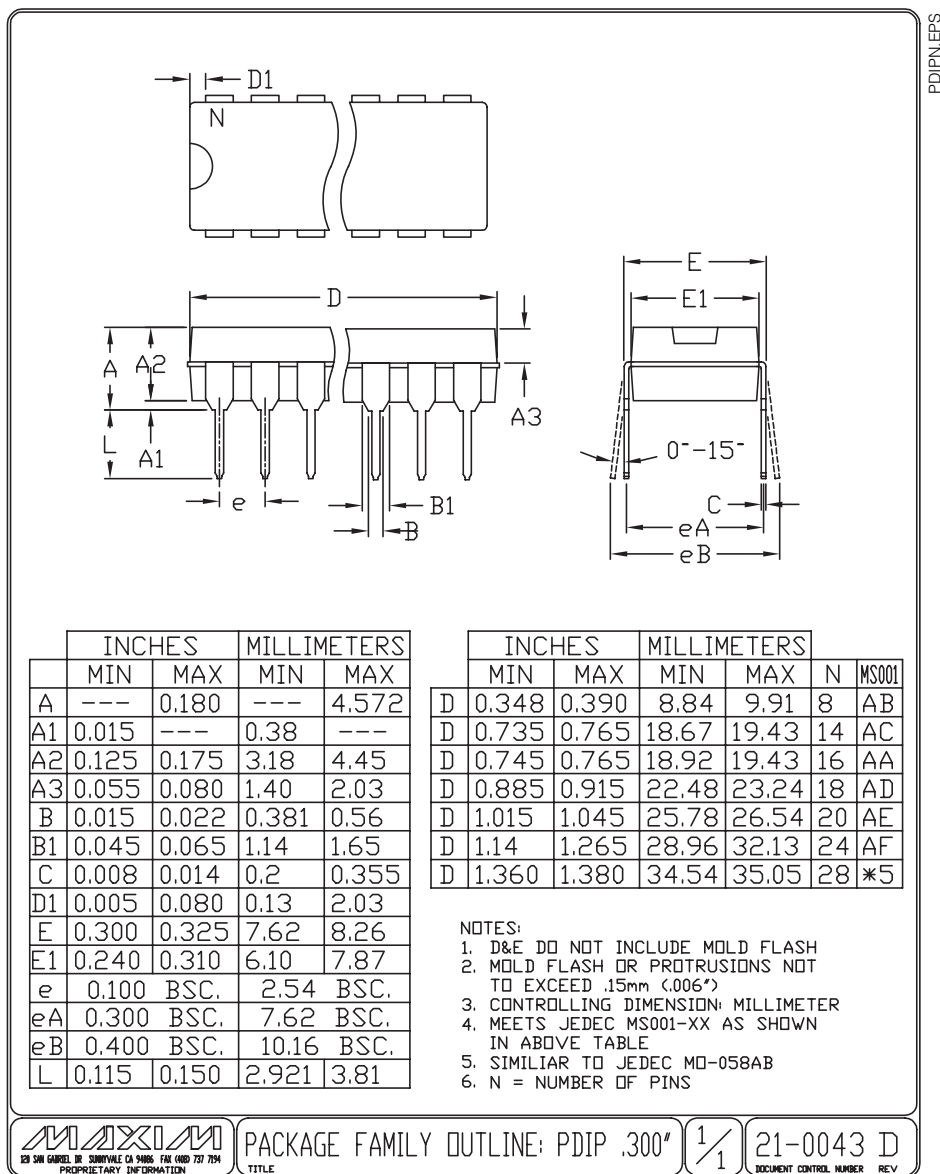


SOICN EPS

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

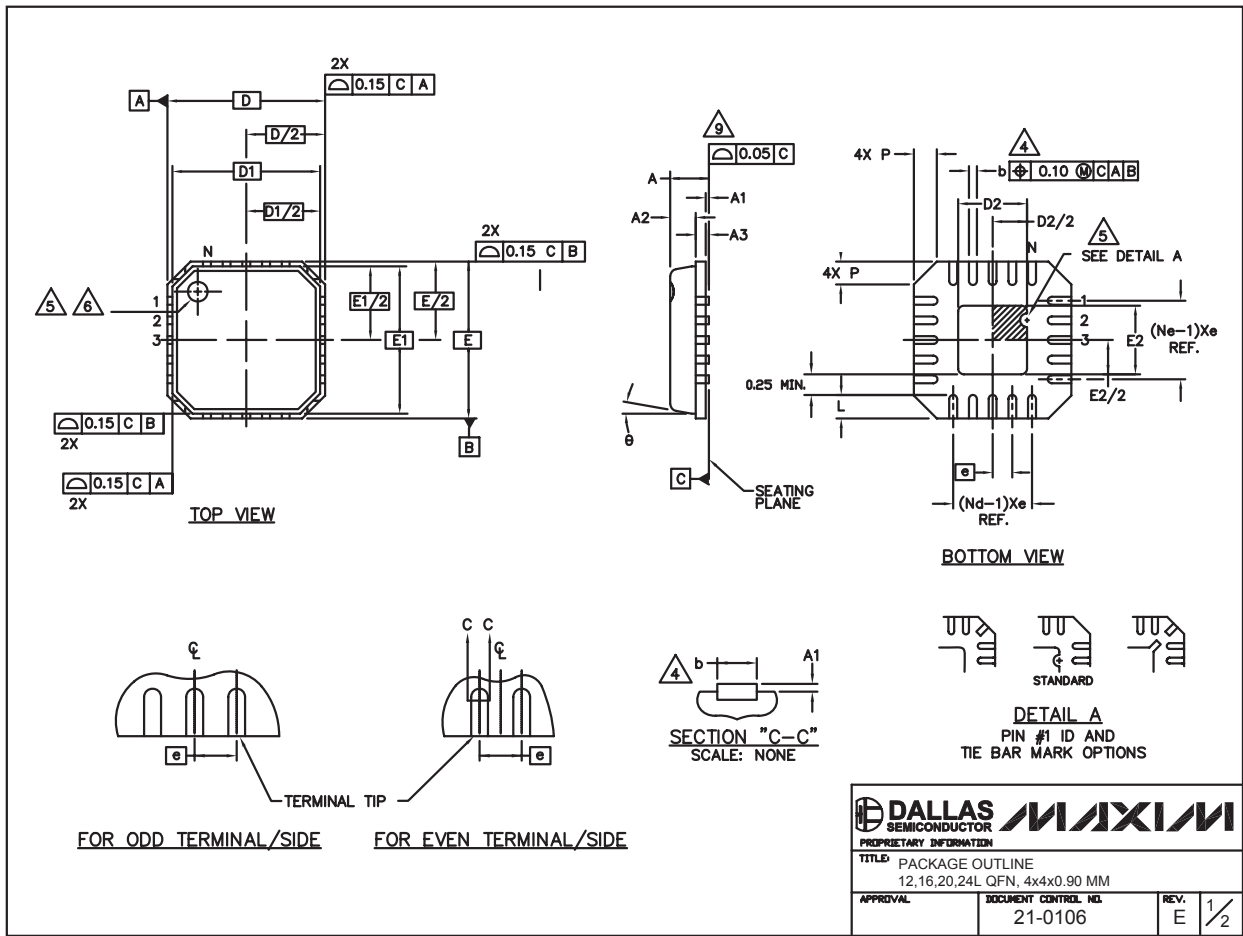


MAX398/MAX399

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX398/MAX399

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. — 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

	COMMON DIMENSIONS			N _{TE}
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3	0.20 REF.			
D	4.00 BSC			
D1	3.75 BSC			
F	4.00 BSC			
E1	3.75 BSC			
θ	0°	—	12°	
P	0.24	0.42	0.60	

S V Q	PITCH VARIATION A			N _{TE}	S V Q	PITCH VARIATION B			N _{TE}	S V Q	PITCH VARIATION C			N _{TE}	S V Q	PITCH VARIATION D			N _{TE}
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
□	0.80 BSC				□	0.65 BSC				□	0.50 BSC				□	0.50 BSC			
N	12			3	N	16			3	N	20			3	N	24			3
Nd	3			3	Nd	4			3	Nd	5			3	Nd	6			3
Ne	3			3	Ne	4			3	Ne	5			3	Ne	6			3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PKG. CODE	EXPOSED PAD VARIATION			MIN.	NOM.	MAX.
	D2	E2				
G1244-2	1.95	2.10	2.25	1.95	2.10	2.25
G1644-1	1.95	2.10	2.25	1.95	2.10	2.25
G2044-3	1.95	2.10	2.25	1.95	2.10	2.25
G2044-4	1.55	1.70	1.85	1.55	1.70	1.85
G2444-1	1.95	2.10	2.25	1.95	2.10	2.25

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0106	REV. E	2/2

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/94	–	—
1	9/94	Initial release of data sheet	–
2	7/95	–	–
3	7/96	–	–
4	5/99	Errors in commercial data	–
5	6/99	Add QSOP Package	–
6	10/01	Add QFN Package	–
7	1/07	Add Exposed Pad info for QFN	–
8	6/07	Exposed pad designation	1, 7, 12

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