

## HCPL-7723/0723

### 50-MBd 2-ns PWD High-Speed CMOS Optocoupler

#### Description

Available in either 8-pin DIP or SO.8 package style respectively, the Broadcom<sup>®</sup> HCPL-7723 or HCPL-0723 optocoupler utilize the latest CMOS IC technology to achieve outstanding speed performance of minimum 50 MBd data rate and 2-ns maximum pulse width distortion.

Basic building blocks of HCPL-7723/0723 are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

**CAUTION!** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

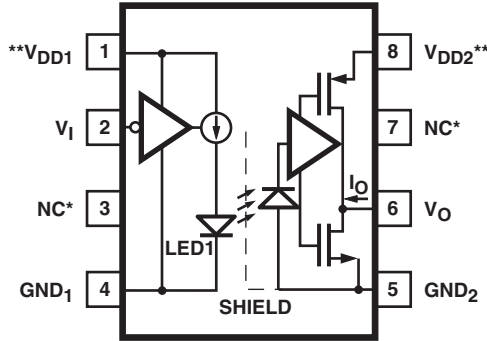
#### Features

- +5V CMOS compatibility
- High speed: 50 MBd min.
- 2-ns max. pulse width distortion
- 22-ns max. propagation delay
- 16 ns max. propagation delay skew
- 10 kV/ $\mu$ s min. common mode rejection
- -40 to 85°C temperature range
- Safety and regulatory approvals:
  - UL recognized:
    - 5000  $V_{\text{rms}}$  for 1 min. per UL1577 for HCPL-7723 for option 020
    - 3750  $V_{\text{rms}}$  for 1 min. per UL1577 for HCPL-0723
  - CSA component acceptance notice #5
  - IEC/EN/DIN EN 60747-5-5
    - $V_{\text{iorm}} = 630 V_{\text{peak}}$  for HCPL-7723 option 060
    - $V_{\text{iorm}} = 567 V_{\text{peak}}$  for HCPL-0723 option 060

#### Applications

- Digital fieldbus isolation: CC-Link, DeviceNet, Profibus, SDS, Isolated A/D or D/A conversion
- Multiplexed data transmission
- High-speed digital input/output
- Computer peripheral interface
- Microprocessor system interface

# Functional Diagram



\* PIN 3 IS THE ANODE OF THE INTERNAL LED AND MUST BE LEFT UNCONNECTED FOR GUARANTEED DATASHEET PERFORMANCE. PIN 7 IS NOT CONNECTED INTERNALLY.

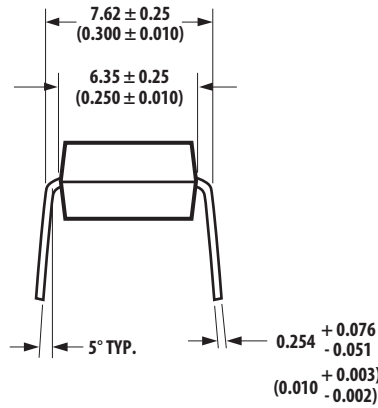
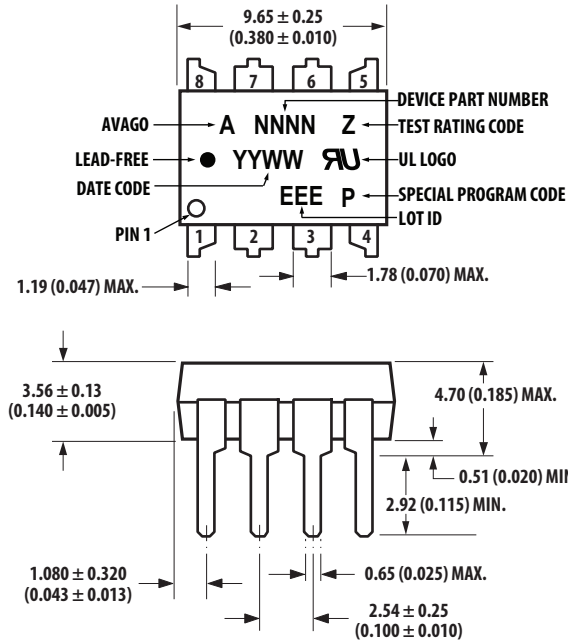
\*\* A 0.01 to 0.1  $\mu$ F BYPASS CAPACITOR MUST BE CONNECTED AS CLOSE AS POSSIBLE BETWEEN PINS 1 AND 4, AND 5 AND 8.

# Truth Table

| V <sub>I</sub> Input | LED1 | V <sub>O</sub> Output |
|----------------------|------|-----------------------|
| H                    | OFF  | H                     |
| L                    | ON   | L                     |

# Package Outline Drawings

## HCPL-7723 8-Pin DIP Package



DIMENSIONS IN MILLIMETERS (INCHES).

\*MARKING CODE LETTER FOR OPTION NUMBERS

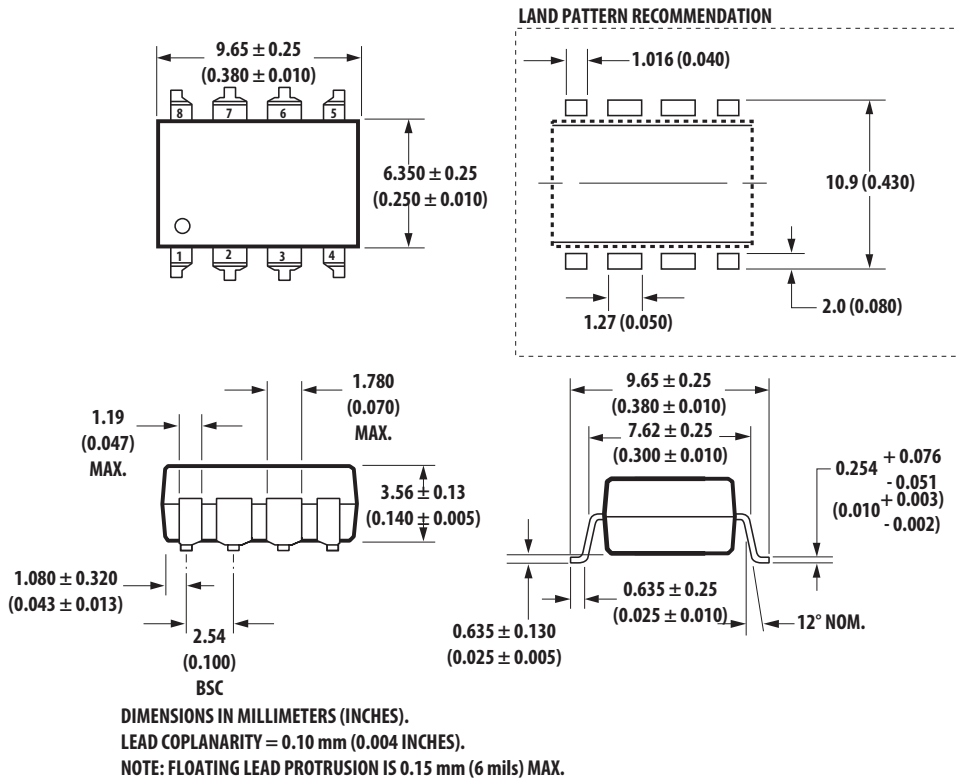
"L" = OPTION 020

"V" = OPTION 060

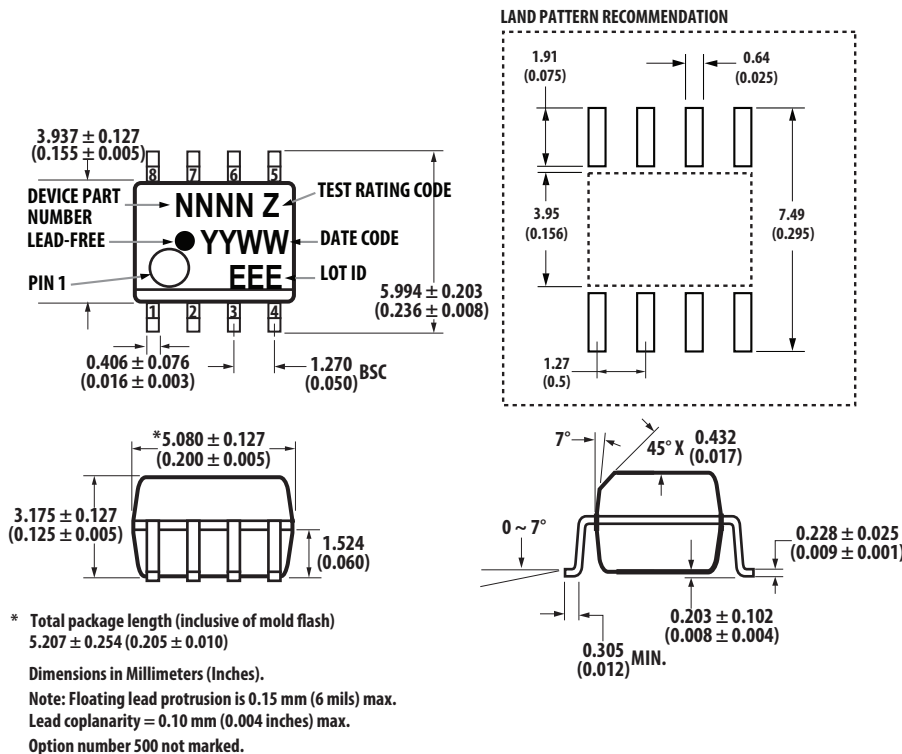
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

# HCPL-7723 Package with Gull Wing Surface Mount Option 300



# HCPL-0723 Small Outline SO-8 Package



## Device Selection Guide

| 8-Pin DIP (300 mil) | Small Outline SO-8 |
|---------------------|--------------------|
| HCPL-7723           | HCPL-0723          |

## Ordering Information

HCPL-0723 and HCPL-7723 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

| Part Number | Option         |                    | Package       | Surface Mount | Gull Wing | Tape and Reel | UL5000 Vrms / 1 Minute Rating | IEC/EN/DIN EN 60747-5-5 | Quantity      |
|-------------|----------------|--------------------|---------------|---------------|-----------|---------------|-------------------------------|-------------------------|---------------|
|             | RoHS Compliant | Non RoHS Compliant |               |               |           |               |                               |                         |               |
| HCPL-7723   | -000E          | no option          | 300 mil DIP-8 |               |           |               |                               |                         | 50 per tube   |
|             | -300E          | -300               |               | X             | X         |               |                               |                         | 50 per tube   |
|             | -500E          | -500               |               | X             | X         | X             |                               |                         | 1000 per reel |
|             | -020E          | -020               |               |               |           |               | X                             |                         | 50 per tube   |
|             | -320E          | -320               |               | X             | X         |               | X                             |                         | 50 per tube   |
|             | -520E          | -520               |               | X             | X         | X             | X                             |                         | 1000 per reel |
|             | -060E          | -060               |               |               |           |               |                               | X                       | 50 per tube   |
|             | -360E          | -360               |               | X             | X         |               |                               | X                       | 50 per tube   |
|             | -560E          | -560               |               | X             | X         | X             |                               | X                       | 1000 per reel |
| HCPL-0723   | -000E          | no option          | SO-8          | X             |           |               |                               |                         | 100 per tube  |
|             | -500E          | -500               |               | X             |           | X             |                               |                         | 1500 per reel |
|             | -060E          | -060               |               | X             |           |               |                               | X                       | 100 per tube  |
|             | -560E          | -560               |               | X             |           | X             |                               | X                       | 1500 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-7723-560E to order product of Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

Example 2:

HCPL-0723 to order product of Small Outline SO-8 package in Tube packaging and non RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

**NOTE:** The notation #XXX is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use -XXE.

## Regulatory Information

The HCPL-7723/0723 have been approved by the following organizations:

- **UL** — Recognized under UL1577, component recognition program, File E55361.
- **CSA** — Approval under CSA Component Acceptance Notice #5, File CA88324.
- **IEC/EN/DIN EN 60747-5-5** — Approved with Maximum Working Insulation Voltage:
  - $V_{iorm} = 567 V_{peak}$  for HCPL-0723
  - $V_{iorm} = 630 V_{peak}$  for HCPL-7723

## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Insulation and Safety Related Specifications

| Parameter   | Symbol | Value |      | Unit | Conditions  |
|---|--------|-------|------|------|---|
|   |        | 7723  | 0723 |      |   |
| Minimum External Air Gap (Clearance)              | L(I01) | 7.1   | 4.9  | mm   | Measured from input terminals to output terminals, shortest distance through air.             |
| Minimum External Tracking (Creepage)              | L(I02) | 7.4   | 4.8  | mm   | Measured from input terminals to output terminals, shortest distance path along body.         |
| Minimum Internal Plastic Gap (Internal Clearance) |        | 0.08  | 0.08 | mm   | Insulation thickness between emitter and detector; also known as distance through insulation. |
| Tracking Resistance (Comparative Tracking Index)  | CTI    | ≥175  | ≥175 | V    | DIN IEC 112/VDE 0303 Part 1.  |
| Isolation Group                                   |        | IIIa  | IIIa |      | Material Group (DIN VDE 0110, 1/89, Table 1).   |

All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs, which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

| Description   | Symbol          | Characteristic              |                              | Unit        |
|---|-----------------|-----------------------------|------------------------------|-------------|
|   |                 | HCPL-7723                   | HCPL-0723                    |             |
| Installation Classification per DIN VDE 0110/39, Table 1<br>For Rated Mains Voltage $\leq 150V_{rms}$<br>For Rated Mains Voltage $\leq 300V_{rms}$<br>For Rated Mains Voltage $\leq 600V_{rms}$ |                 | I – IV<br>I – III<br>I – IV | I – IV<br>I – III<br>I – III |             |
| Climatic Classification   |                 | 55/85/21                    | 55/85/21                     |             |
| Pollution Degree (DIN VDE 0110/39)  |                 | 2                           | 2                            |             |
| Maximum Working Insulation Voltage  | $V_{IORM}$      | 630                         | 567                          | $V_{peak}$  |
| Input to Output Test Voltage, Method b <sup>a</sup><br>$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1s$ ,<br>Partial Discharge $< 5 pC$                                  | $V_{PR}$        | 1181                        | 1063                         | $V_{peak}$  |
| Input to Output Test Voltage, Method a <sup>a</sup><br>$V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10s$ ,<br>Partial Discharge $< 5 pC$                                       | $V_{PR}$        | 1008                        | 907                          | $V_{peak}$  |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60s$ )  | $V_{IOTM}$      | 8000                        | 6000                         | $V_{peak}$  |
| Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure   |                 |                             |                              |             |
| Case Temperature  | $T_S$           | 175                         | 150                          | $^{\circ}C$ |
| Input Current   | $I_{S, INPUT}$  | 230                         | 150                          | mA          |
| Output Power  | $P_{S, OUTPUT}$ | 600                         | 600                          | mW          |
| Insulation Resistance at $T_S$ , $V_{IO} = 500V$  | $R_S$           | $\geq 10^9$                 | $\geq 10^9$                  | $\Omega$    |

a. Refer to the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

**NOTE:** These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

## Absolute Maximum Ratings

| Parameter                                  | Symbol   | Min. | Max.            | Unit |
|--|--|------|-----------------|------|
| Storage Temperature                        | $T_S$  | -55  | 125             | °C   |
| Ambient Operating Temperature <sup>a</sup> | $T_A$  | -40  | 85              | °C   |
| Supply Voltages                            | $V_{DD1}, V_{DD2}$                                 | 0    | 6.0             | V    |
| Input Voltage                              | $V_I$  | -0.5 | $V_{DD1} + 0.5$ | V    |
| Output Voltage                             | $V_O$  | -0.5 | $V_{DD2} + 0.5$ | V    |
| Average Output Current                     | $I_O$  | —    | 10              | mA   |
| Lead Solder Temperature                    | 260°C for 10 sec., 1.6 mm below seating plane.     |      |                 |      |
| Solder Reflow Temperature Profile          | See <a href="#">Solder Reflow Profile</a> section. |      |                 |      |

a. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee functionality

## Recommended Operating Conditions

| Parameter                        | Symbol             | Min. | Max.      | Unit |
|----------------------------------|--------------------|------|-----------|------|
| Ambient Operating Temperature    | $T_A$              | -40  | 85        | °C   |
| Supply Voltages                  | $V_{DD1}, V_{DD2}$ | 4.5  | 5.5       | V    |
| Logic High Input Voltage         | $V_{IH}$           | 2.0  | $V_{DD1}$ | V    |
| Logic Low Input Voltage          | $V_{IL}$           | 0.0  | 0.8       | V    |
| Input Signal Rise and Fall Times | $t_{ir}, t_{if}$   | —    | 1.0       | ms   |

## Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at  $T_A = +25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = +5\text{V}$ .

| Parameter                                    | Symbol     | Min. | Typ. | Max. | Unit | Test Conditions                              |
|--|------------|------|------|------|------|--|
| Logic Low Input Supply Current <sup>a</sup>  | $I_{DD1L}$ | —    | 8.4  | 10   | mA   | $V_I = 0\text{V}$ ; <a href="#">Figure 1</a> |
| Logic High Input Supply Current <sup>a</sup> | $I_{DD1H}$ | —    | 0.6  | 3    | mA   | $V_I = V_{DD1}$ ; <a href="#">Figure 2</a>   |
| Output Supply Current                        | $I_{DD2L}$ | —    | 2.1  | 5    | mA   | <a href="#">Figure 3</a>                     |
|  | $I_{DD2H}$ | —    | 2.0  | 5    | mA   | <a href="#">Figure 4</a>                     |
| Input Current                                | $I_I$      | -10  | —    | 10   | μA   |  |
| Logic High Output Voltage                    | $V_{OH}$   | 4.4  | 5.0  | —    | V    | $I_O = -20\ \mu\text{A}$ , $V_I = V_{IH}$    |
|  |            | 4.0  | 4.8  | —    | V    | $I_O = -4\ \text{mA}$ , $V_I = V_{IH}$       |
| Logic Low Output Voltage                     | $V_{OL}$   | —    | 0    | 0.1  | V    | $I_O = 20\ \mu\text{A}$ , $V_I = V_{IL}$     |
|  |            | —    | 0.5  | 1.0  | V    | $I_O = 4\ \text{mA}$ , $V_I = V_{IL}$        |

a. The LED is ON when  $V_I$  is low and OFF when  $V_I$  is high.

## Switching Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at  $T_A = +25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = +5\text{V}$ .

| Parameter  | Symbol    | Min. | Typ. | Max. | Unit              | Test Conditions   |
|--|-----------|------|------|------|-------------------|---|
| Propagation Delay Time to Logic Low Output <sup>a</sup>          | $t_{PHL}$ | —    | 16   | 22   | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels; <a href="#">Figure 5</a>                               |
| Propagation Delay Time to Logic High Output <sup>a</sup>         | $t_{PLH}$ | —    | 16   | 22   | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels; <a href="#">Figure 5</a>                               |
| Pulse Width  | PW        | 20   | —    | —    | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels   |
| Maximum Data Rate  |           | 50   | —    | —    | MBd               | $C_L = 15\text{ pF}$ CMOS Signal Levels   |
| Pulse Width Distortion <sup>b</sup> $ t_{PHL} - t_{PLH} $        | $ PWD $   | —    | 1    | 2    | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels; <a href="#">Figure 6</a>                               |
| Propagation Delay Skew <sup>c</sup>                              | $t_{PSK}$ | —    | —    | 16   | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels   |
| Output Rise Time (10% to 90%)                                    | $t_R$     | —    | 8    | —    | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels   |
| Output Fall Time (90% to 10%)                                    | $t_F$     | —    | 6    | —    | ns                | $C_L = 15\text{ pF}$ CMOS Signal Levels   |
| Common Mode Transient Immunity at Logic High Output <sup>d</sup> | $ CM_H $  | 10   | 15   | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{V}$ , $T_A = 25^\circ\text{C}$ ,<br>$V_I = V_{DD1}$ , $V_O > 0.8 V_{DD2}$   |
| Common Mode Transient Immunity at Logic Low Output <sup>d</sup>  | $ CM_L $  | 10   | 15   | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{V}$ , $T_A = 25^\circ\text{C}$ ,<br>$V_I = 0\text{V}$ , $V_O < 0.8\text{V}$ |

- $t_{PHL}$  propagation delay is measured from the 50% level on the falling edge of the  $V_I$  signal to the 50% level of the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level on the rising edge of the  $V_I$  signal to the 50% level of the rising edge of the  $V_O$  signal.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
- $t_{PSK}$  is equal to the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8V_{DD2}$ .  $CM_L$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8\text{V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.



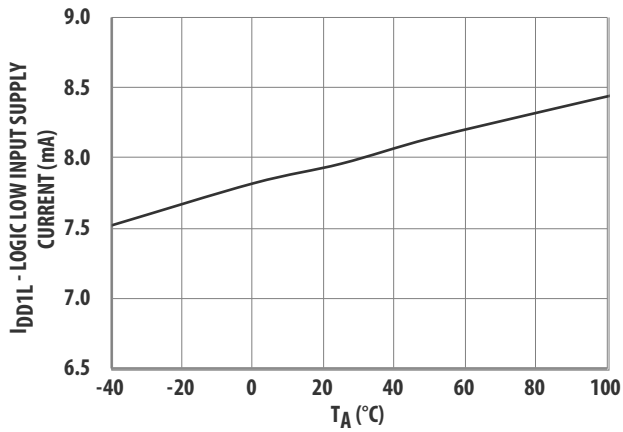
## Package Characteristics

All typical specifications are at  $T_A = 25^\circ\text{C}$ .

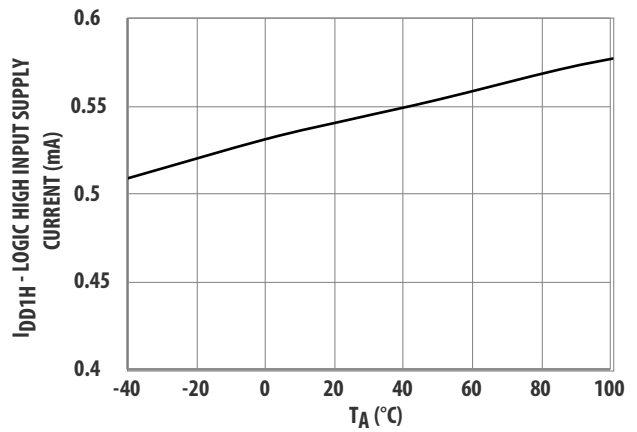
| Parameter   |            | Symbol         | Min. | Typ.      | Max. | Unit               | Test Conditions                                     |
|---|------------|----------------|------|-----------|------|--------------------|---|
| Input-Output Momentary Withstand Voltage <sup>a, b, c</sup> | -7723      | $V_{ISO}$      | 3750 | —         | —    | $V_{rms}$          | RH $\leq$ 50%, t = 1 min, $T_A = 25^\circ\text{C}$  |
|   | Option 020 |                | 5000 | —         | —    |                    |   |
|   | -0723      |                | 3750 | —         | —    |                    |   |
| Input-Output Resistance <sup>a</sup>                        |            | $R_{I-O}$      | —    | $10^{12}$ | —    | $\Omega$           | $V_{I-O} = 500\text{ Vdc}$                          |
| Input-Output Capacitance                                    |            | $C_{I-O}$      | —    | 0.6       | —    | pF                 | f = 1 MHz   |
| Input Capacitance <sup>d</sup>                              |            | $C_I$          | —    | 3.0       | —    | pF                 |   |
| Input IC Junction-to-Case Thermal Resistance                | -7723      | $\theta_{jci}$ | —    | 145       | —    | $^\circ\text{C/W}$ | Thermocouple located at center underside of package |
|   | -0723      |                | —    | 160       | —    |                    |   |
| Output IC Junction-to-Case Thermal Resistance               | -7723      | $\theta_{jco}$ | —    | 145       | —    | $^\circ\text{C/W}$ |   |
|   | -0723      |                | —    | 135       | —    |                    |   |
| Package Power Dissipation                                   |            | $P_{PD}$       | —    | —         | 150  | mW                 |   |

- a. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- b. In accordance with UL1577, each HCPL-0723 is proof tested by applying an insulation test voltage  $\geq 4500 V_{rms}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ ). Each HCPL-7723 is proof tested by applying an insulation test voltage  $\geq 4500 V_{rms}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ .)
- c. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, Optocoupler Input-Output Endurance Voltage.
- d.  $C_I$  is the capacitance measured at pin 2 ( $V_I$ ).

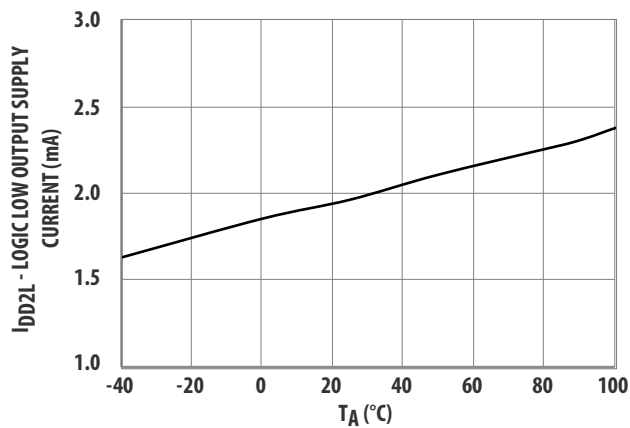
**Figure 1: Typical Logic Low Input Supply Current vs. Temperature**



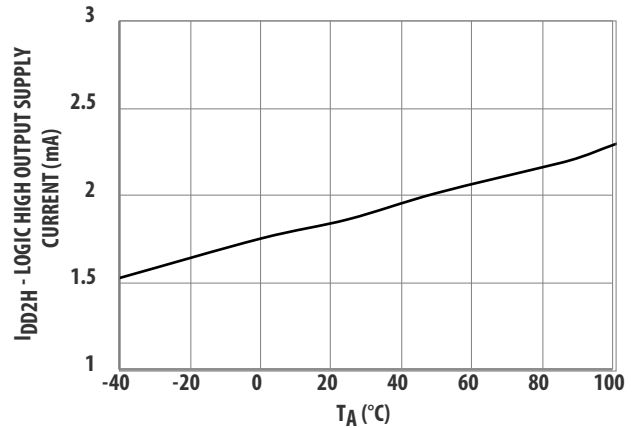
**Figure 2: Typical Logic High Input Supply Current vs. Temperature**



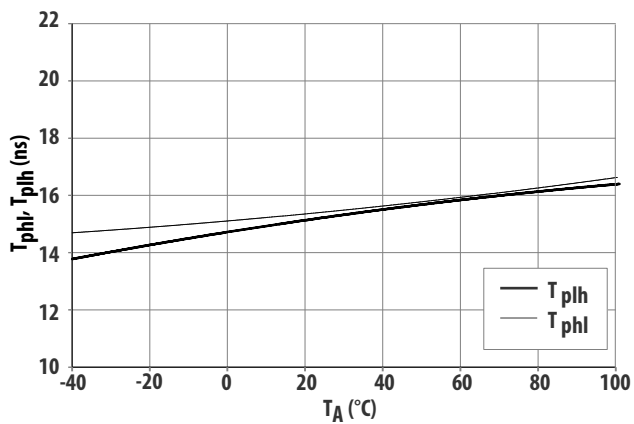
**Figure 3: Typical Logic Low Output Supply Current vs. Temperature**



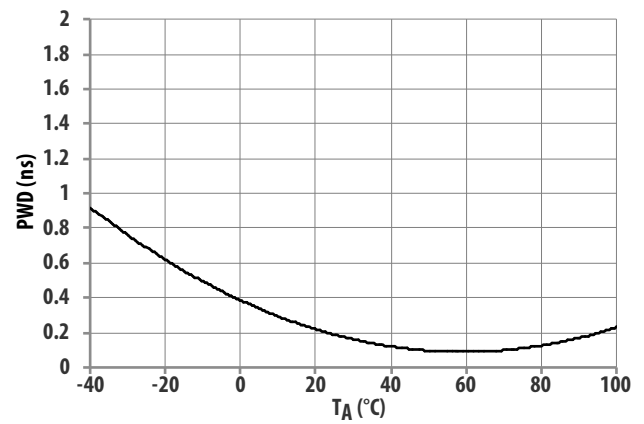
**Figure 4: Typical Logic High Output Supply Current vs. Temperature**



**Figure 5: Typical Propagation Delay vs. Temperature**



**Figure 6: Typical Pulse Width Distortion vs. Temperature**



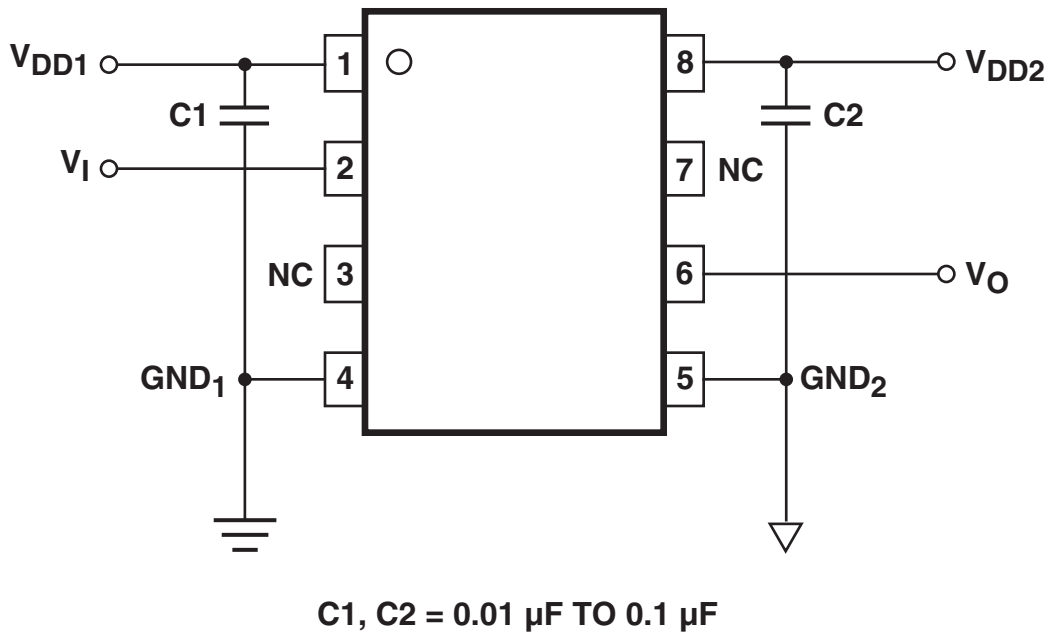
# Application Information

## Bypassing and PC Board Layout

The HCPL-7723/0723 optocouplers are extremely easy to use. No external interface circuitry is required because the HCPL-7723/0723 use high-speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in [Figure 7](#), the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . Each capacitor should be placed as close as possible to the input and output power-supply pins of the optocoupler.

**Figure 7: Functional Diagram**



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