# 1ch Gate Driver Providing Galvanic Isolation 2500Vrms Isolation Voltage

## BM60051FV-C

### General Description

The BM60051FV-C is a gate driver with an isolation voltage of 2500Vrms, I/O delay time of 260ns, minimum input pulse width of 180ns, and incorporates the fault signal output function, under voltage lockout (UVLO) function, short circuit protection (SCP) function, active miller clamping function, temperature monitoring function, switching controller function and output state feedback function.

### Key Specifications

| | |
|---|---|
| ■Isolation Voltage: | 2500 [Vrms] (Max) |
| ■Maximum Gate Drive Voltage: | 24 [V] (Max) |
| ■I/O Delay Time: | 260 [ns] (Max) |
| ■Minimum Input Pulse Width: | 180 [ns] (Max) |

### Packages

| | W(Typ) x D(Typ) x H(Max) |
|---|---|
| SSOP-B28W | 9.2mm x 10.4mm x 2.4mm |

### Features

- ■ Fault signal output function
- ■Under voltage lockout function
- ■Short circuit protection function
- ■Active Miller Clamping
- ■Temperature monitor
- ■Switching controller
- ■Output State Feedback Function
- ■UL1577 Recognized:File No. E356010
- ■AEC-Q100 Qualified (Note 1)
  (Note 1:Grade1)

### Applications

- ■ Automotive isolated IGBT/MOSFET inverter gate drive.
- ■ Automotive DC-DC converter.
- ■ Industrial inverters system.
- ■ UPS system.

### Typical Application Circuit

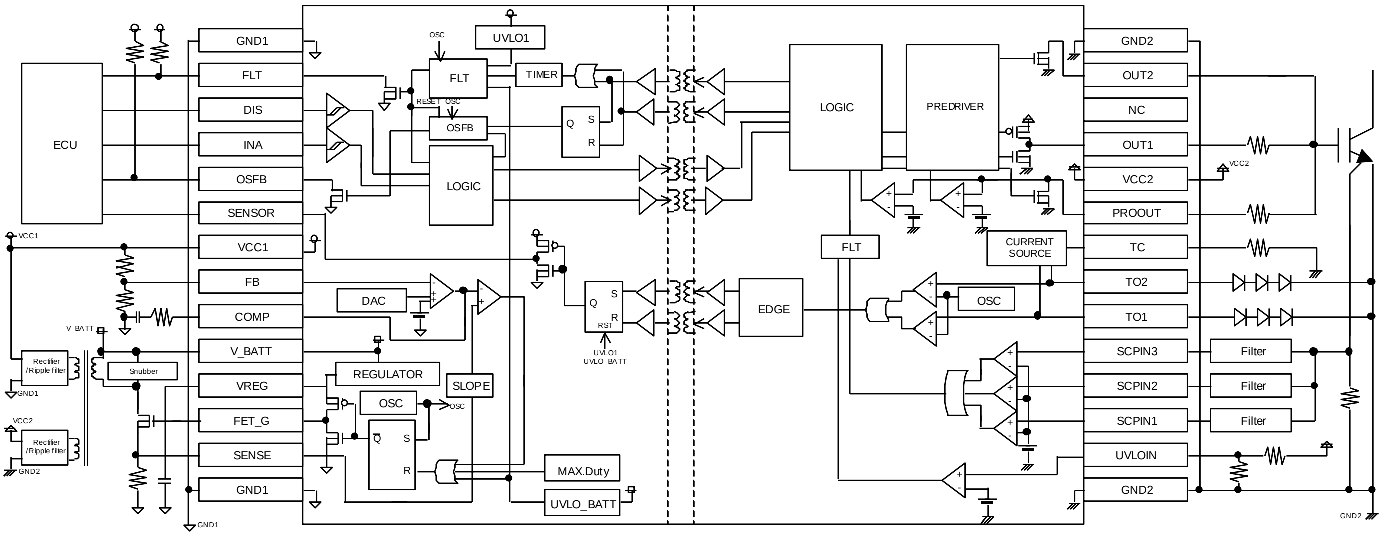



Figure 1. Typical Application Circuit

〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays

## Recommended Range Of External Constants

| Pin Name | Symbol | Recommended Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| TC(Note2) | $R_{TC}$ | 1.25 | - | 50 | kΩ |
| TC(Note3) | $R_{TC}$ | 0.1 | 1 | 10 | MΩ |
| VBATT | $C_{VBATT}$ | 3 | - | - | µF |
| VCC1 | $C_{VCC1}$ | 0.2 | - | - | µF |
| VCC2 | $C_{VCC2}$ | 0.4 | - | - | µF |
| VREG | $C_{VREG}$ | 0.1 | 1 | 10 | µF |

(Note2) Use Temperature monitor
(Note3) No use Temperature monitor

## Pin Configuration
(TOP VIEW)

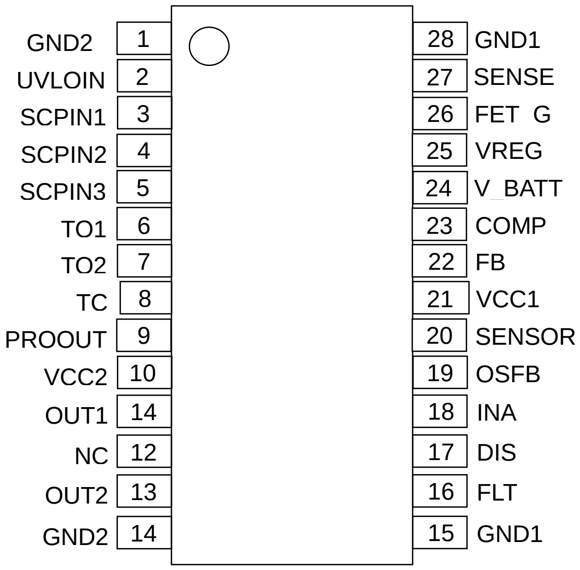



Figure 2. Pin configuration

## Pin Descriptions

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | GND2 | Output-side ground pin |
| 2 | UVLOIN | Output-side UVLO setting pin |
| 3 | SCPIN1 | Short circuit current detection pin 1 |
| 4 | SCPIN2 | Short circuit current detection pin 2 |
| 5 | SCPIN3 | Short circuit current detection pin 3 |
| 6 | TO1 | Constant current output pin / sensor voltage input pin 1 |
| 7 | TO2 | Constant current output pin / sensor voltage input pin 2 |
| 8 | TC | Constant current setting resistor connection pin |
| 9 | PROOUT | Soft turn-OFF pin /Gate voltage input pin |
| 10 | VCC2 | Output-side power supply pin |
| 11 | OUT1 | Output pin |
| 12 | NC | No connect |
| 13 | OUT2 | Output pin for Miller Clamp |
| 14 | GND2 | Output-side ground pin |
| 15 | GND1 | Input-side ground pin |
| 16 | FLT | Fault output pin |
| 17 | DIS | Input enabling signal input pin |
| 18 | INA | Control input pin |
| 19 | OSFB | Output state feedback output pin |
| 20 | SENSOR | Temperature information output pin |
| 21 | VCC1 | Input-side power supply pin |
| 22 | FB | Error amplifier inverting input pin for switching controller |
| 23 | COMP | Error amplifier output pin for switching controller |
| 24 | V_BATT | Main power supply pin |
| 25 | VREG | Power supply pin for driving MOS FET for switching controller |
| 26 | FET_G | MOS FET control pin for switching controller |
| 27 | SENSE | Current feedback resistor connection pin for switching controller |
| 28 | GND1 | Input-side ground pin |

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Main Power Supply Voltage | $V_{BATTMAX}$ | -0.3 to+40.0(Note 4) | V |
| Input-Side Control Block Supply Voltage | $V_{CC1MAX}$ | -0.3 to +7.0(Note 4) | V |
| Output-Side Supply Voltage | $V_{CC2MAX}$ | -0.3 to +30.0(Note 5) | V |
| INA, DIS Pin Input Voltage | $V_{INMAX}$ | -0.3 to +$V_{CC1}$+0.3V or +7.0V(Note 4) | V |
| FLT, OSFB Pin Input Voltage | $V_{FLTMAX}$ | -0.3 to +7.0V (Note 4) | V |
| FLT Pin, OSFB Pin Output Current | $I_{FLT}$ | 10 | mA |
| SENSOR Pin Output Current | $I_{SENSOR}$ | 10 | mA |
| FB Pin Input Voltage | $V_{FBMAX}$ | -0.3 to +$V_{CC1}$+0.3V or +7.0V(Note 4) | V |
| FED_G Pin Output Current (Peak5μs) | $I_{FET\_GPEAK}$ | 1000 | mA |
| SCPIN1 Pin, SCPIN2 Pin, SCPIN3 Pin Input Voltage | $V_{SCPINMAX}$ | -0.3 to +6.0(Note 5) | V |
| UVLOIN Pin Input Voltage | $V_{UVLOINMAX}$ | -0.3 to $V_{CC2}$+0.3(Note 5) | V |
| TO1 Pin, To2 Pin Input Voltage | $V_{TOMAX}$ | -0.3 to $V_{CC2}$+0.3(Note 5) | V |
| TO1 Pin, TO2 Pin Output Current | $I_{TOMAX}$ | 8 | mA |
| OUT1 Pin Output Current (Peak5μs) | $I_{OUT1PEAK}$ | 5000(Note 6) | mA |
| OUT2 Pin Output Current (Peak5μs) | $I_{OUT2PEAK}$ | 5000(Note 6) | mA |
| PROOUT Pin Output Current (Peak5μs) | $I_{PROOUTPEAK5}$ | 2500(Note 6) | mA |
| PROOUT Pin Output Current (Peak10μs) | $I_{PROOUTPEAK10}$ | 1000(Note 6) | mA |
| Power Dissipation | Pd | 1.12(Note 7) | W |
| Operating Temperature Range | Topr | -40 to +125 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Junction Temperature | Tjmax | +150 | °C |

(Note 4) Relative to GND1
(Note 5) Relative to GND2
(Note 6) Should not exceed Pd and Tj=150°C
(Note 7) Derate above Ta=25°C at a rate of 9.0mW/°C. Mounted on a glass epoxy of 114.3 mm × 76.2 mm × 1.6 mm.
**Caution**: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Main Power Supply Voltage | $V_{BATT}$(Note 8) | 4.5 | 24.0 | V |
| Input-side Control Block Supply Voltage | $V_{CC1}$(Note 8) | 4.5 | 5.5 | V |
| Output-side Supply Voltage | $V_{CC2}$(Note 9) | 9 | 24 | V |
| Output side UVLO voltage | $V_{UV2TH}$(Note 9) | 6 | - | V |

(Note 8) GND1 reference
(Note 9) GND2 reference

## Insulation Related Characteristics

| Parameter | Symbol | Characteristic | Unit |
|---|---|---|---|
| Insulation Resistance ($V_{IO}$=500V) | $R_S$ | >$10^9$ | Ω |
| Insulation Withstand Voltage / 1min | $V_{ISO}$ | 2500 | Vrms |
| Insulation Test Voltage / 1sec | $V_{ISO}$ | 3000 | Vrms |

## Electrical Characteristics

(Unless otherwise specified Ta=-40°C to125°C, $V_{BATT}$=5V to 24V, $V_{CC1}$=4.5V to 5.5V, $V_{CC2}$=9V to 24V)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Main Power Supply Circuit Current 1 | $I_{BATT1}$ | 0.37 | 0.84 | 1.47 | mA | FET_G Pin switching operating |
| Main Power Supply Circuit Current 2 | $I_{BATT2}$ | 0.34 | 0.77 | 1.35 | mA | FET_G Pin No Switching |
| Input Side Circuit Current 1 | $I_{CC11}$ | 0.13 | 0.31 | 0.49 | mA | OUT=L |
| Input Side Circuit Current 2 | $I_{CC12}$ | 0.13 | 0.31 | 0.49 | mA | OUT=H |
| Input Side Circuit Current 3 | $I_{CC13}$ | 0.25 | 0.42 | 0.59 | mA | INA =10kHZ, Duty=50% |
| Input Side Circuit Current 4 | $I_{CC14}$ | 0.31 | 0.53 | 0.74 | mA | INA =20kHZ, Duty=50% |
| Output Side Circuit Current | $I_{CC2}$ | 2.7 | 4.7 | 7.1 | mA | $R_{TC}$=10kΩ |
| **Switching Power Supply Controller** | | | | | | |
| FET_G Output Voltage H1 | $V_{FETGH1}$ | 4.5 | 5.0 | 5.5 | V | $I_{OUT}$=0A(open) |
| FET_G Output Voltage H2 | $V_{FETGH2}$ | 4.0 | 4.5 | - | V | V_BATT=4.5V $I_{OUT}$=0A(open) |
| FET_G Output Voltage L | $V_{FETGL}$ | 0 | - | 0.3 | V | $I_{OUT}$=0A(open) |
| FET_G ON-Resistance (Source-side) | $R_{ONGH}$ | 3 | 6 | 12 | Ω | 10mA |
| FET_G ON-Resistance (Sink-side) | $R_{ONGL}$ | 0.3 | 0.6 | 1.3 | Ω | 10mA |
| Oscillation Frequency | $f_{OSC\_SW}$ | 80 | 100 | 120 | kHz | |
| Soft-start Time | $t_{SS}$ | - | - | 50 | ms | |
| FB Pin Threshold Voltage | $V_{FB}$ | 1.47 | 1.50 | 1.53 | V | |
| FB Pin Input Current | $I_{FB}$ | -0.8 | 0 | +0.8 | µA | |
| COMP Pin Sink Current | $I_{COMPSINK}$ | -160 | -80 | -40 | µA | |
| COMP Pin Source Current | $I_{COMPSOURCE}$ | 40 | 80 | 160 | µA | |
| V_BATT UVLO OFF Voltage | $V_{UVLOBATTH}$ | 4.05 | 4.25 | 4.45 | V | |
| V_BATT UVLO ON Voltage | $V_{UVLOBATTL}$ | 3.95 | 4.15 | 4.35 | V | |
| Maximum ON DUTY | $D_{ONMAX}$ | 75 | 85 | 95 | % | |
| **Logic Block** | | | | | | |
| Logic High Level Input Voltage | $V_{INH}$ | 0.7×$V_{CC1}$ | - | $V_{CC1}$ | V | INA、DIS |
| Logic Low Level Input Voltage | $V_{INL}$ | 0 | - | 0.3×$V_{CC1}$ | V | INA、DIS |
| Logic Pull-Down Resistance | $R_{IND}$ | 25 | 50 | 100 | kΩ | INA |
| Logic Pull-Up Resistance | $R_{INU}$ | 25 | 50 | 100 | kΩ | DIS |
| Logic Input Filtering Time | $t_{INFIL}$ | 80 | 130 | 180 | ns | INA |
| DIS Input Filtering Time | $T_{DISFIL}$ | 4 | 10 | 20 | µs | |
| DIS Input Delay Time | $t_{DDIS}$ | 4 | 10 | 20 | µs | |
| **Output** | | | | | | |
| OUT1 ON-Resistance (Source-side) | $R_{ONH}$ | 0.2 | 0.55 | 1.3 | Ω | $I_{OUT}$=40mA |
| OUT1 ON-Resistance (Sink-side) | $R_{ONL}$ | 0.2 | 0.55 | 1.3 | Ω | $I_{OUT}$=40mA |
| OUT1 Maximum Current | $I_{OUTMAX}$ | 5.0 | - | - | A | $V_{CC2}$=15V Guaranteed by design |
| PROOUT ON-Resistance | $R_{ONPRO}$ | 0.5 | 1.2 | 2.7 | Ω | $I_{PROOUT}$=40mA |
| Turn ON time | $t_{PON}$ | 140 | 200 | 260 | ns | |
| Turn OFF time | $t_{POFF}$ | 140 | 200 | 260 | ns | |
| Propagation Distortion | $t_{PDIST}$ | -60 | 0 | +60 | ns | $t_{POFF}$ - $t_{PON}$ |
| Rise Time | $t_{RISE}$ | - | 30 | 50 | ns | Load=1nF |
| Fall Time | $t_{FALL}$ | - | 30 | 50 | ns | Load=1nF |
| OUT2 ON-Resistance | $R_{ON2}$ | 0.4 | 0.9 | 2.0 | Ω | $I_{OUT}$=40mA |
| OUT2 ON Threshold Voltage | $V_{OUT2ON}$ | 1.8 | 2.0 | 2.2 | V | |
| OUT2 Output Delay Time | $t_{OUT2ON}$ | - | 15 | 50 | ns | |
| Common Mode Transient Immunity | CM | 100 | - | - | kV/µs | Design assurance |

**Electrical Characteristics - continued**
(Unless otherwise specified Ta=-40°C to125°C, $V_{BATT}$=5V to 24V, $V_{CC1}$=4.5V to 5.5V, $V_{CC2}$=8V to 24V)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Monitor** | | | | | | |
| TC Pin Voltage | $V_{TC}$ | 0.975 | 1.000 | 1.025 | V | |
| TOx Pin Output Current | $I_{TO}$ | 0.97 | 1.00 | 1.03 | mA | $R_{TC}$=10kΩ |
| SENSOR Output Frequency | $f_{OSC\_TO}$ | 8 | 10 | 14 | kHz | |
| SENSOR Output Duty1 | $D_{SENSOR1}$ | 87 | 90 | 93 | % | $V_{TOx}$=1.35V |
| SENSOR Output Duty2 | $D_{SENSOR2}$ | 47 | 50.0 | 53 | % | $V_{TOx}$=2.59V |
| SENSOR Output Duty3 | $D_{SENSOR3}$ | 5 | 10 | 15 | % | $V_{TOx}$=3.84V |
| TOx Pin Disconnect Detection Voltage | $V_{TOH}$ | 7 | 8 | 9 | V | |
| SENSOR ON Resistance (Source-side) | $R_{SENSORH}$ | - | 60 | 160 | Ω | $I_{SENSOR}$=5mA |
| SENSOR ON Resistance (Sink-side) | $R_{SENSORL}$ | - | 60 | 160 | Ω | $I_{SENSOR}$=5mA |
| **Protection Functions** | | | | | | |
| Input-side UVLO OFF Voltage | $V_{UVLO1H}$ | 4.05 | 4.25 | 4.45 | V | |
| Input-side UVLO ON Voltage | $V_{UVLO1L}$ | 3.95 | 4.15 | 4.35 | V | |
| Input-side UVLO Filtering Time | $t_{UVLO1FIL}$ | 2 | 10 | 30 | µs | |
| Input-side UVLO Delay Time (OUT) | $t_{DUVLO1OUT}$ | 2 | 10 | 30 | µs | |
| Input-side UVLO Delay Time (FLT) | $t_{DUVLO1FLT}$ | 2 | 10 | 30 | µs | |
| Output-side UVLO OFF Threshold Voltage | $V_{UVLO2H}$ | 0.95 | 1.00 | 1.05 | V | |
| Output-side UVLO ON Threshold Voltage | $V_{UVLO2L}$ | 0.85 | 0.90 | 0.95 | V | |
| Output-side UVLO Filtering Time | $t_{UVLO2FIL}$ | 2 | 10 | 30 | µs | |
| Output-side UVLO Delay Time (OUT) | $t_{DUVLO2OUT}$ | 2 | 10 | 30 | µs | |
| Output-side UVLO Delay Time (FLT) | $t_{DUVLO2FLT}$ | 3 | - | 65 | µs | |
| Short Current Detection Voltage | $V_{SCDET}$ | 0.67 | 0.70 | 0.73 | V | |
| Short Current Detection Filtering Time | $t_{SCPFIL}$ | 0.15 | 0.30 | 0.45 | µs | |
| Short Current Detection Delay time (OUT) | $t_{DSCPOUT}$ | 0.16 | 0.33 | 0.50 | µs | OUT1=30kΩ Pull down |
| Short Current Detection Delay Time (PROOUT) | $t_{DSCPPRO}$ | 0.17 | 0.35 | 0.53 | µs | PROOUT=30kΩ Pull up |
| Short Current Detection Delay Time (FLT) | $t_{DSCPFLT}$ | 1 | - | 35 | µs | |
| Soft Turn OFF Release Time | $t_{SCPOFF}$ | 30 | - | 110 | µs | OUT1=30kΩ Pull up |
| FLT Output ON-Resistance | $R_{FLTL}$ | - | 30 | 80 | Ω | $I_{FLT}$=5mA |
| Fault Output Holding Time | $t_{FLTRLS}$ | 20 | 40 | 60 | ms | |
| Gate State H Detection Threshold Voltage | $V_{OSFBH}$ | 4.5 | 5.0 | 5.5 | V | |
| Gate State L Detection Threshold Voltage | $V_{OSFBL}$ | 4.0 | 4.5 | 5.0 | V | |
| OSFB Output Filtering Time | $t_{OSFBFIL}$ | 1.5 | 2.0 | 2.5 | µs | |
| OSFB Output ON-Resistance | $R_{OSFB}$ | - | 30 | 80 | Ω | $I_{OSFB}$=5mA |
| OSFB Output Holding Time | $t_{OSFBRLS}$ | 20 | 40 | 60 | ms | |

## Typical Performance Curves

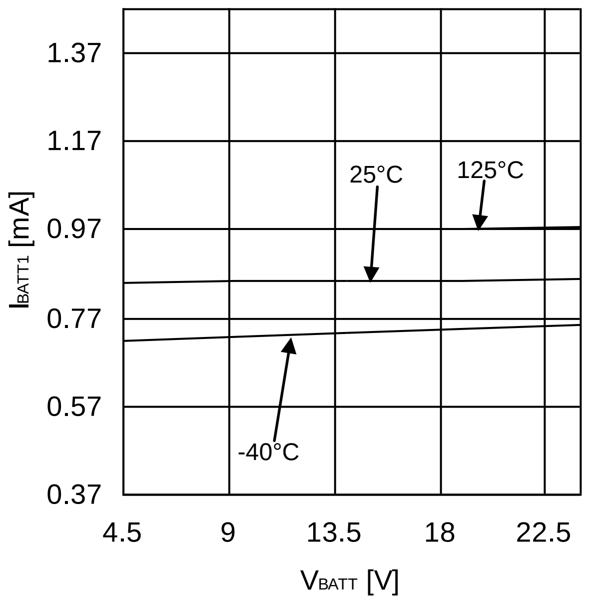



Figure 3. Main Power SupplyCircuit Current 1
(FET_G Pin switching operating)

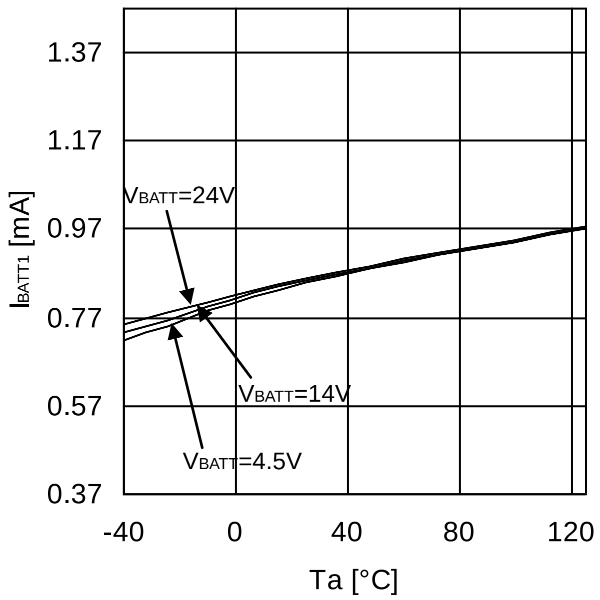



Figure 4. Main Power SupplyCircuit Current 1
(FET_G Pin switching operating)

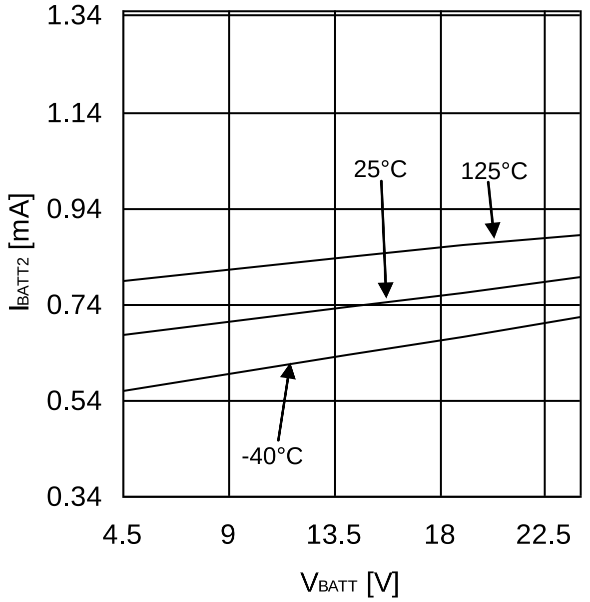



Figure 5. Main Power SupplyCircuit Current 2
(FET_G Pin no switching)

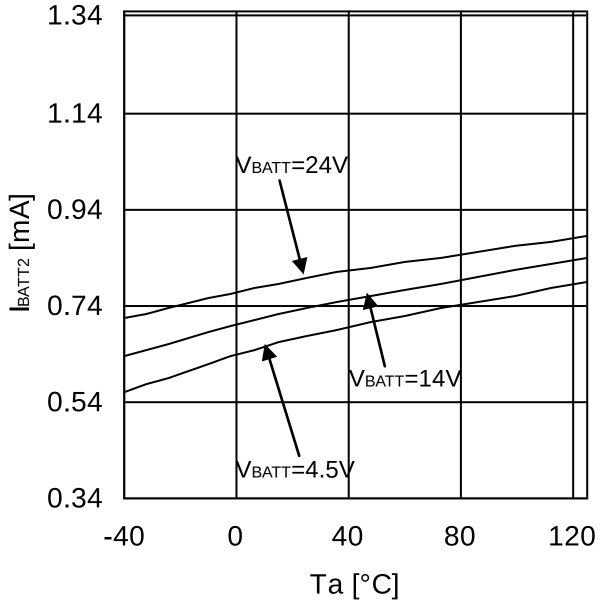



Figure 6. Main Power SupplyCircuit Current 2
(FET_G Pin no switching)

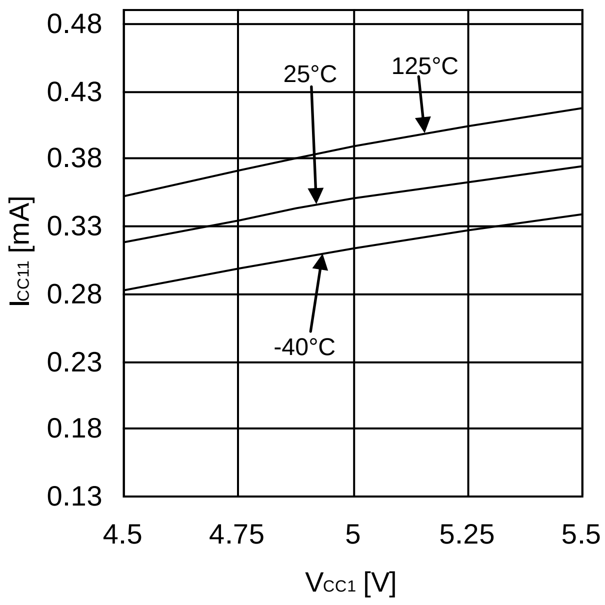



Figure 7. Input Side Circuit Current 1
(OUT1=L)

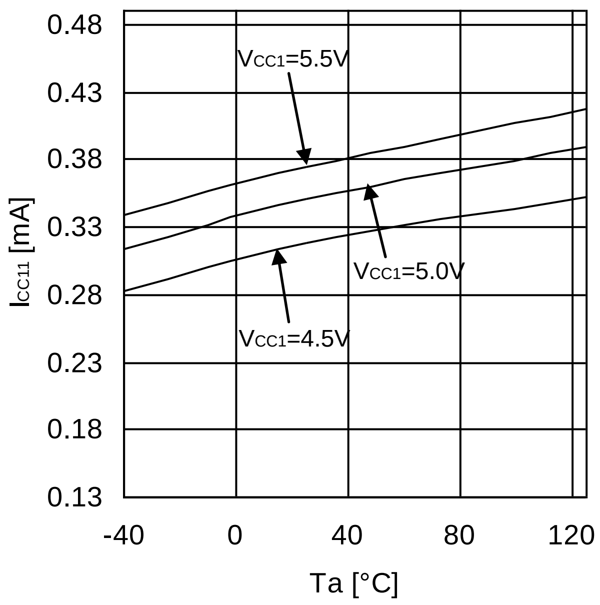



Figure 8. Input Side Circuit Current 1
(OUT1=L)

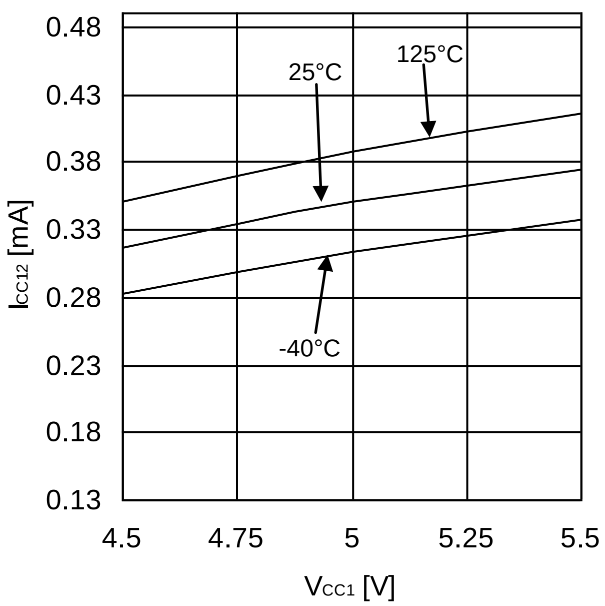



Figure 9. Input Side Circuit Current 2
(OUT1=H)

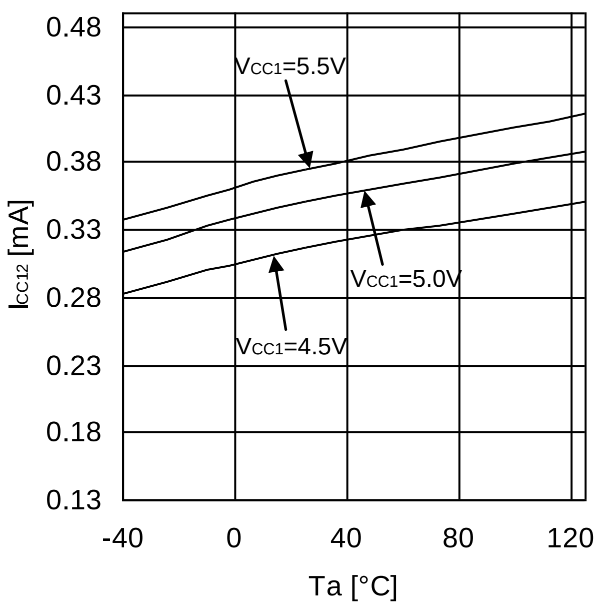



Figure 10. Input Side Circuit Current 2
(OUT1=H)

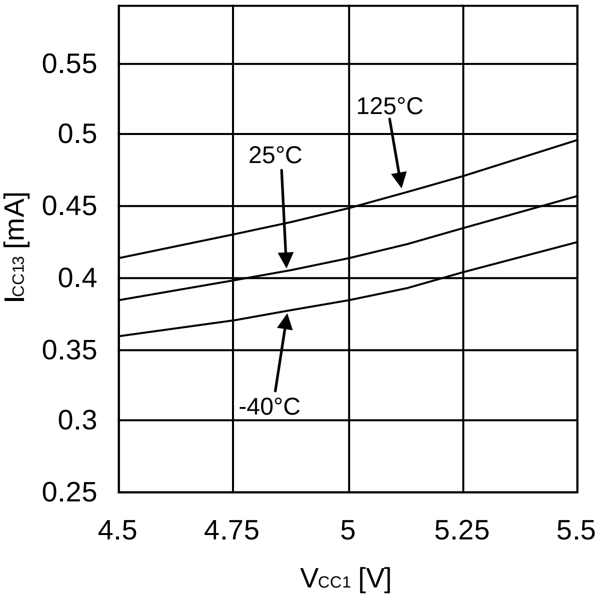



Figure 11. Input Side Circuit Current 3
(INA=10kHz, Duty=50%)

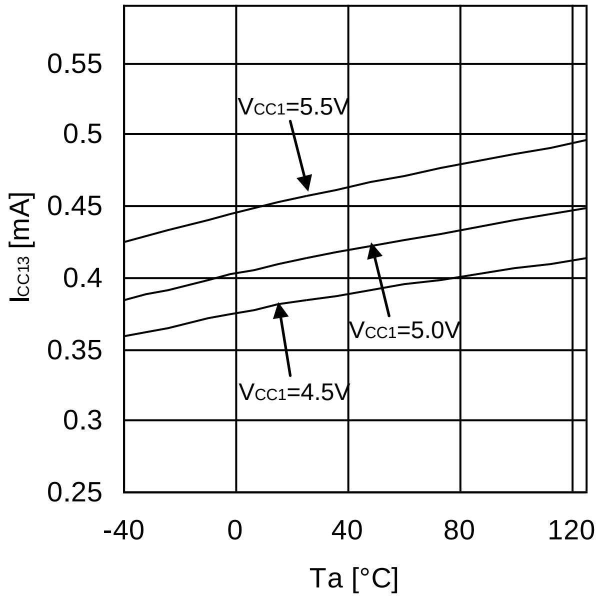



Figure 12. Input Side Circuit Current 3
(INA=10kHz, Duty=50%)

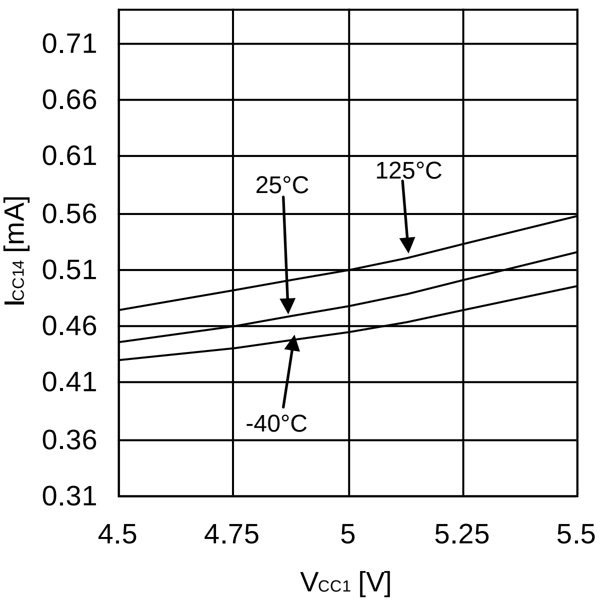



Figure 13. Input Side Circuit Current 4
(INA=20kHz, Duty=50%)

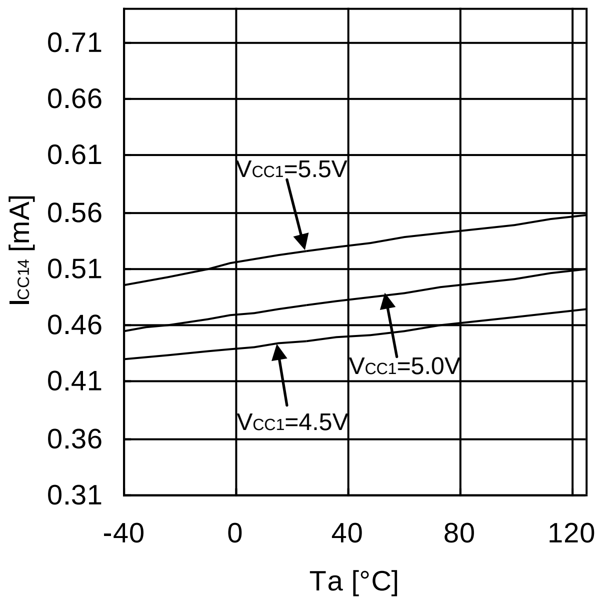



Figure 14. Input Side Circuit Current 4
(INA=20kHz, Duty=50%)

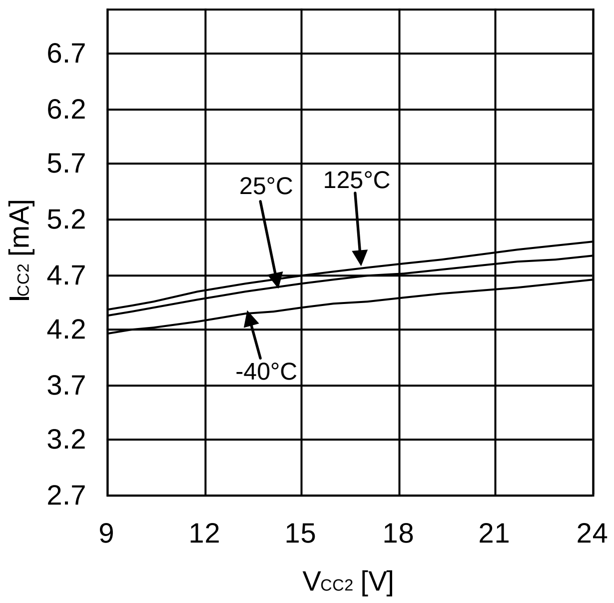



Figure 15. Output Side Circuit Current (OUT=L, $R_{TC}$=10kΩ)

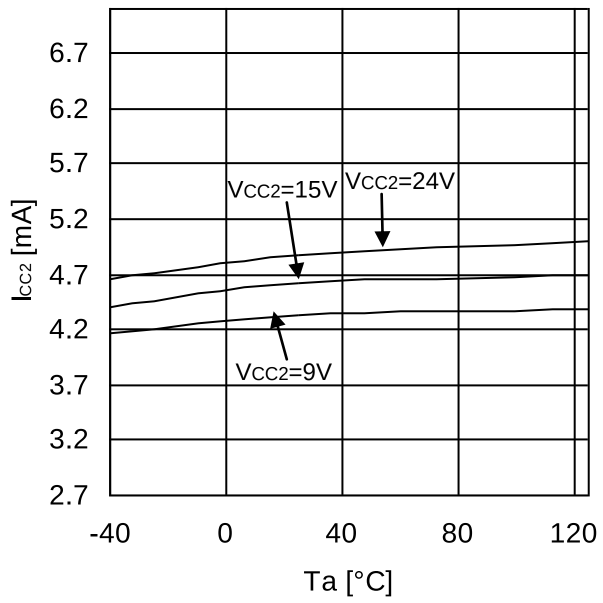



Figure 16. Output Side Circuit Current (OUT=L, $R_{TC}$=10kΩ)

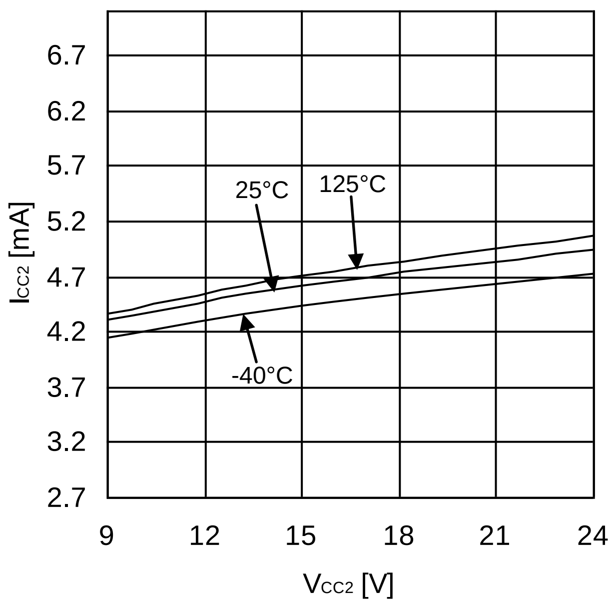



Figure 17. Output Side Circuit Current (OUT=H, $R_{TC}$=10kΩ)

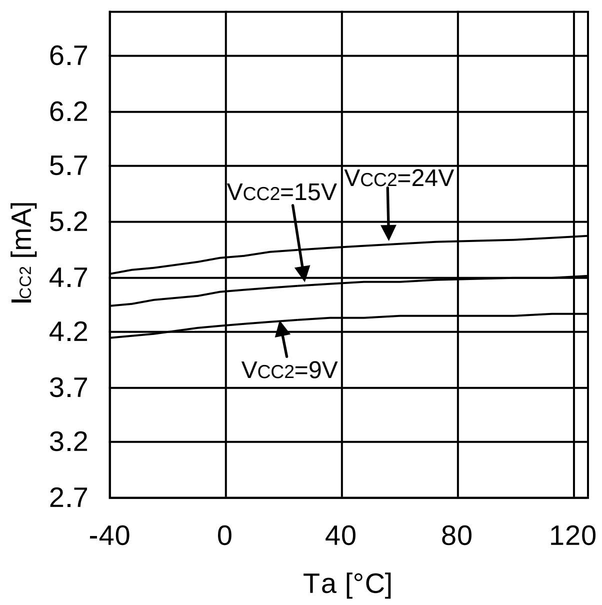



Figure 18. Output Side Circuit Current (OUT=H, $R_{TC}$=10kΩ)

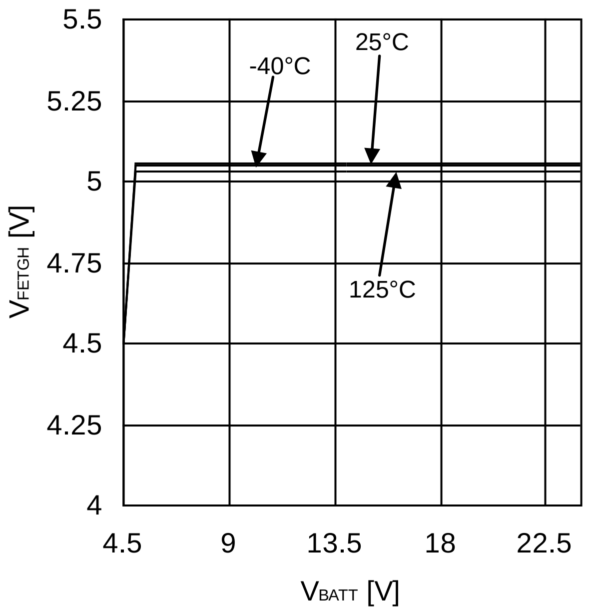



Figure 19. FET_G Output Voltage H1/H2

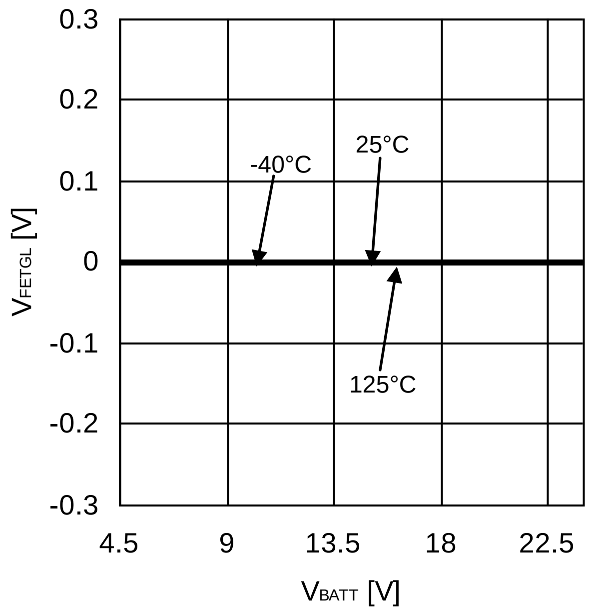



Figure 20. FET_G Output Voltage L

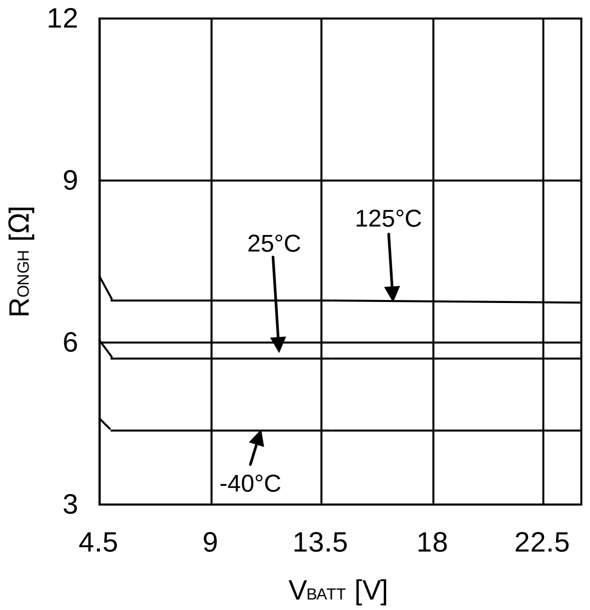



Figure 21. FET_G ON-Resistance (Source-side)

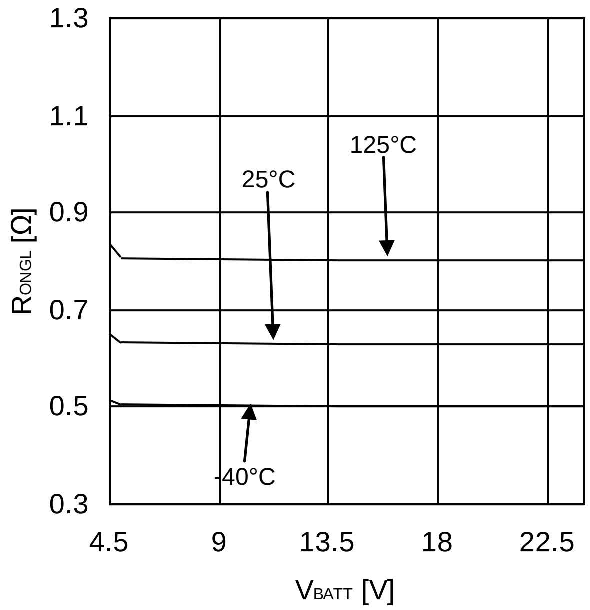



Figure 22. FET_G ON-Resistance (Sink-side)

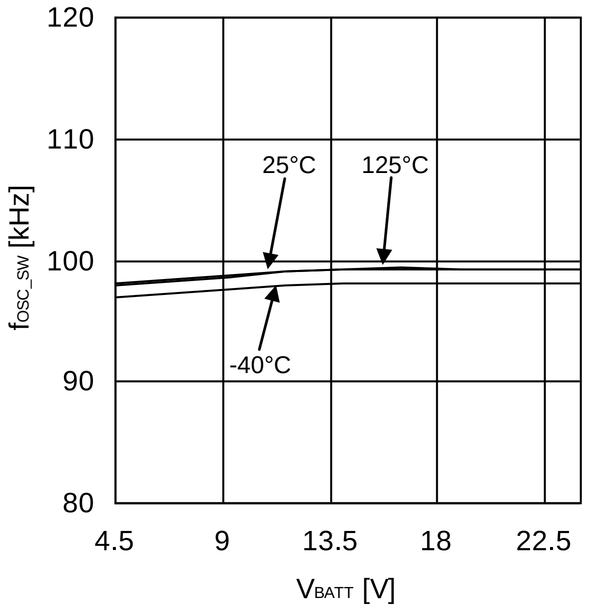



Figure 23. Oscillation Frequency

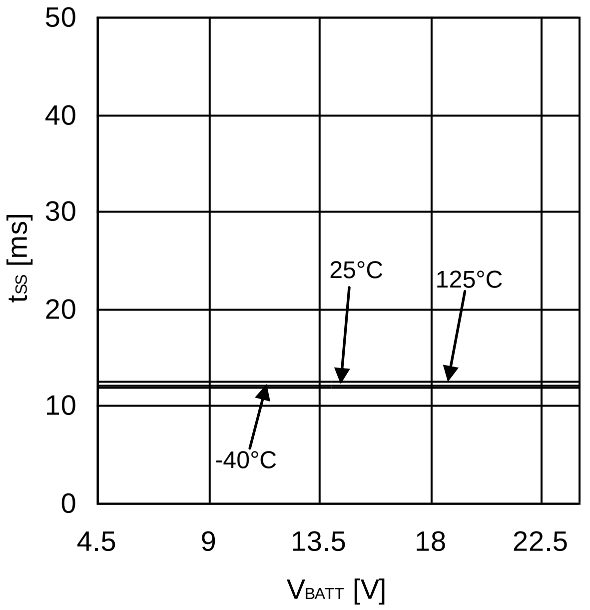



Figure 24. Soft-start Time

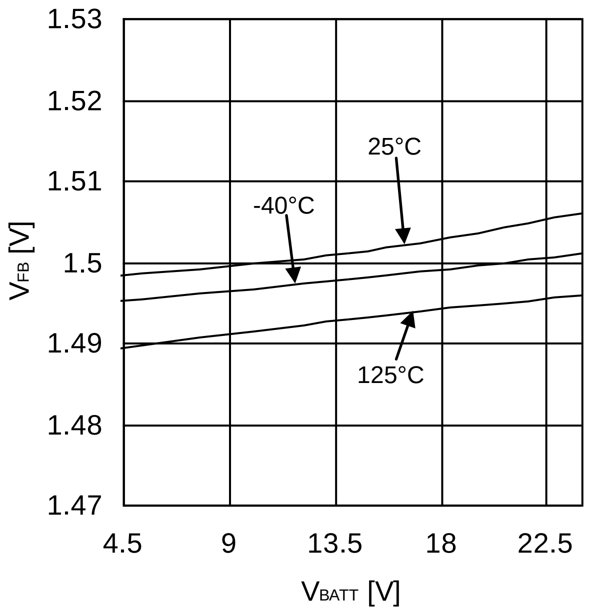



Figure 25. FB Pin Threshold Voltage

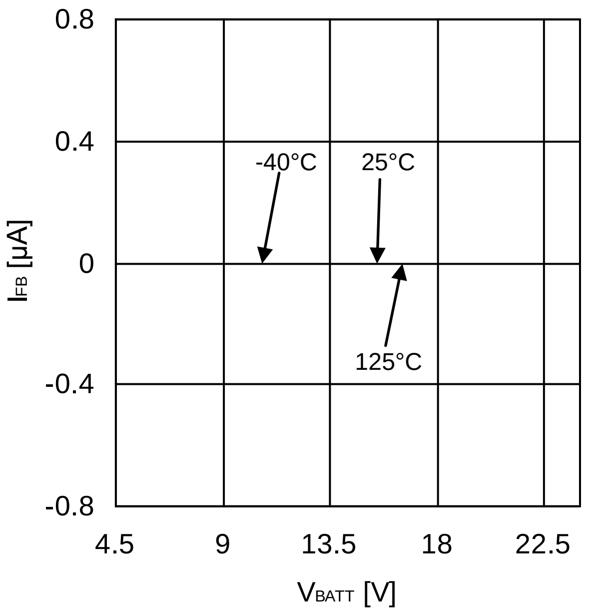



Figure 26. FB Pin Input Current

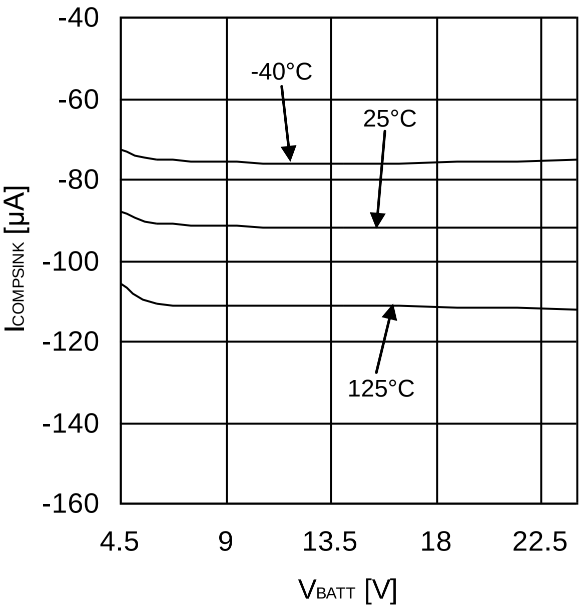



Figure 27. COMP COMP Pin Sink Current

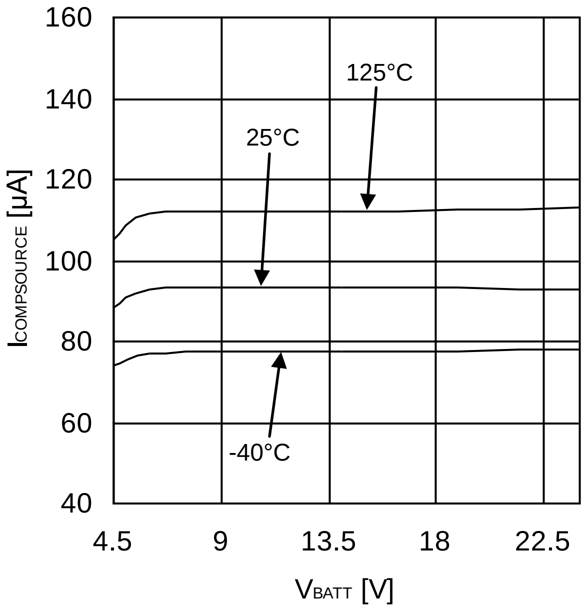



Figure 28. COMP Pin Source Current

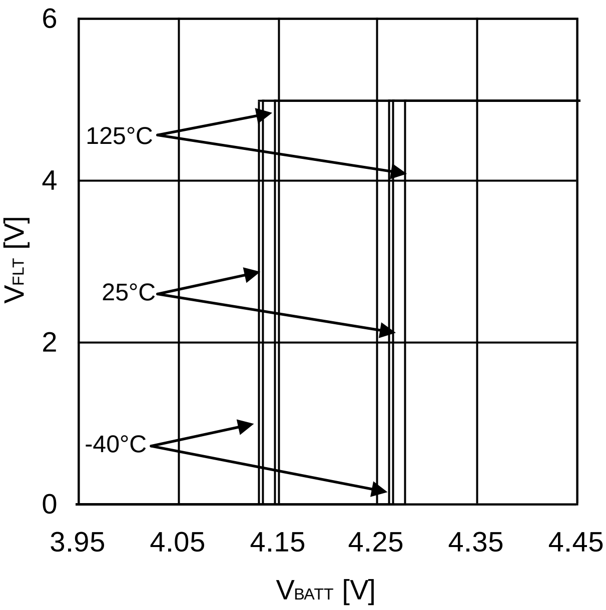



Figure 29. V_BATT UVLO ON/OFFVoltage

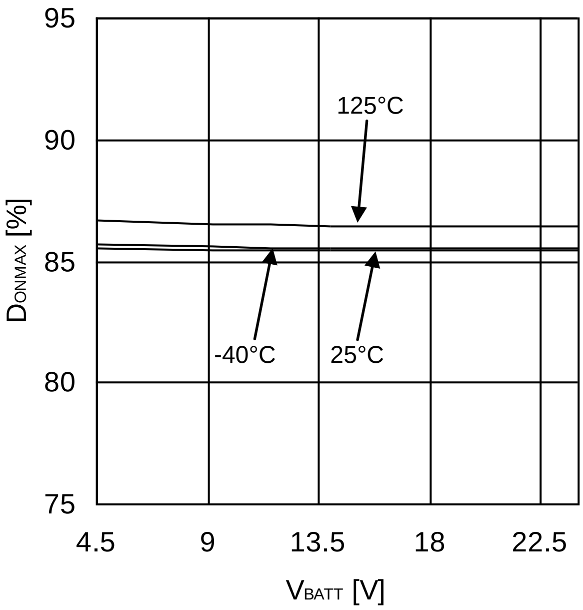



Figure 30. Maximum ON DUTY

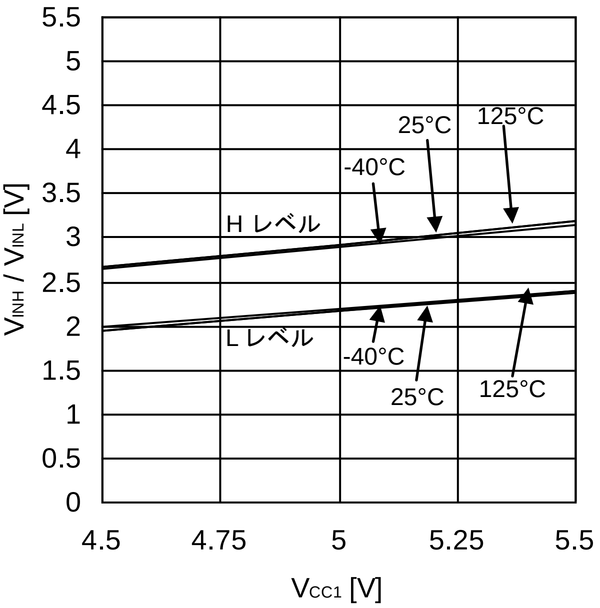



Figure 31. Logic High / Low Level Input Voltage (INA, DIS)

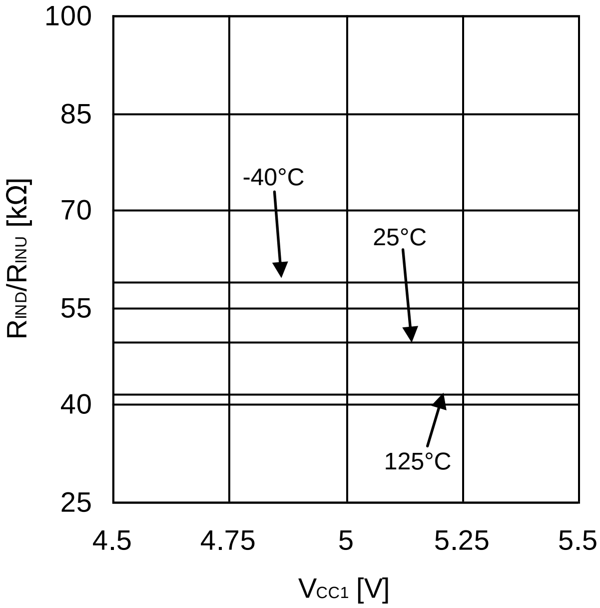



Figure 32. Logic Pull-Down Resistance (INA) Pull-Up Resistance (DIS)

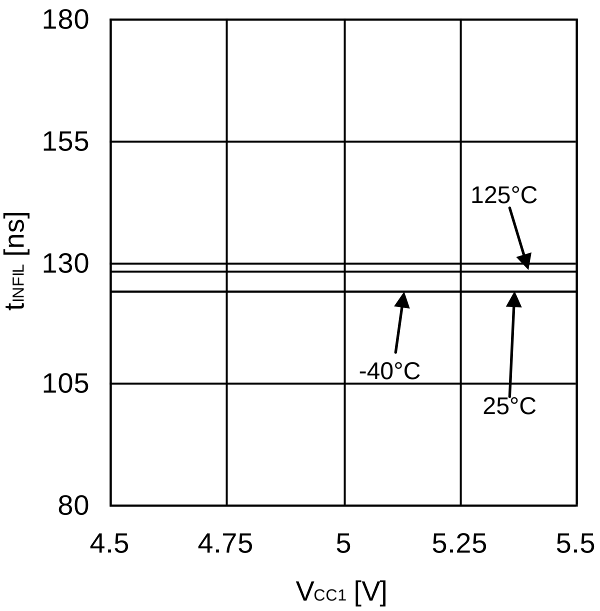



Figure 33. Logic Input Filtering Time (L pulse)

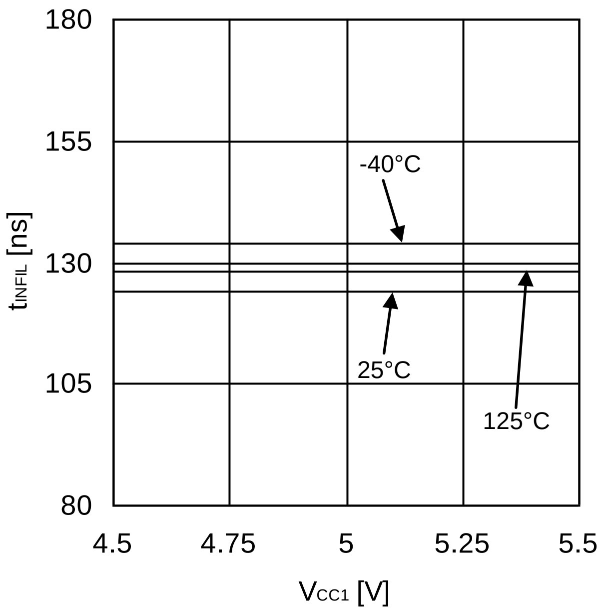



Figure 34. Logic Input Filtering Time (H pulse)

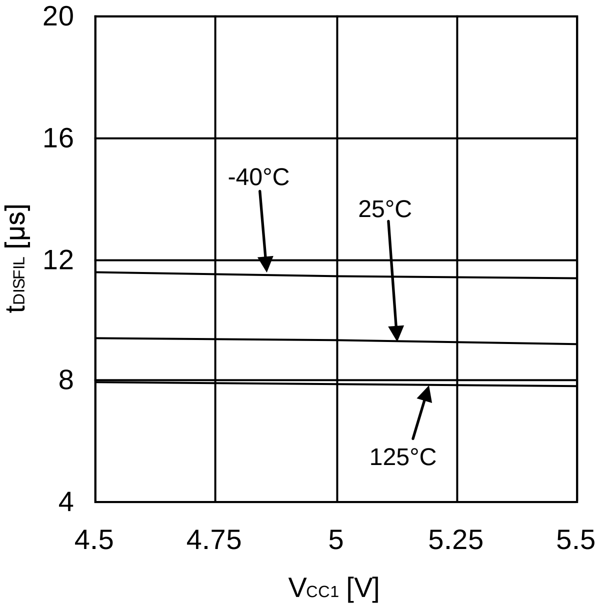



Figure 35. DIS Input Filtering Time

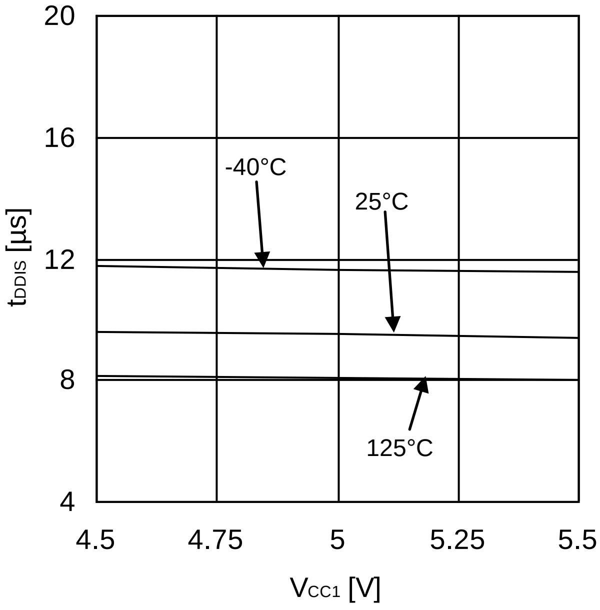



Figure 36. DIS Input Delay Time

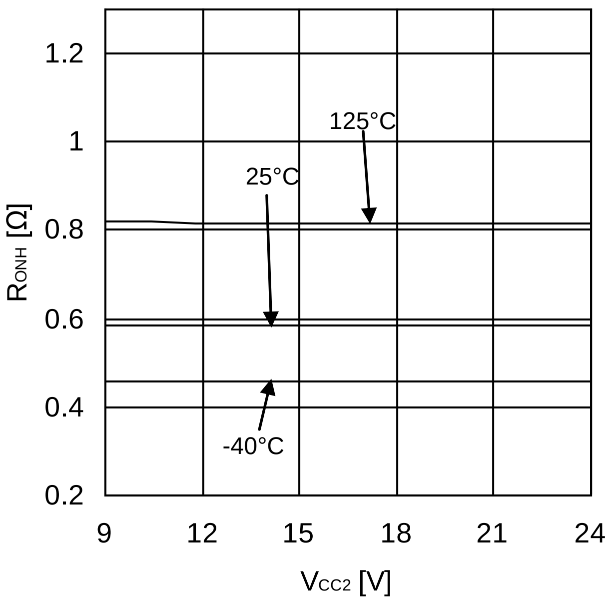



Figure 37. OUT1 ON-Resistance(Source-side)
($I_{OUT1}$=40mA)

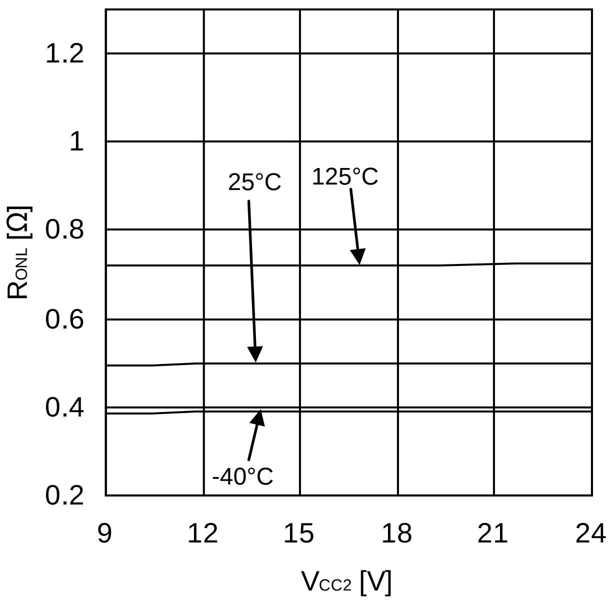



Figure 38. OUT1 ON-Resistance (Sink-side)
($I_{OUT1}$=40mA)

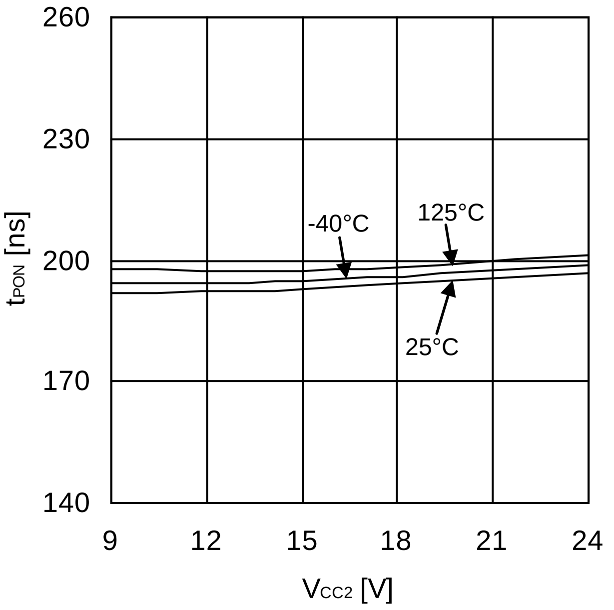



Figure 39. Turn ON time

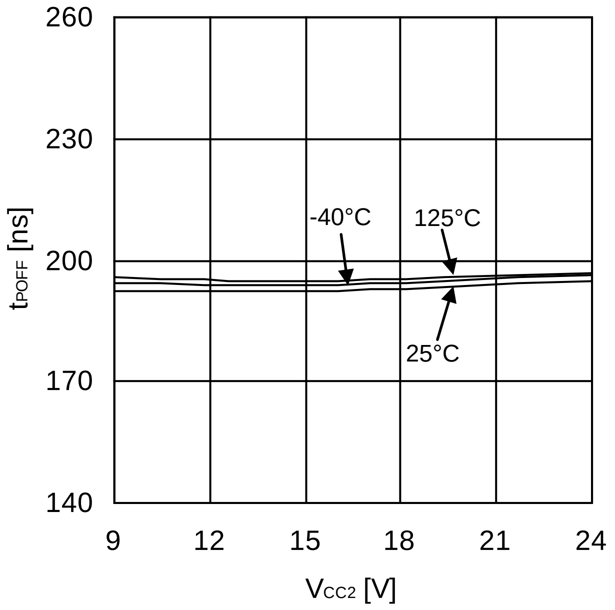



Figure 40. Turn OFF time

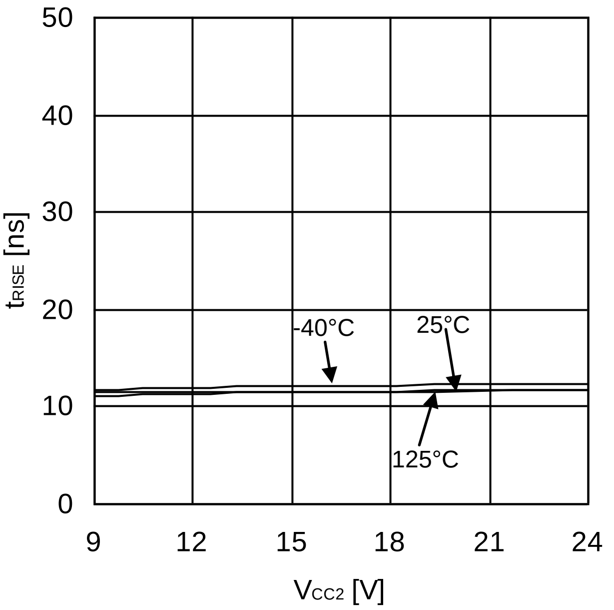



Figure 41. Rise time

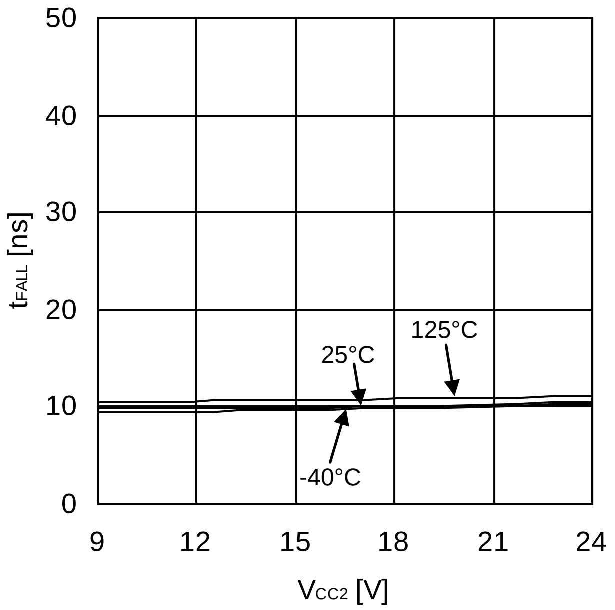



Figure 42. Fall time

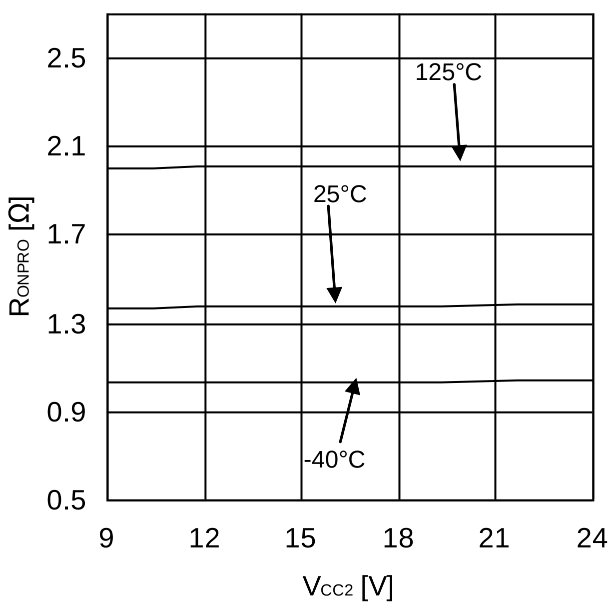



Figure 43. PROOUT ON-Resistance
($I_{PROOUT}$=40mA)

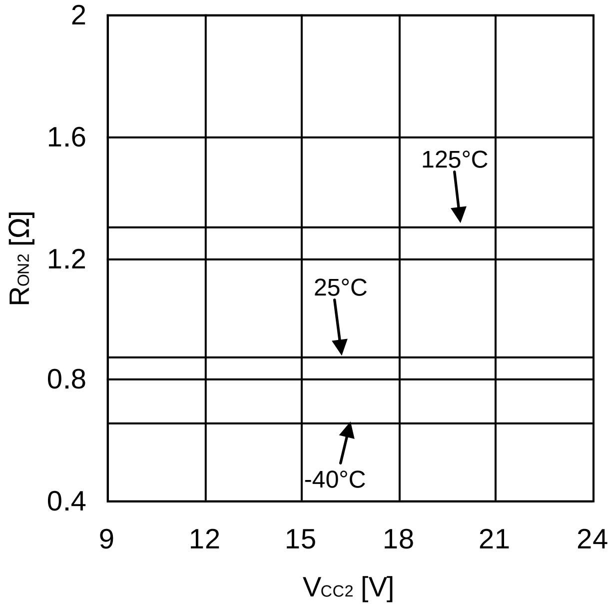



Figure 44. OUT2 ON-Resistance
($I_{OUT2}$=40mA)

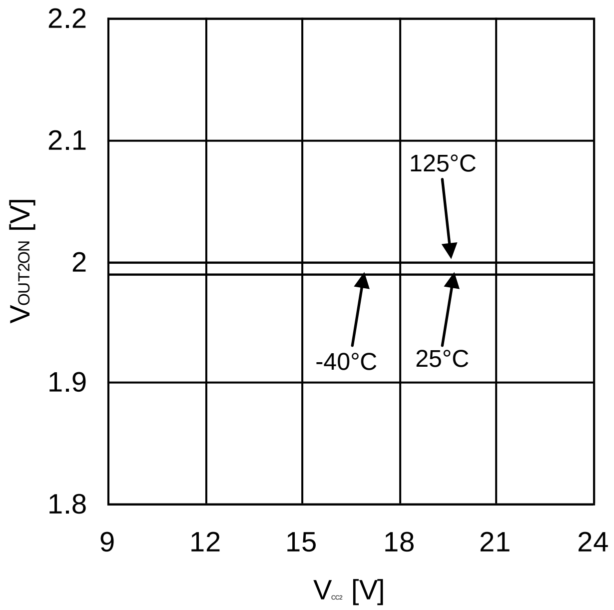



Figure 45. OUT2 ON Threshold Voltage

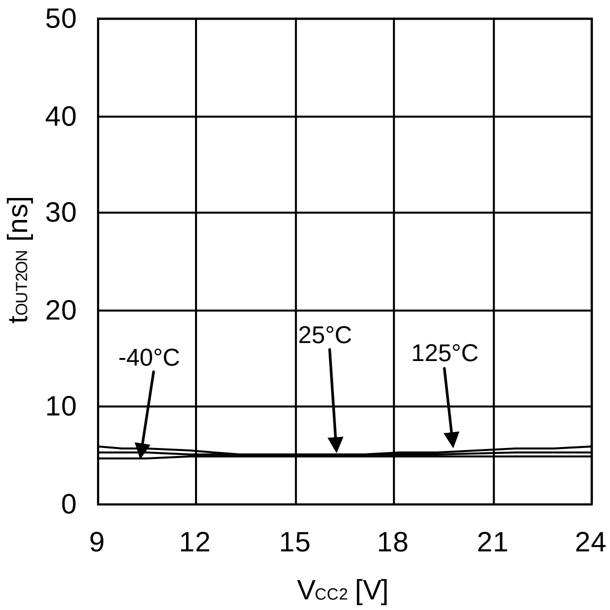



Figure 46. OUT2 Output Delay Time

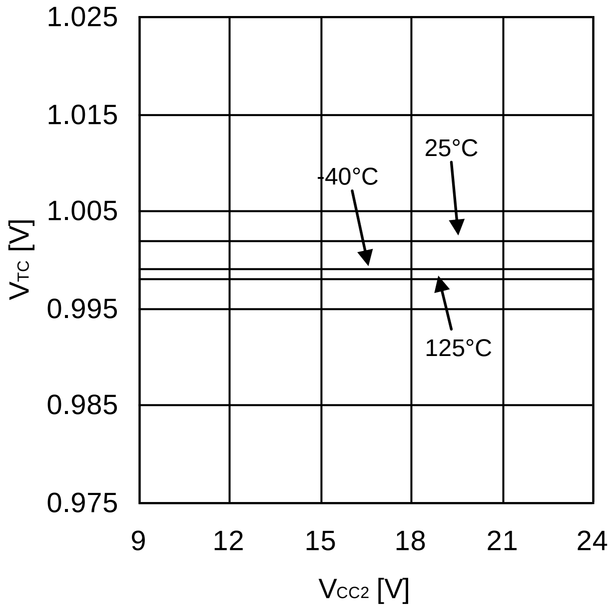



Figure 47. TC Pin Voltage

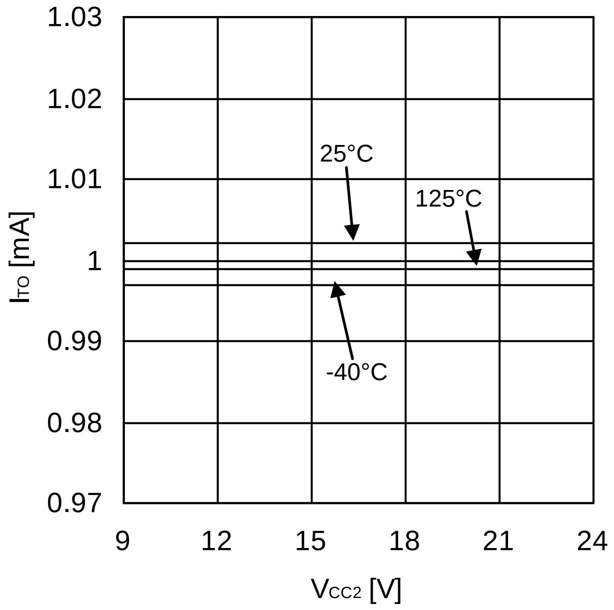



Figure 48. TOx Pin Output Current (RTC=10kΩ)

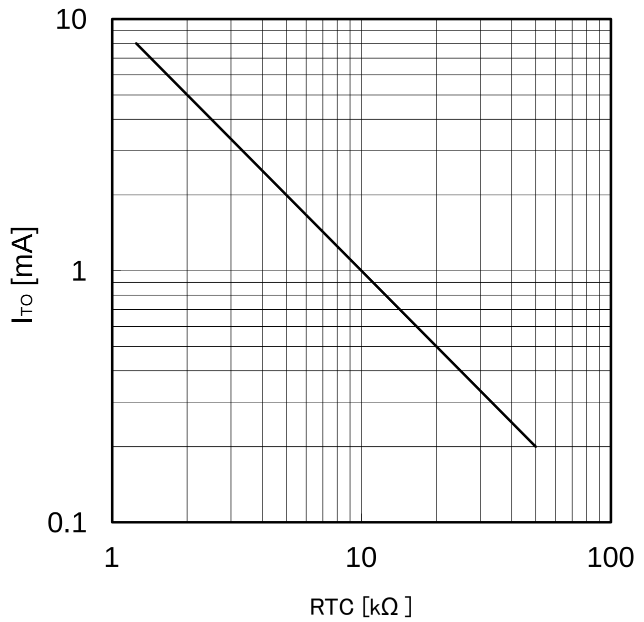



Figure 49. TOx Pin Output Current

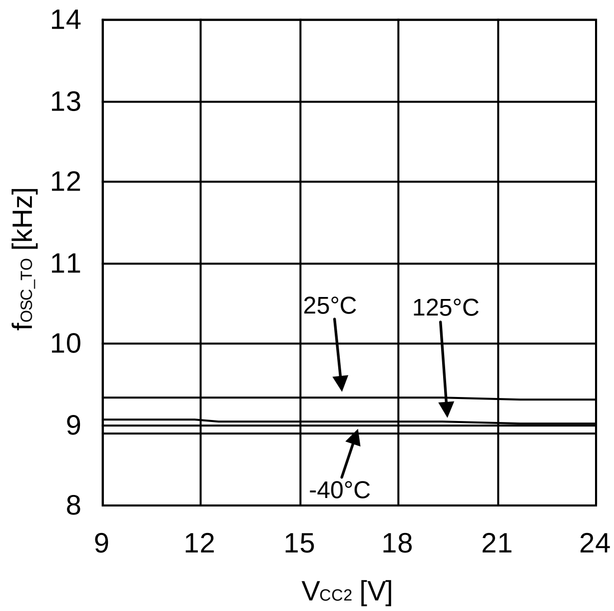



Figure 50. SENSOR Output Frequency

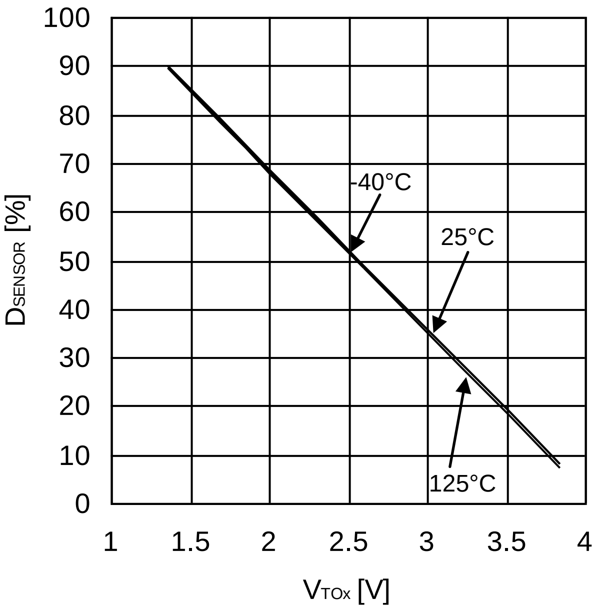



Figure 51. SENSOR Output Duty

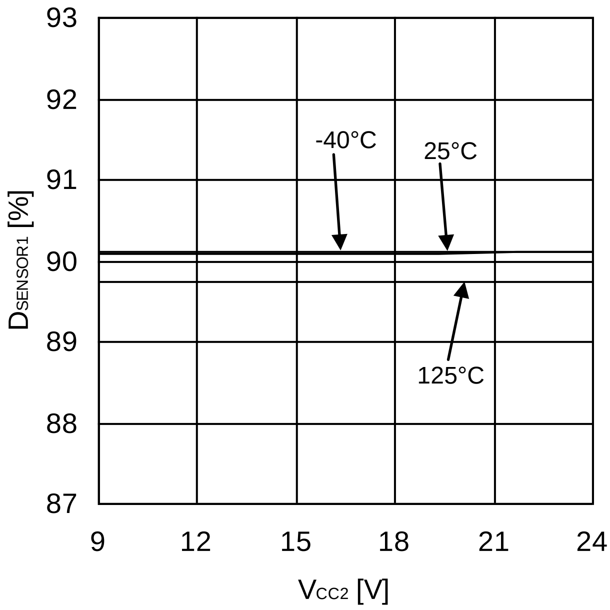



Figure 52. SENSOR Output Duty1
(VTOx=1.35V)

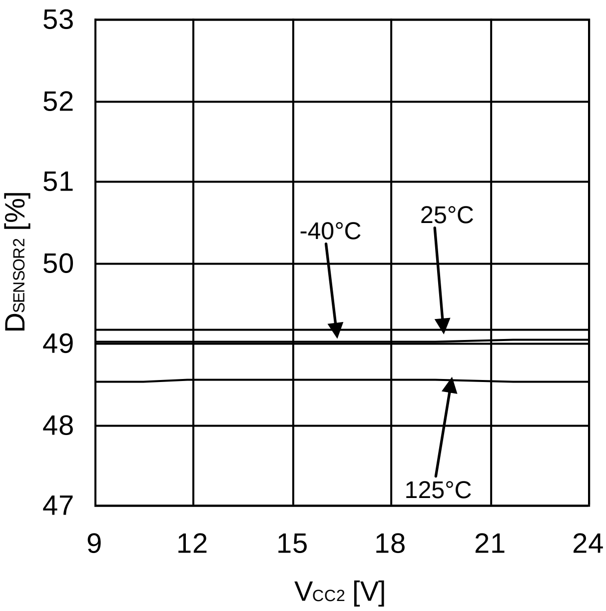



Figure 53. SENSOR Output Duty2
(VTOx=2.59V)

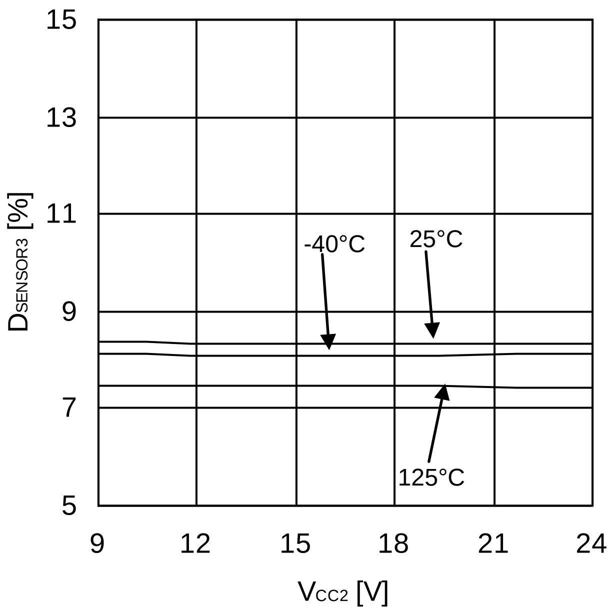



Figure 54. SENSOR Output Duty3
(VTOx=3.84V)

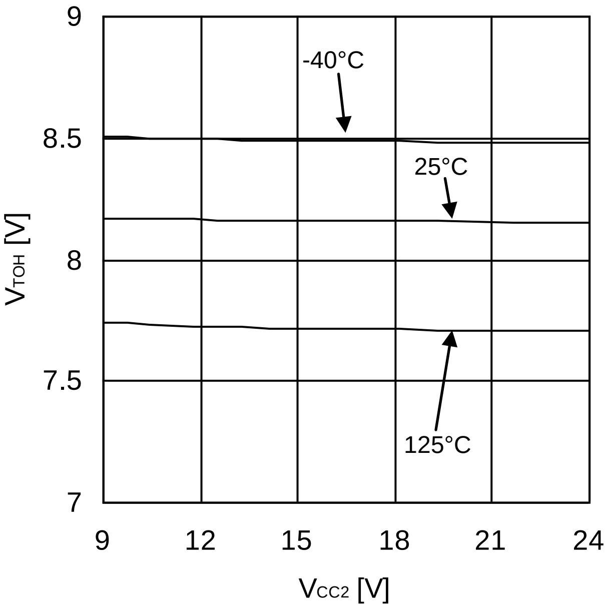



Figure 55. TOx Pin Disconnect Detection Voltage

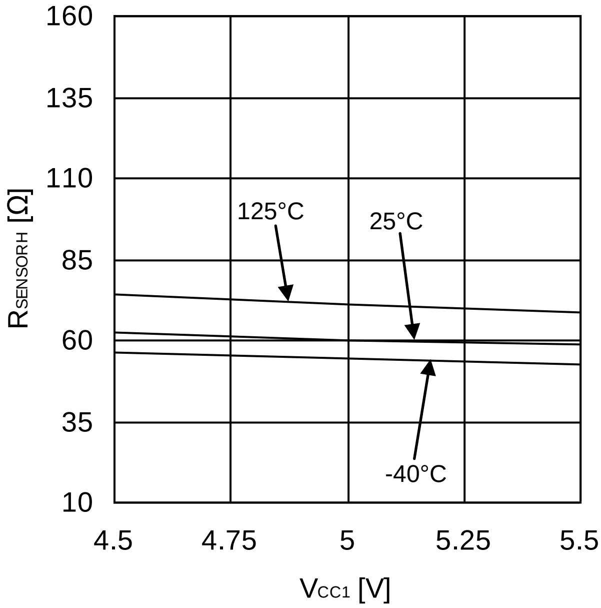



Figure 56. SENSOR ON Resistance(Source-side) ($I_{SEBSOR}$=5mA)

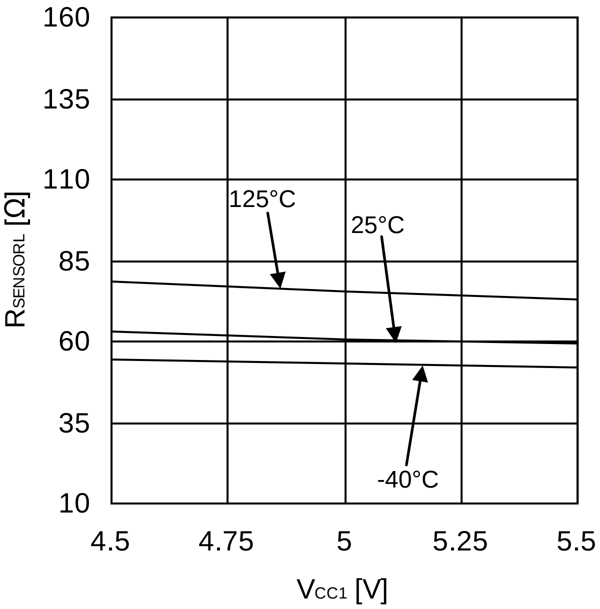



Figure 57. SENSOR ON Resistance (Sink-side) ($I_{SENSOR}$=5mA)

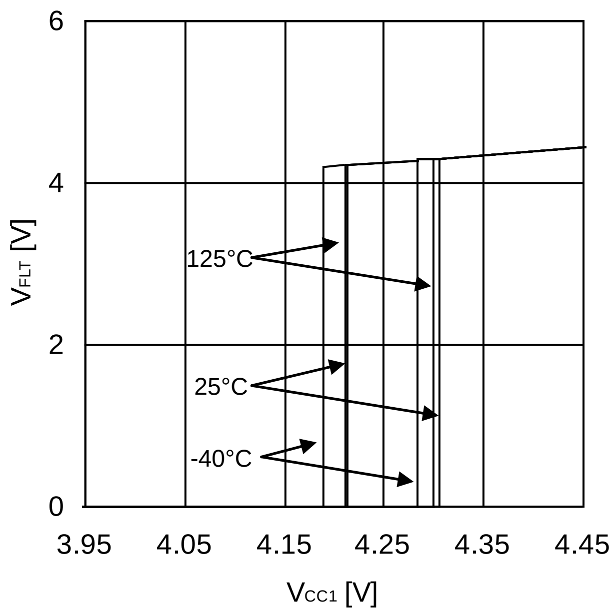



Figure 58. Input-side UVLO ON/OFF Voltage

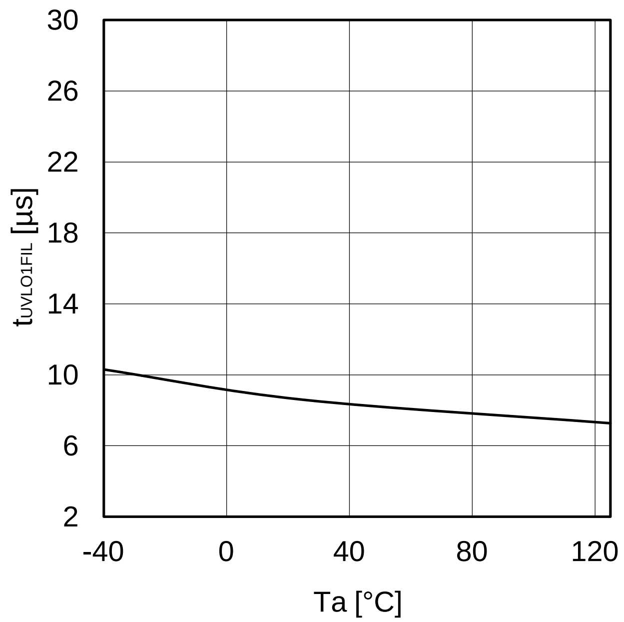



Figure 59. Input-side UVLO Filtering Time

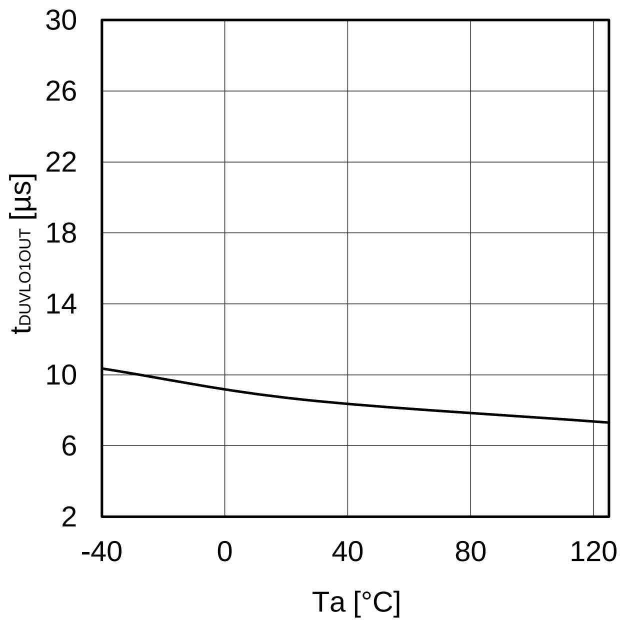



Figure 60. Input-side UVLO Delay Time (OUT1)

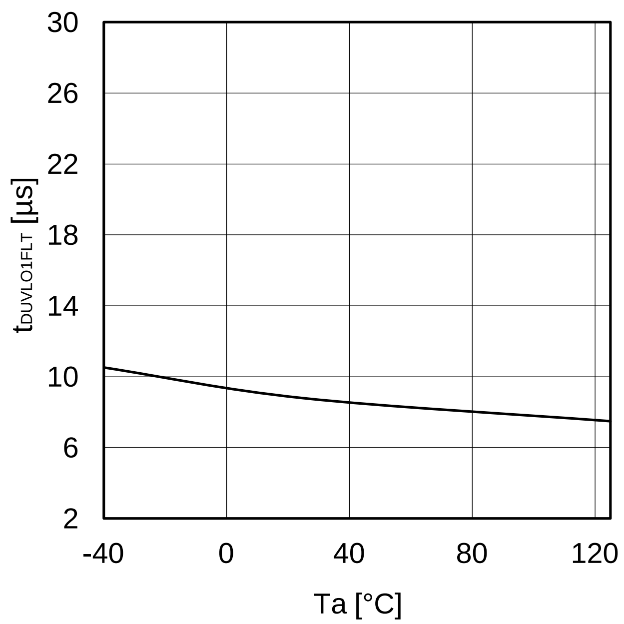



Figure 61. Input-side UVLO Delay Time (FLT)

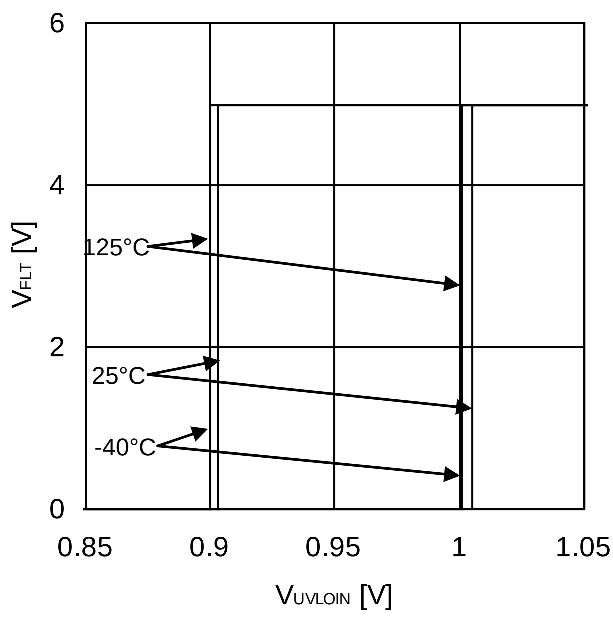



Figure 62. Output-side UVLO ON / OFF Threshold Voltage

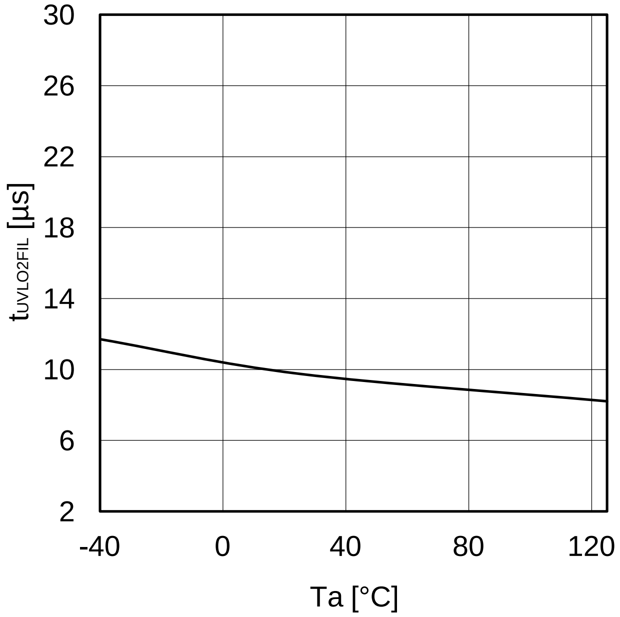



Figure 63. Output-side UVLO Filtering Time

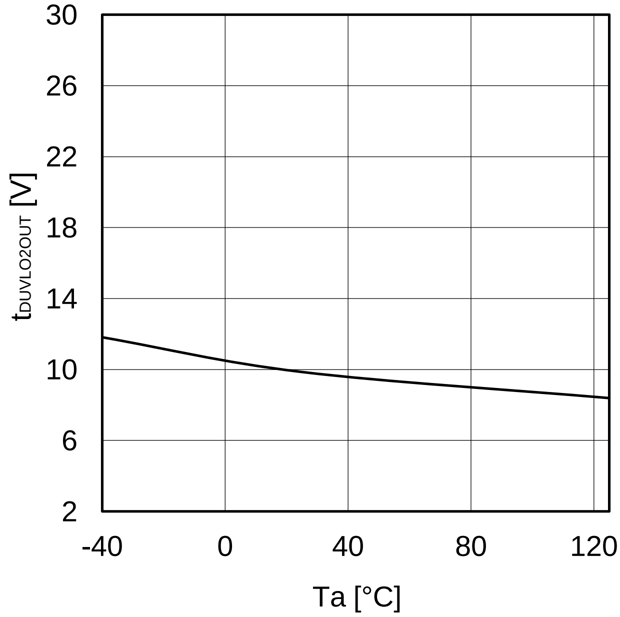



Figure 64. Output-side UVLO Delay Time (OUT1)

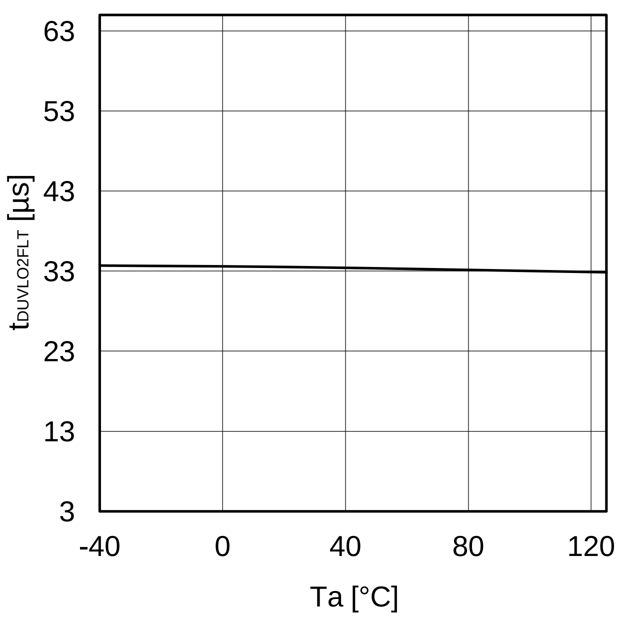



Figure 65. Output-side UVLO Delay Time (FLT)

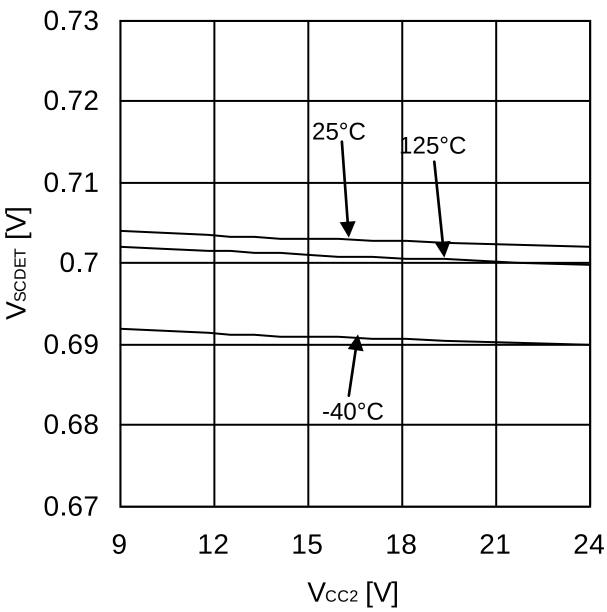



Figure 66. Short Current Detection Voltage

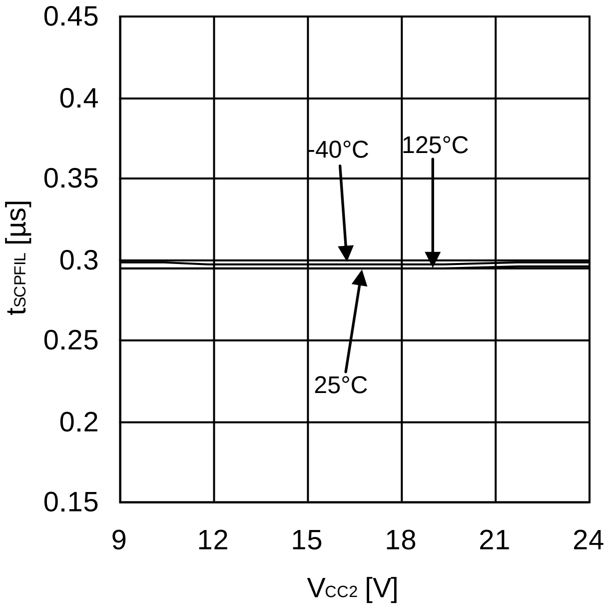



Figure 67. Short Current Detection Filtering Time

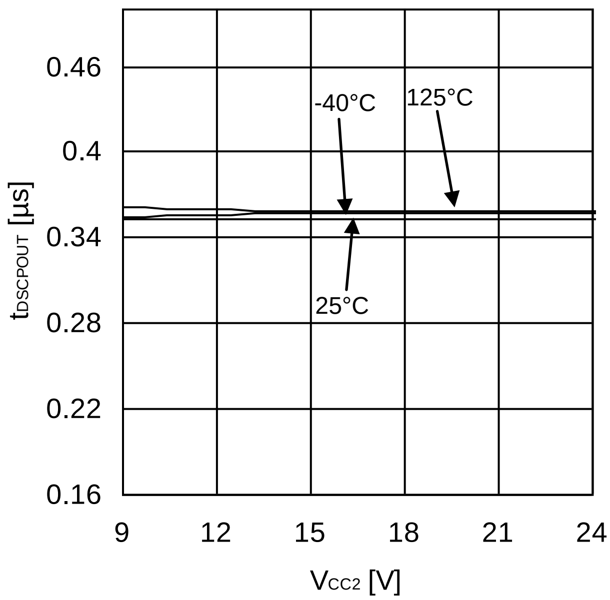



Figure 68. Short Current Detection Delay time (OUT1)

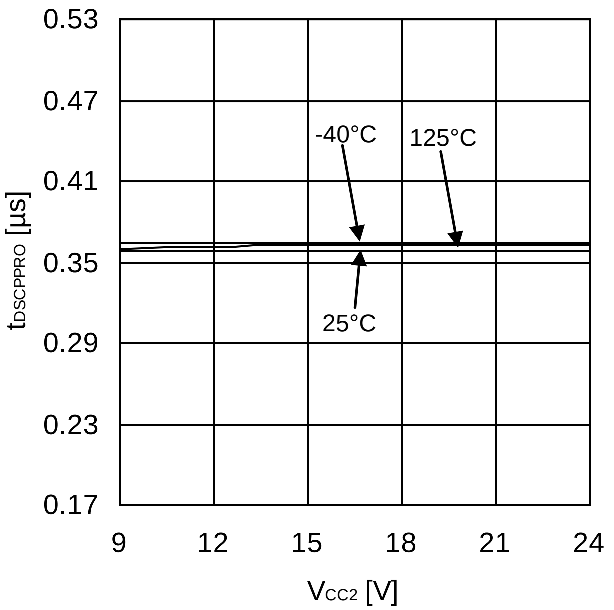



Figure 69. Short Current Detection Delay time (PROOUT)

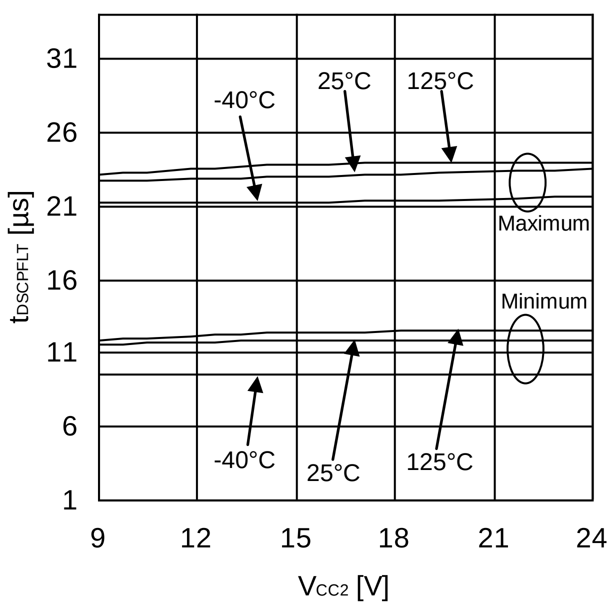



Figure 70. Short Current Detection Delay time (FLT)

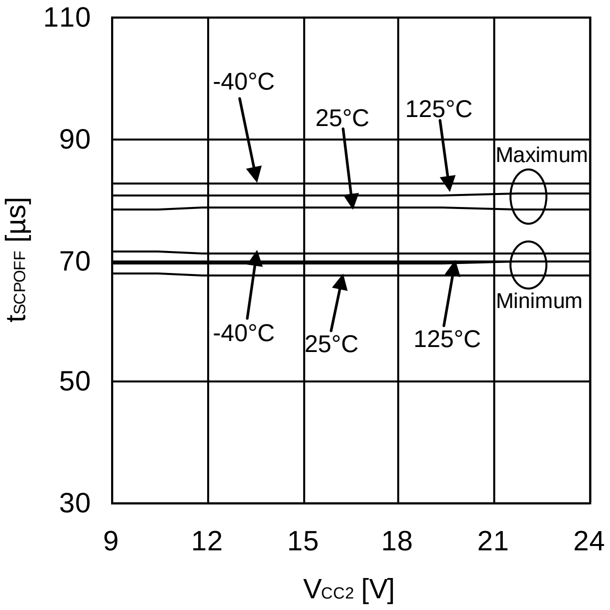



Figure 71. Soft Turn OFF Release Time

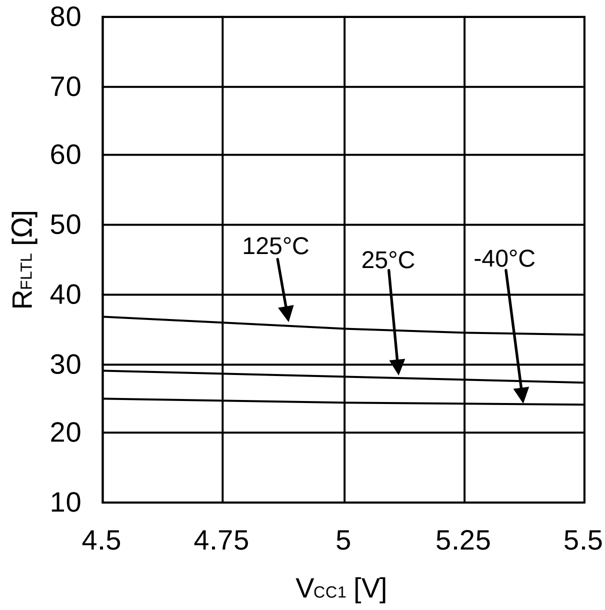



Figure 72. FLT Output ON-Resistance ($I_{FLT}$=5mA)

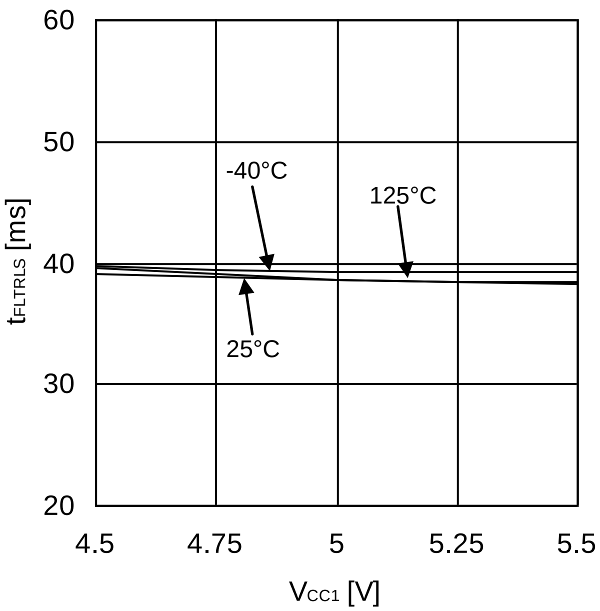



Figure 73. Fault Output Holding Time

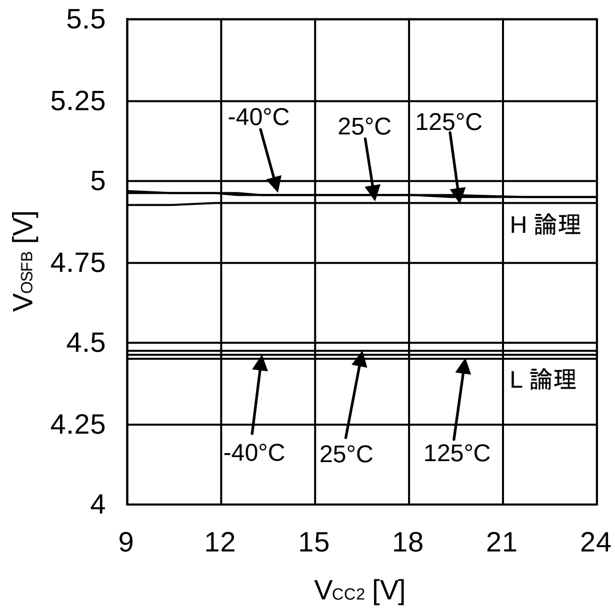



Figure 74. Gate State H /L Detection Threshold Voltage

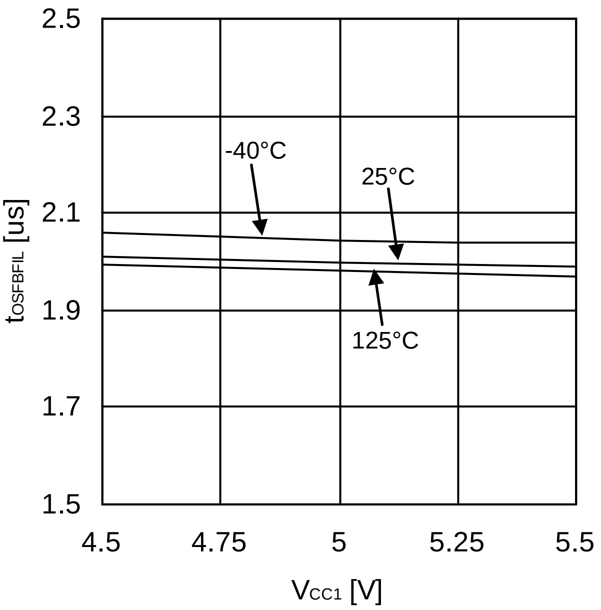



Figure 75. OSFB Output Filtering Time

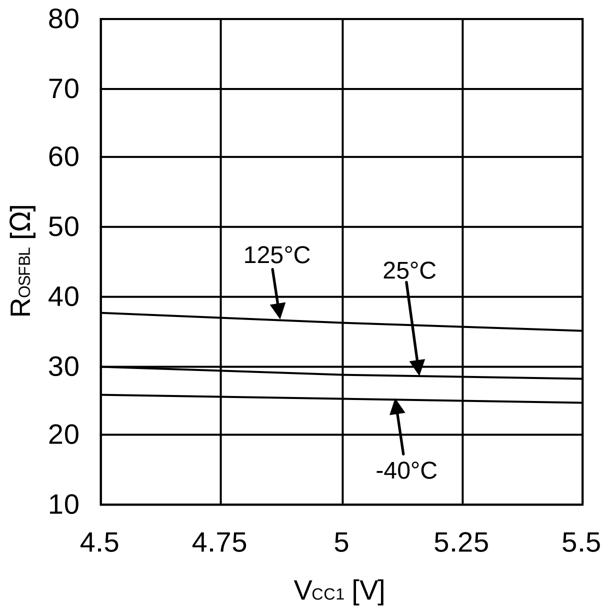



Figure 76. OSFB Output ON-Resistance ($I_{OSFB}$=5mA)

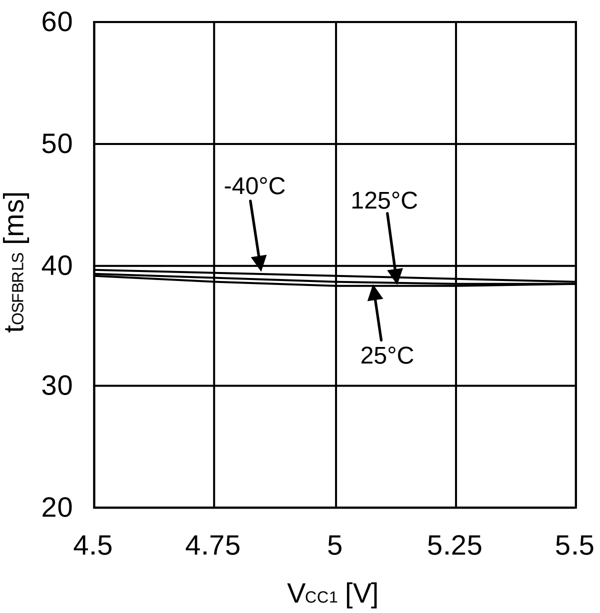



Figure 77. OSFB Output Holding Time

## Description of Pins and Cautions on Layout of Board

1. V_BATT (Main power supply pin)
   This is the main power supply pin. Connect a bypass capacitor between V_BATT and GND1 in order to suppress voltage variations. Be sure to apply a power supply even when the switching power supply is not used, since the internal reference voltage of the input side chip is generated from this power supply.

2. VCC1 (Input-side power supply pin)
   The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the driving current of the internal transformer, connect a bypass capacitor between the VCC1 and the GND1 pins.

3. GND1 (Input-side ground pin)
   The GND1 pin is a ground pin on the input side.

4. VCC2 (Output-side positive power supply pin)
   The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to the driving current of the internal transformer and output current, connect a bypass capacitor between the VCC2 and the GND2 pins.

5. GND2 (Output-side ground pin)
   The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of output device.

6. INA, DIS (Control input pin, input enabling signal input pin)
   They are pins for deciding the output logic.

| DIS | INA | OUT1 |
|---|---|---|
| H | X | L |
| L | L | L |
| L | H | H |

X: Don't care

7. FLT (Fault output pin)
   The FLT pin is an open drain pin that outputs a fault signal when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated).

| State | FLT |
|---|---|
| While in normal operation | Hi-Z |
| When a Fault occurs (UVLO / SCP) | L |

8. OSFB (Output pin for monitoring gate condition)
   This is an open drain pin which compares gate logic of the output element monitored with PROOUT pin and DIS/INA pin input logic, and outputs L when they disaccord.

| Status | DIS | INA | PROOUT(input) | OSFB |
|---|---|---|---|---|
| Normal operation | H | X | H | L |
| | H | X | L | Hi-Z |
| | L | L | H | L |
| | L | L | L | Hi-Z |
| | L | H | H | Hi-Z |
| | L | H | L | L |
| Fault | X | X | X | Hi-Z |

X: Don't care

9. SENSOR (Temperature information output pin)
   This is a pin which outputs the voltage of either TO1 or TO2, whichever is lower, converted to Duty cycle.

10. FB (Error amplifier inverting input pin for switching controller)
    This is a voltage feedback pin of the switching controller. Connect it to VCC1 when the switching controller is not used.

11. COMP (Error amplifier output pin for switching controller)
    This is the gain control pin of the switching controller. Connect a phase compensation capacitor and resistor. When the switching controller is not used, connect it to GND1.

12. VREG (Power supply pin for the driving MOS FET of the switching controller)
    This is the power supply pin for the driving MOSFET of the switching controller transformer drive. Be sure to connect a capacitor between VREG and GND1 even when the switching controller is not used, in order to prevent oscillation and suppress voltage variation due to FET_G output current.

### Description of Pins and Cautions on Layout of Board – continued

13. FET_G (MOS FET control pin for switching controller)
    This is a MOSFET control pin for the switching controller transformer drive. Leave it unconnected when the switching controller is not used.

14. SENSE (Connection to the current feedback resistor of the switching controller)
    This is a pin connected to the resistor of the switching controller current feedback. FET_G pin output duty is controlled by the voltage value of this pin. Connect it to VCC1 when switching controller is not used.

15. OUT(Output pin)
    The OUT pin is a gate driving pin.

16. OUT2 (Miller clamp pin)
    This is the miller clamp pin for preventing a rise of gate voltage due to miller current of output element connected to OUT1. OUT2 should be unconnected when miller clamp function is not used.

17. PROOUT (Soft turn-OFF pin)
    This is a pin for soft turn-OFF of output pin when short-circuit protection is in action. It also functions as a pin for monitoring gate voltage for miller clamp function and output state feedback function.

18. SCPIN1, SCPIN2, SCPIN3 (Short circuit current detection pin)
    These are the pins used to detect current for short circuit protection. When the SCPIN1 pin, SCPIN2 pin or SCPIN3 pin voltage exceeds the voltage set with the $V_{SCDET}$ parameter, the SCP function will be activated, this will make the IC function in an open state. To avoid such trouble, connect a resistor between the SCPIN and the GND2 or short the SCPIN pin to GND2 when the SCP function is not used.

19. TC (Resistor connection pin for setting constant current source output)
    The TC pin is a resistor connection pin for setting the constant current output. If an arbitrary resistance value is connected between TC and GND2, it is possible to set the constant current value output from TO.

20. TO1, TO2 (Constant current output / sensor voltage input pin)
    The TO1 pin and the TO2 pin are constant current output / voltage input pins. It can be used as a sensor input by connecting an element with arbitrary impedance between TOx pin and GND. Furthermore, the TOx pin disconnect detection function is built-in.

21. UVLOIN (Output-side UVLO setting input pin)
    The UVLOIN pin is a pin for deciding UVLO setting value of VCC2. The threshold value of UVLO can be set by dividing the resistance voltage of VCC2 and inputting such value.

**Description of Functions and Examples of Constant Setting**

1. Fault status output
   This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated) and hold the fault signal until fault output holding time ($t_{FLTRLS}$) is completed.

| Status | FLT pin |
|---|---|
| Normal | Hi-Z |
| Fault occurs | L |

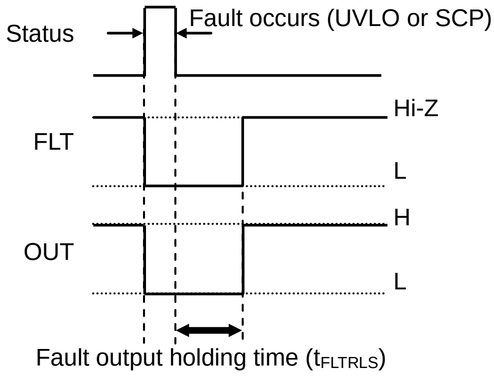



Figure 78. Fault Status Output Timing Chart

2. Under voltage Lockout (UVLO) function
   The BM60051FV-C incorporates the under voltage lockout (UVLO) function on V_BATT, VCC1 and VCC2. When the power supply voltage drops to the UVLO ON voltage, the OUT pin and the FLT pin will both output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. However, during the fault output holding time set in “Fault status output” section, the OUT pin and the FLT pin will hold the “L” signal. In addition, to prevent mis-triggers due to noise, mask time $t_{UVLO1FIL}$ and $t_{UVLO2FIL}$ are set on both low and high voltage sides.

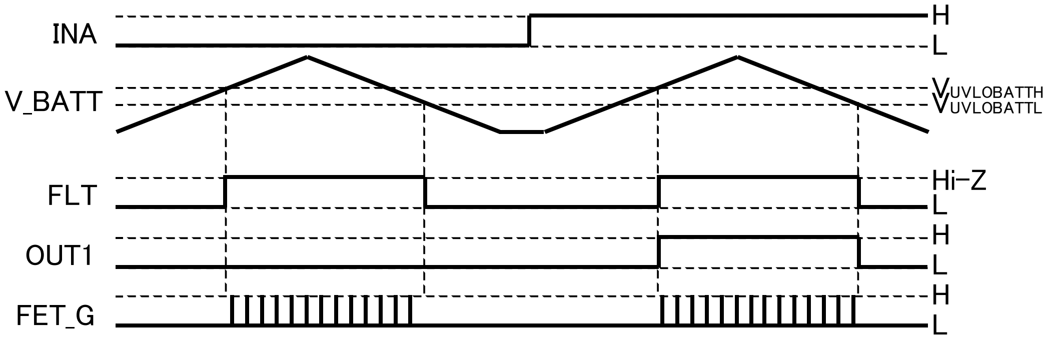



Figure 79. V_BATT UVLO Function Operation Timing Chart

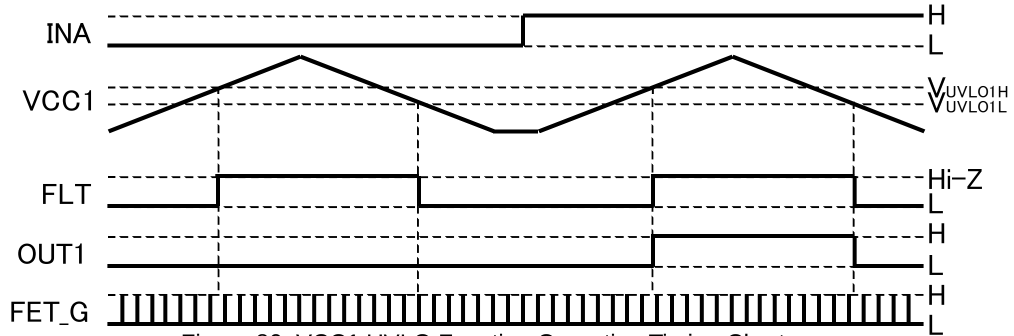



Figure 80. VCC1 UVLO Function Operation Timing Chart

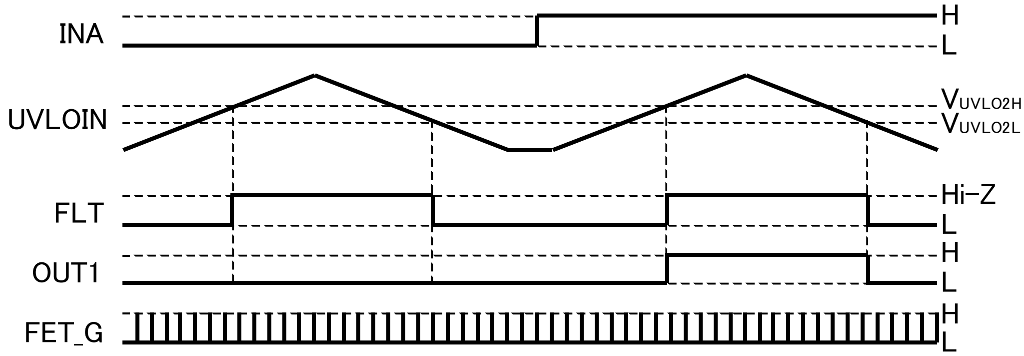



Figure 81. VCC2 UVLO Function Operation Timing Chart

**Description of Functions and Examples of Constant Setting - continued**

3. Short circuit protection (SCP) function
   When the SCPIN pin voltage exceeds a voltage set with the $V_{SCDET}$ parameter, the SCP function will be activated. When the SCP function is activated, the OUT pin voltage will be set to the “Hi-Z” level and the PROOUT pin voltage will go to the “L” level first (soft turn-OFF).Next, when the short-circuit current falls below the threshold value and after $t_{SCPOFF}$ has passed, OUT pin and PROOUT pin become L. Finally, when the fault output holding time is completed, the SCP function will be released.

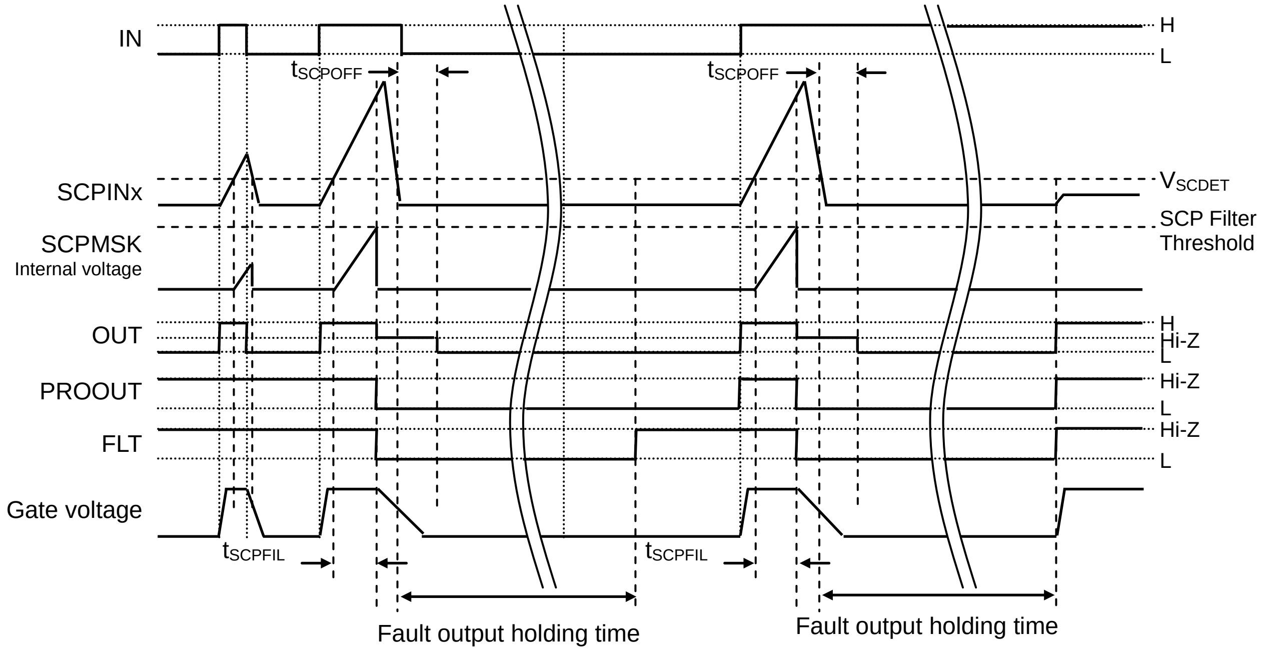



Figure 82. SCP Operation Timing Chart

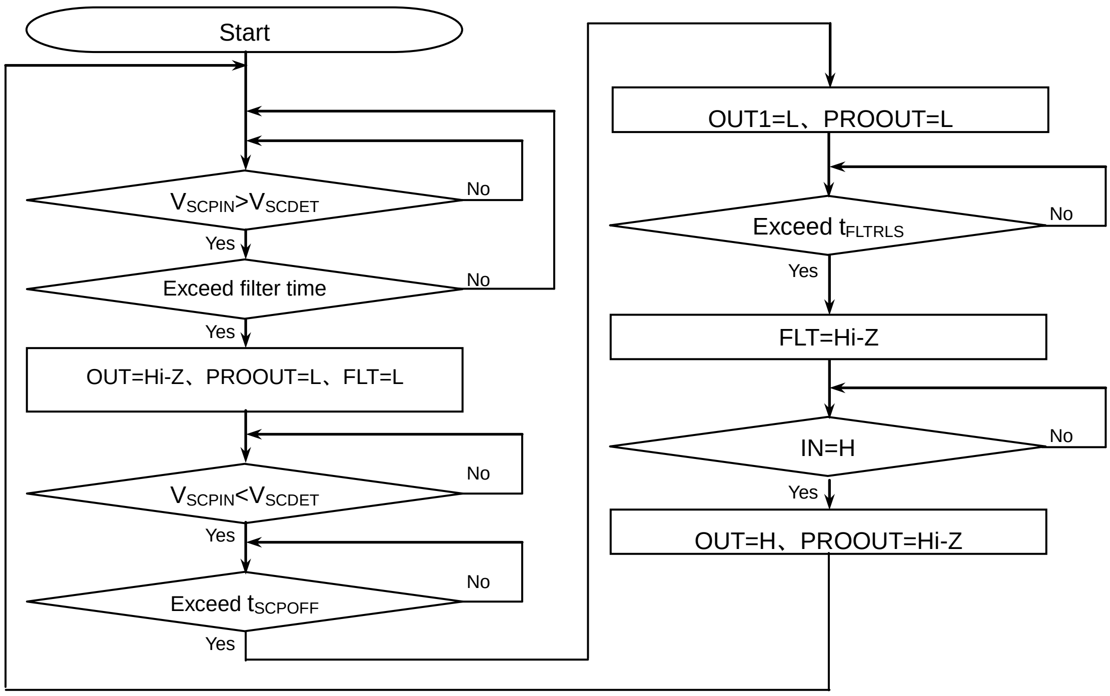



Figure 83. SCP Operation Status Transition Diagram

**Description of Functions and Examples of Constant Setting - continued**

4. Miller Clamp function
When OUT1=L and PROOUT pin voltage < $V_{OUT2ON}$, internal MOS of OUT2 pin is turned ON, and miller clamp function operates. While the short-circuit protection function is activated, miller clamp function operates after lapse of soft turn-OFF release time $t_{SCPOFF}$.

| Short current | SCPIN | INA | PROOUT | OUT2 |
|---|---|---|---|---|
| Detected | Not less than $V_{SCDET}$ | X | X | Hi-Z |
| Not detected | X | L | Not less than $V_{OUT2ON}$ | Hi-Z |
| | X | L | Not more than $V_{OUT2ON}$ | L |
| | X | H | X | Hi-Z |

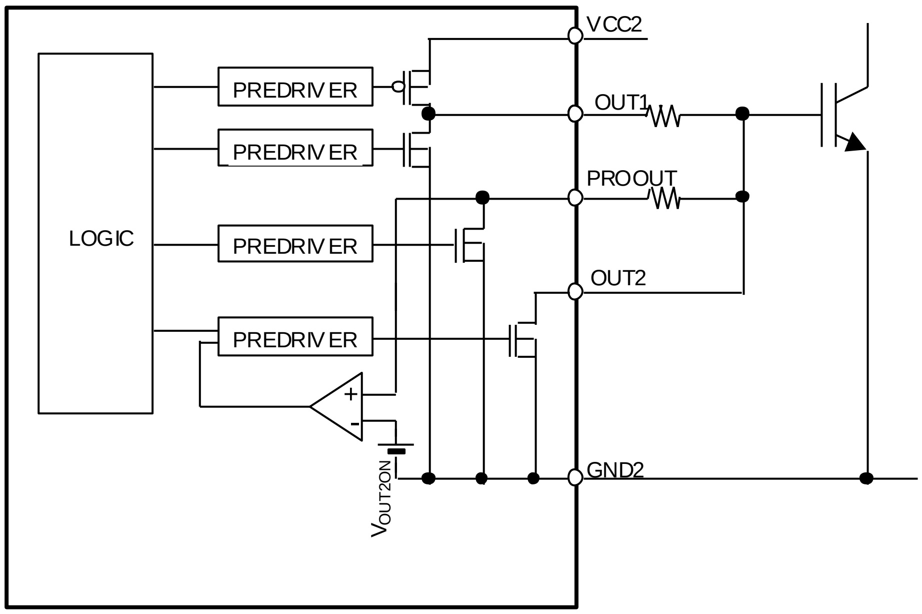



Figure 84. Block Diagram of Miller Clamp Function

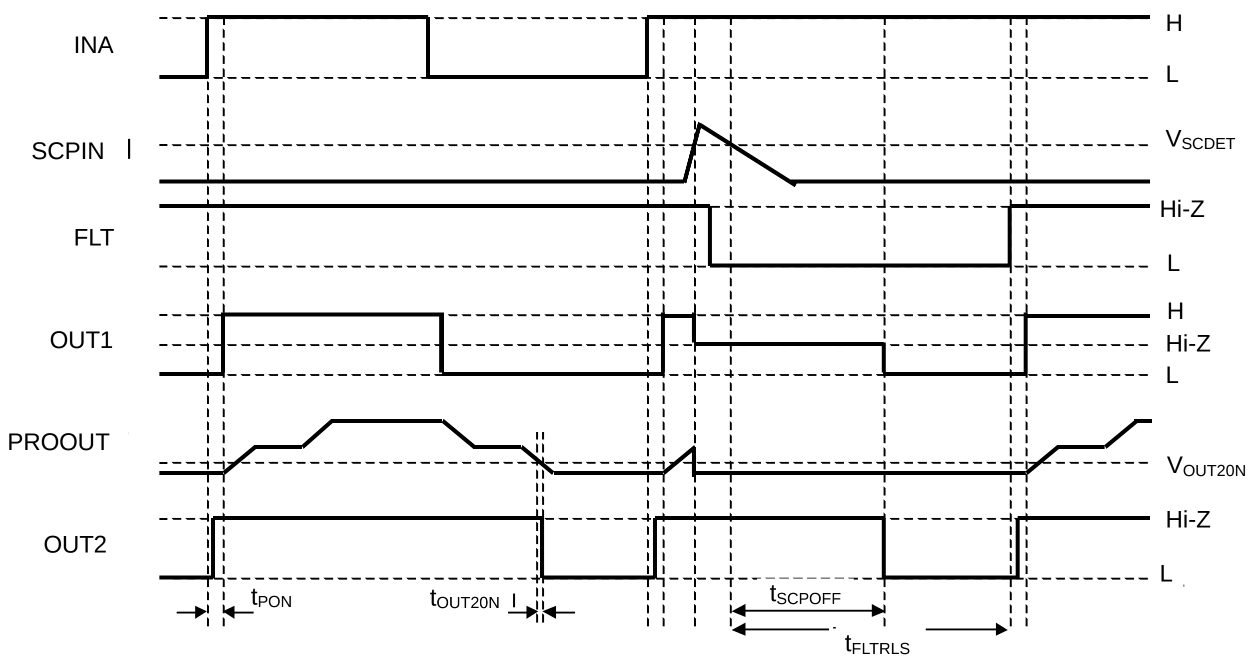



Figure 85. Timing chart of Miller Clamp Function

**Description of Functions and Examples of Constant Setting - continued**

5. Temperature monitor function
   Constant current is supplied from TOx pins from the built-in constant current circuit. This current value can be adjusted in accordance with the resistance value connected between TC and GND2. Furthermore, $TO_X$ pin has voltage input function, and outputs signal of TOx pin voltage converted to Duty from SENSOR pin. When voltage of either one of $TO_X$ pins is no less than disconnect detection voltage $V_{TOH}$, SENSOR pin outputs L. Therefore, when only one of the $TO_X$ pins is used, connect a resistor between the other TO pins and GND2 to keep pin voltage at no more than $V_{TOH}$.

$$\text{Constant current value} = \frac{V_{TC} \times 10}{R_{TC}}$$

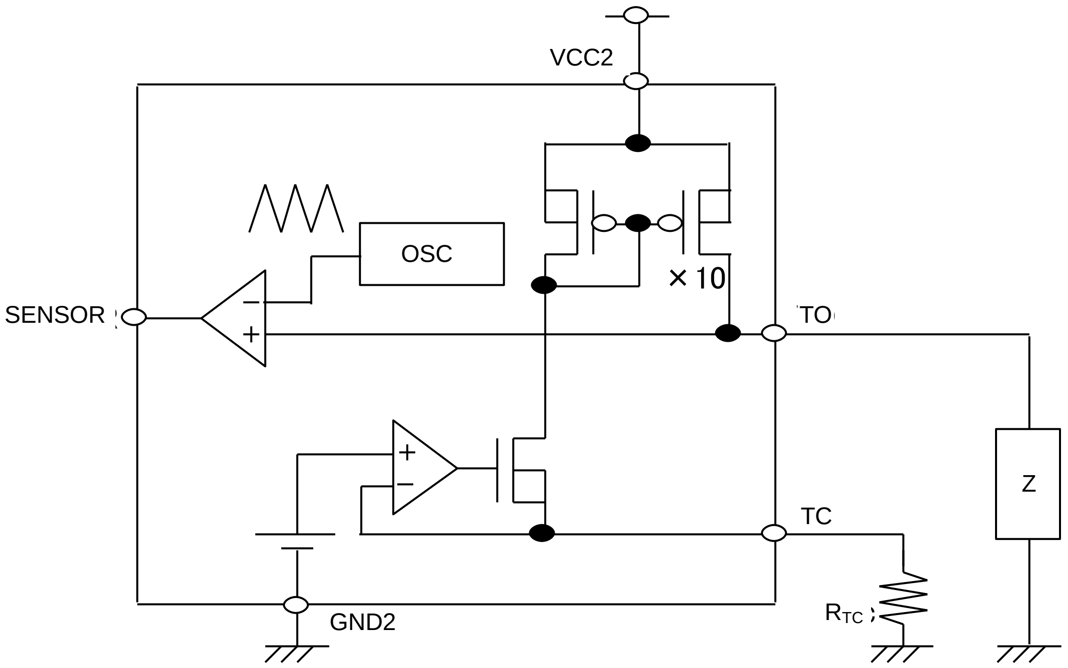
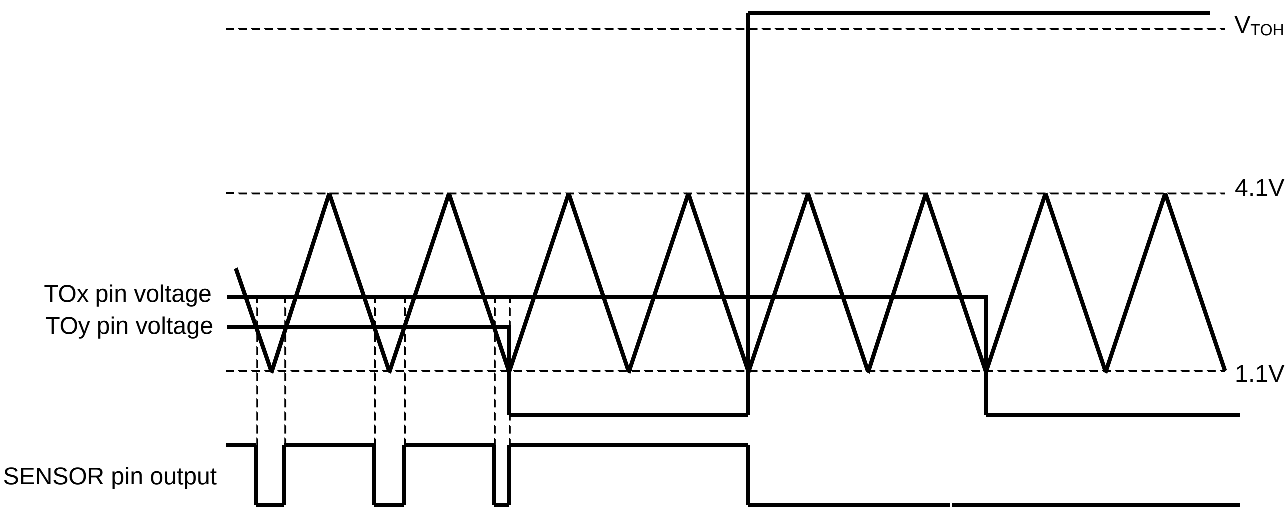



Figure 86. Block Diagram of Temperature Monitor Function




When voltage is no more than $V_{TOH}$, either one of TO1 and TO2 terminals with lower voltage has precedence.

Figure 87. Timing Chart of Temperature Monitor Function

**Description of Functions and Examples of Constant Setting - continued**

6. Switching regulator

(1) Basic action

This IC has a built-in switching power supply controller which repeats ON/OFF synchronizing with internal clock. When VBATT voltage is supplied (VBATT > $V_{UVLOBATTH}$), FTE_G pin starts switching by soft-start. Output voltage is determined by the following equation by external resistance and winding ratio “n” of flyback transformer (n= $V_{OUT2}$ side winding number/$V_{OUT1}$ side winding number)

$$V_{OUT2} = V_{FB} \times \{(R_1 + R_2)/R_2\} \times n [V]$$

(2) MAX DUTY

When, for example, output load is large, and voltage level of SENSE pin does not reach current detection level, output is forcibly turned OFF by Maximum On Duty ($D_{ONMAX}$).

(3) Pinconditions when the switching power supply controller is not used

Implement pin treatment as shown below when switching power supply is not used.

| Pin Number | Pin Name | Treatment Method |
|---|---|---|
| 22 | FB | Connect to VCC1 |
| 23 | COMP | Connect to GND1 |
| 24 | V_BATT | Connect power supply |
| 25 | VREG | Connect capacitor |
| 26 | FET_G | No connection |
| 27 | SENSE | Connect to VCC1 |

7. Gate state monitoring function

When gate logic and input logic of output device monitored with PROOUT pin are compared, a logic L is output from OSFB pin when they disaccord. In order to prevent the detection error due to delay of input and output, OSFB filter time $t_{OSFBON}$ is provided.

**Description of Functions and Examples of Constant Setting - continued**

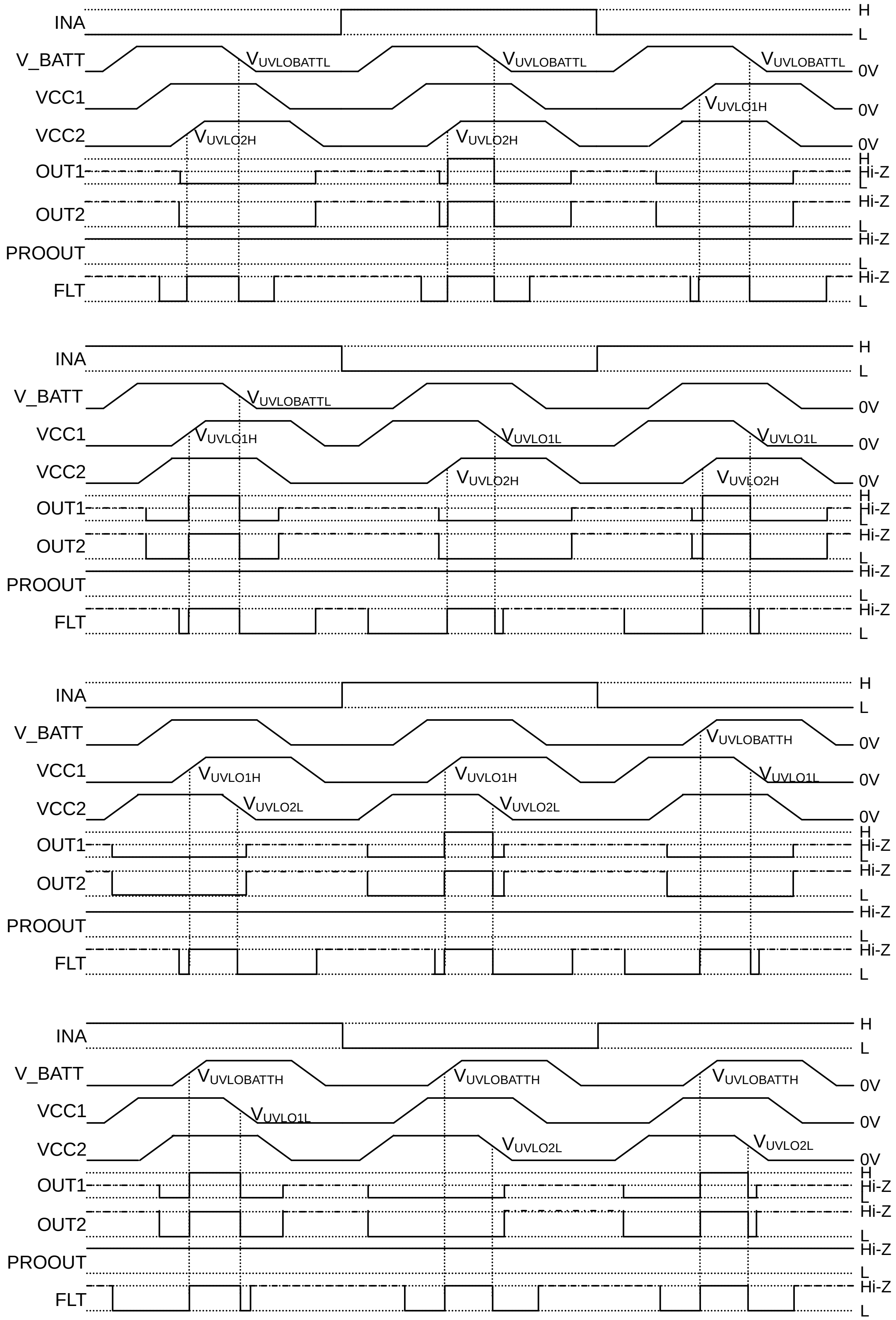
8. I/O condition table

| No. | Status | Input | | | | | | | Output | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCC1 | UVLOIN | VBATT | SCPINx | DIS | INA | PROOUT | OUT1 | OUT2 | PROOUT | FLT | OSFB |
| 1 | SCP | ○ | H | ○ | H | L | H | X | Z | Z | L | L | Z |
| 2 | VCC1UVLO | UVLO | X | X | L | X | X | H | L | Z | Z | L | Z |
| 3 | VCC1UVLO | UVLO | X | X | L | X | X | L | L | L | Z | L | Z |
| 4 | VCC2UVLO | X | L | X | L | X | X | H | L | Z | Z | L | Z |
| 5 | VCC2UVLO | X | L | X | L | X | X | L | L | L | Z | L | Z |
| 6 | VBATT1UVLO | X | X | UVLO | L | X | X | H | L | Z | Z | L | Z |
| 7 | VBATT1UVLO | X | X | UVLO | L | X | X | L | L | L | Z | L | Z |
| 8 | Disable | ○ | H | ○ | L | H | X | H | L | Z | Z | Z | L |
| 9 | Disable | ○ | H | ○ | L | H | X | L | L | L | Z | Z | Z |
| 10 | Normal Operation L Input | ○ | H | ○ | L | L | L | H | L | Z | Z | Z | L |
| 11 | Normal Operation L Input | ○ | H | ○ | L | L | L | L | L | L | Z | Z | Z |
| 12 | Normal Operation H Input | ○ | H | ○ | L | L | H | H | H | Z | Z | Z | Z |
| 13 | Normal Operation H Input | ○ | H | ○ | L | L | H | L | H | Z | Z | Z | L |

○: VCC1 > UVLO, X: Don't care, Z: Hi-Z

**Description of Functions and Examples of Constant Setting - continued**

9. Power supply startup / shutoff sequence




-·-·-·- : Since the VCC2 to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

------- : Since the VCC1 pin voltage is low and the FLT output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 88. Power Supply Startup / Shutoff Sequence

## Selection of Components Externally Connected

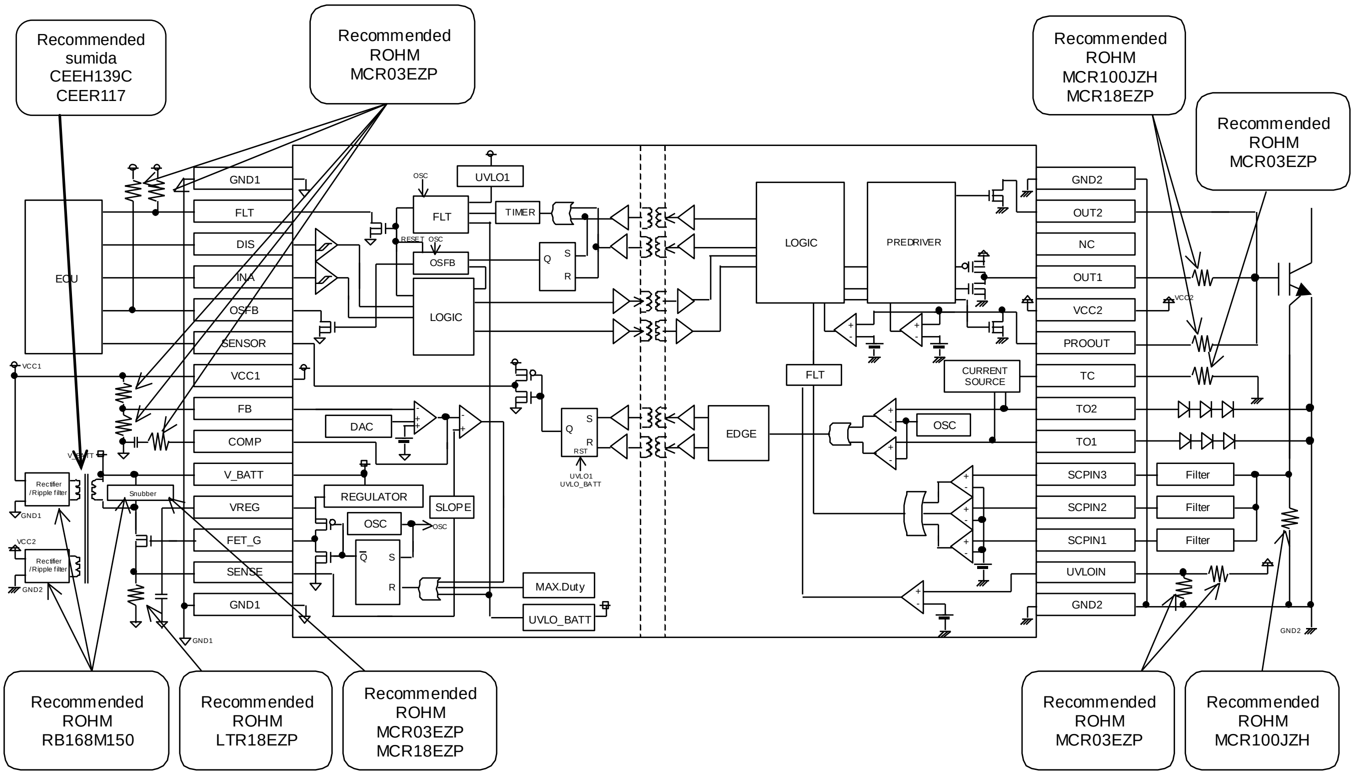



Figure 89. For using switching power supply controller

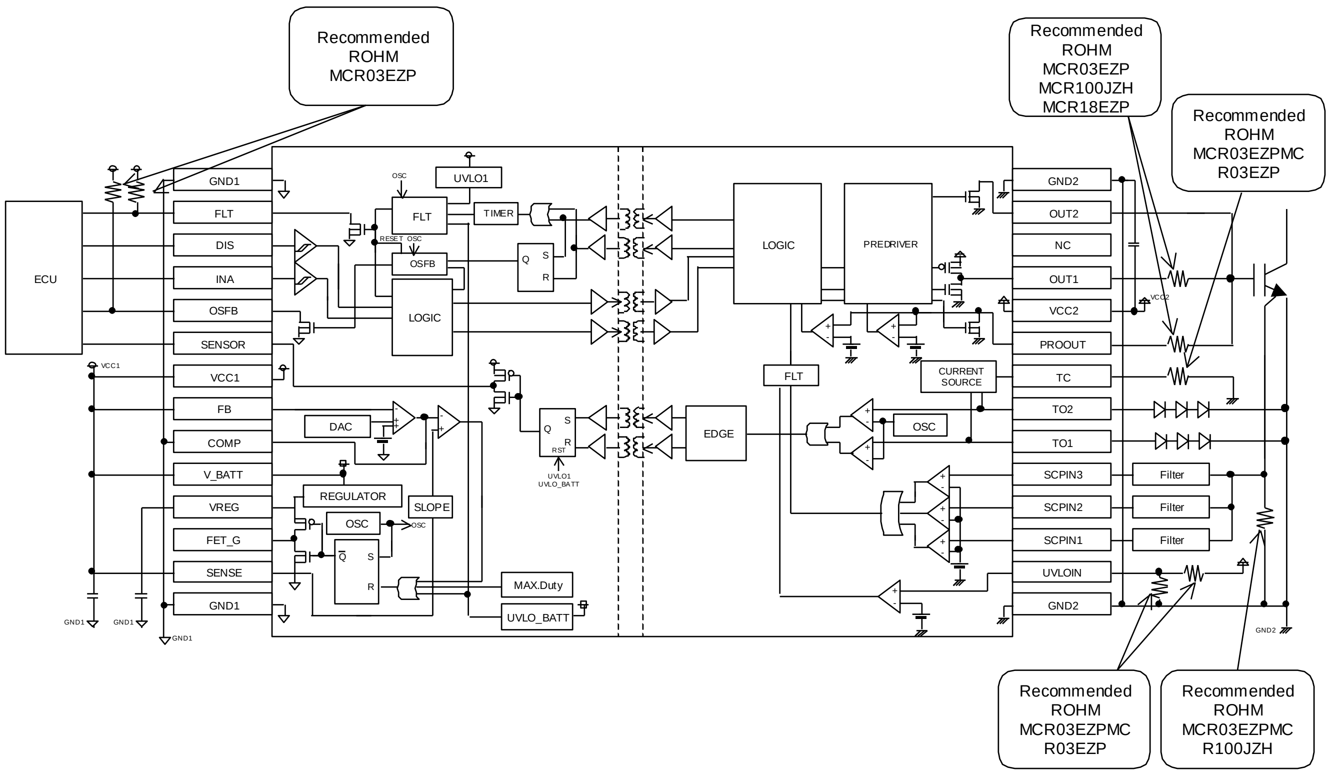



Figure 90. For no using switching power supply controller

## Power Dissipation

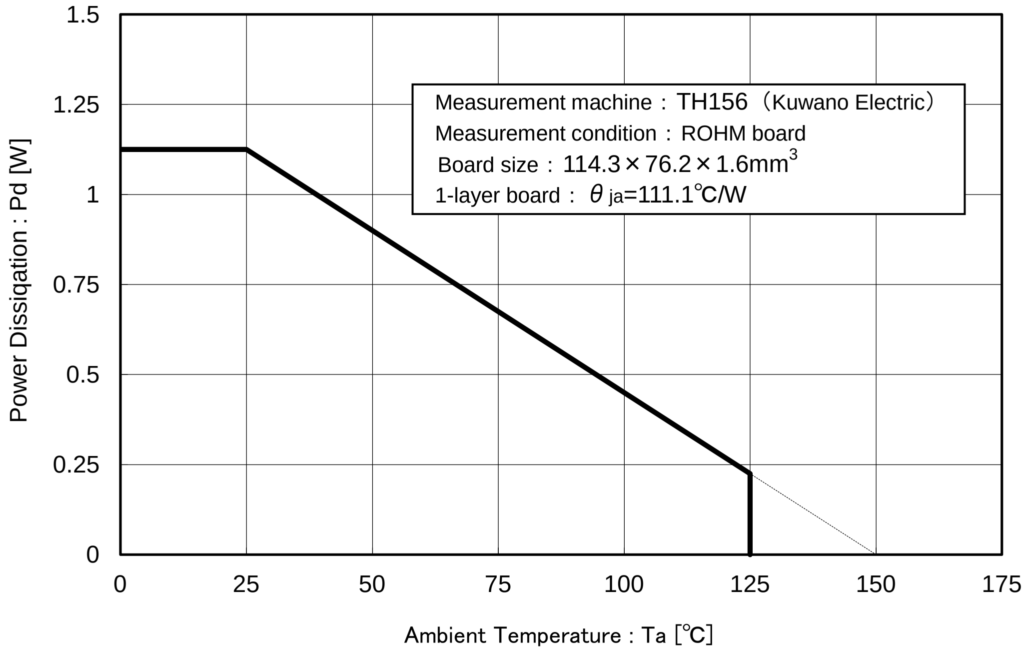
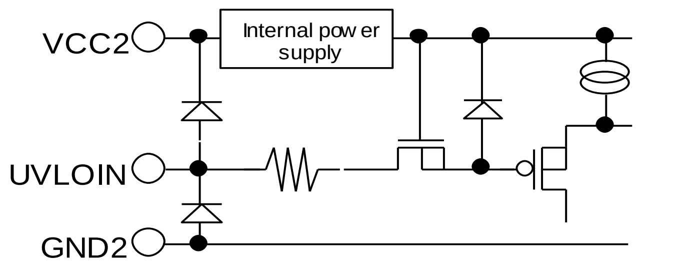
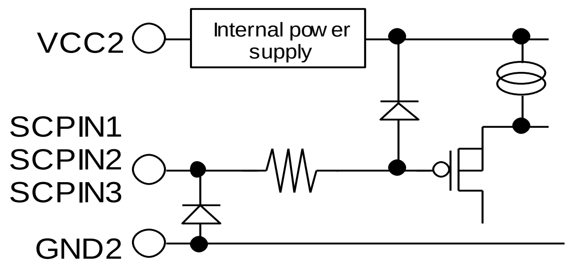
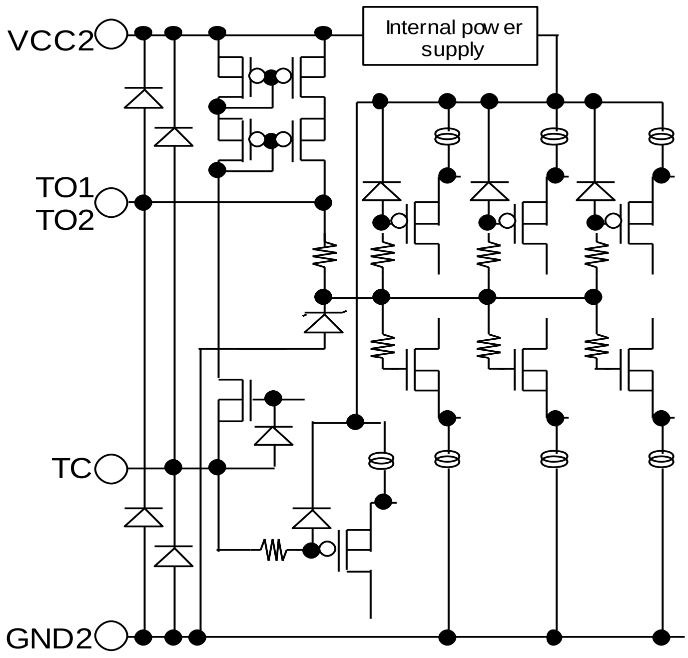



Figure 91. SSOP-B28W Power Dissipation Curve (Pd-Ta Curve)

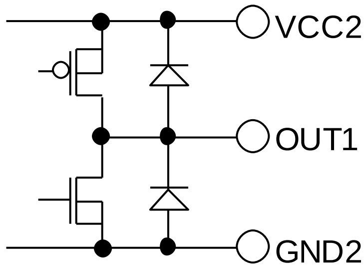
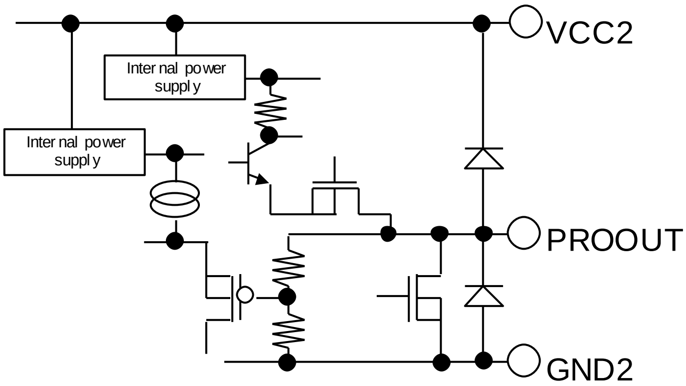
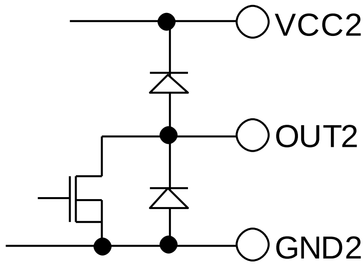
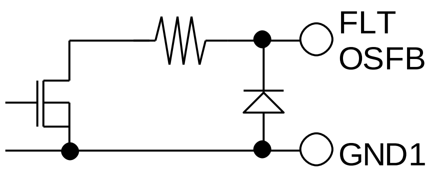
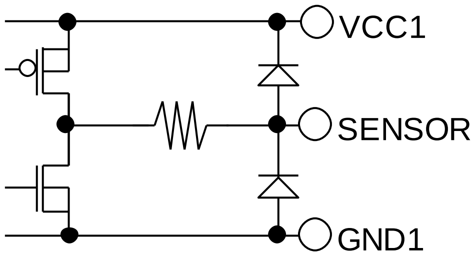
**Thermal Design**

Please make sure that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded, the IC may malfunctions or some problems (ex. abnormal operation of various parasitic elements and increasing of leak current) may occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly obeyed under all circumstances.

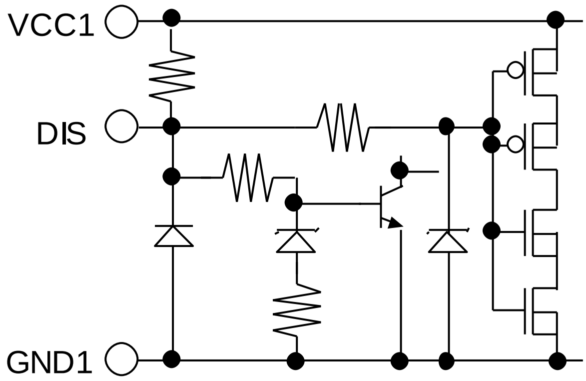
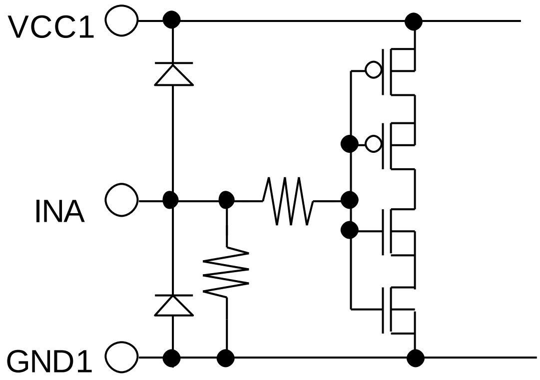
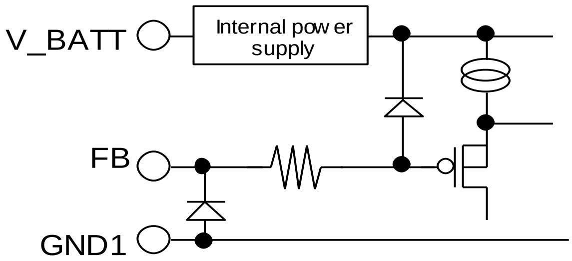
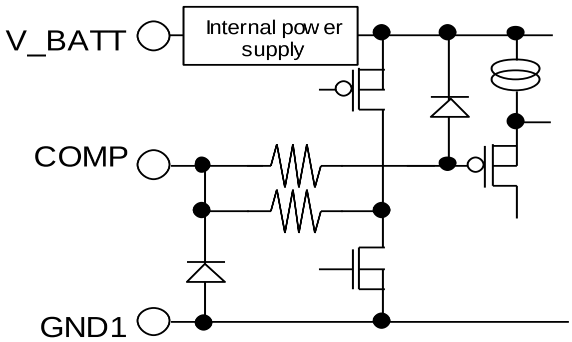
### I/O Equivalent Circuit

| Pin No. | Pin Name | Pin Function | Input Output Equivalent Circuit Diagram |
|---|---|---|---|
| 2 | UVLOIN | Output-side UVLO setting pin |   |
| 3 | SCPIN1 | Short circuit current detection pin 1 |   |
| 4 | SCPIN2 | Short circuit current detection pin 2 | |
| 5 | SCPIN3 | Short circuit current detection pin 3 | |
| 6 | TO1 | Constant current output pin / sensor voltage input pin 1 |   |
| 7 | TO2 | Constant current output pin / sensor voltage input pin 2 | |
| 8 | TC | Constant current setting resistor connection pin | |

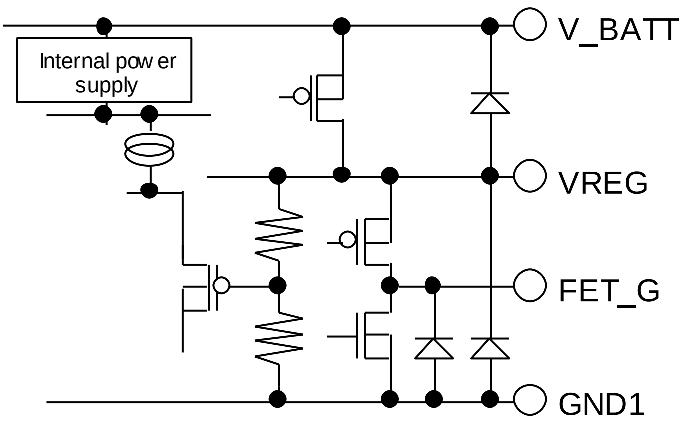
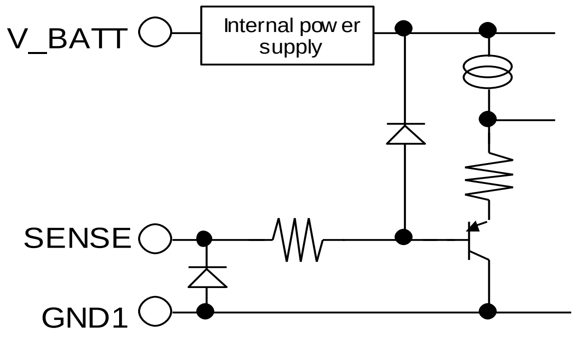
### I/O Equivalent Circuit - continued

| Pin No. | Pin Name / Pin Function | Input Output Equivalent Circuit Diagram |
|---|---|---|
| 11 | OUT1 |   |
| | Output pin | |
| 9 | PROOUT |   |
| | Soft turn-OFF pin /Gate voltage input pin | |
| 13 | OUT2 |   |
| | Output pin for Miller Clamp | |
| 16 | FLT |   |
| | Fault output pin | |
| 19 | OSFB | |
| | Output state feedback output pin | |
| 20 | SENSOR |   |
| | Temperature information output pin | |

### I/O Equivalent Circuit - continued

| Pin No. | Pin Name / Pin Function | Input Output Equivalent Circuit Diagram |
|---|---|---|
| 17 | DIS<br>Input enabling signal input pin |  |
| 18 | INA<br>Control input pin |  |
| 22 | FB<br>Error amplifier inverting input pin for switching controller |  |
| 23 | COMP<br>Error amplifier output pin for switching controller |  |

### I/O Equivalent Circuit - continued

| Pin No. | Pin Name / Pin Function | Input Output Equivalent Circuit Diagram |
|---|---|---|
| 25 | VREG<br>Power supply pin for driving MOS FET of switching controller |  |
| 26 | FET_G<br>MOS FET control pin for switching controller | |
| 27 | SENSE<br>Current feedback resistor connection pin for switching controller |  |

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

11. **Unused Input Terminals**
Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

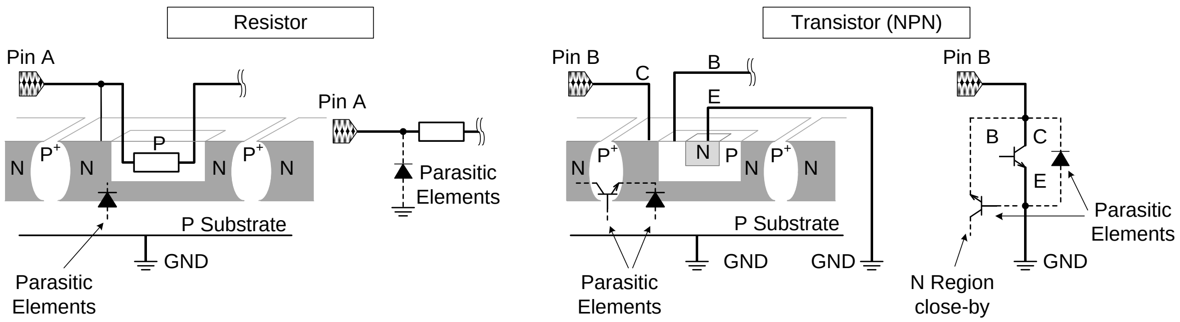
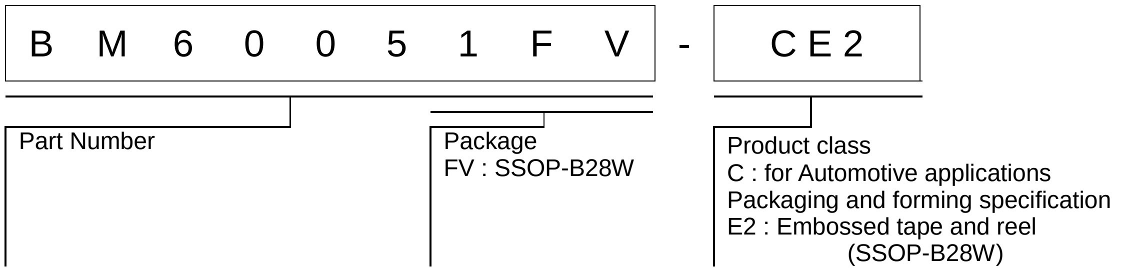


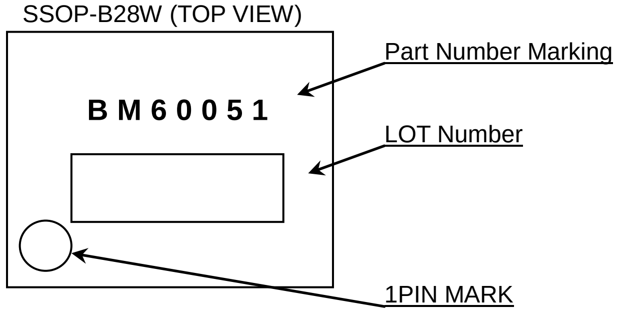

Figure 24. Example of monolithic IC structure

13. **Ceramic Capacitor**
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

## Ordering Information

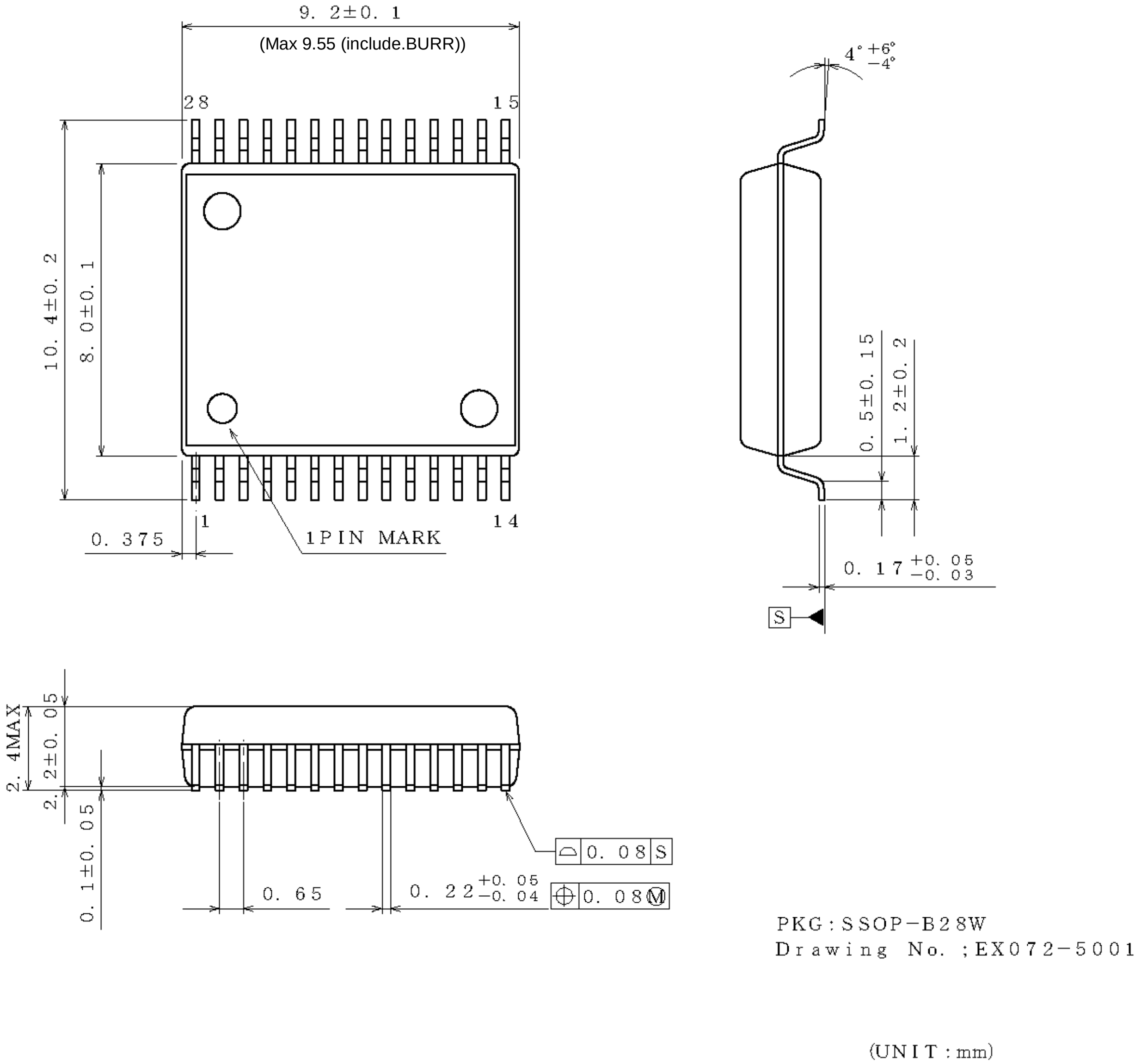



## Marking Diagram



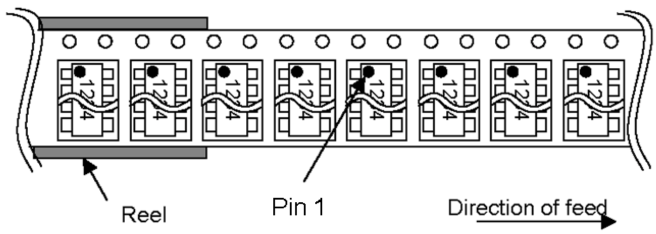
**Physical Dimension, Tape and Reel Information**

| Package Name | SSOP-B28W |
|---|---|




< Tape and Reel Information >

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 1500pcs |
| Direction of feed | E2<br>The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |



**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 25.Apr.2014 | 001 | New Release |
| 13.May.2015 | 002 | P.1 Features Adding item (UL1577 Recognized)<br>P.21,22 Typical Performance Curves Correcting mistakes |

# Notice

## Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

QR code printed on ROHM Products label is for ROHM’s internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

## Precaution Regarding Intellectual Property Rights

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