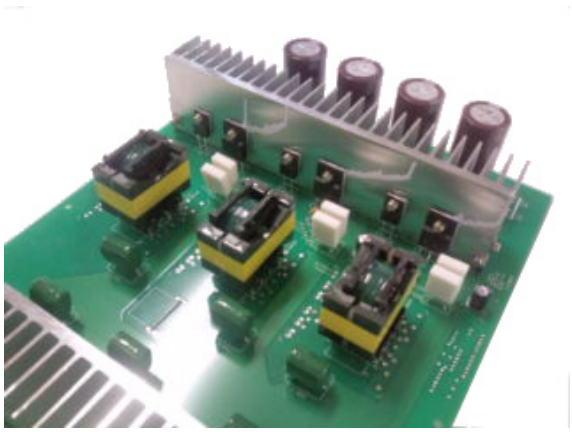
Easy Multi Interleave
Controller for multi-phase
interleaved PFC

MH2501SC/MH2511SC



Application Note ver.1.0

Shindengen Electric Manufacturing Co., Ltd.

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		**Check the polarity of the input and output terminals. Make sure they are properly connected before turning on power. <<Failure to do so may lead to failure of the protective element or generate smoke or fire.>>**
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Notes

The figures in this document are provisional. For nominal values, please refer to the formal specifications.

[Indication of IC]

Master — Function of master IC only

Master / Slave — Function common to master IC and slave IC

1 Outline

MH2501SC (“master IC” hereinafter) and MH2511SC (“slave IC” hereinafter) comprise ICs for a current-critical interleaved PFC circuit. Interleaving with master and slave ICs ensures low noise and high efficiency, which are characteristics of current-critical PFCs, even in high power regions. One-phase PFC can be configured using just the master IC.

1.1 Features

1. High efficiency and low noise via master-slave interleaved critical current mode
2. Two or greater phase interleaving achieved by connecting slave ICs in parallel
3. One-phase PFC configurable using just the master IC
4. Support for wide range of input voltages with guaranteed VCC withstand voltage of 26 V
5. Variety of protective functions
   (overvoltage protection, overcurrent protection, feedback open/short protection, and output diode short protection)

1.2 Block diagram

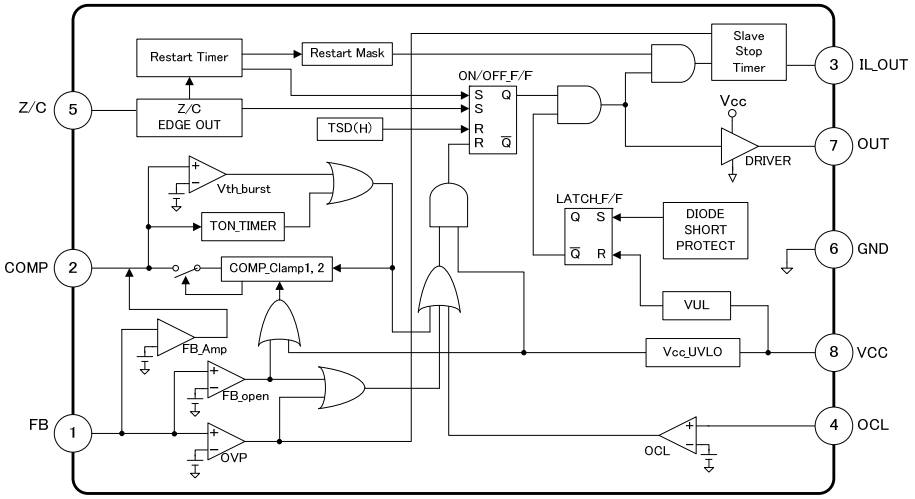


Fig. 1 Master IC (MH2501SC) block diagram

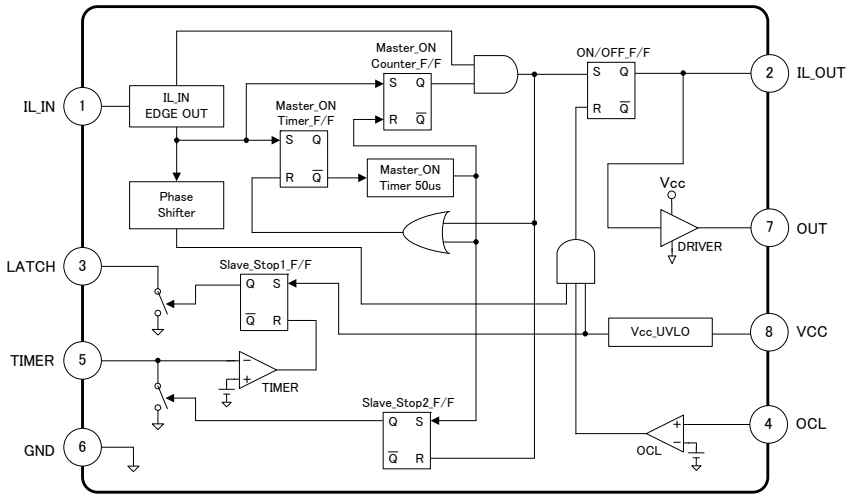
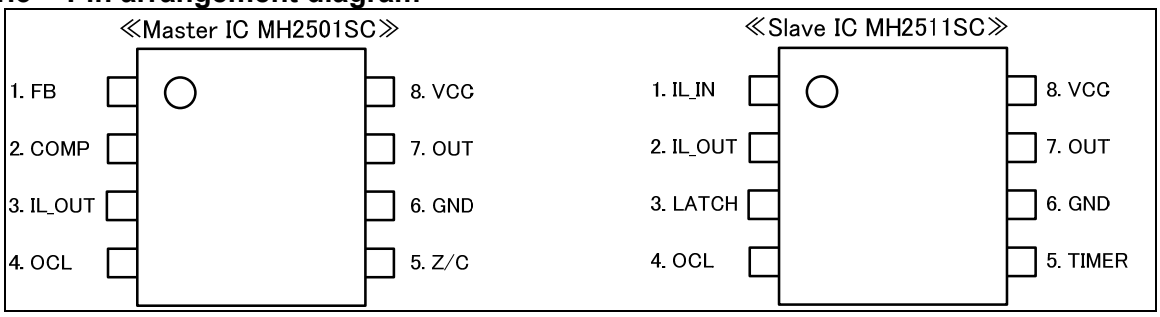


Fig. 2 Slave IC (MH2511SC) block diagram

1.3 Pin arrangement diagram



Package: SOP8

Fig. 3 Pin arrangement diagrams for MH2501SC and MH2511SC

1.4 Pin function list

<< Master IC MH2501SC>>

Pin No.	Symbol	Function
1	FB	**Input pin of feedback error amplifier**
2	COMP	**Output pin of feedback error amplifier**
3	IL_OUT	**Output pin for signal for interleaving** Connected to IL_IN pin of a slave IC
4	OCL	**Input pin for overcurrent detection**
5	Z/C	**Zero current detection pin of master IC**
6	GND	**GND pin**
7	OUT	**Output pin for driving MOSFET of master IC**
8	VCC	**Power supply voltage input pin**

<< Slave IC MH2511SC>>

Pin No.	Symbol	Function
1	IL_IN	**Input pin for signal for interleaving** Connected to IL_OUT pin of the master IC or previous–phase slave IC
2	IL_OUT	**Output pin for signal for interleaving** Connected to IL_IN of the next slave IC
3	LATCH	**Output pin for latching** Stops the operation of the master IC in case of problems with a slave
4	OCL	**Input pin for overcurrent detection**
5	TIMER	**Timer capacitor connection pin for detection in one-phase configuration** Detects whether a slave IC is operating
6	GND	**GND pin**
7	OUT	**Output pin for driving MOSFET of slave IC**
8	VCC	**Power supply voltage input pin**

2 Operating principles

2.1 Operating principles of current-critical PFC with ON range control

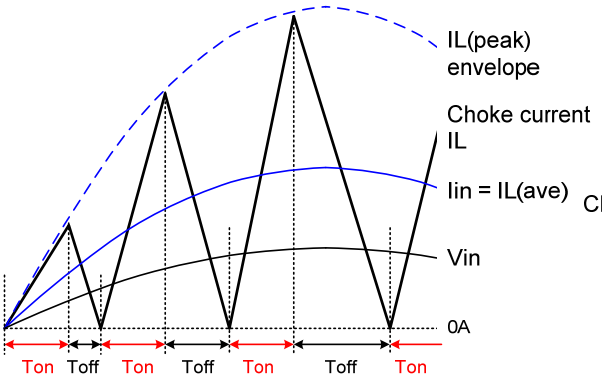


Fig. 4 Critical operation

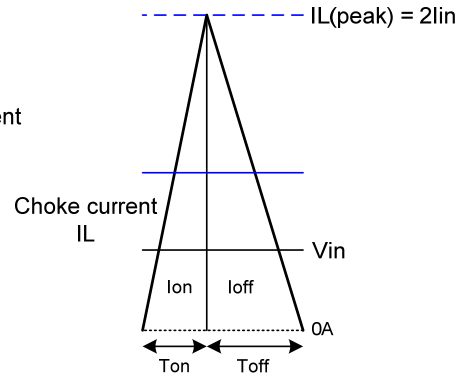


Fig. 5 Waveform of a single switching cycle

This IC employs a current-critical system. As shown in Fig. 4, the choke current IL forms triangle waves, starting and ending at 0 A repeatedly. The IC also uses an ON range control system. The ON range T_{on} is determined by the load and is fixed. The OFF range T_{off} varies with the input voltage V_{in} at every switching. The switching period varies.

The following formulas give the currents:
T_{on} and L are fixed. The peak value of IL, IL(peak), is proportional to V_{in}. Since V_{in} is sinusoidal, IL(peak) is sinusoidal. (Formula 1)

$$IL(peak) = \frac{V_{in} \times T_{on}}{L} \quad [\mathrm{A}] \qquad \ldots(1)$$

The switching frequency is significantly higher than the AC commercial frequency. V_{in} is considered constant during a single switching cycle (Fig. 5).

The input current I_{in} equals IL(ave), which is IL with its high frequency component removed by the capacitor C_{in} and averaged. Since IL is a triangle wave, IL(ave) is half of IL(peak). (Formula 2)

$$I_{in} = IL(ave) = \frac{IL(peak)}{2} \quad [\mathrm{A}] \qquad \ldots(2)$$

We substitute Formula 1 into Formula 2.

$$I_{in} = IL(ave) = \frac{IL(peak)}{2} = \frac{V_{in} \times T_{on}}{2L} \quad [\mathrm{A}] \qquad \ldots(3)$$

As Formula 3 shows, I_{in} is proportional to V_{in} due to the ON range control of this IC. The power factor is improved. Fig. 6 shows waveform examples on the circuit.

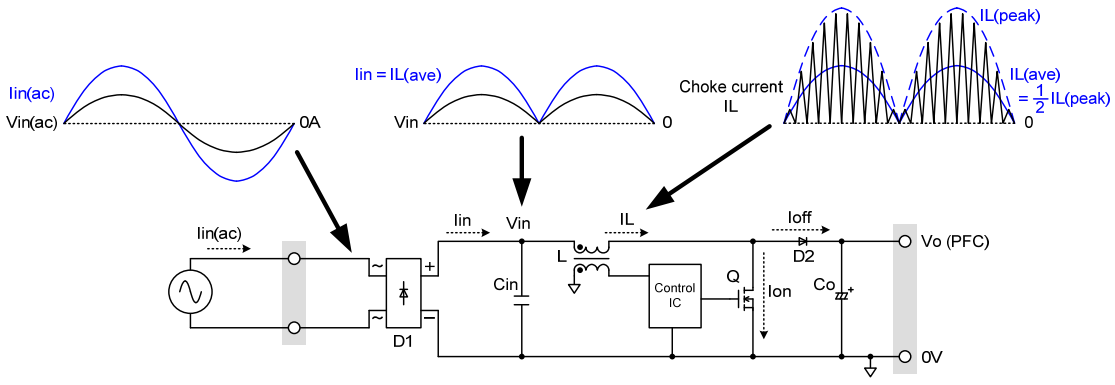


Fig. 6 Waveform examples on the circuit

2.2 Zero current detection Master

This IC detects the control coil voltage to turn on the switching device. The Z/C pin determines turn-on timing.

As shown in Fig. 7, the main switch activates when the Z/C pin voltage drops below the zero detection voltage (0.5 V). The main switch is turned on after every switching cycle once the energy of the choke coil is fully discharged (i.e., a current-critical operation is performed). Hysteresis of +1 V is added to the zero detection voltage to increase noise resistance. Unless a voltage exceeding +1.5 V is applied to the Z/C pin, the switch operates in the restart cycle (150 µs). This IC incorporates an on-dead timer. This function disables the on-trigger for a period (Tondead) after the gate-off signal is turned on, thereby preventing unintended operations due to ringing generated at gate-off. A ringing voltage may be generated at gate-off, resulting in detection of the on-trigger and turning on the switch before the current critical point.
See ***Section 4.5*** for constants for the components around the Z/C pin.

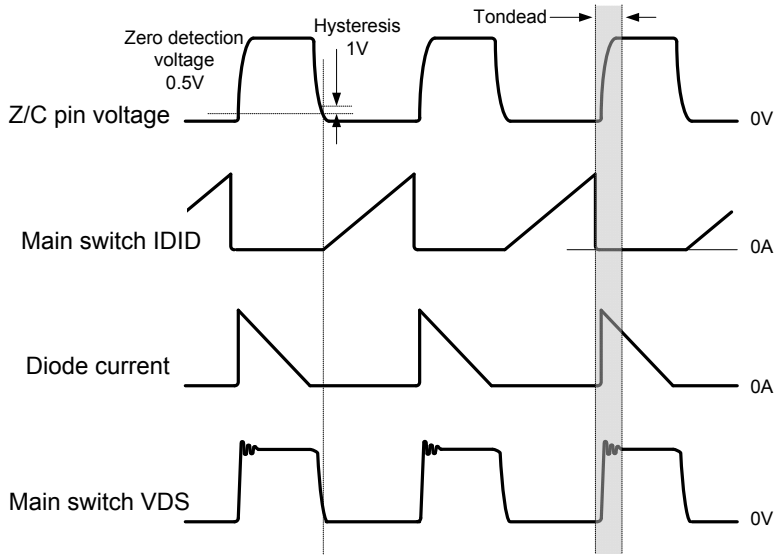


Fig. 7 Turn-on timing (Z/C pin)

2.3 Interleaving Master Slave

Multi-phase interleaved critical conduction mode PFC is configured by connecting the master IC and several slave ICs.

* Master IC pin names are identified by an appended “M”; slave IC pin names are identified by an appended “S” and a unique slave identification number at the end.

The IL_OUT(M) pin of the master IC is a signal output pin that activates interleaving by a slave IC. The IL_OUT(M) pin is connected to the IL_IN(S1) pin of the slave IC.。
As shown in Fig. 8, for multi-phase interleaving of three or more phases, the IL_OUT(S1) pin is connected to the IL_IN(S2) pin of the next slave IC.
To reduce noise, insert a resistor and a capacitor near the IL_IN pin. We recommend a 1 kΩ resistor and a 47 pF capacitor.

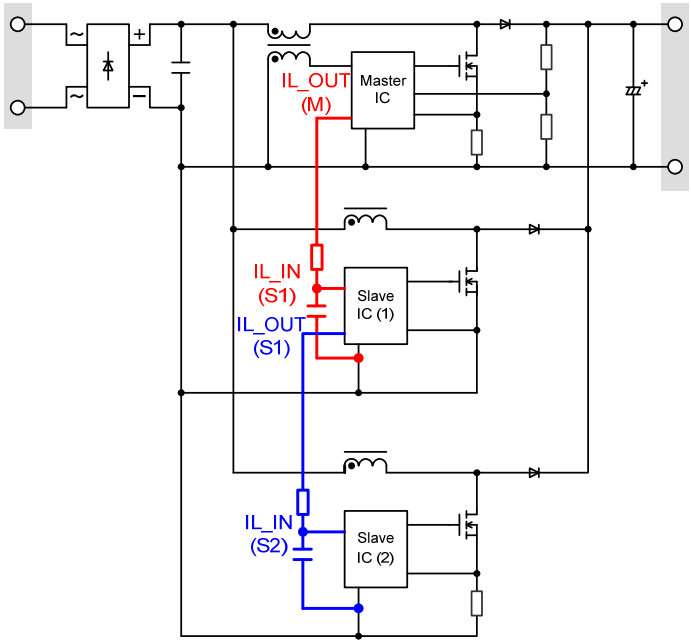


Fig. 8 Example of interleaved connection

This section discusses turn-on timing and transmission of the ON range in an interleaved circuit. Fig. 9 shows the operating sequence. The arrows in Fig. 9 indicate the transmission order of ON range. See Fig. 9 for waveform and arrow numbers referenced in the text below.

1) The OUT (M) of the master IC outputs a Hi signal determined by the negative edge of the Z/C pin and the COMP pin voltage.

2) The IL_OUT(M) signal of the master IC is output in sync with the OUT(M) (waveform C and arrow 1).

3) The IL_OUT(M) signal of the master IC is input to the IL_IN(S1) pin of the slave IC via CR as shown in Fig. 8 (waveforms C and D and arrow 2).
In the slave IC (1), the counter circuit stores the ON range of the IL_IN(S1).

4) The OUT(S1) of the slave IC (1) is turned on when the master IC is turned off to output the stored ON range. The ON range is the same as that of the OUT(M) (waveform E and arrow 3).

5) The IL_OUT(S1) signal of the slave IC (1) is output in sync with the OUT(S1) (waveform F and arrow 4).

6) To achieve multi-phase interleaving, connect the IL_OUT(S1) pin to the IL_IN(S2) pin of the next slave IC (2) (waveform F and arrow 5).

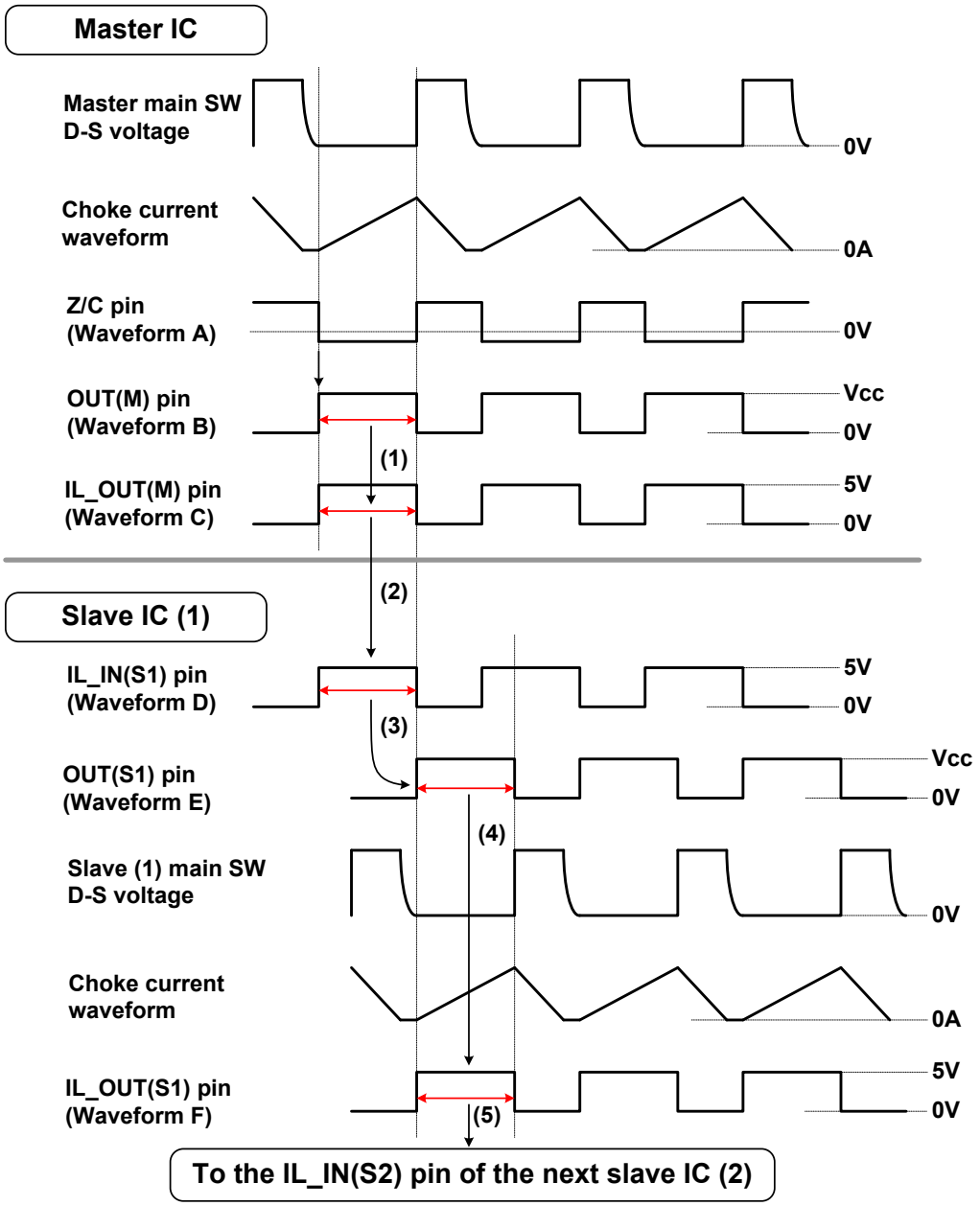


Fig. 9 Interleaved operating sequence

2.4 Startup and shutdown sequences

Master Slave

Fig. 10 shows the startup and shutdown sequences for interleaved operation. VCC is common to the master IC and slave IC.

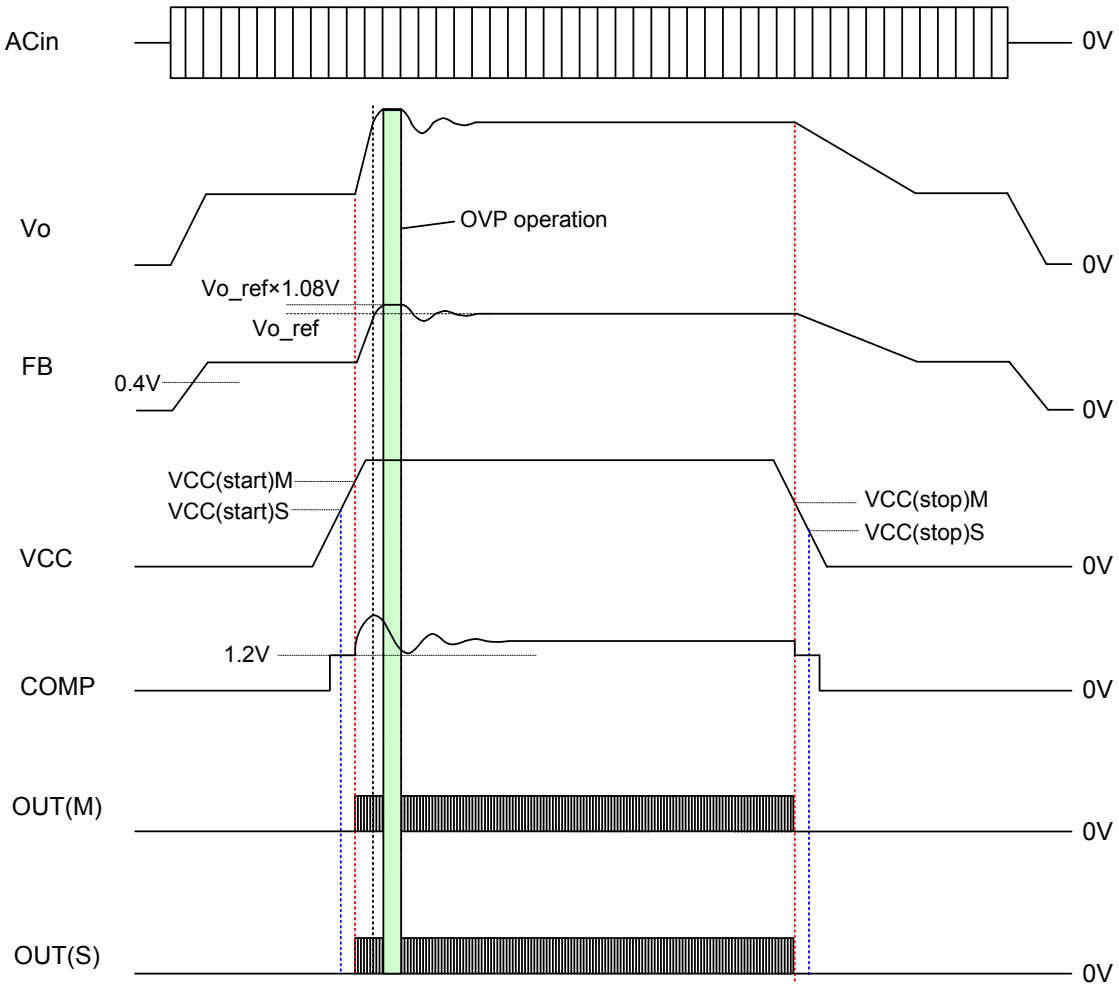


Fig. 10 Startup and shutdown sequences

(a) Oscillation start sequence

(1) When a voltage is applied to the VCC pin, the COMP is charged to 1.2 V.

(2) When the VCC voltage reaches VCC(start)S, the slave IC starts up. However, the gate signal is not output, since the master IC has not started up.

(3) When the VCC voltage reaches VCC(start)M, the master IC also starts up and starts the gate output. The slave IC also starts gate output.

(4) Immediately after startup, gate output stops due to the OVP operation, suppressing an increase in output voltage.

(b) Oscillation stop sequence

(1) When the VCC voltage has fallen to VCC(stop)M, the master IC shuts down and stops the gate output. The slave IC also stops the gate output. The COMP voltage is clamped to 1.2 V.

(2) When the VCC voltage has fallen to VCC(stop)S, the slave IC shuts down.

2.5 Output voltage control Master

This IC detects the output voltage and changes the ON range of the main switch to control the output voltage.
As shown in Fig. 11, the output voltage is divided using the resistors R191 to 195 and R196 and the fraction of the voltage is applied to the FB pin. This stabilizes the output voltage relative to which the FB pin voltage is 2.5 V.
The COMP pin voltage, the output of a feedback error amplifier, is proportional to the ON range of the main switch. The switch is activated when the voltage is 1.2 V or greater. The ON range reaches the maximum when the voltage is 4.0 V (Fig. 12). This feedback controls the COMP pin voltage and stabilizes the output voltage.

Connect a capacitor (C191) near the FB and GND pins to reduce noise. A capacitor with excessive capacity may affect response. We recommend 1000 pF to 2200 pF.

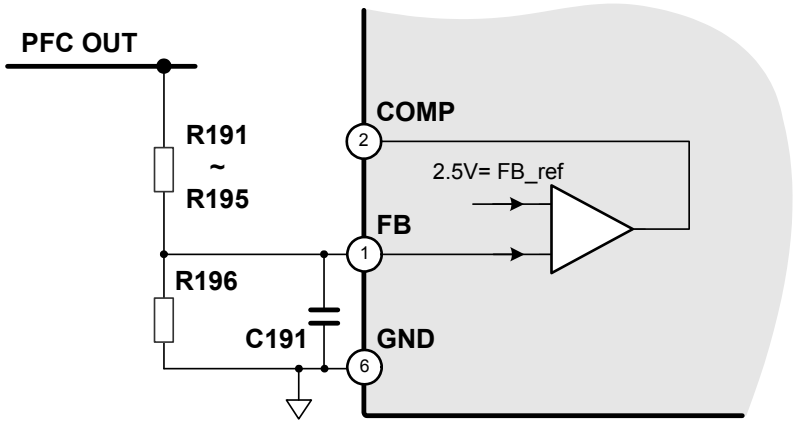


Fig. 11 FB pin internal block diagram

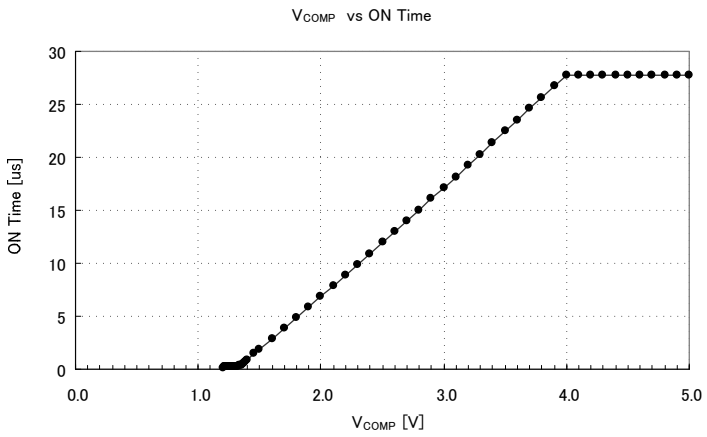


Fig. 12 Relationship between COMP pin voltage and ON range

2.6 Phase compensation Master

The PFC converter must be adjusted so that it does not respond to commercial AC input frequencies. Capacitors (C113 and C114) and a resistor (R117) are connected between the COMP pin and GND pin of the master IC to correct the phase of the amplifier and reduce the feedback loop gain at commercial AC input frequencies. Fig. 13 shows an example circuit. We recommend a C114 of about 2.2 uF, C113 of 0.22 uF, and R117 of 1 kΩ. See ***Section 4.6*** for information on adjusting the COMP pin.

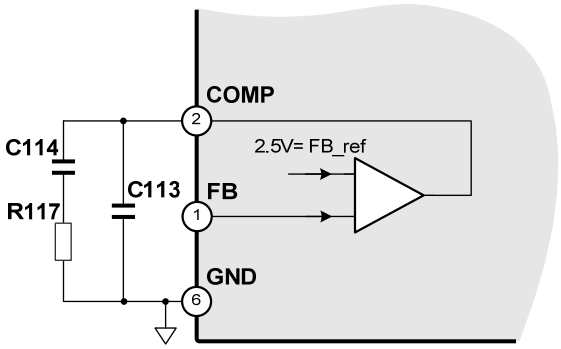


Fig. 13 COMP pin connection example

2.7 Gate driver Master Slave

The signal output from the OUT pin determines the turn-on and turn-off timings for each switch. The OUT pin receives a supply from the power supply voltage VCC. The gate driver capacity is 0.5 A (Source) and 1.2 A (Sink).

Fig. 14 shows examples of commonly used driver circuits.
When a discharging diode (D112) is used as shown in Examples A and B, use a small-capacity Schottky diode or other such diode. Do not use a snappy (hard) recovery diode. We recommend D1NS4 (axial) or M1FM3 (surface mounting).

If the Qg of MOSFET (Q111) is large and when full discharge is not possible, add a PNP transistor (Q112) on the discharge side as shown in the example C), Fig. 14.

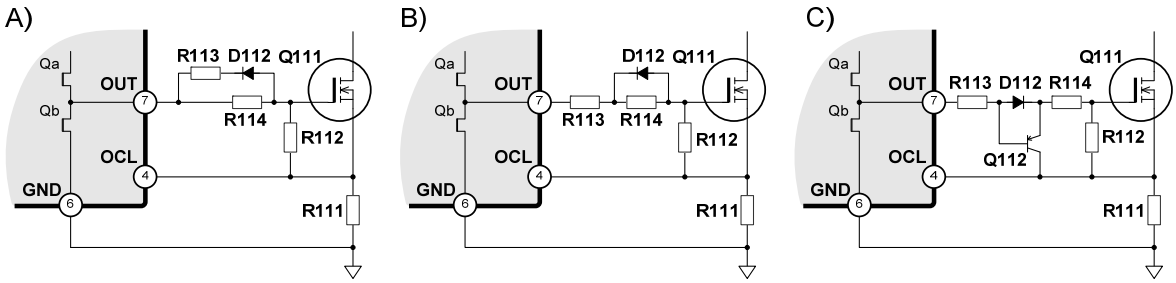


Fig. 14 Gate driver circuit

2.8 Protection functions

2.8.1 Overcurrent protection

Master / Slave

For overcurrent protection, the OCL pin monitors a voltage determined by the overcurrent detection resistor (R111), which is connected between the source and GND of the MOSFET, as shown in Fig. 15.

The main switch turns off when the OCL pin voltage rises to 0.5 V or greater. Set the overcurrent detection point above the maximum drain current during normal operations and lower than the choke saturation current.
This IC has the leading edge blank timer (TLEB). The overcurrent detection is not accepted for a certain period after the gate-on signal has been turned on to prevent unintended activation of overcurrent protection due to noise generated immediately after gate-on (see Fig. 16).

To prevent unintended operations due to switching noise, insert a capacitor (C116) as shown in Fig. 15. Place the capacitor near the OCL and GND pins. We recommend a capacitor of about 1000 pF. You can also add a R118 to further reduce unintended operations due to noise. The resistance should be 100 Ω to 1 kΩ. See ***Section 4.8*** for OCL pin design procedure.

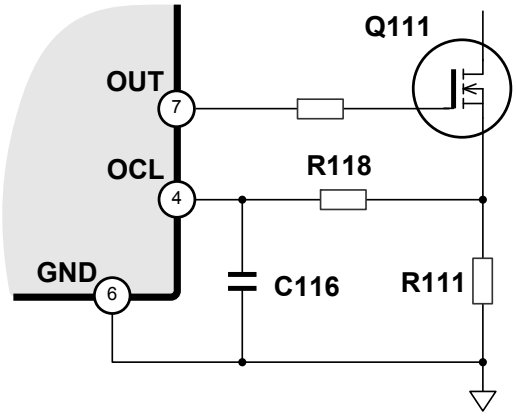


Fig. 15 OCL pin connection example

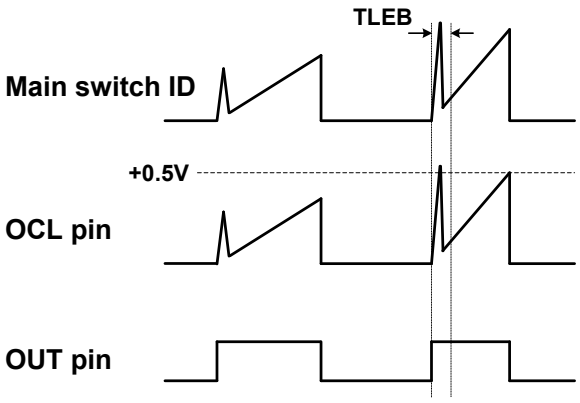


Fig. 16 Overcurrent protection operating sequence

2.8.2 Output overvoltage protection (OVP)

Master / Slave

For output overvoltage protection (OVP), when the FB pin voltage rises to 2.7 V (FB_ref x 1.08) or greater as shown in Fig. 17, the gate outputs of the master IC and slave IC are stopped to suppress increases in output voltage. This reduces the stress on electrolytic capacitors and other components.
A PFC circuit is generally designed to respond slowly to prevent response to commercial frequencies. The output voltage may rise temporarily in a transitional state, such as startup and a dramatic change in load. This function provides effective protection against such increases.

Fig. 18 shows the sequence of OVP operations. During OVP operations, the IL_OUT of the master IC is forced to output a pulse for a fixed time of 80 µs. If the IL_IN pin of the slave IC receives a pulse exceeding 50µs, no OUT signal are output. The slave IC will stop safely.

Protection function	FB pin threshold	Gate output	Other state
Output overvoltage protection (OVP)	2.7 V or greater (FB_ref x 1.08 V)	OFF	Output voltage setting x 1.08 or greater The master IC outputs a slave stop signal.

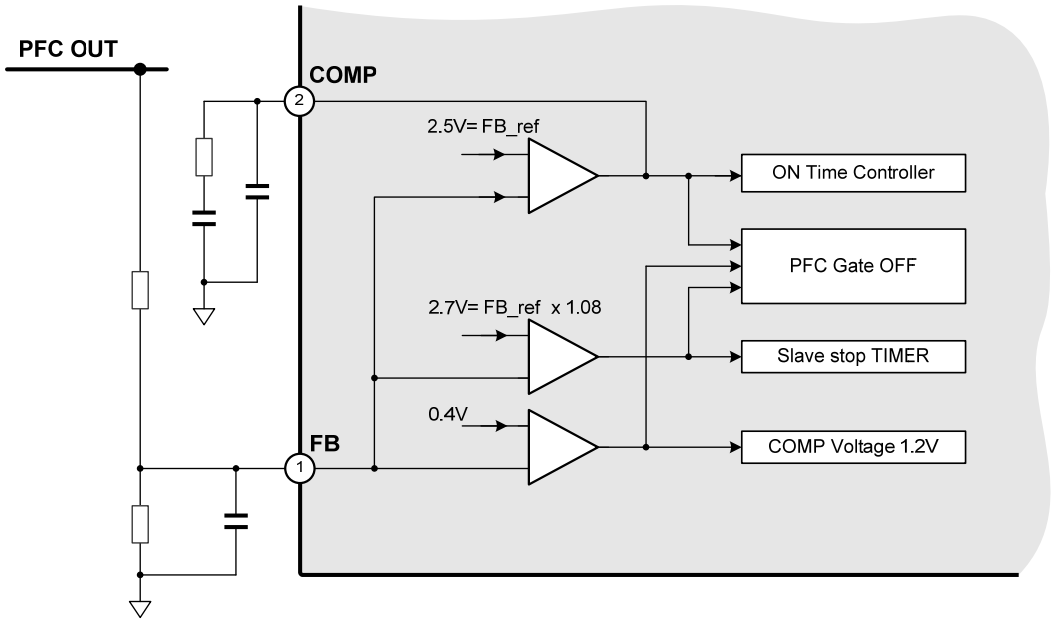


Fig. 17 FB pin internal block diagram

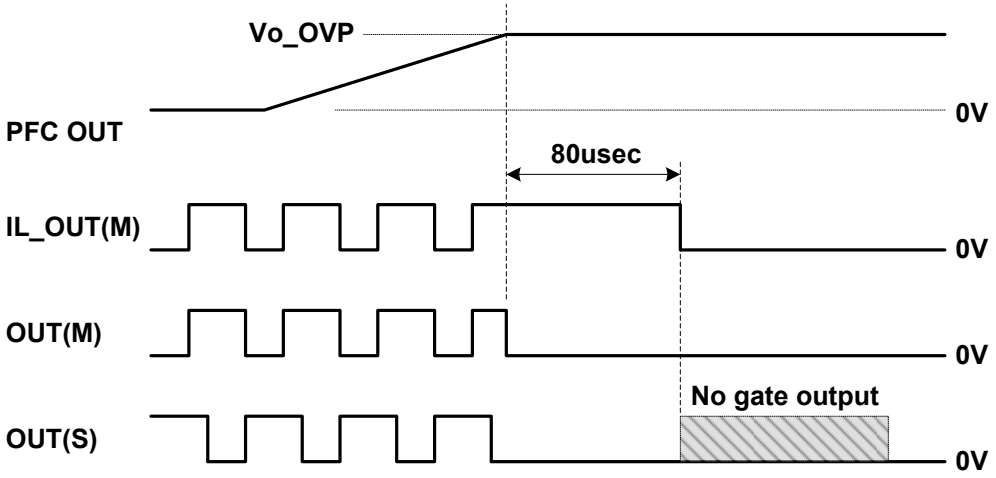


Fig. 18 OVP operating sequence

2.8.3 Low input voltage protection and FB pin open/short protection

Master

The low input voltage protection halts the gate output when the input voltage falls and the FB pin voltage falls to 0.4 V or less. This reduces stress on the MOSFET and other components.

When the FB pin is opened or when the FB pin is short-circuited with the GND, the FB pin voltage drops to 0.4 V or less. This function halts gate output.

Protection function	FB pin threshold	Gate output	Other state
Low input voltage protection FB pin open/short protection	0.4 V or less	OFF	COLM pin voltage = 1.2 V

2.8.4 Output diode short protection

Master

A short-circuited output diode results in the detection of an overcurrent, and the internal counter of the master IC begins counting. Once the counter counts to 512, the IC is latched and stopped. This function prevents the IC from continuing to operate with the diode short-circuited. For unlatching, the VCC voltage needs to be discharged and then input again.
The internal counter is reset when the Z/C pin reaches 4 V or more to disable the function at startup or in the event of an overload.

Fig. 19 shows the sequence of steps involved in the output diode short protection feature of a master IC. When the output diode of a slave IC is short-circuited, the IC is latched and stopped in a similar sequence.

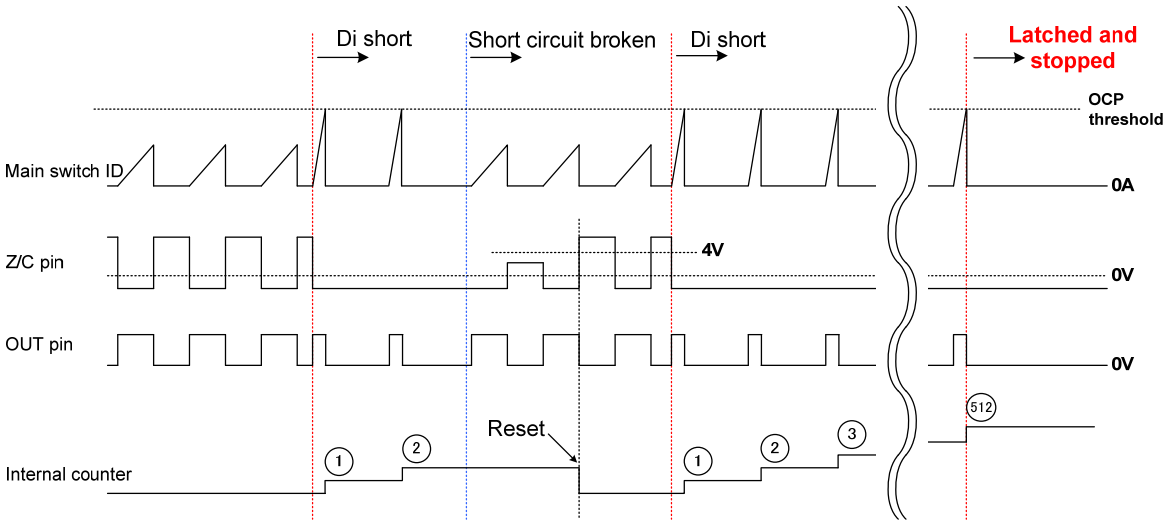


Fig. 19 Operating sequence in output diode short protection

2.8.5 VCC pin undervoltage protection (UVLO)

Master / Slave

To turn VCC on and off safely, the oscillation start/stop voltages differ between the master IC and the slave IC. When a voltage is applied to the VCC pin, the slave IC is activated first to ensure that the slave IC will be stable when the master IC is activated. When the voltage supply to VCC is stopped, the master IC stops first to ensure that all the ICs stop safely.

The table below shows the absolute maximum rating and oscillation start and stop voltages of the VCC pin.

Voltage between VCC & GND	Master IC MH2501SC	Slave IC MH2511SC
Absolute maximum rating	26 V (common to master and slave)	
Oscillation start voltage	11 V	9.5 V (starts earlier)
Oscillation stop voltage	9 V (stops earlier)	7.5 V

2.8.6 Thermal shutdown

Master

Oscillation stops if the master IC generates excessive heat for any reason and when the IC junction temperature exceeds the operation stop temperature (TSD) of 130°C. If the IC junction temperature falls to about 70°C, oscillation resumes automatically.

2.9 Application circuit

2.9.1 Slave stop protection

Master / Slave

The TIMER and LATCH pins of the slave IC and the COMP pin of the master IC can be used to keep the master IC from operating independently while the slave IC is not working due to an external problem. For example, if the interleaving signal wire is disconnected.

Fig. 20 shows an example of a 3-phase connection circuit. Fig. 21 shows the circuit operating sequence.

As shown in Fig. 20, the control coil of each choke coil is connected to the TIMER and LATCH pins of the slave IC and the COMP pin of the master IC. See Fig. 20 for the structure and polarity of each choke coil.

During normal operations, the TIMER pin voltage is kept near 0 V by charging and discharging each control coil. The LATCH pin is in a low impedance state (GND level).

If a slave IC fails to function due to a problem, the TIMER pin voltage increases. When the voltage reaches 2.5 V, the LATCH pin enters and remains in a high impedance state (open collector). This activates the transistor connected between the COMP and GND pins of the master IC and halts the oscillation of the master IC.

The LATCH pin is unlatched when VCC is reduced to 7.5 V or less. If you do not intend to use this function, short-circuit the TIMER pin and the GND.

During certain periods, only the master IC operates while the slave IC does not—for instance, when the output overvoltage protection (OVP) is on at startup. In this case, the TIMER pin is discharged by the switch in the slave IC to 0 V.
As soon as the OVP is released, the slave IC stops discharging the TIMER pin. See ***Section 2.8.2*** for more information on output overvoltage protection (OVP).

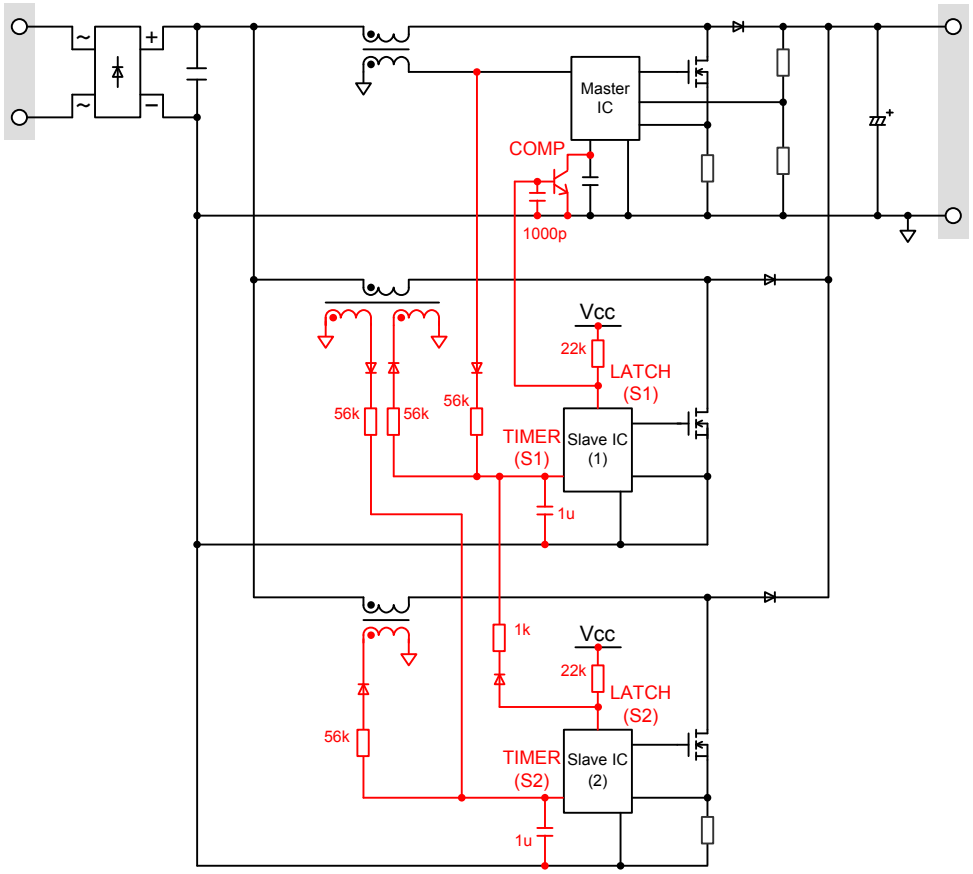


Fig. 20 Examples of circuit configurations that protect against problems with the slave

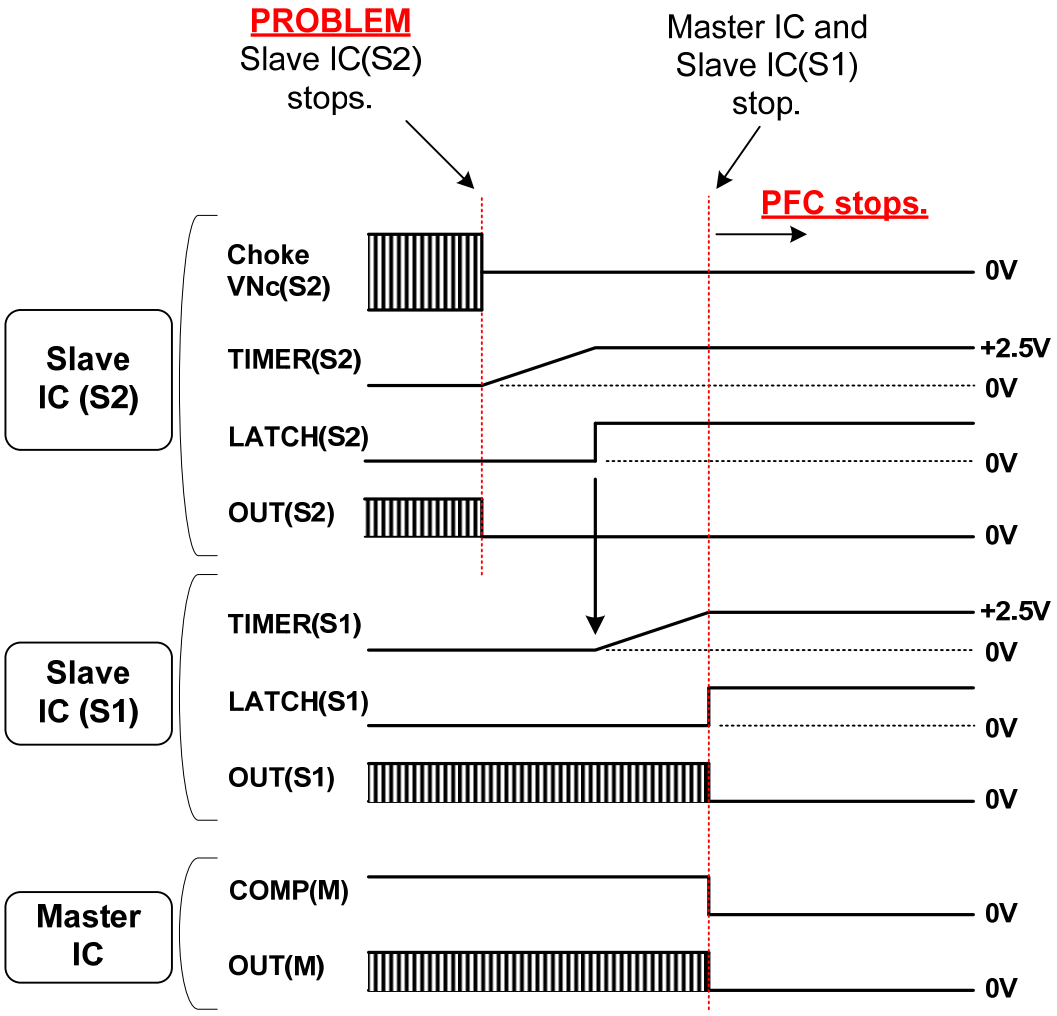


Fig. 21 Operating sequence of protection circuit intended to protect against problems with the slave (interleave signal disconnection)

2.9.2 Remote ON/OFF

Master

The master IC can be turned off by remote control by either method (1) or (2) below. To cancel the remote-off, release the state (1) or (2).

(1) Short-circuit COMP and GND.
(2) Reduce VCC to UVLO or less.

During interleaved operation, the slave IC is automatically stopped by stopping the master IC by one of the above methods.

2.9.3 Switching the number of phases

To turn off just the slave IC only, use a transistor or similar component to short-circuit the IL_IN pin of the slave IC and GND pin, as shown in Fig. 22. Blocking the interleaving signal turns off the slave ICs onwards. An external signal changes the number of phases. R127 and R137 are current limiting resistors for the IL_OUT pin.

When also using slave stop protection as described in ***Section 2.9.1***, be sure to short-circuit the GND and the TIMER pin of the slave IC you want to stop by blocking the interleaving signal before blocking the interleaving signal. For example, to stop the slave ICs from the IC (1) onwards, short-circuit C125 first, then turn on Q123 (see arrow (1) in Fig. 22). Perform a similar procedure (see arrow (2) in Fig. 22) to stop from the slave IC (2) onwards.

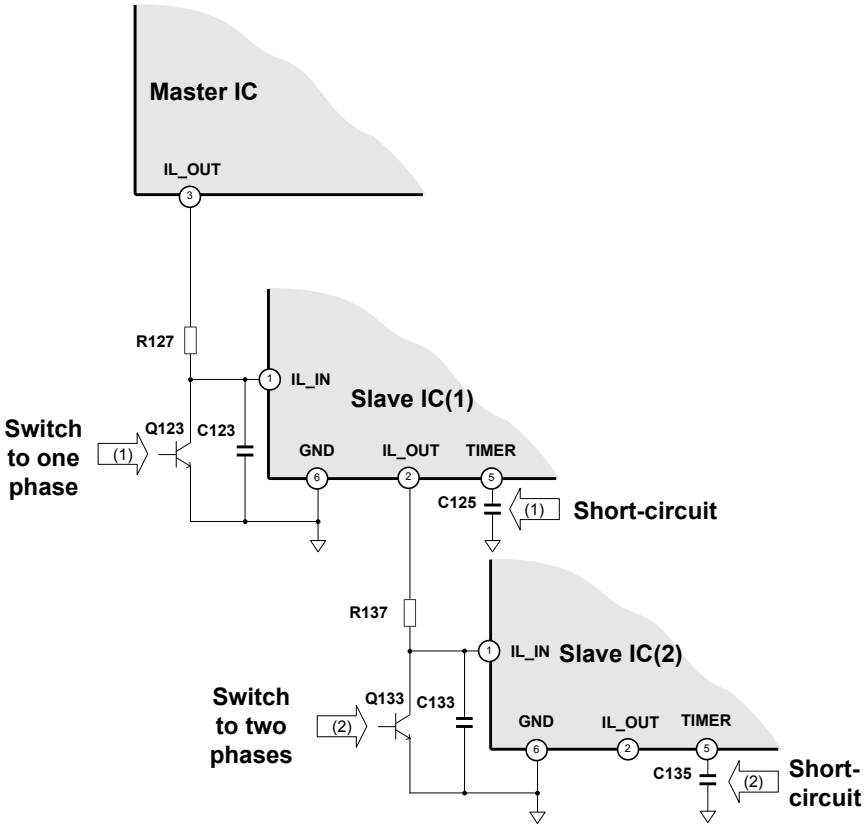
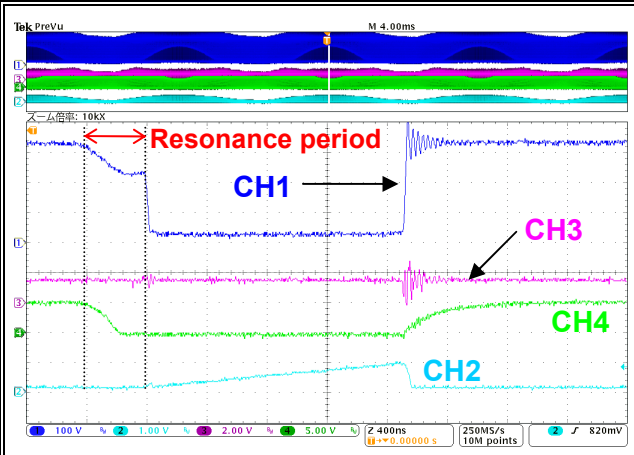


Fig. 22 Switching the number of phases

2.10 Example of operation waveforms

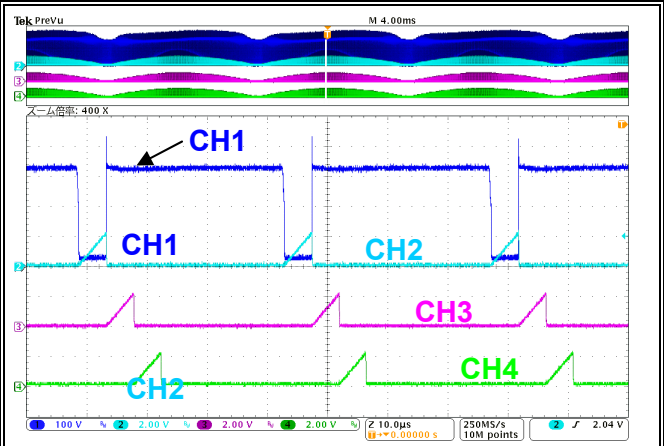
Operation waveforms of the typical circuit diagram (Input: 180 to 264 VAC, Output voltage: 390 V, Output capacity: 4 kW and 3-phase interleaved configuration) as shown in Section 3.1



Waveform 1: Critical operation by zero current

Input voltage: 200 VAC
Output power: 500 W (Vo = 320 V)

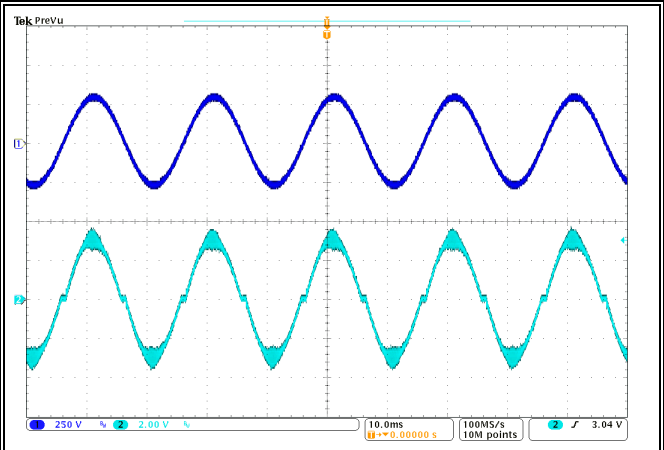
CH1	Vds(M)	100V/div
CH2	Id(M)	1A/div
CH3	V COMP	2V/div
CH4	V Z/C	5V/div
TIME		400ns/div



Waveform 2: Main switch current (3-phase interleaving)

Input voltage: 200 VAC
Output power: 4 kW (Vo = 320 V)

CH1	Vds(M)	100V/div
CH2	Id(M)	2A/div
CH3	Id(S1)	2A/div
CH4	Id(S2)	2A/div
TIME		10us/div



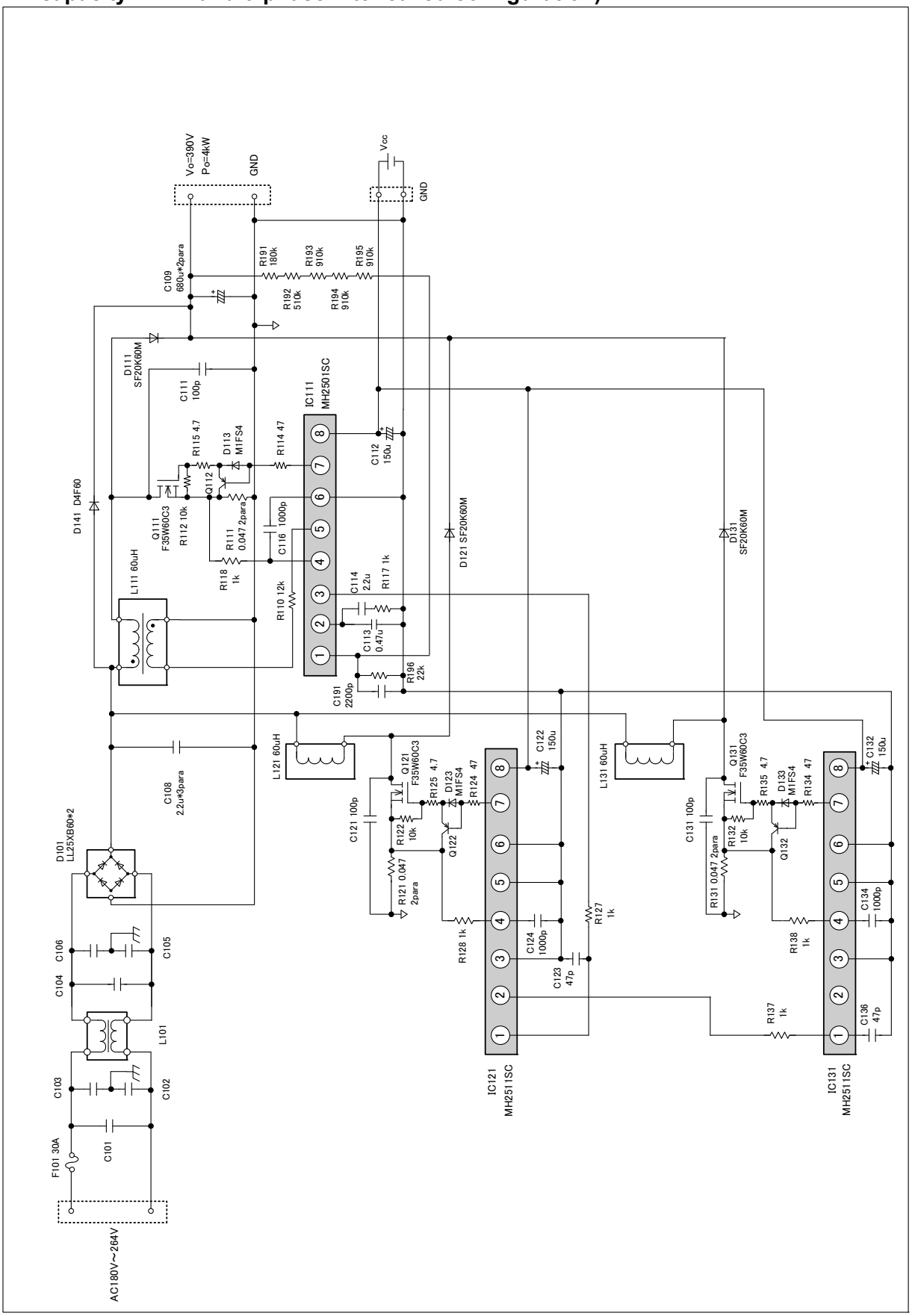
Waveform 3: Input voltage and current

Input voltage: 200 VAC
Output power: 4 kW (Vo = 320 V)

CH1	Vin(ac)	250V/div
CH2	Iin(ac)	20A/div
TIME		10ms/div

3 Circuit example

3.1 Typical circuit diagram (Input: 180 to 264 VAC, Output voltage: 390 V, Output capacity: 4 kW and 3-phase interleaved configuration)



4 Determining peripheral circuit constants

The characteristics of a PFC circuit also depend largely on peripheral components besides IC. For optimum design, clarify the specifications for the required power supply and select components as described below.

4.1 Selecting choke coils (L111, L121, L131…)

Choke coils are important components that can determine the performance of a PFC circuit. Work out the ideal constants for PFC circuit specifications using the formulas below. Inquire with coil manufacturers, if necessary.
Check for rising core and coil temperatures in an actual device before finalizing coil and core sizes.

<Selecting the core size>
Select the core size to make sure that core gap lg does not exceed 2 mm.
Use formulas (1) to (5) below to calculate the core gap lg.

$$\mathrm{lg} = 4\pi \times \frac{Ae \times Np^2}{\mathrm{Lp}} \times 10^{-7} \quad [\mathrm{mm}] \quad \cdots (1)$$

$$Lp = Ton \times \frac{Vin(AC)\min \times \sqrt{2}}{\mathrm{Idp}} \times 10^{3} \quad [\mathrm{mH}] \quad \cdots (2)$$

$$Idp = \frac{Ps \times 2 \times \sqrt{2}}{\eta \times \mathrm{Vin(AC)min}} \quad [\mathrm{A}] \quad \cdots (3)$$

$$Ton = Don \times T\max = \frac{Don}{f\min} \quad [s] \quad \cdots (4)$$

$$Don = \frac{Vo - Vin(AC)\min \times \sqrt{2}}{Vo} \quad \cdots (5)$$

Ae represents the effective cross sectional area [mm^2] of the core, Ps the output power [W] (1.2 to 1.5 times as high as Po(max)) at the droop point, and fmin the minimum oscillation frequency [Hz] (auto-sensing power supply: 40 k to 60 kHz, 100 V/ 200 V group: 50 k to 70 kHz). The figures in parentheses are provided as guidelines only.

<Number of turns of Np coil>
The result given by formula (6), rounded down to the nearest integer, gives the number of turns of the Np choke coil.

$$Np = Ton \times \frac{Vin(AC)\min \times \sqrt{2}}{\Delta \mathrm{B} \times \mathrm{Ae}} \times 10^{9} \quad [Turn] \quad \cdots (6)$$

ΔB represents the magnetic flux density variation [mT] of the core. ΔB can vary significantly from core to core. Inquire with the coil manufacturer.

<Number of turns of Nc coil>
Apply formula (7) to select the minimum integer for the number of turns of the Nc coil. A minimum voltage of 1.5 V should be generated in the control coil at maximum input voltage.

$$Nc > 1.5 \times \frac{Np}{Vo - \{\sqrt{2} \times Vin(AC)\max\}} \quad [Turn] \quad \cdots (7)$$

In the case of an auto-sensing power supply, assuming that Vin(AC)max is 264 V and that PFC output voltage Vo is 390 V, a ratio of the numbers of turns of Np and Nc is approximately 10 to 1.

Example) The number of turns of Np with an auto-sensing power supply is 50.
Assuming that Vin(AC)max = 264 V and Vo = 390 V, Nc > 4.5 and Nc = 5 turns.

<Selecting the coil>

Select the cross-sectional area of the Np coil based on the effective current IL(rms) [A] and the current density of the choke coil [A/mm^2]. Note that current density will vary with the type of copper wire (single wire or litz wire), number of strands, and other factors. Fig. 23 shows IL(rms) at an input of 85 VAC. Refer to the chart when inquiring with the coil manufacturer.

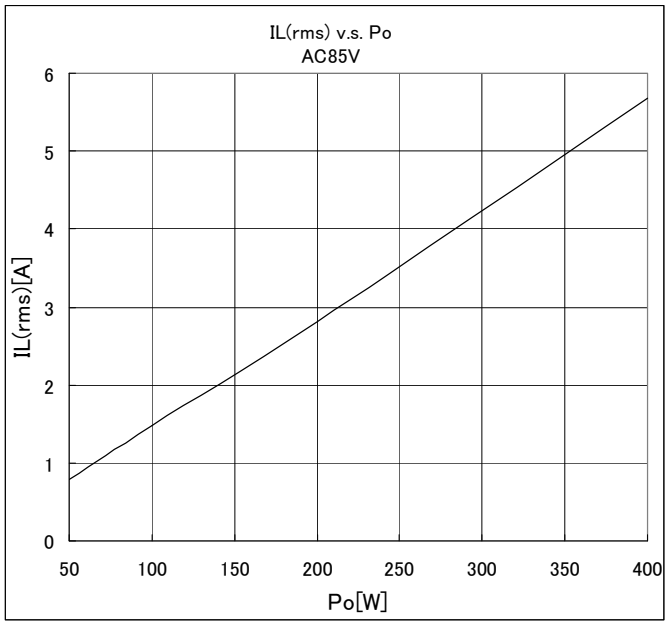


Fig. 23 IL(rms) at an input of 85 VAC

4.2 Selecting the MOSFET (Q111, Q121, Q131…)

Select a MOSFET with a current rating higher than the maximum drain current Idp multiplied by the margin.
Check the junction temperature on the actual device before final selection of a MOSFET and heat sink.

Use the following as a guide to margins for the product current rating and product withstand voltage.

$$\text{Product withstand voltage} > Vo \times 1.25 \quad [\text{V}] \quad \text{... (8)}$$

$$\text{Product current rating} > Idp \times 1.25 \quad [A] \quad \text{... (9)}$$

Vo is the set output voltage.

4.3 Selecting an output diode (D111, D121, D131…)

Select a diode with a current rating 6 to 8 times the maximum load current Io_max., using the value as a guideline. For an interleaved circuit, divide Io_max by the number of phases to obtain current per phase. Check the junction temperature on the actual device before final selection of a diode and heat sink.

4.4 Selecting a bypass diode (D141)

Select a bypass diode (D141) with a peak surge forward current IFSM greater than the maximum inrush current. The maximum inrush current varies with pattern impedance and input voltage. Simulate to check the current, or measure with the actual device.

Example of recommended component: D4F60 (Shindengen)

4.5 Adjusting constants for components around Z/C pin

You can adjust the turn-on timing by adding a capacitor C115 between the resistor R110, the Z/C pin, and GND (Fig. 24). Adjust the timing so that the switch activates when the drain-source voltage (Vds) reaches the lower limit in the resonance period (see Waveform 1 in ***Section 2.10***). This will help reduce switching losses.
The C115 should be around 15 pF. Adjust the R110 while referring to formulas (10) and (11) below and monitoring Vds at the maximum input voltage on the actual device.
The maximum current flowing into and out of the Z/C pin, which determines the turn-on timing, is ± 5 mA. The resistor R110 needs to be adjusted to ensure that the current flowing to the Z/C pin does not exceed 80% of the maximum current.

Specifically, select a resistance greater than RZC, the resistance given by formulas (10) and (11).

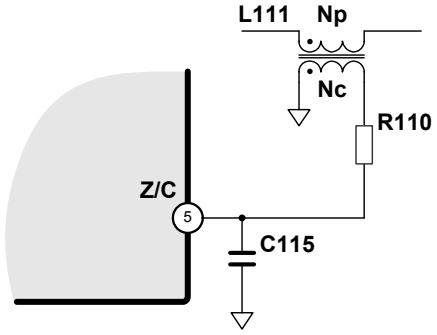


Fig. 24 Circuit around Z/C pin

◆ Positive side of control coil

$$R_{ZC}+ = \frac{Vo \times \left(\frac{Nc}{Np}\right) - 6.5}{4 \times 10^{-3}} \quad [\Omega] \quad \cdots(10)$$

* 6.5 V is the zener voltage in the Z/C pin.

◆ Negative side of control coil

$$R_{ZC}- = \frac{\left(-Vin(AC)\max \times \sqrt{2}\right) \times \left(\frac{Nc}{Np}\right)}{-4 \times 10^{-3}} \quad [\Omega] \cdots(11)$$

For instance, assume Vo = 400 V, Vin(AC)max = 276 V, Np = 50 turns, and Nc = 5 turns.

◆ Positive side of control coil : $R_{ZC}+ = \frac{400 \times \left(\frac{5}{50}\right) - 6.5}{4 \times 10^{-3}} = 8.4[k\Omega]$

◆ Negative side of control coil : $R_{ZC}- = \frac{\left(-276 \times \sqrt{2}\right) \times \left(\frac{5}{50}\right)}{-4 \times 10^{-3}} = 9.8[k\Omega]$

Set the Z/C control resistor R110 to 9.8 kΩ or more.

4.6 Adjusting phase compensation (R117, C113, and C114)

A transconductance amplifier (gm amplifier) is used as the error amplifier for the master IC. To adjust the phase compensation circuit, connect the capacitors and the resistor while referring to Fig. 25.

Formula (12) gives the capacitance of C114. The cutoff frequency fc should be about 20 Hz. The capacitance of C113 should be about a tenth that of C114.

$$C114 \fallingdotseq \frac{140}{2\pi \times fc} \quad [\mu F] \quad \text{... (12)}$$

* Amplifier transconductance:140 [μA / V]

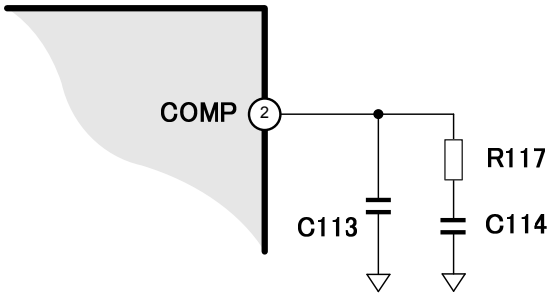


Fig. 25 Circuit around COMP pin

Increasing the resistance of R117 lets you adjust the gain in a high frequency region above the cutoff frequency fc. If the resistance is too high, the waveform may be distorted. Set to between 1 kΩ and 10 kΩ.

* Recommended constants: R117=1kΩ, C113=0.22μF, C114=2.2μF

Adjustments of the phase compensation circuit should vary with the constants of other components. Use the calculation method given above as a rough guide. Check the operating waveform, power factor, and other factors on the actual device for final adjustments.

4.7 Adjusting the output voltage (R191 to R196)

Use external voltage dividing resistors to set the desired output voltage. Connect resistors R191 to R196 to set the output voltage. (See Fig. 26.)
The error amplifier input threshold is 2.5 V. Apply formula (13) to determine voltage dividing resistances. To reduce losses, we recommend targeting a total resistance for the upper voltage dividing resistors (R191 to R195) of about 2 MΩ when the PFC output voltage is about 400 V.
To prevent unintended noise-induced operations, insert a capacitor C191 between the FB and GND pins. Since this capacitor can affect feedback response, we recommend a capacitance of about 1000 pF to 2200 pF.

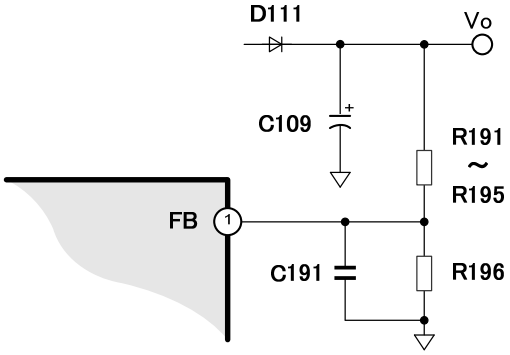


Fig. 26 Circuit around FB pin

$$(R191 + R192 + R193 + R194 + R195) = \frac{R196 \times (Vo - 2.5)}{2.5} \quad [\Omega] \quad \text{... (13)}$$

Note that the precision of each resistance will directly affect the precision of the output voltage. We recommend using high-precision resistors.

4.8 Adjusting the overcurrent protection point (R111, R121, R131…)

Use overcurrent detection resistor R111 (and R121 and R131) to adjust the overcurrent protection point Ps. Apply formula (14) to determine the resistance of R111 (and R121 and R131).

Ps should be about 1.2 to 1.5 times the maximum load power Pomax. When increasing the overcurrent protection point, carefully consider the magnetic saturation of the choke coil.

$$R111(R121, R131) = V_{OCL} \times \frac{\eta \times Vin(AC)\min}{2 \times \sqrt{2} \times Ps} \times n \quad [\Omega] \text{ ... (14)}$$

VOCL is the overcurrent protection voltage of 0.5 V. n is the number of interleaved phases.

4.9 Selecting the output capacitor (C109)

The overvoltage detection voltage (***Section 2.8.2***) is set to 1.08 times the output voltage. Determine the withstand voltage of output capacitor C109, accounting for the overvoltage detection voltage plus a margin.

$$Vo(OVP) = Vo \times 1.08 \quad [V] \qquad \text{... (15)}$$

Adjust the capacitance of the C109 according to the output capacity and hold time.

5 Precautions for protective functions

The protective functions built into the master IC and slave IC will not work if the IC fails to function properly due to an anomaly. In case of IC malfunctions, to prevent smoke and fire, the IC must be protected with an external protection element or circuit. Some precautions related to protective functions are given below.

<Thermal shutdown>
The master IC incorporates a thermal shutdown function. Due to transient thermal resistance, the function may not be able to track temperatures adequately in cases of extreme temperature change resulting from a certain anomaly.

The function detects the temperature of the IC only. This means the protection will not work even if the temperatures of external power devices (e.g., MOSFETs and diodes) rise. For extra safety, establish separate temperature detection and protection features for power devices.

The slave IC lacks a thermal shutdown function. If only the slave IC will generate heat in the event of an anomaly, insert an overcurrent protection element in the VCC supply line.

<Overvoltage protection>
The master IC incorporates an overvoltage protection function. In cases of extreme voltage increases resulting from certain anomalies, the function may not work. For an additional margin of safety, use an external protection circuit to detect the output voltage on a different line from the FB line and to stop the master IC. See ***Section 2.9.2*** Remote ON/OFF for procedures for turning off the master IC.

Fig. 27 shows an example of an external overvoltage protection circuit.

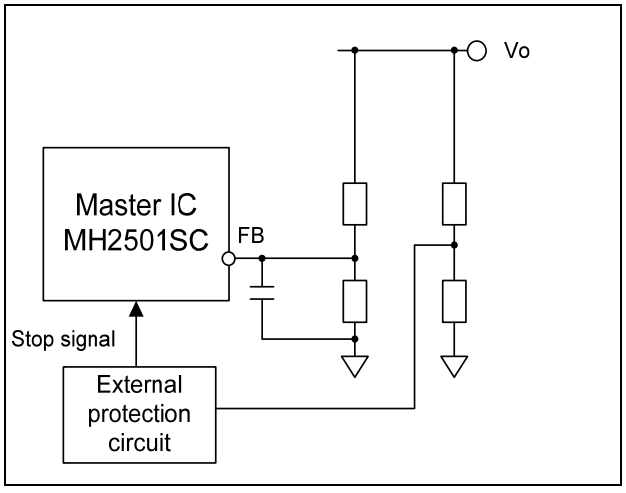


Fig. 27 External overvoltage protection circuit

<Diode short protection>
The master IC incorporates a diode short protection function. If the output diode short-circuits due to a certain anomaly, this function shuts down the master IC to protect the IC and the MOSFET from secondary damage. With certain OCL settings or allowable loss of external MOSFET, the IC or the MOSFET may be damaged before the protection activates. To reduce this risk, review the OCL setting or your MOSFET selection or take alternative measures (e.g., using a fuse or other element to ensure the IC stops safely even if damaged).

<Slave stop protection>
Note that various factors may keep the slave stop protection from functioning properly, including chattering noise in the IL_IN pin caused by a short circuit between the IL_IN pin and another pin, or other anomalies.
Increase the filter constant to protect the IL_IN pin against noise in case of an anomaly. For extra safety, add temperature detection or other functions to the power devices.

6 Precautions for pattern layouts

PCB pattern design can significantly affect power supply characteristics. Since the MH2501SC and the MH2511SC switch high voltage and current, great care is required when laying out patterns. To minimize noise attributable to the inductance component of the patterns, make the patterns of the main circuit as thick and as short as possible. Design the patterns for controls to minimize electromagnetic interference. The precautions for the main items are summarized below. Always check to confirm that the IC functions properly after designing the patterns.

6.1 Wiring for main current routes

There are two high current switching lines: one from the positive side of the input capacitor via the main choke and the main switch back to the Input capacitor GND (violet -> red -> violet in Fig. 28); the other from the MOSFET drain via the diode and the output capacitor back to the Input capacitor GND (blue -> violet in Fig. 28). Make these two patterns as thick and as short as possible.

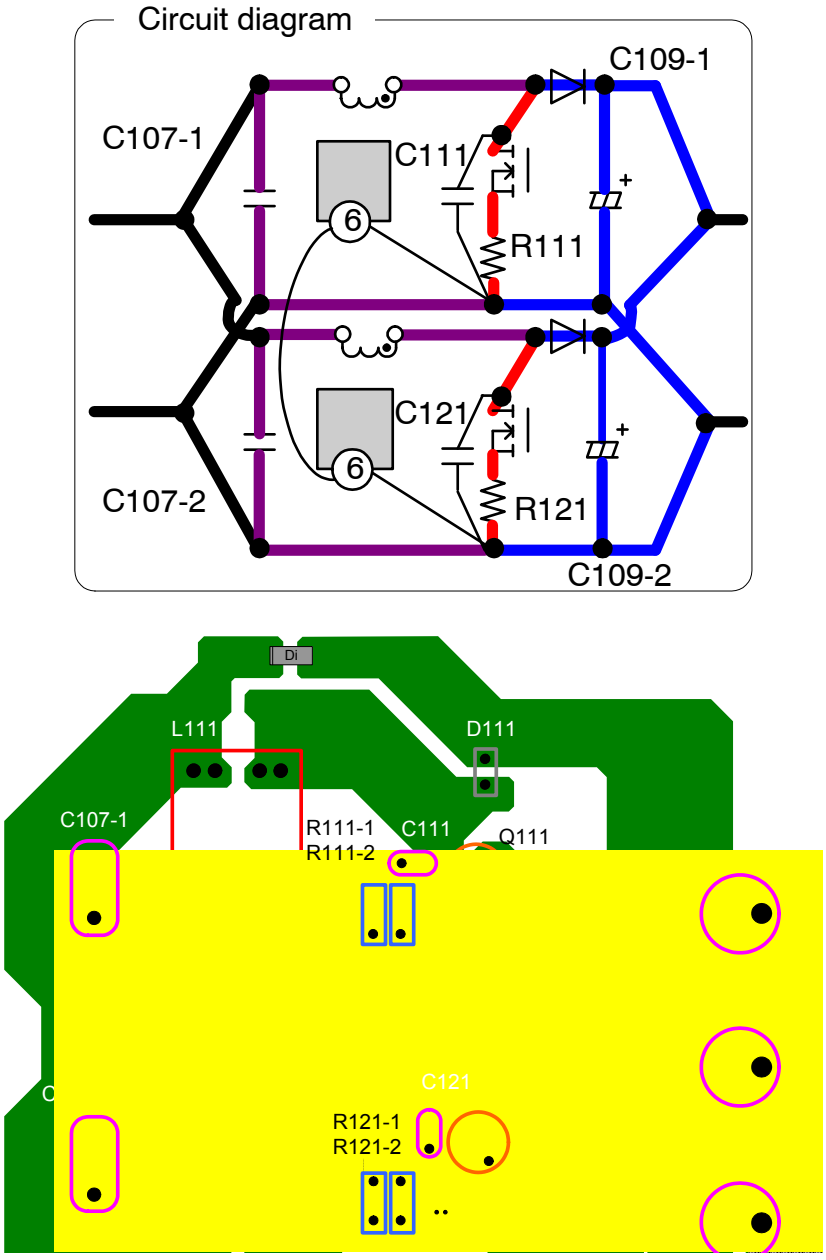


Fig. 28 Ideal wiring for main current routes

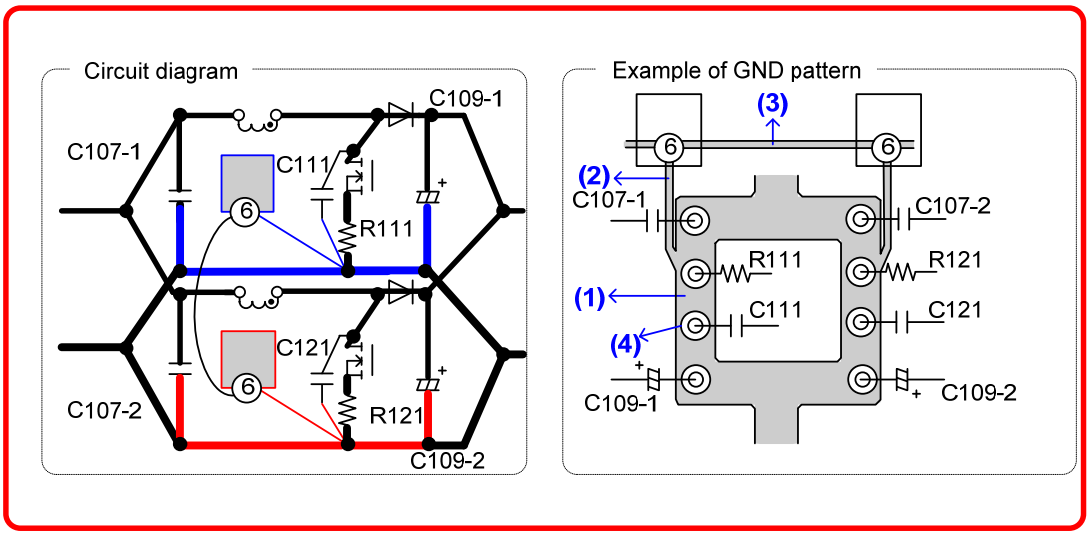
6.2 GND wiring

Ground wiring can significantly affect the stability of power supply operations. When a high current is switched, if the GND is affected, so is the IC control. Separate the GND line from the high current switching lines as described in ***Section 6.1***.

Specifically, note the following aspects:

(1) Do not use a common GND line. Connect each IC current detection resistor to the input capacitor with separate GND lines.
(2) Connect the GND of each IC to the GND of each current detection resistor at a single point.
(3) Do not route the GND between ICs should via the high current switching GND lines (the red and blue lines in the diagram below). Make the line as short as possible.
(4) Connect the GND of the resonating capacitor to the GND of the current detection resistor by the shortest possible distance.
* See (1) to (4) in Fig. 29.

Comply with the above precautions for GND wiring.
The next page shows examples of GND wiring that comply with these precautions. Use them as a guide in pattern layouts.



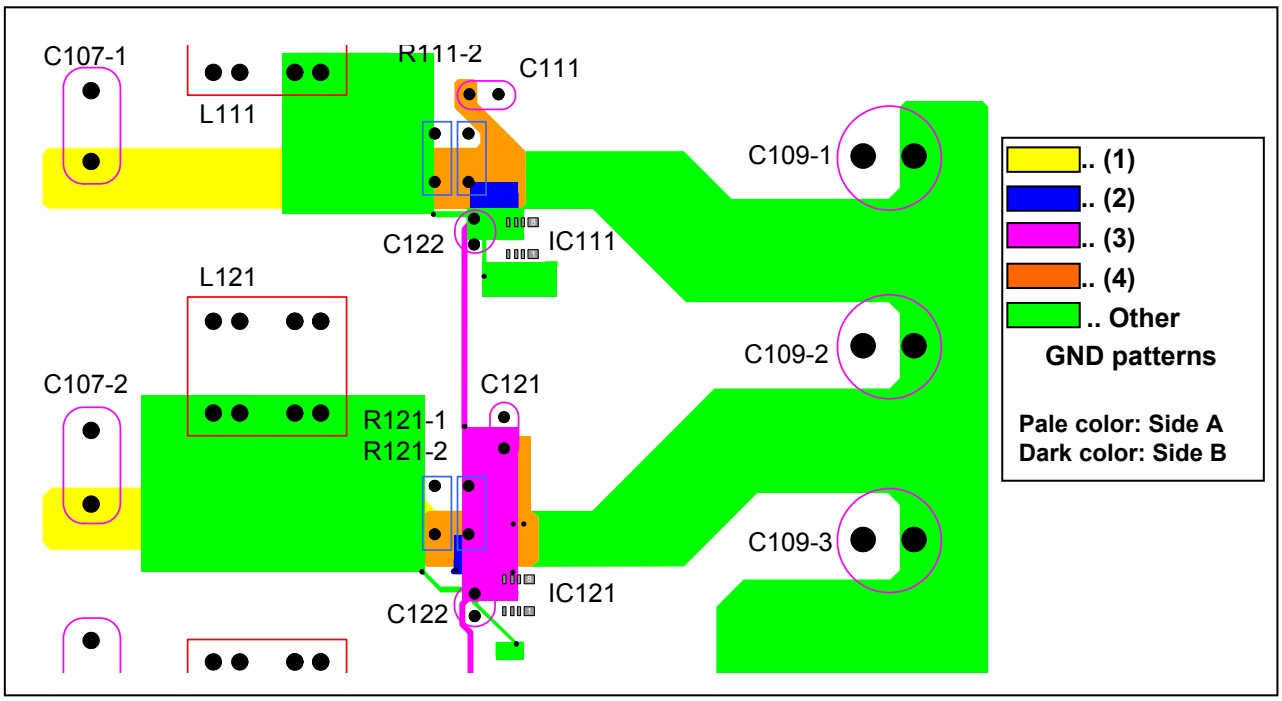


Fig. 29 Design example of GND patterns

6.3 Wiring of components around MOSFET

Parasitic oscillation may result if the wiring of the MOSFET gate loop is too long or too close to a noise source. Keep the following in mind when wiring the gate loop:

- Make the wiring from the OUT pin of the master or slave IC to the MOSFET gate as short as possible.
- Position the wiring between the OUT pin and the gate at an adequate distance from magnetic components, such as choke coils.
- Place the MOSFET as close as possible to the resonating capacitor. Connect the GND of the resonating capacitor to the GND of the current detection resistor.
- Use a resistor with a low inductance component as a detection resistor.

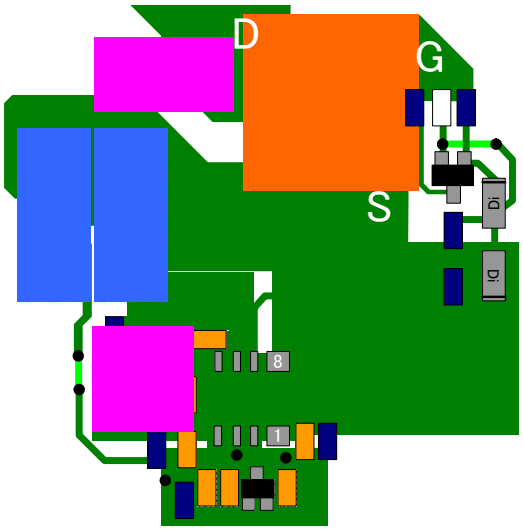


Fig. 30 Design example of patterns around the MOSFET

6.4 Wiring of IC peripheral components

Place the IC peripheral components as close as possible to the IC pins. The components used to stabilize control include a backup capacitor connected to the Vcc pin, a phase compensation component connected to the COMP pin, and an output voltage detection component connected to the FB pin. Connect each component to the GND pin of the IC at a single point, if possible. (See the wiring in pink.)

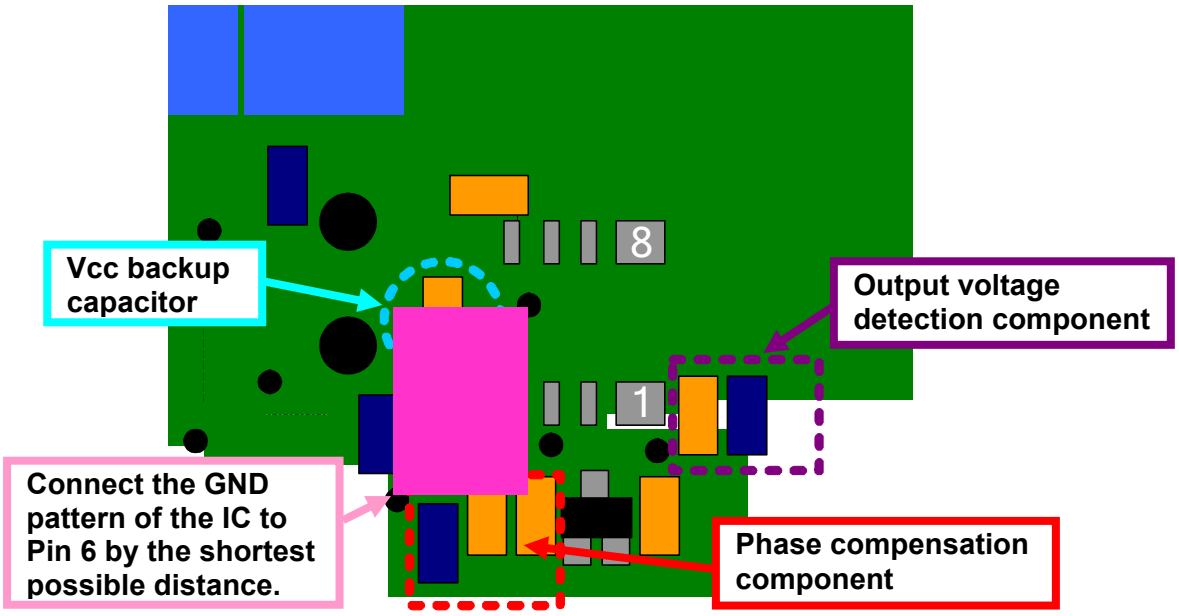
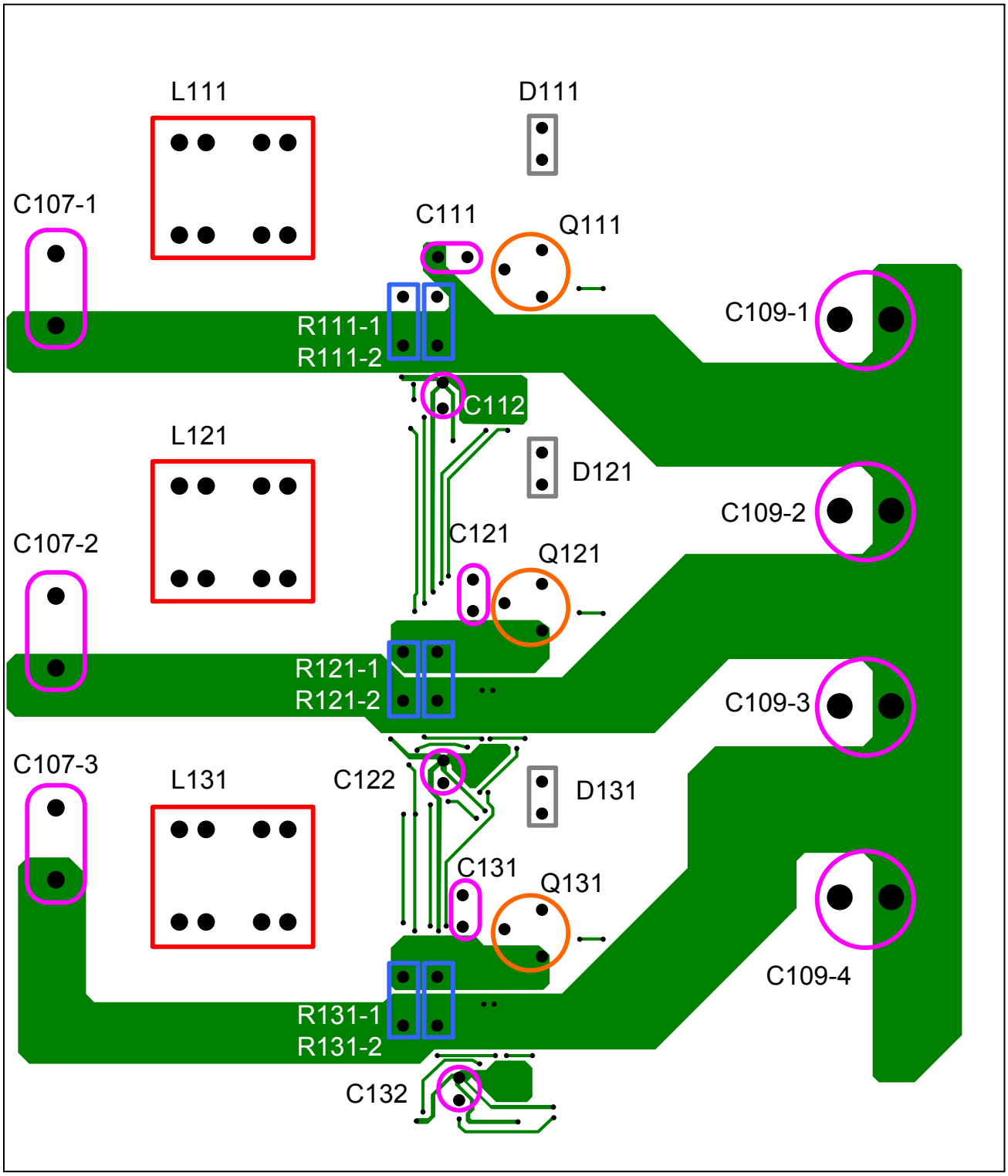


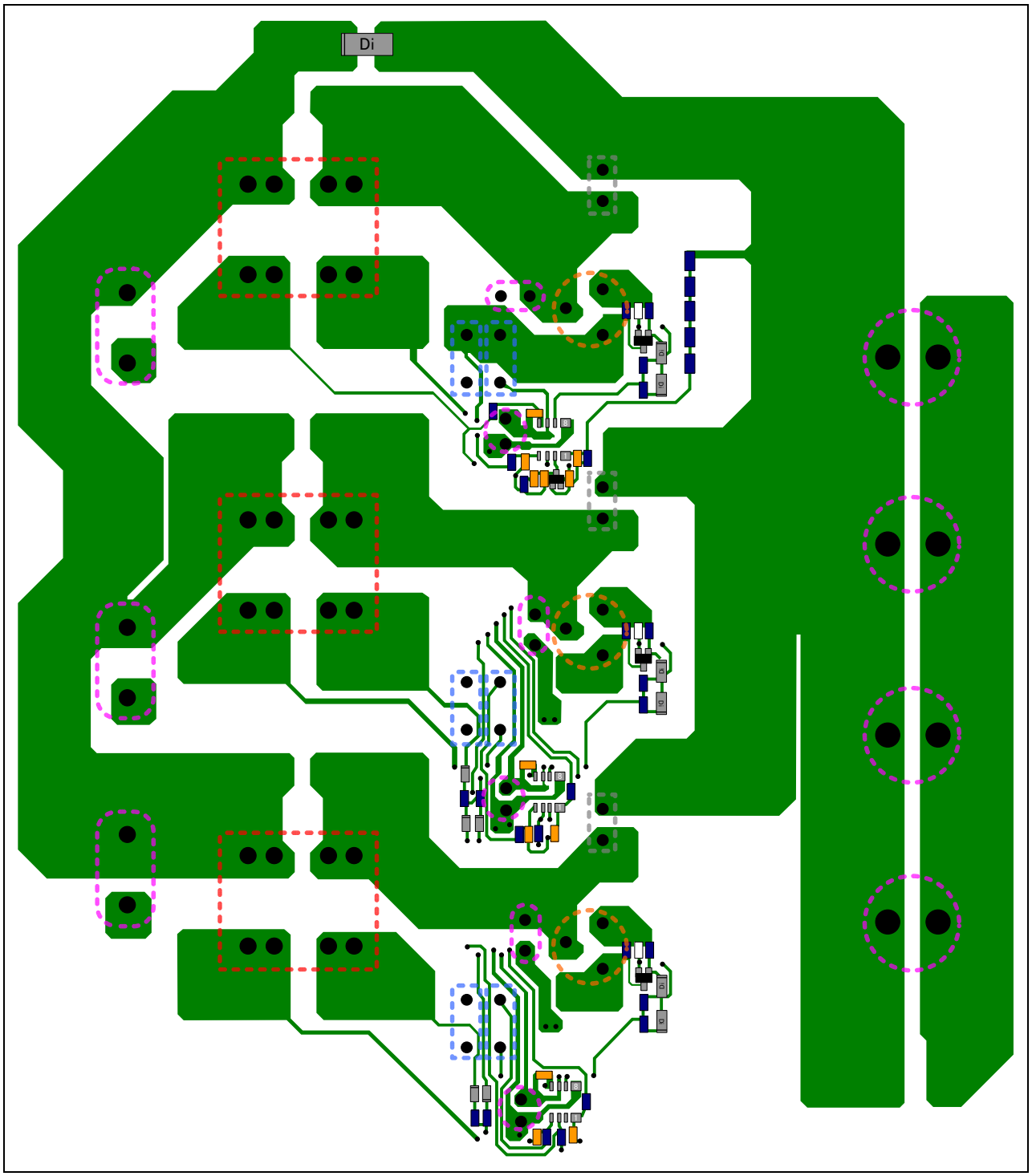
Fig. 31 Design example of IC peripheral patterns

6.5 Pattern layout example

6.5.1 Side A



6.5.2 Side B



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