

N-Channel Power MOSFET

40V, 135A, 3.8mΩ

FEATURES

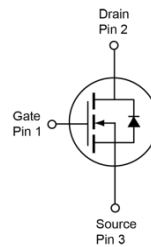
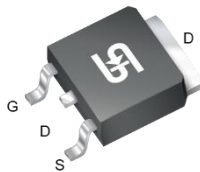
- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	3.8
	$V_{GS} = 4.5V$	5
Q_g	53	nC

APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC converter
- Secondary Synchronous Rectification


TO-252 (DPAK)


Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	135
		$T_A = 25^\circ\text{C}$	19
Pulsed Drain Current	I_{DM}	540	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	38	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	217	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	125
		$T_C = 125^\circ\text{C}$	25
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	2.6
		$T_A = 125^\circ\text{C}$	0.5
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	49	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.2	1.5	2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 40V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 40V$ $T_J = 125^{\circ}C$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10V, I_D = 19A$	$R_{DS(on)}$	--	2.8	3.8	m Ω
	$V_{GS} = 4.5V, I_D = 17A$		--	3.4	5	
Forward Transconductance (Note 3)	$V_{DS} = 5V, I_D = 19A$	g_{fs}	--	55	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = 10V, V_{DS} = 20V, I_D = 19A$	Q_g	--	104	--	nC
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 20V, I_D = 17A$	Q_g	--	53	--	
Gate-Source Charge		Q_{gs}	--	14	--	
Gate-Drain Charge		Q_{gd}	--	23	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 20V$ $f = 1.0MHz$	C_{iss}	--	5509	--	pF
Output Capacitance		C_{oss}	--	548	--	
Reverse Transfer Capacitance		C_{rss}	--	332	--	
Gate Resistance	$f = 1.0MHz$	R_g	0.4	1.3	2.6	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 20V, I_D = 19A, R_G = 2\Omega,$	$t_{d(on)}$	--	8	--	ns
Turn-On Rise Time		t_r	--	21	--	
Turn-Off Delay Time		$t_{d(off)}$	--	57	--	
Turn-Off Fall Time		t_f	--	35	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = 19A$	V_{SD}	--	--	1	V
Reverse Recovery Time	$I_S = 19A,$ $di/dt = 100A/\mu s$	t_{rr}	--	37	--	ns
Reverse Recovery Charge		Q_{rr}	--	27	--	nC

Notes:

1. Silicon limited current only.
2. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $V_{DD} = 25V$, $R_G = 25\Omega$, $I_{AS} = 38A$, Starting $T_J = 25^\circ\text{C}$
3. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Switching time is essentially independent of operating temperature.

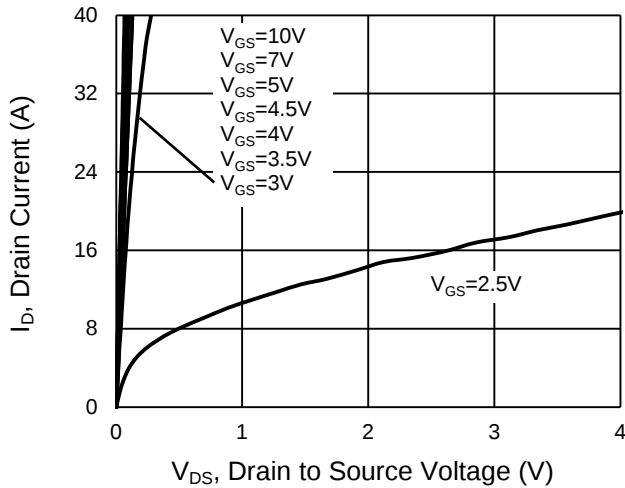
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM038N04LCP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

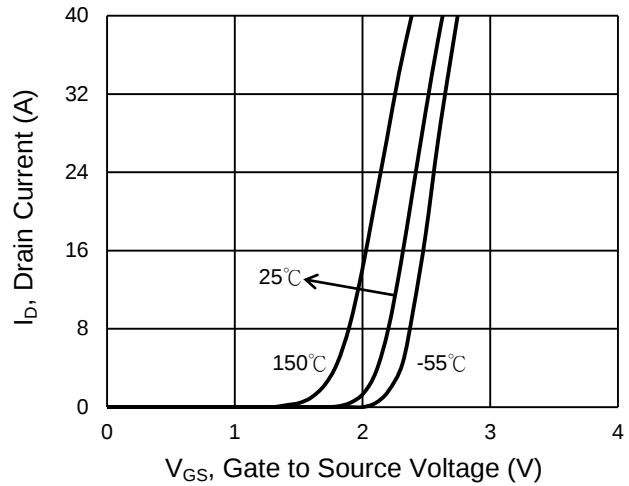
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

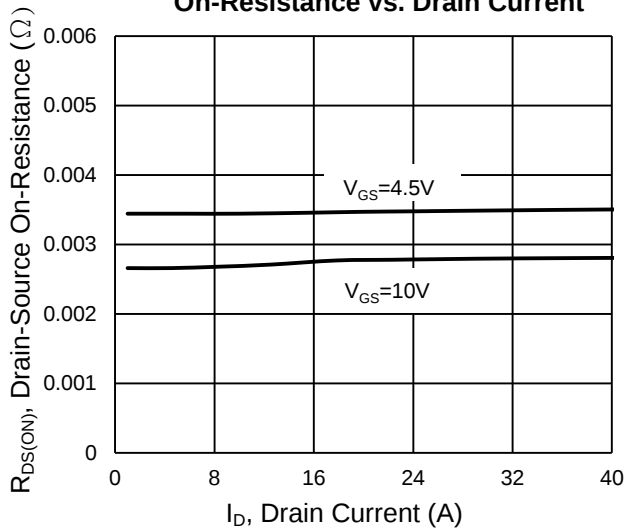
Output Characteristics



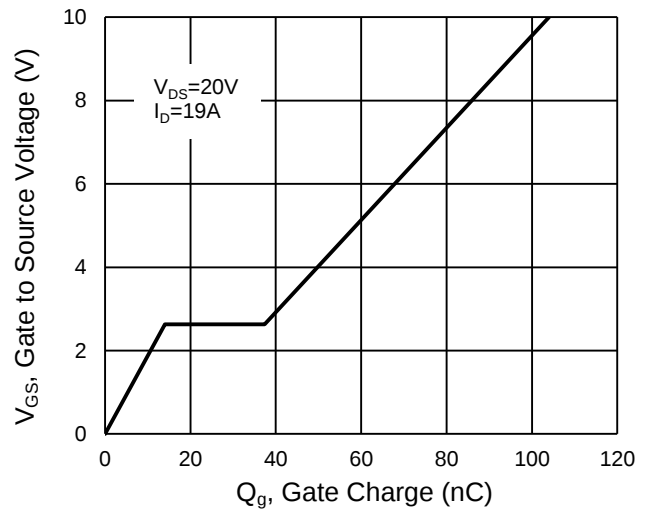
Transfer Characteristics



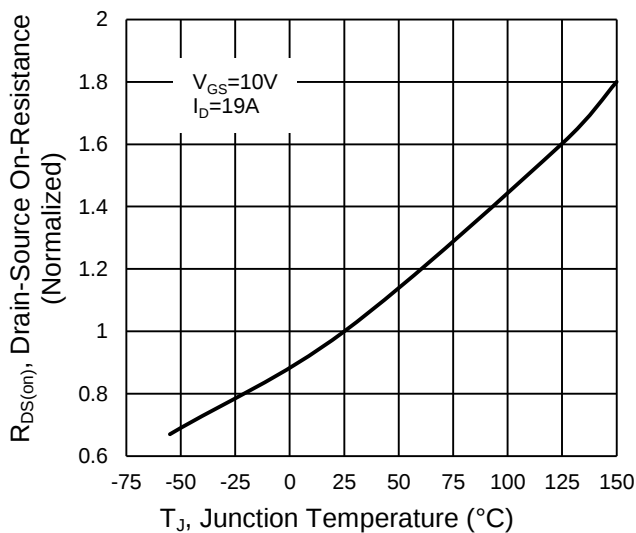
On-Resistance vs. Drain Current



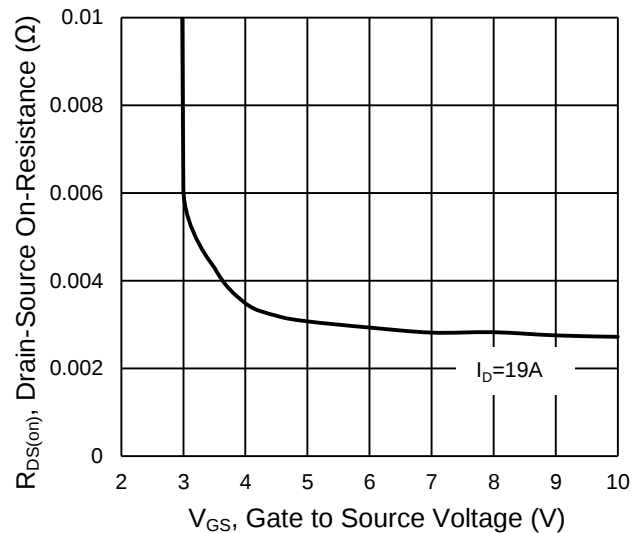
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



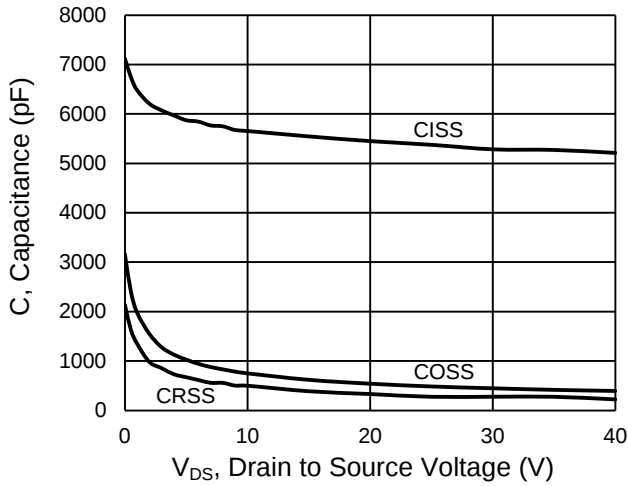
On-Resistance vs. Gate-Source Voltage



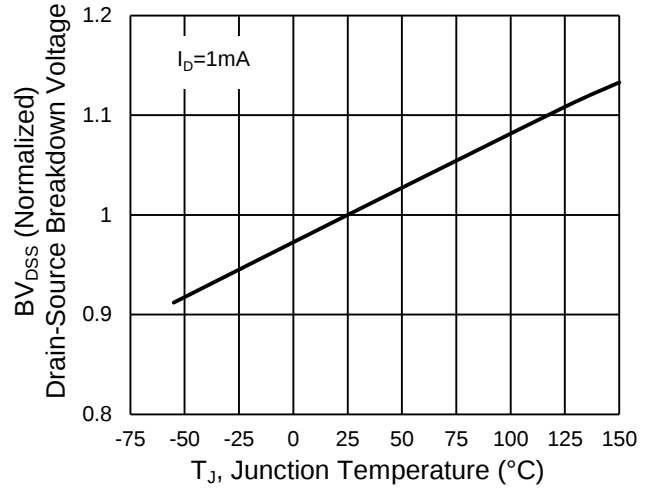
CHARACTERISTICS CURVES

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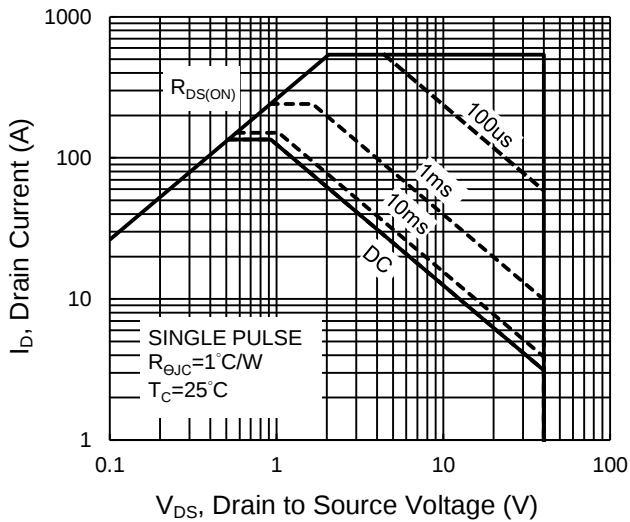
Capacitance vs. Drain-Source Voltage



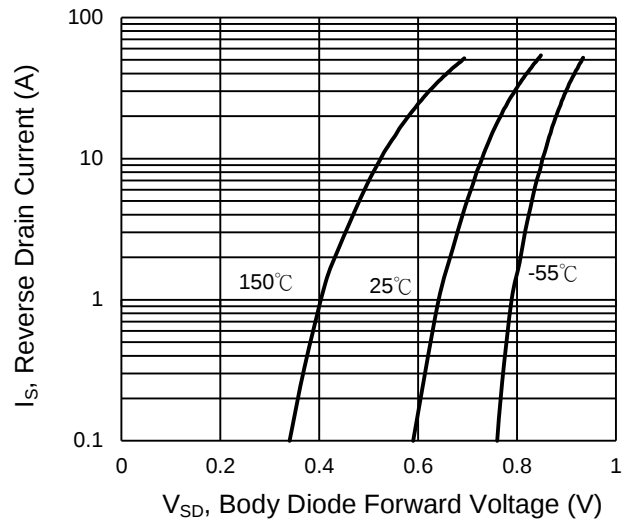
BV_{DSS} vs. Junction Temperature



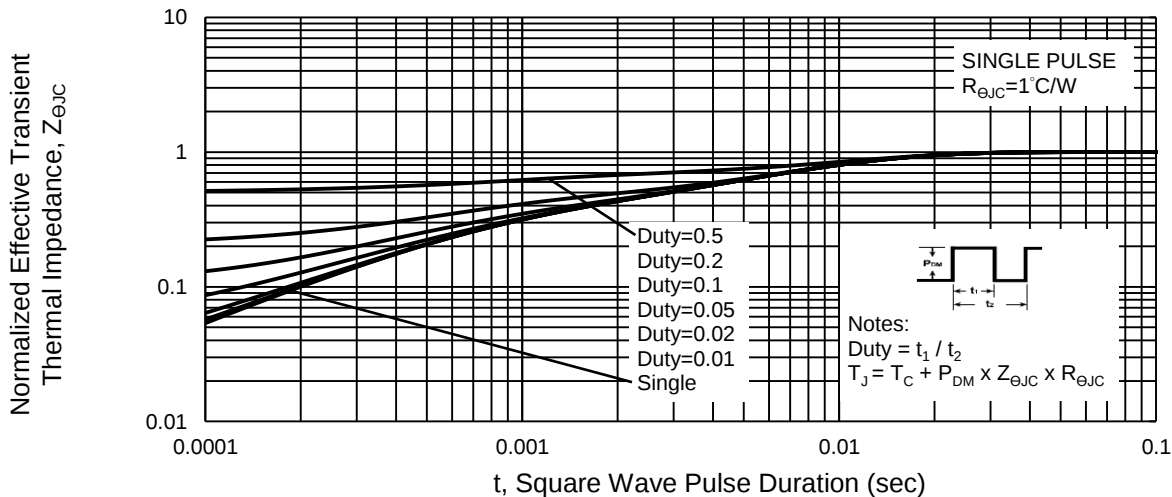
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

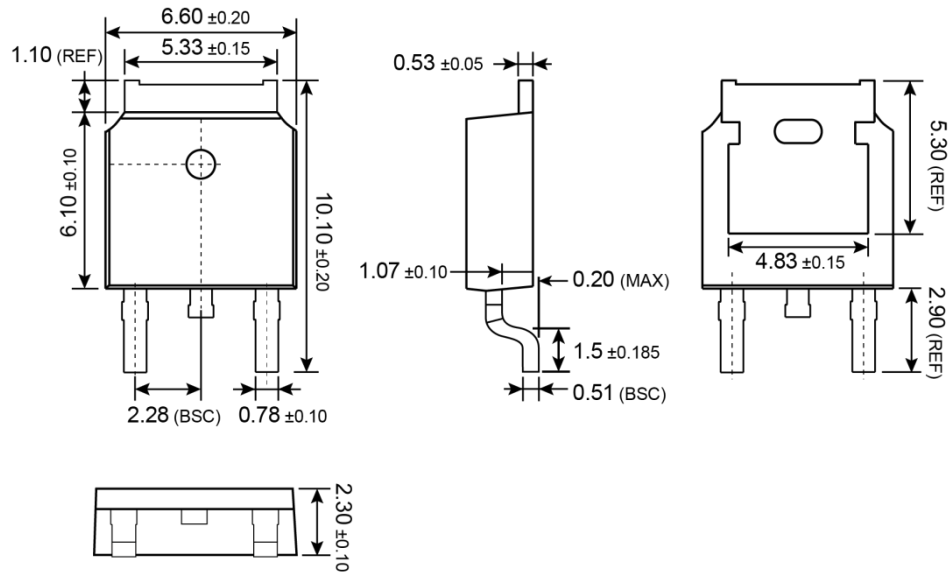


Normalized Thermal Transient Impedance, Junction-to-Case

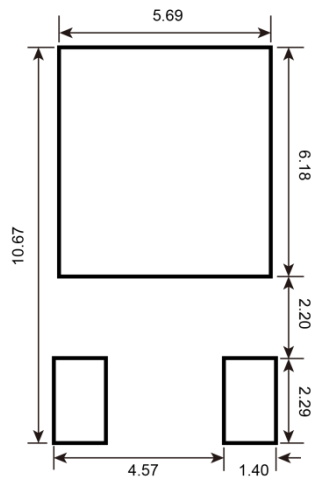


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code

O = Jan

P = Feb

Q = Mar

R = Apr

S = May

T = Jun

U = Jul

V = Aug

W = Sep

X = Oct

Y = Nov

Z = Dec

L = Lot Code (1~9, A~Z)

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