

N-channel 800 V, 0.23 Ω typ., 16 A MDmesh™ K5 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

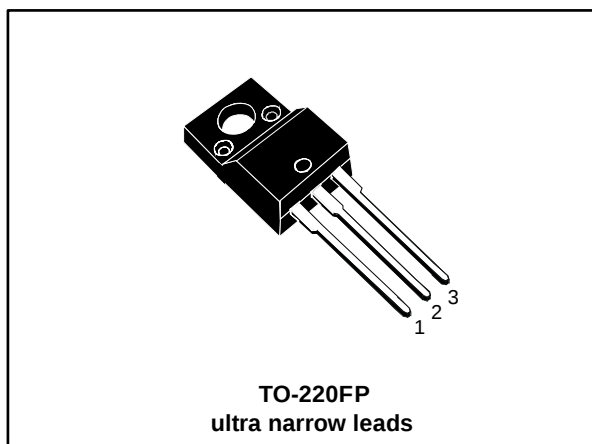
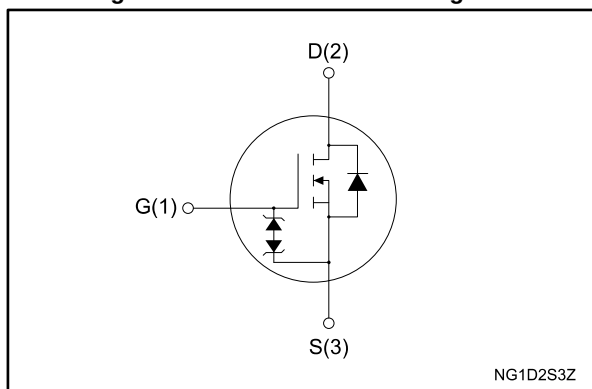


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STFU23N80K5	800 V	0.28 Ω	16 A	35 W

- Industry's lowest R_{DS(on)} X area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STFU23N80K5	23N80K5	TO-220FP ultra narrow leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±30	V
I _D	Drain current (continuous) at T _{case} = 25 °C	16	A
	Drain current (continuous) at T _{case} = 100 °C	10	
I _{DM} ⁽¹⁾	Drain current (pulsed)	64	A
P _{TOT}	Total dissipation at T _{case} = 25 °C	35	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t= 1 s, T _C = 25 °C)	2500	V
T _{stg}	Storage temperature range	-55 to 150	°C
T _j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾I_{SD} ≤ 16 A, di/dt=100 A/μs, V_{DS} peak < V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

⁽³⁾V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	3.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR} ⁽¹⁾	Avalanche current, repetitive or not repetitive	5	A
E _{AS} ⁽²⁾	Single pulse avalanche energy	400	mJ

Notes:

⁽¹⁾Pulse width limited by T_{jmax}.

⁽²⁾Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 800 V			1	μA
		V _{GS} = 0 V, V _{DS} = 800 V, T _{case} = 125 °C ⁽¹⁾			50	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 8 A		0.23	0.28	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	1000	-	pF
C _{oss}	Output capacitance		-	65	-	
C _{rss}	Reverse transfer capacitance		-	1.5	-	
C _{O(tr)} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 640 V, V _{GS} = 0 V	-	165	-	pF
C _{O(er)} ⁽²⁾	Equivalent output capacitance	V _{DS} = 0 to 640 V, V _{GS} = 0 V	-	59	-	
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	4.7	-	Ω
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 16 A, V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	33	-	nC
Q _{gs}	Gate-source charge		-	6	-	
Q _{gd}	Gate-drain charge		-	25	-	

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 8\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	14	-	ns
t_r	Rise time		-	9	-	
$t_{d(off)}$	Turn-off delay time		-	48	-	
t_f	Fall time		-	9	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 16\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	410		ns
Q_{rr}	Reverse recovery charge		-	7		μC
I_{RRM}	Reverse recovery current		-	34		A
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	650		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	32		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

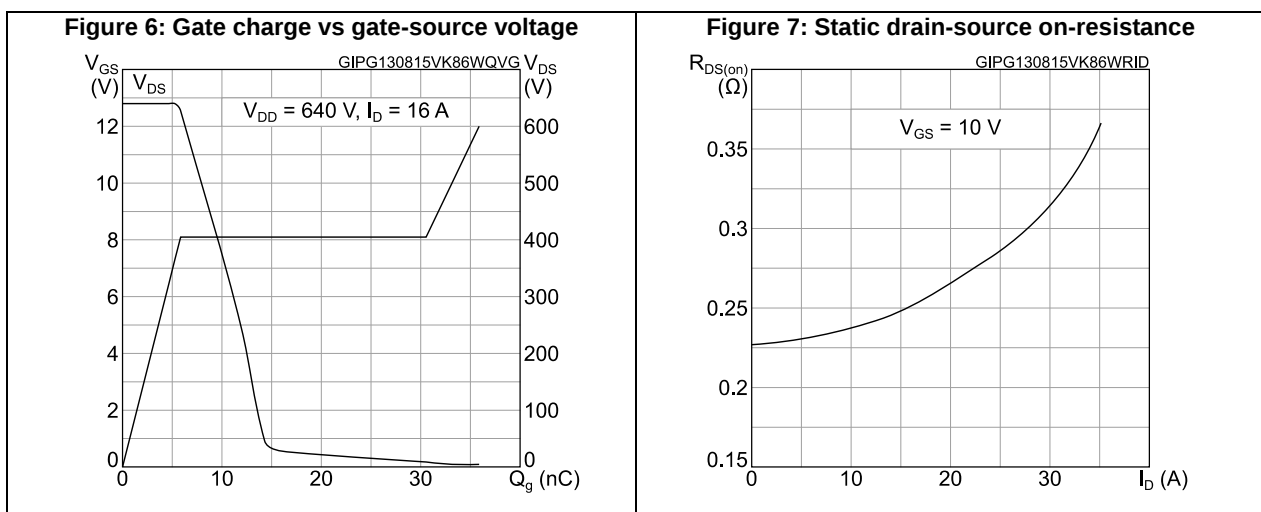
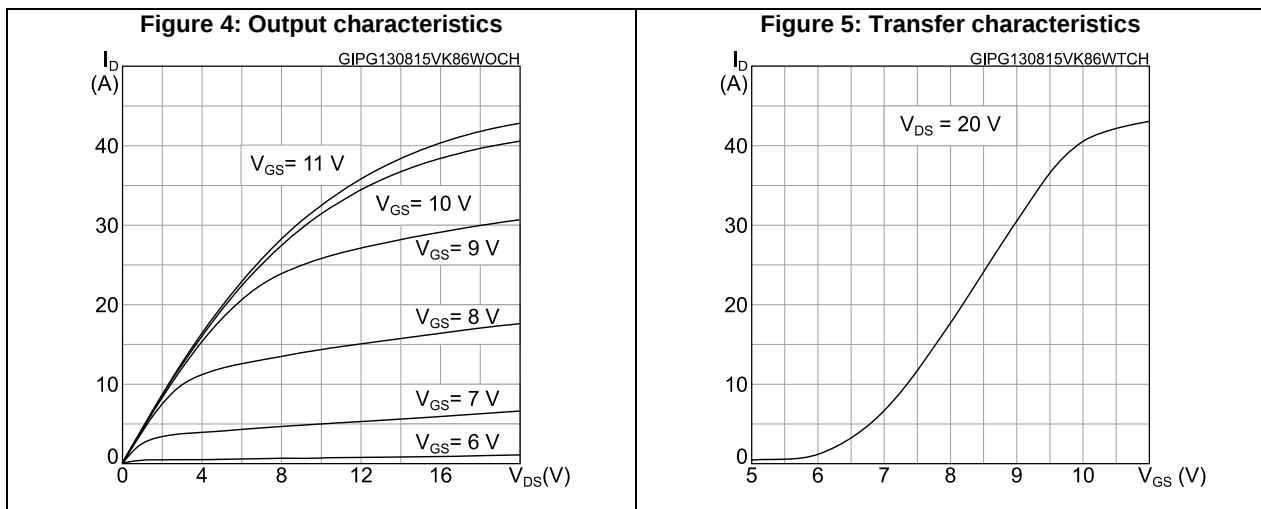
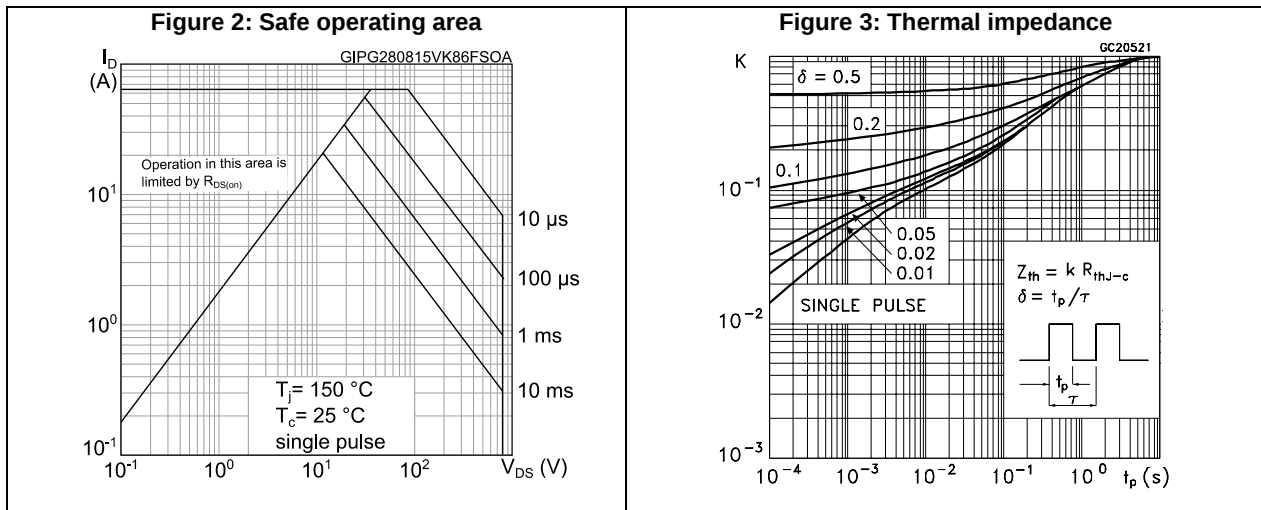


Figure 8: Capacitance variations

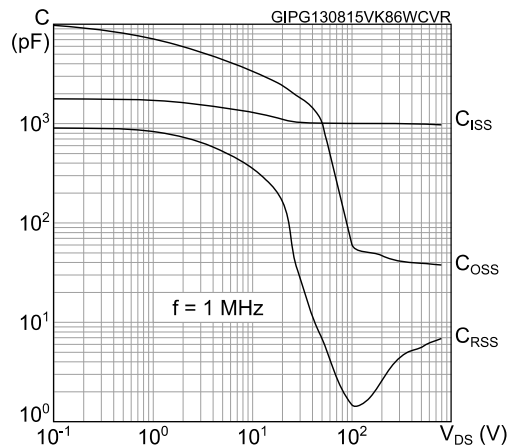


Figure 9: Normalized gate threshold voltage vs temperature

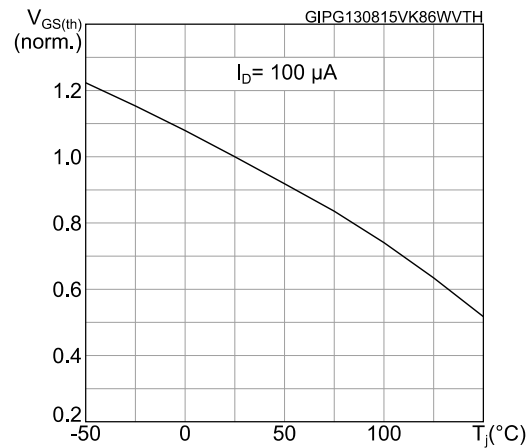


Figure 10: Normalized on-resistance vs temperature

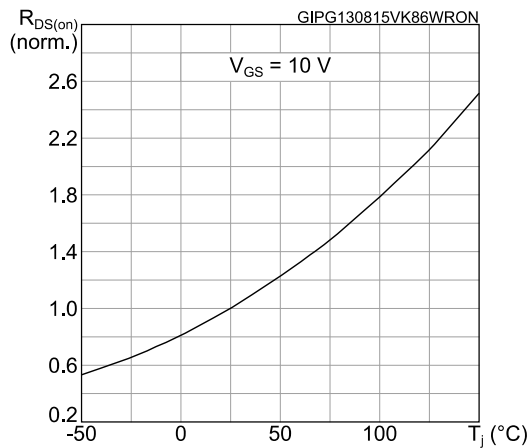
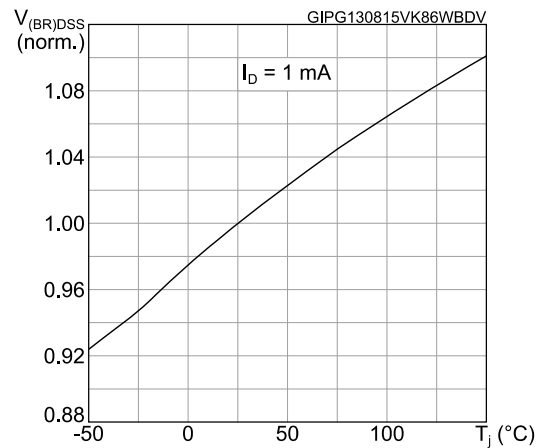
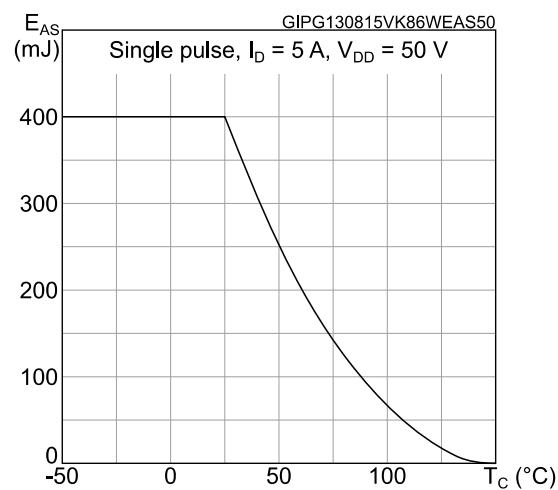
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Maximum avalanche energy vs temperature



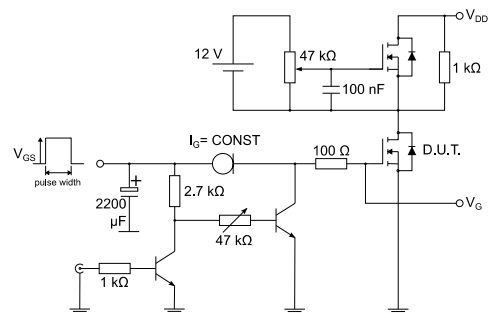
3 Test circuits

Figure 13: Test circuit for resistive load switching times



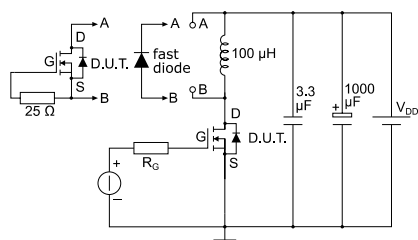
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Figure 14: Test circuit for gate charge behavior



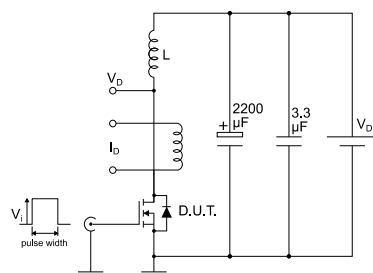
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Figure 15: Test circuit for inductive load switching and diode recovery times



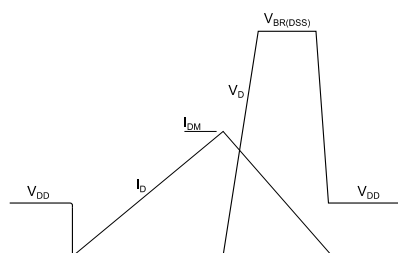
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Figure 16: Unclamped inductive load test circuit



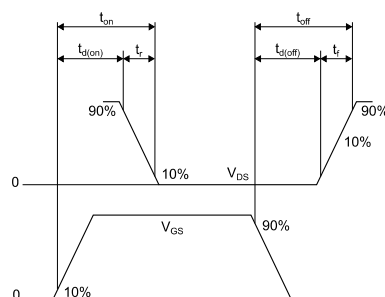
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 19: TO-220FP ultra narrow leads package outline

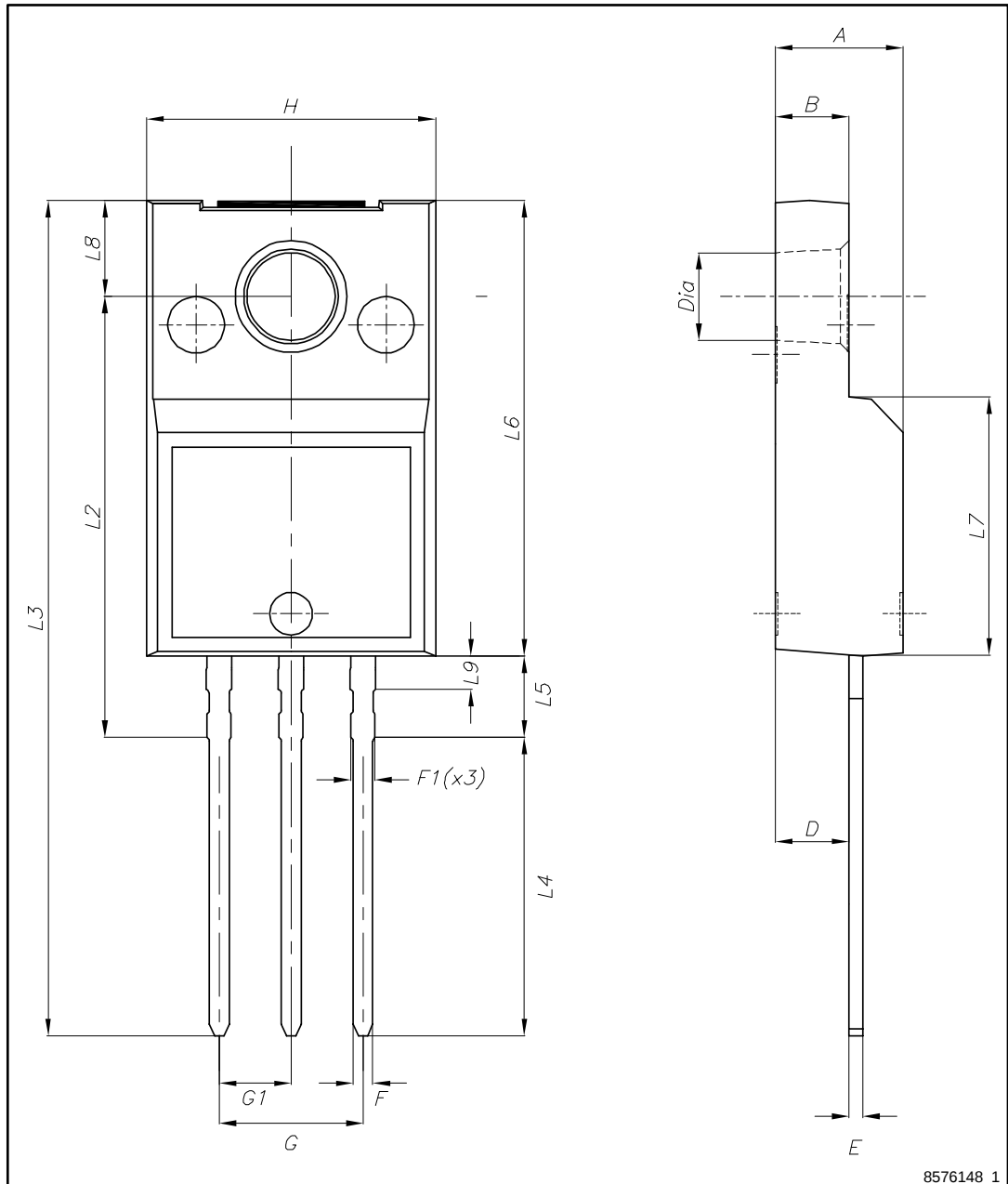


Table 10: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-Feb-2017	1	First release

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