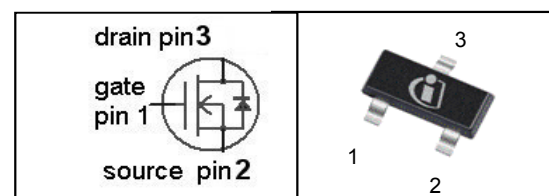


**OptiMOS™ Small-Signal-Transistor**
**Features**

- N-channel
- Enhancement mode
- Logic level
- Avalanche rated
- fast switching
- Pb-free lead-plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


**Product Summary**

$V_{DS}$		60	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	3	$\Omega$
	$V_{GS}=4.5\text{ V}$	4	
$I_D$		0.3	A

**PG-SOT23**


Type	Package	Tape and Reel Information	Marking	HalogenFree	Packing
2N7002	PG-SOT-23	H6327: 3000 pcs/reel	72s	Yes	Non Dry

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_A=25\text{ °C}$	0.30	A
		$T_A=70\text{ °C}$	0.24	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	1.2	
Avalanche energy, single pulse	$E_{AS}$	$I_D=0.3\text{ A}, R_{GS}=25\ \Omega$	1.3	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=0.3\text{ A}, V_{DS}=48\text{ V},$ $di/dt=200\text{ A}/\mu\text{s},$ $T_{j,max}=150\text{ °C}$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$		$\pm 20$	V
ESD class		JESD22-A114 (HBM)	class 0 (<250V)	
Power dissipation	$P_{tot}^{(2)}$	$T_A=25\text{ °C}$	0.5	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	

<sup>(1)</sup> J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - minimal footprint <sup>(2)</sup>	$R_{thJA}$		-	-	250	K/W
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**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1.5	2.1	2.5	
Drain-source leakage current	$I_{D(off)}$	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	0.1	$\mu\text{A}$
		$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	5	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	10	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=0.25\text{ A}$	-	2.0	4	$\Omega$
		$V_{GS}=10\text{ V}, I_D=0.5\text{ A}$	-	1.6	3	
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=0.24\text{ A}$	0.2	0.36	-	S

<sup>(2)</sup> Performed on a 40x40mm<sup>2</sup> FR4 PCB with both sided Cu sense-force traces, each 1mm wide, 70  $\mu\text{m}$  thick and 20mm long.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	13	20	pF
Output capacitance	$C_{oss}$		-	4.1	6	
Reverse transfer capacitance	$C_{rss}$		-	2.0	3	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=0.5\text{ A}, R_G=6\ \Omega$	-	3.0	4.5	ns
Rise time	$t_r$		-	3.3	5	
Turn-off delay time	$t_{d(off)}$		-	5.5	9	
Fall time	$t_f$		-	3.1	5	

**Gate Charge Characteristics**

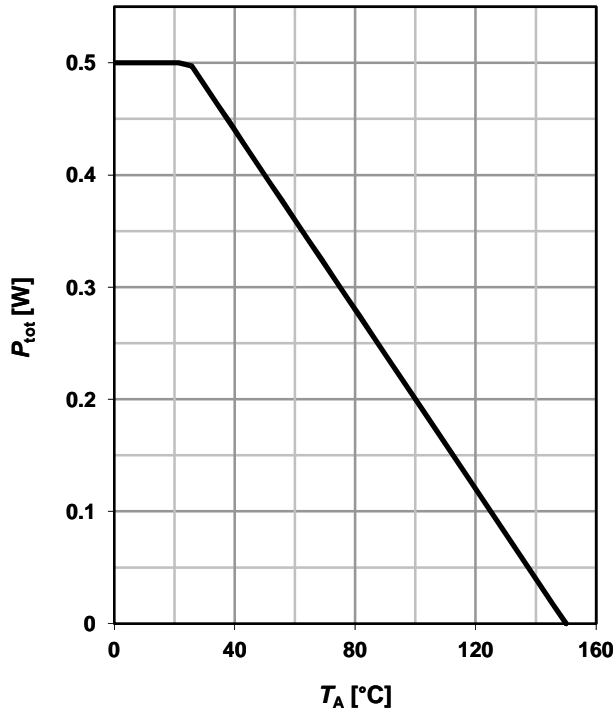
Gate to source charge	$Q_{gs}$	$V_{DD}=48\text{ V}, I_D=0.5\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	0.05	0.1	nC
Gate to drain charge	$Q_{gd}$		-	0.2	0.4	
Gate charge total	$Q_g$		-	0.4	0.6	
Gate plateau voltage	$V_{plateau}$		-	4.0	-	V

**Reverse Diode**

Diode continuous forward current	$I_S$	$T_A=25\text{ }^\circ\text{C}$	-	-	0.3	A
Diode pulse current	$I_{S,pulse}$		-	-	1.2	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=0.5\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.96	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=30\text{ V}, I_F=0.5\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	8.5	13	ns
Reverse recovery charge	$Q_{rr}$		-	2.4	4	nC

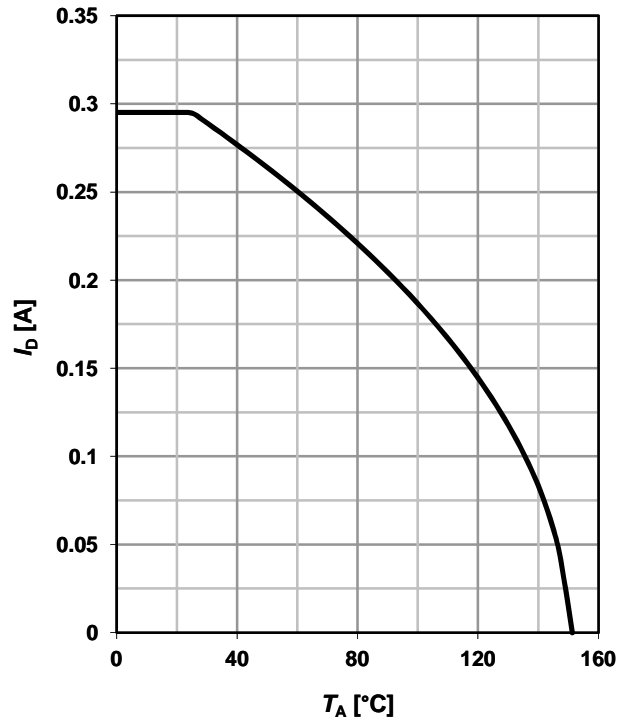
**1 Power dissipation**

$P_{tot}=f(T_A)$



**2 Drain current**

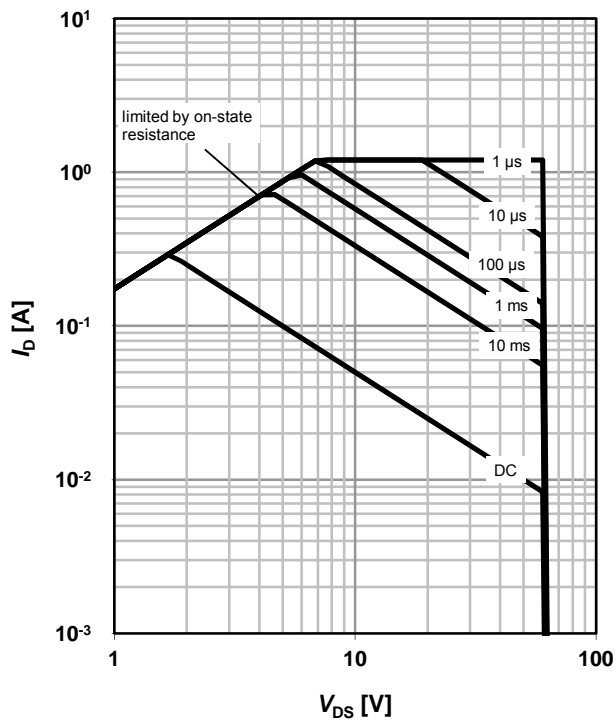
$I_D=f(T_A); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_A=25\text{ °C}; D=0$

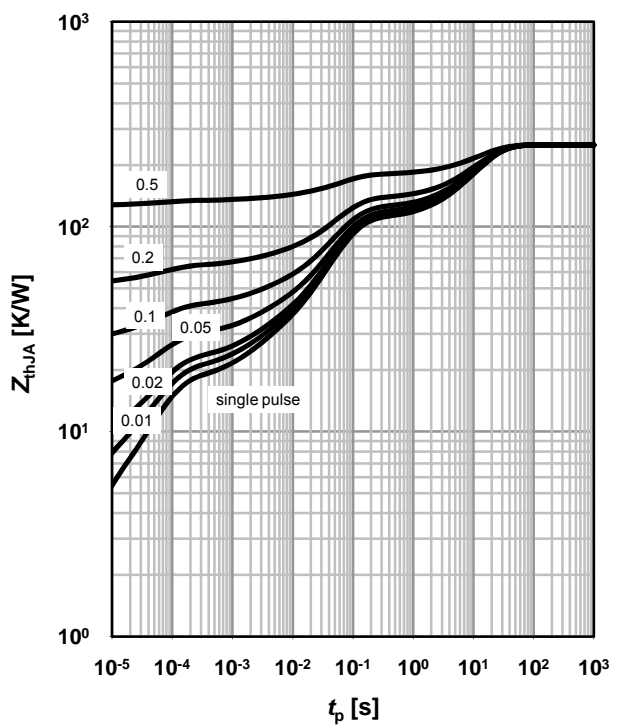
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJA}=f(t_p)$

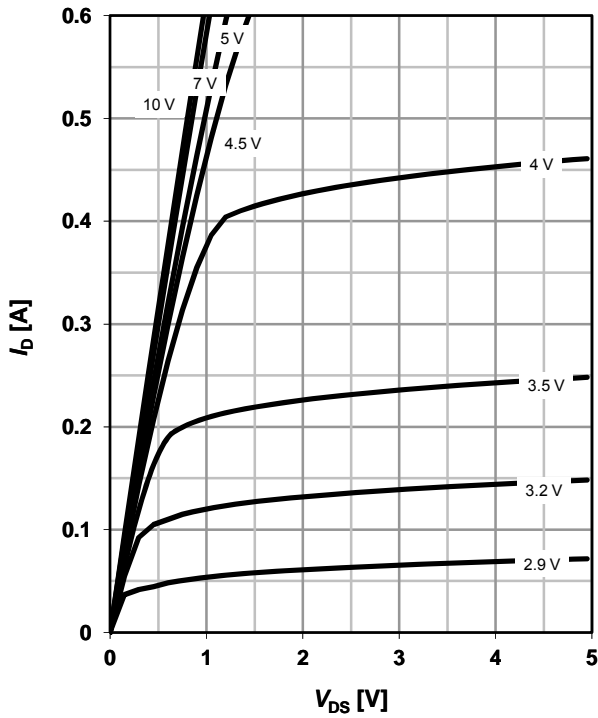
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

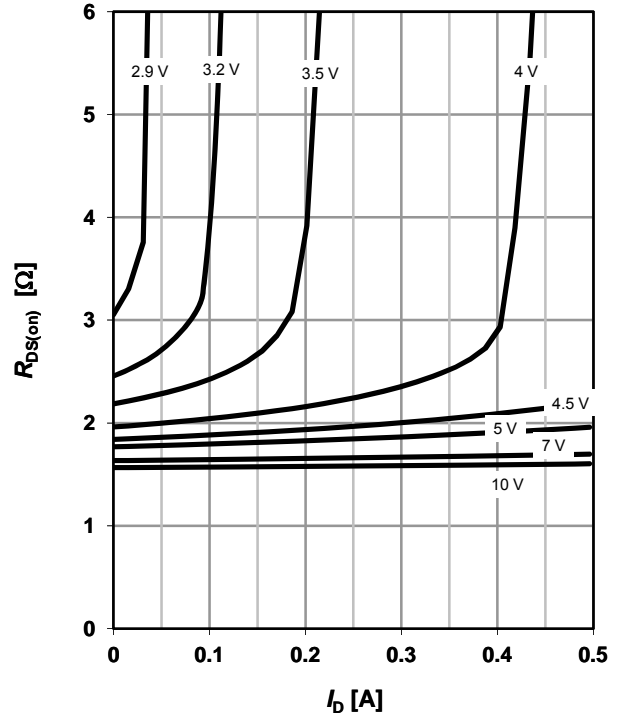
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

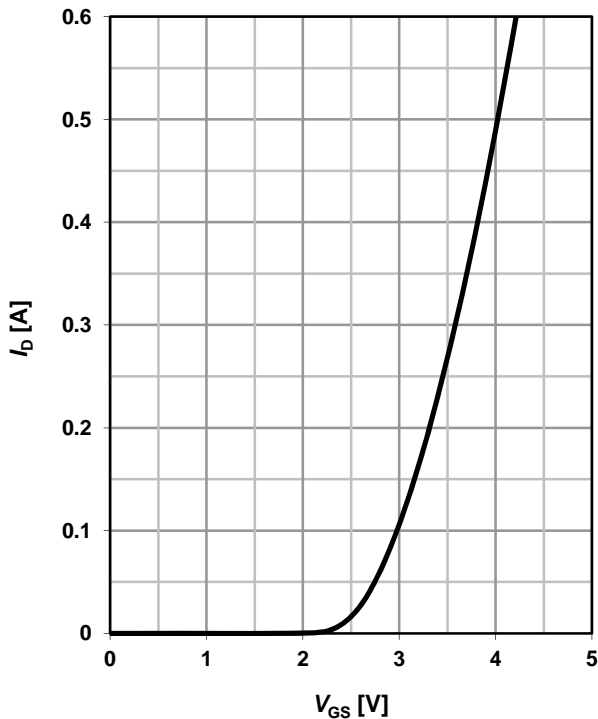
$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

parameter:  $V_{GS}$



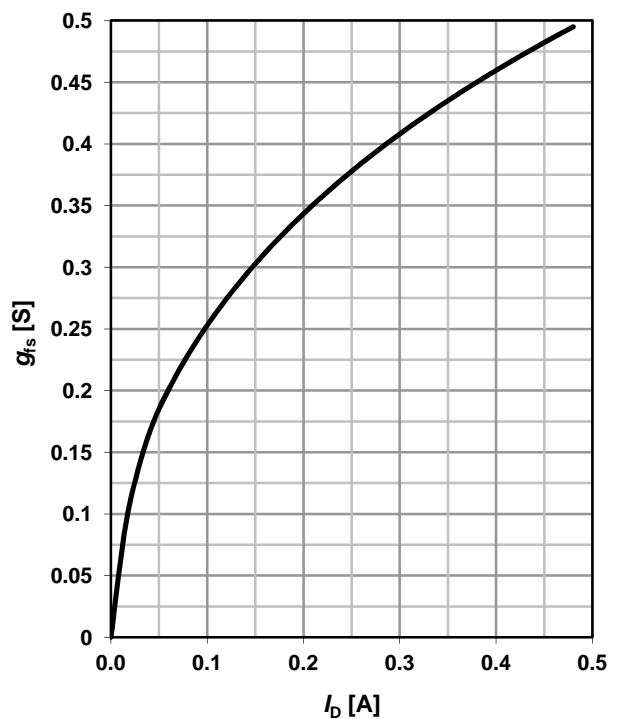
**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$



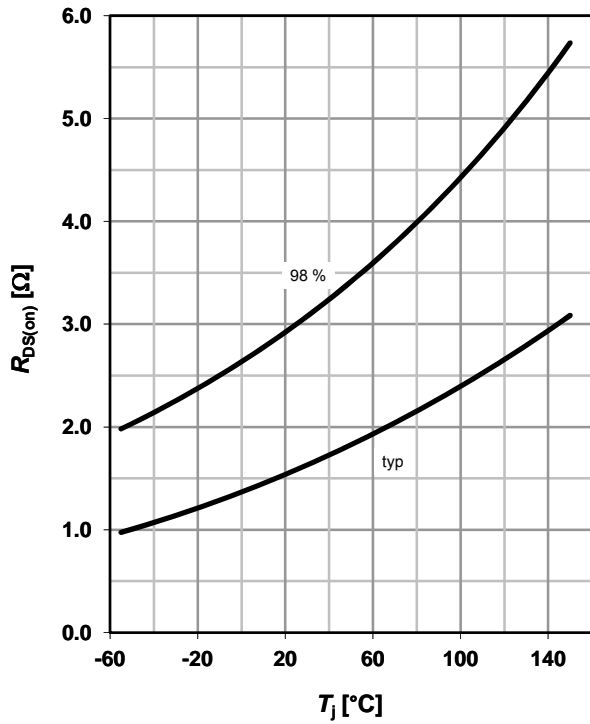
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



**9 Drain-source on-state resistance**

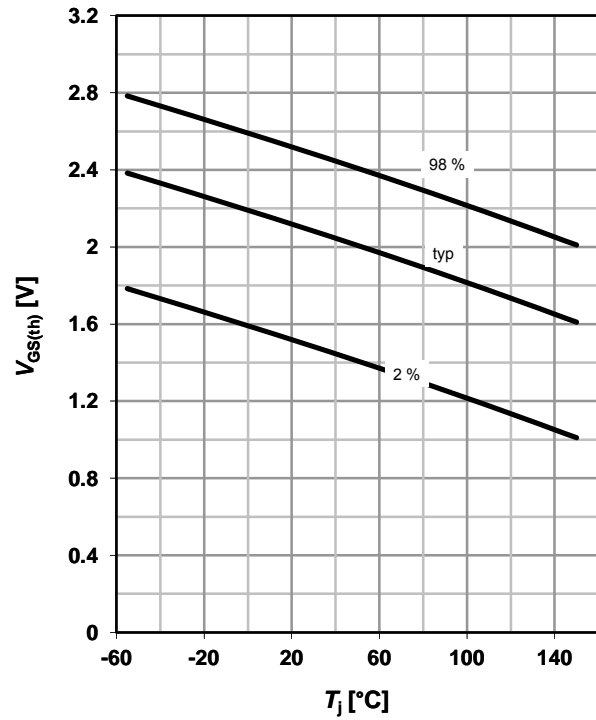
$R_{DS(on)}=f(T_j); I_D=0.3\text{ A}; V_{GS}=10\text{ V}$



**10 Typ. gate threshold voltage**

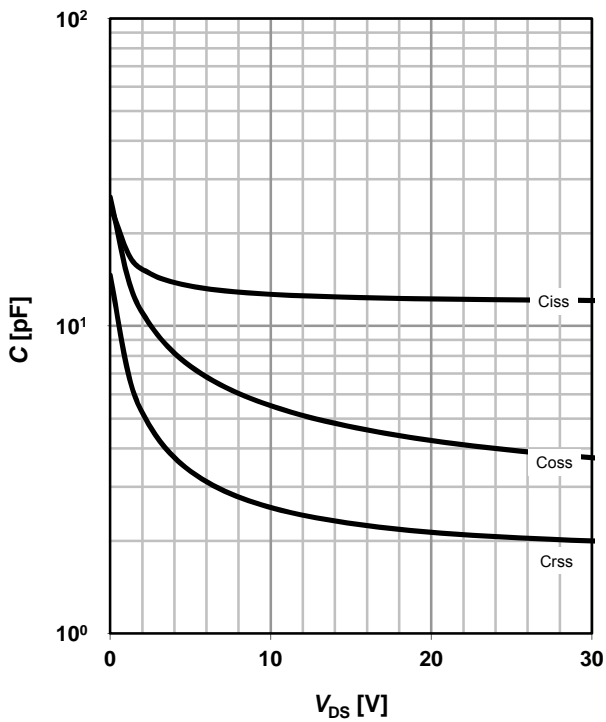
$V_{GS(th)}=f(T_j); V_{DS}=V_{GS}; I_D=250\ \mu\text{A}$

parameter:  $I_D$



**11 Typ. capacitances**

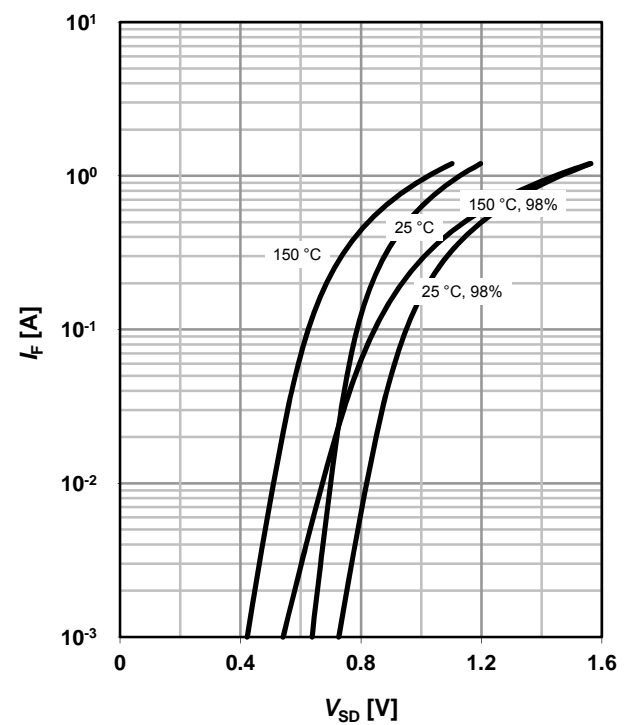
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}; T_j=25^\circ\text{C}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

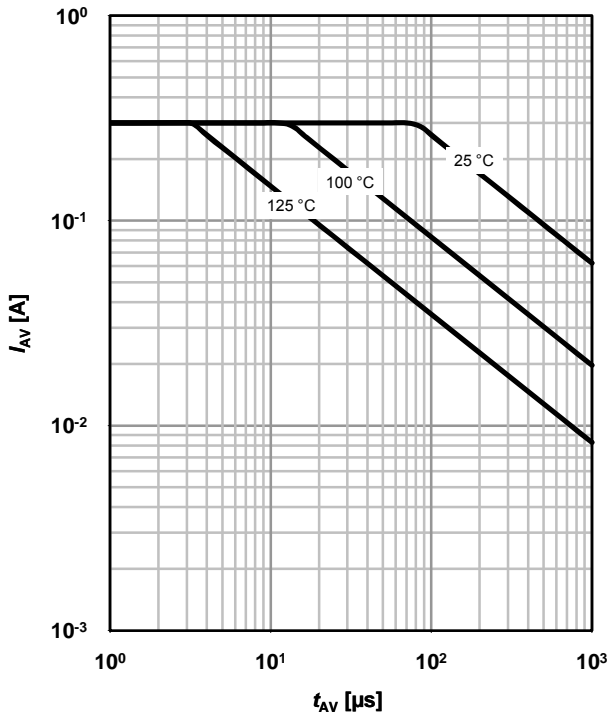
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25\Omega$

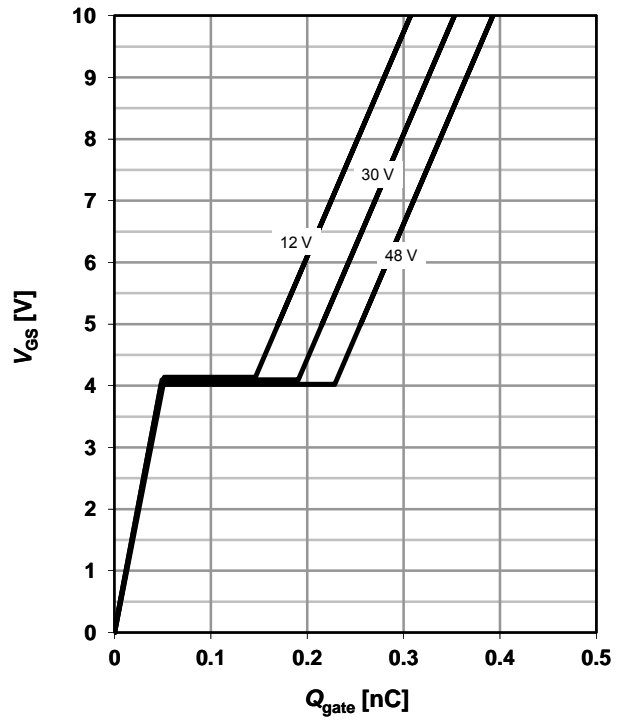
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

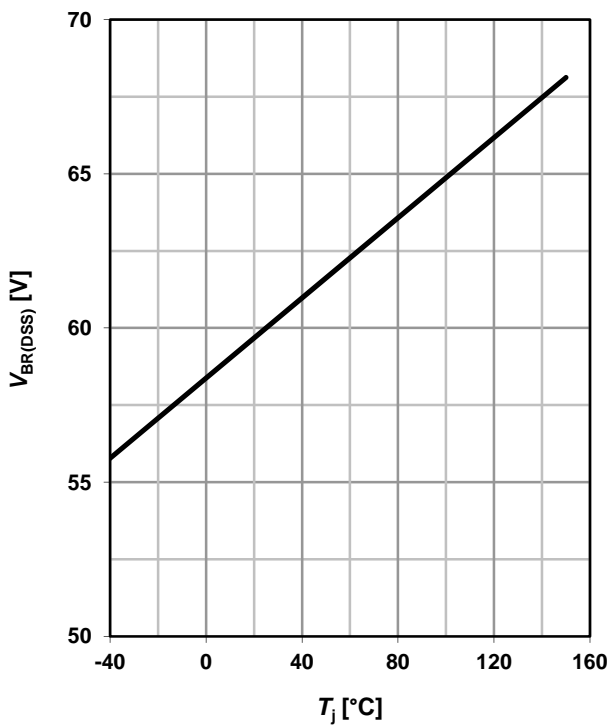
$V_{GS}=f(Q_{gate}); I_D=0.5\text{ A pulsed}$

parameter:  $V_{DD}$

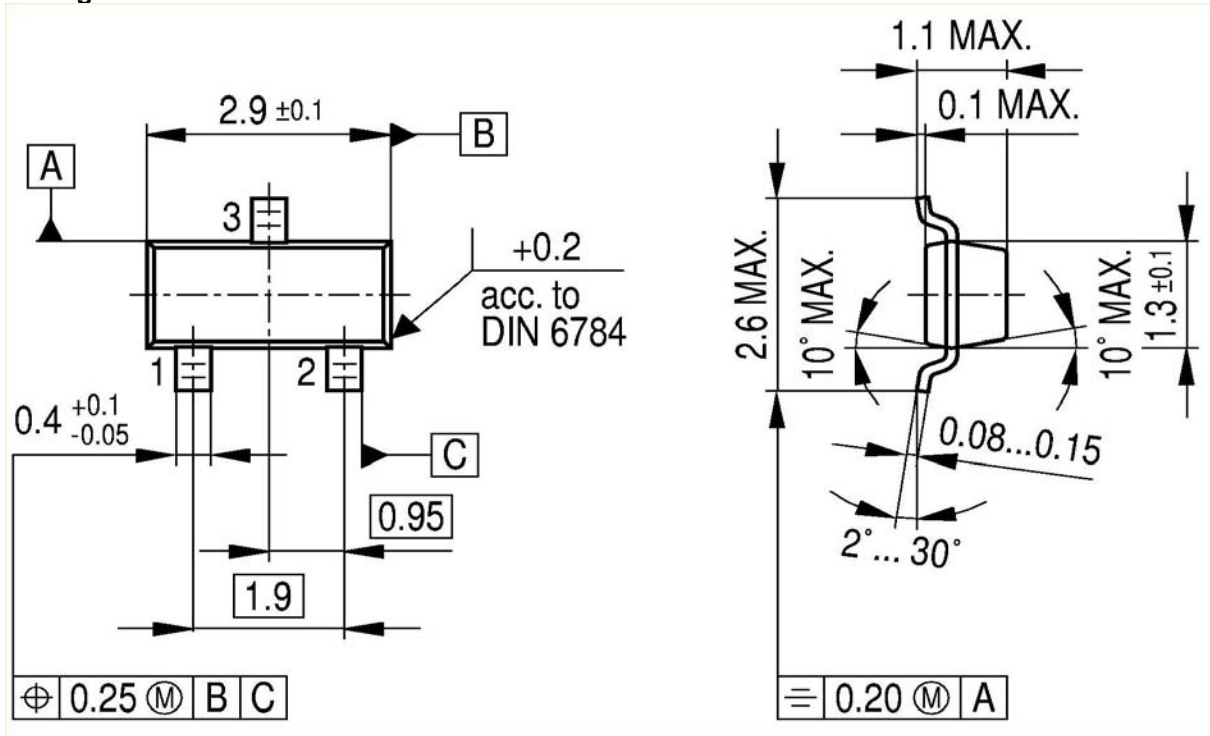


**15 Drain-source breakdown voltage**

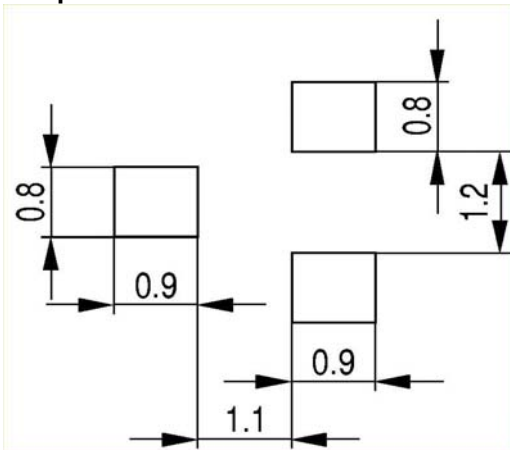
$V_{BR(DSS)}=f(T_j); I_D=250\ \mu\text{A}$



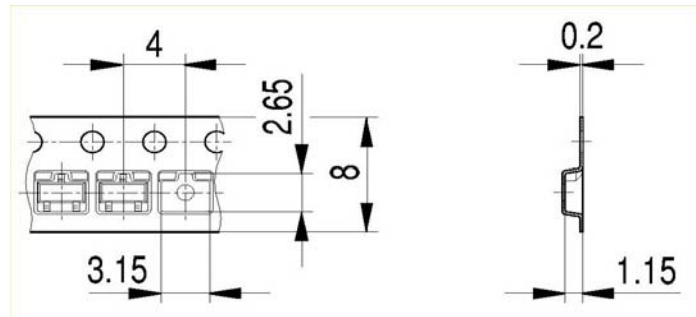
Package Outline:



Footprint:



Packing:



Dimensions in mm



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