General Description

The MAX14836 transceiver is suitable for 24V binary sensors. Additional 24V digital inputs and outputs are provided. Two internal linear regulators generate common sensor power requirements: 5V and 3.3V.

On-board DIO and DO drivers are independently configurable for push-pull, high-side (pnp), or low-side (npn) operation. The device detects a wake-up condition and generates a wake-up signal on the active-low $\overline{WU}$ output.

An SPI interface allows configuration and monitoring of the devices. Extensive alarm conditions are detected and communicated through the $\overline{IRQ}$ output and the SPI interface. The device features reverse-polarity, short-circuit, and thermal protection. All power lines are monitored for undervoltage conditions.

Both DIO and DO drivers are specified for sinking/sourcing 200mA.

The MAX14836 is available in a 4mm x 4mm, 24-pin TQFN package, and is specified over the -40°C to +105°C temperature range.

Applications

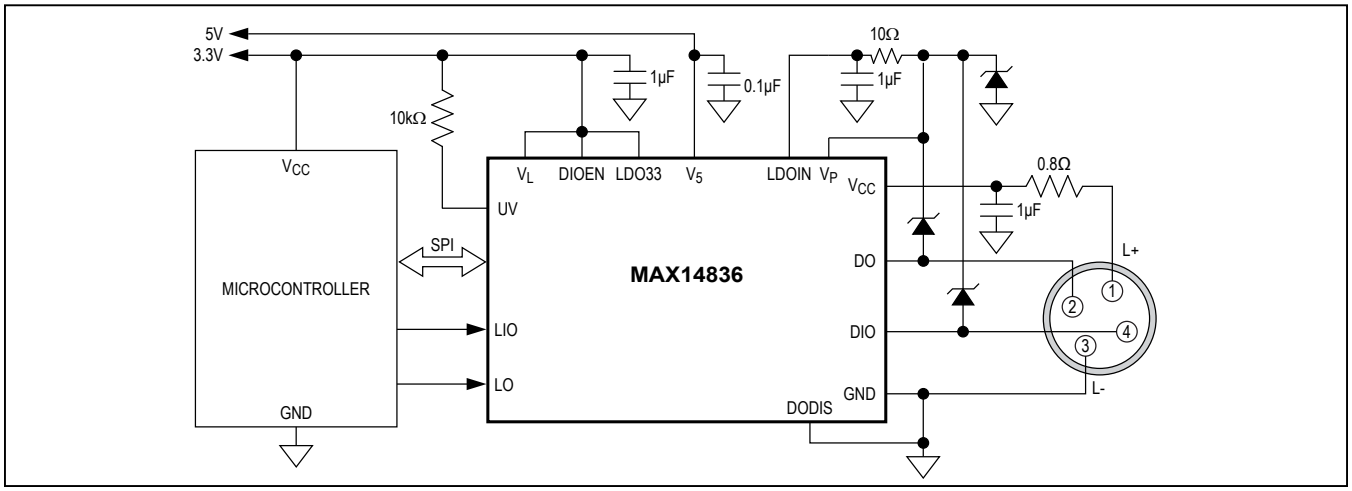
- Industrial Sensors

Ordering Information *appears at end of data sheet.*

Features and Benefits

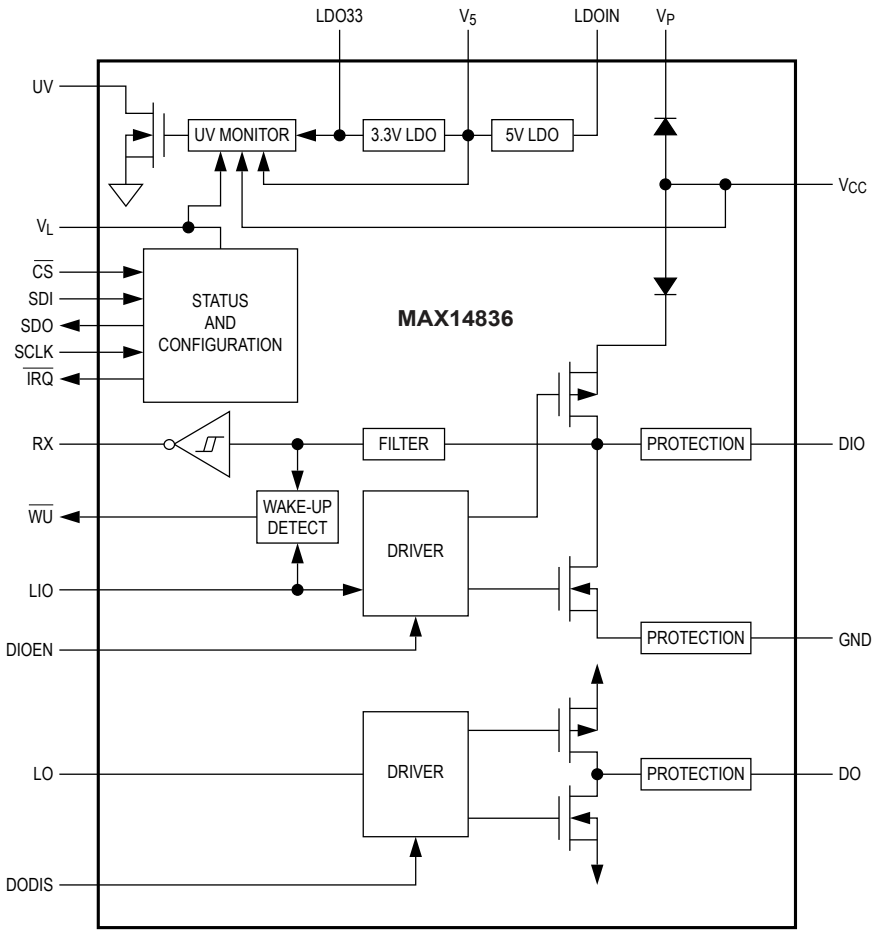
- High Configurability and Integration Enable Faster Time-to-Market and Reduce SKUs
  - Push-Pull, High-Side, or Low-Side Outputs
  - DIO and DO Drivers Can Be Connected in Parallel to Increase Current and Reduce Output Resistance
  - 200mA Specified DIO and DO Output Drive
  - 2.5V to 5V Logic Interface Levels
  - 5V and 3.3V Linear Regulators
  - 400µs Wake-Up Detection on DIO Line
  - 3µF DIO Load-Drive Capability
  - 2µF DO Load-Drive Capability
  - EMI Emission Control Through Slew-Controlled Driver
- Integrated Protection Enables Robust Solutions
  - Reverse-Polarity-Protected 24V Supply Output
  - SPI Interface for Configuration and Monitoring
  - Reverse-Polarity and Short-Circuit Protection on All 24V Inputs/Outputs
  - High-Temperature Warning and Thermal Shutdown
  - Extensive Fault Monitoring and Reporting
  - -40°C to +105°C Operating Temperature Range
- Space-Saving 4mm x 4mm TQFN Package Saves Circuit Footprint

Typical Application Circuit



maxim integrated™

Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} ..... -40V to +40V
V_P ..... MIN: the higher of -0.3V and (V_{CC} - 0.3V)
MAX: the higher of 40V and (V_{CC} + 40V)
LDOIN ..... -0.3V to +40V
V_5 ..... -0.3V to the lesser of (V_{LDOIN} + 0.3V) and +6V
LDO33 ..... -0.3V to the lesser of (V_5 + 0.3V) and +6V
V_L ..... -0.3V to +6V
DIO, DO ..... MIN: the higher of -40V and (V_{CC} - 40V)
MAX: the lesser of +40V and (V_{CC} + 40V)
Logic Inputs
LIO, DODIS, DIOEN, LO, $\overline{CS}$,
SDI, SCLK ..... -0.3V to (V_L + 0.3V)
Logic Outputs
RX, $\overline{WU}$, SDO, $\overline{IRQ}$ ..... -0.3V to (V_L + 0.3V)
UV ..... -0.3V to +6V
Continuous Current Into V_P ..... ±50mA
Continuous Current Into Any Logic Pin ..... ±50mA
Continuous Power Dissipation
TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range ..... -40°C to +105°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{CC} = 9V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}		9		36	V
V_{CC} Supply Current	I_{CC}	DIO and DO enabled, push-pull and output low, no load on V_5 or LDO33, LDOIN is not connected to V_D		0.65	1.2	mA
V_{CC} Undervoltage-Lockout Threshold	V_{CCUVLO}	V_{CC} falling	6	7.5	8.4	V
V_{CC} Undervoltage-Lockout Threshold Hysteresis	V_{CCUVLO_HYST}			200		mV
V_L Logic-Level Supply Voltage	V_L		2.3		5.5	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND			5	µA
V_L Undervoltage Threshold	V_{LUVLO}	V_L falling	0.65	0.95	1.30	V

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
5V LDO (V_5)						
LDOIN Input Voltage Range	V_{LDOIN}		7		36	V
V_5 Supply Current	I_{5_IN}	LDOIN shorted to V_5, external 5V applied to V_5, no switching, LDO33 disabled		1.5		mA
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 falling		2.4		V
LDOIN Supply Current	I_{LDOIN}	DIO and DO enabled, push-pull and output low, no load on V_5 or LDO33, LDOIN not connected to V_D		2.0	3.2	mA
V_5 Output Voltage Range	V_5	No load on V_5, 7V ≤ V_{LDOIN} ≤ 36V	4.75	5.00	5.25	V
Power Supply Rejection Ratio	V_{5_PSRR}	V_{CC} = V_{LDOIN} = $1V_{P-P}$, f_{LDOIN} = 100Hz	60	88		dB
V_5 Load Regulation		1mA < I_{LOAD} < 10mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5		0.8		%
		1mA < I_{LOAD} < 30mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5, 10Ω–1µF compensation network added to V_5		0.8		
3.3V LDO (LDO33)						
LDO33 Output Voltage	V_{LDO33}	No load on LDO33	3.1	3.3	3.5	V
LDO33 Undervoltage-Lockout Threshold	$V_{LDO33UVLO}$	V_{LDO33} falling		2.4		V
LDO33 Load Regulation		1mA < I_{LOAD} < 20mA, V_{LDOIN} = 7V		0.25		%
24V INTERFACE						
DIO Driver Output Voltage High	$V_{OH\_}$ DIO	DIO high-side enabled, I_{DIO} = -200mA	V_{CC} -1.8	V_{CC} -1.0		V
DIO Driver Output Voltage Low	$V_{OL\_}$ DIO	DIO low-side enabled, I_{DIO} = +200mA		1.3	1.8	V
DIO Driver Source Current Limit	$I_{OH\_}$ DIO	DIO high-side enabled, V_{DIO} < (V_{CC} - 5V)	-480	-300	-200	mA
DIO Driver Sink Current Limit	$I_{OL\_}$ DIO	DIO low-side enabled, V_{DIO} > 5V	200	300	480	mA

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DO Driver Output Voltage High	V_{OH_DO}	DO high-side enabled, I_{DO} = -200mA	V_{CC} - 1.8	V_{CC} - 1.1		V
DO Driver Output Voltage Low	V_{OL_DO}	DO low-side enabled, I_{DO} = +200mA		1.4	1.8	V
DO Driver Source Current Limit	I_{OH_DO}	DO high-side enabled, V_{DO} < (V_{CC} - 5V)	-490	-320	-200	mA
DO Driver Sink Current Limit	I_{OL_DO}	DO low-side enabled, V_{DO} > 5V	200	320	490	mA
DIO Input Threshold High	$V_{IH\_}$ DIO	DIO driver disabled	6.8		8	V
DIO Input Threshold Low	$V_{IL\_}$ DIO	DIO driver disabled	5.2		6.4	V
DIO Input Hysteresis	$V_{HYS\_}$ DIO	DIO driver disabled		1.6		V
DIO Weak Pulldown Current	I_{PDDIO}	DIO driver disabled, V_{DIO} = (V_{CC} - 1V)		76	140	µA
DO Leakage Current	I_{PDDO}	0 ≤ V_{DO} ≤ V_{CC} - 1V	-1		+1	µA
DIO Input Capacitance	C_{DIO}	DIO driver disabled		40		pF
DO Input Capacitance	C_{DO}	DO driver disabled		40		pF
LOGIC INPUTS (LIO, DODIS, DIOEN, LO, $\overline{CS}$, SDI, SCLK)						
Logic Input Voltage Low	V_{IL}		0.3 x V_L			V
Logic Input Voltage High	V_{IH}				0.7 x V_L	V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
Logic Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS (RX, $\overline{WU}$, UV, SDO, $\overline{IRQ}$)						
Logic Output Voltage Low	V_{OL}	I_{OUT} = -5mA			0.4	V
Logic Output Voltage High	V_{OHRX}, V_{OHWU}, V_{OHSDO}, V_{OHIRQ},	I_{OUT} = -5mA (Note 3)	V_L - 0.6			V
SDO Leakage Current	I_{LK_SDO}	SDO disabled, SDO = GND or V_L	-1		+1	µA
THERMAL SHUTDOWN						
Thermal Warning Threshold		Die temperature rising, OTemp bit is set		+127		ºC
Thermal Warning Threshold Hysteresis		Die temperature falling, OTemp bit is cleared		23		ºC
Thermal-Shutdown Threshold		Die temperature rising		+165		ºC
Thermal-Shutdown Hysteresis				20		ºC

AC Electrical Characteristics

(V_{CC} = 9V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIO, DO INTERFACES						
Switching Rate	DR				3	kHz
DRIVER (DIO, DO)						
Driver Low-to-High Propagation Delay	t_{PDLH}	Push-pull or high-side (pnp) configuration, Figure 1		1.5	3.5	µs
Driver High-to-Low Propagation Delay	t_{PDHL}	Push-pull or low-side (npn) configuration, Figure 1		1.6	3.9	µs
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$		0.1	1.8	µs
Driver Rise Time	t_{RISE}	Push-pull or high-side (pnp) configuration, Figure 1		1.5	4.0	µs
Driver Fall Time	t_{FALL}	Push-pull or low-side (npn) configuration, Figure 1		1.3	4.0	µs
RECEIVER (DIO) (Figure 2)						
Receiver Low-to-High Propagation Delay	t_{PRLH}	RxFilter = 1		0.6		µs
		RxFilter = 0		1.7		
Receiver High-to-Low Propagation Delay	t_{PRHL}	RxFilter = 1		0.3		µs
		RxFilter = 0		0.7		
WAKE-UP DETECTION (Figure 3)						
Wake-Up Input Minimum Pulse Width	t_{WUMIN}		190	250	310	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}		520	650	780	µs
$\overline{WU}$ Output Low-Time	t_{WUL}	Valid wake-up condition on DIO	40	50	60	µs

AC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING ($\overline{CS}$, SCLK, SDI, SDO) (Figure 4)						
SCLK Clock Period	t_{CH+CL}		84			ns
SCLK Pulse-Width High	t_{CH}		42			ns
SCLK Pulse-Width Low	t_{CL}		42			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}		20			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		20			ns
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
SDO Propagation Delay	t_{DO}	$V_L \geq 3.0V$			32	ns
		$V_L \geq 2.3V$			36	
SDO Rise and Fall Times	t_{FT}				20	ns
Minimum $\overline{CS}$ Pulse	t_{CSW}		77			ns

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: UV is an open-drain output. Connect UV to a voltage less than 5.5V through an external pullup resistor.

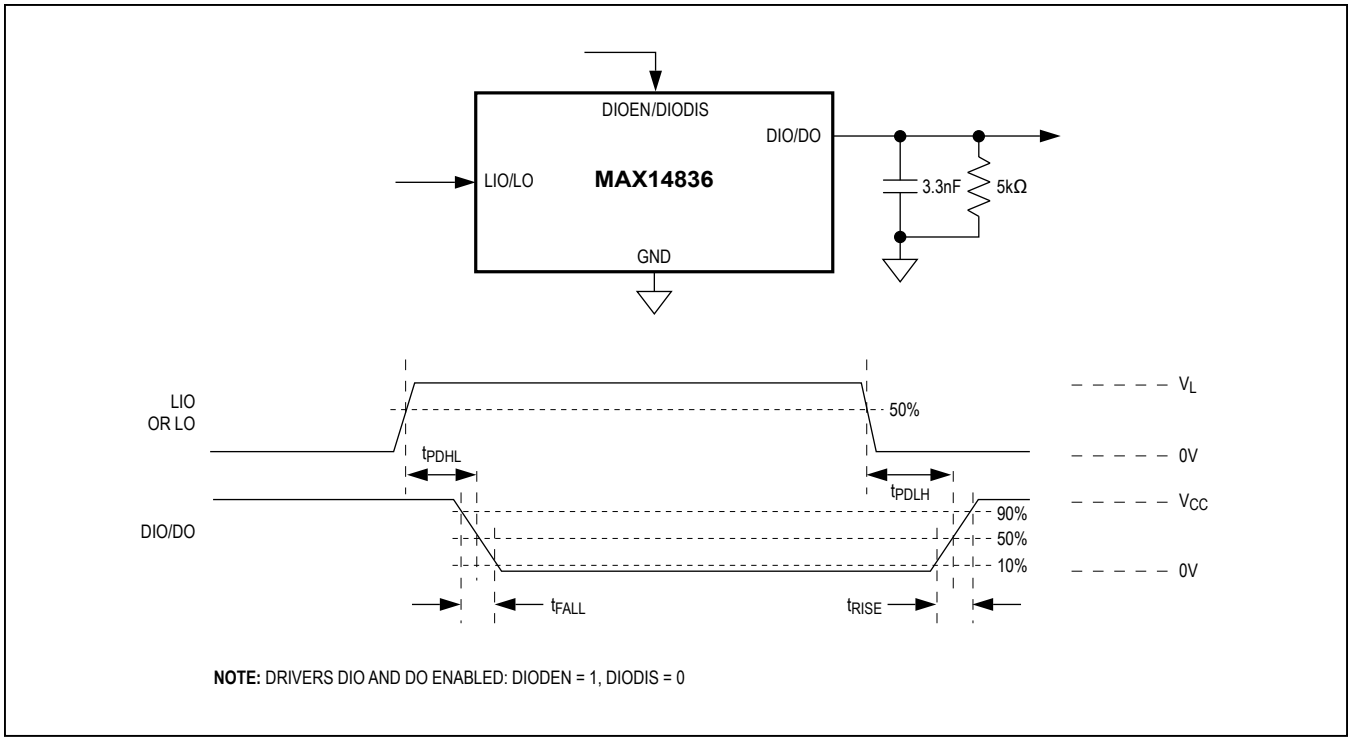


Figure 1. DIO and DO Driver Propagation Delays and Rise/Fall Times

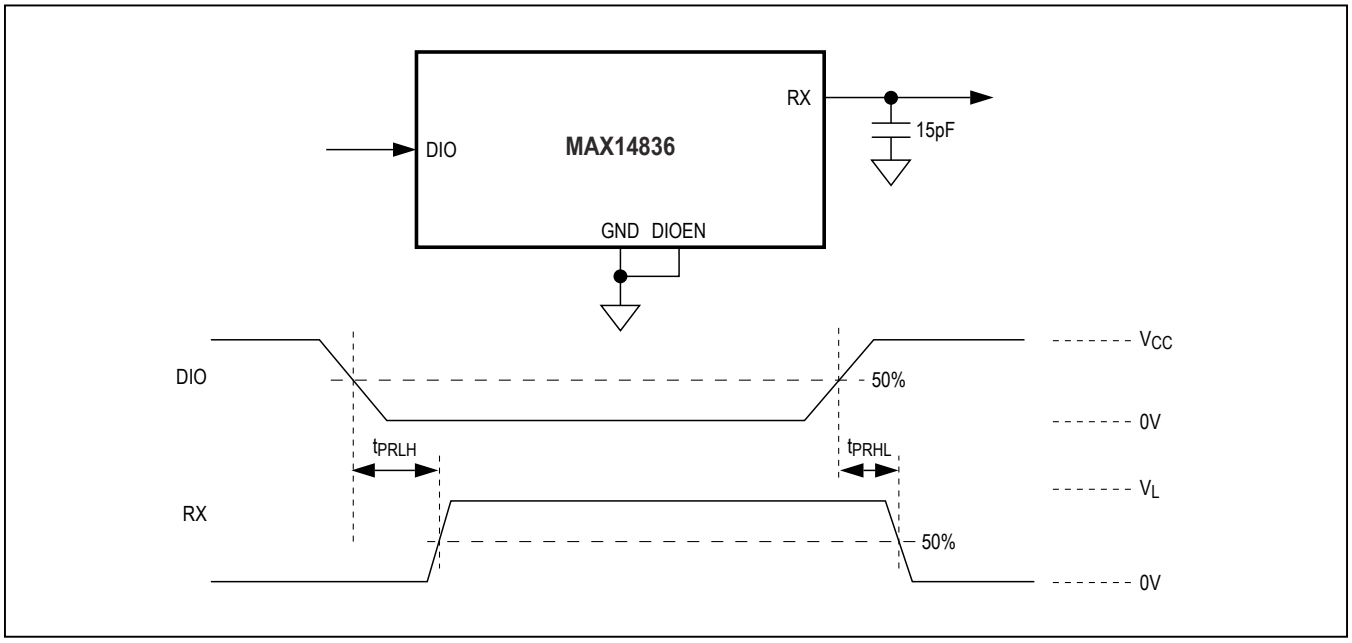


Figure 2. DIO Receiver Propagation Delay

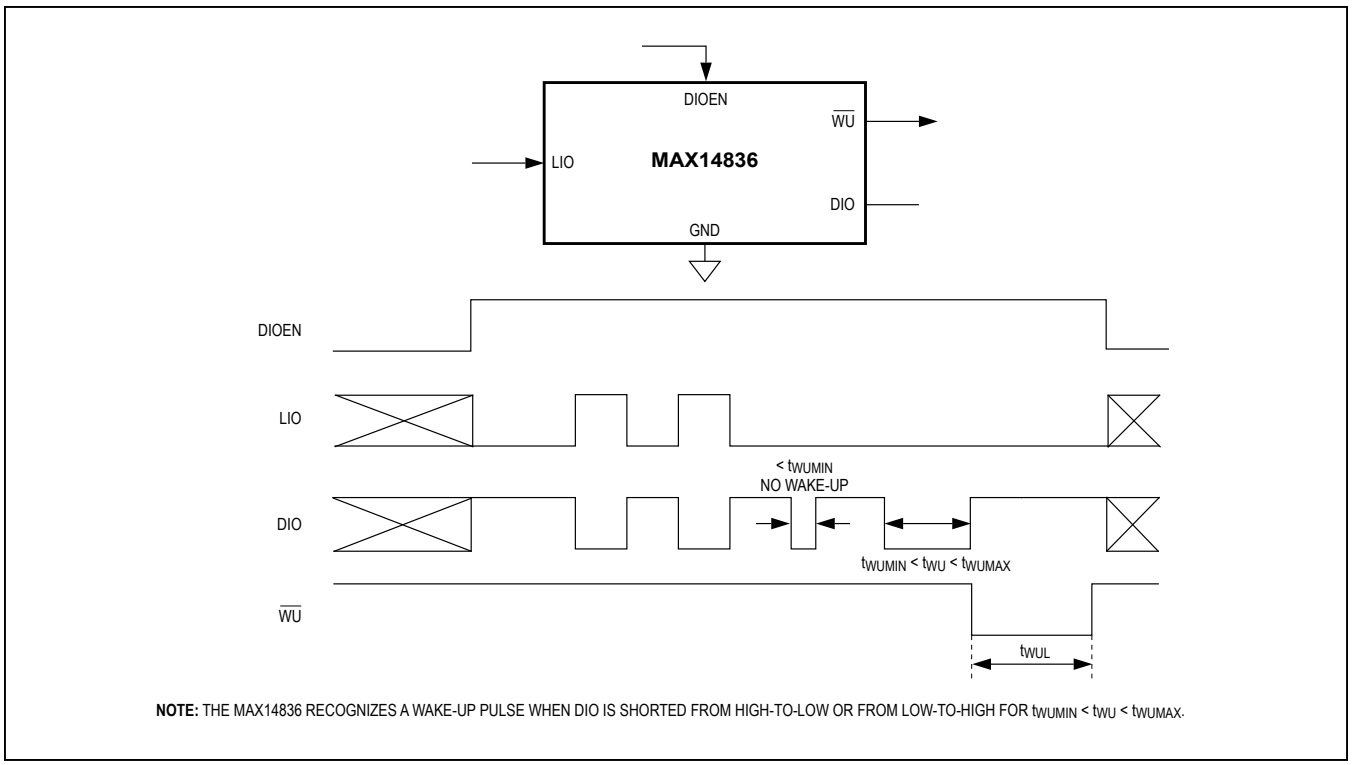


Figure 3. Wake-Up Detection Timing

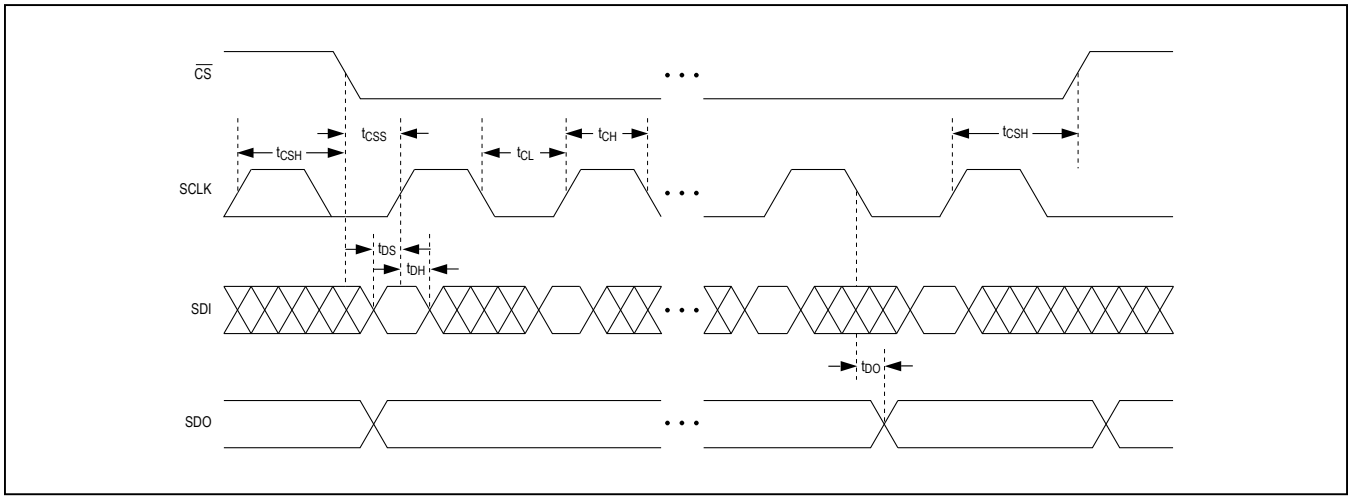
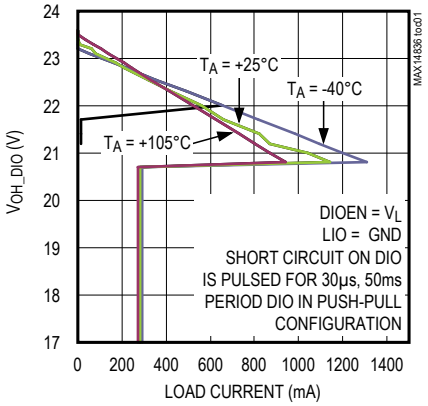


Figure 4. SPI Timing Diagram

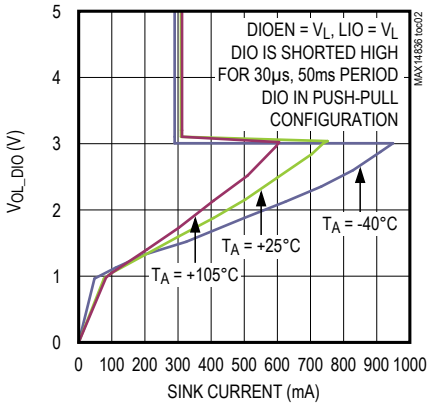
Typical Operating Characteristics

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, DIO and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

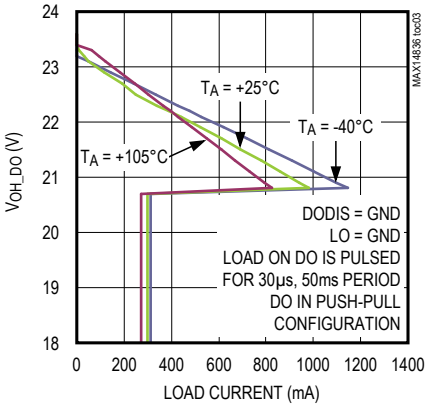
DIO DRIVER OUTPUT HIGH vs. LOAD CURRENT



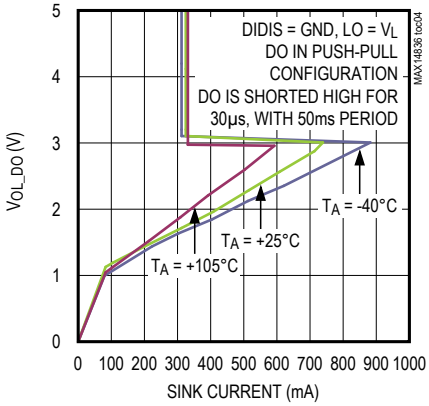
DIO DRIVER OUTPUT LOW vs. SINK CURRENT



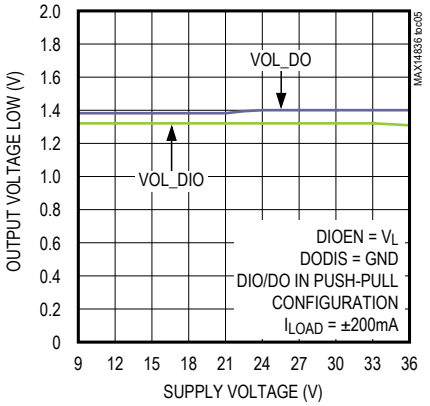
DO DRIVER OUTPUT HIGH vs. LOAD CURRENT



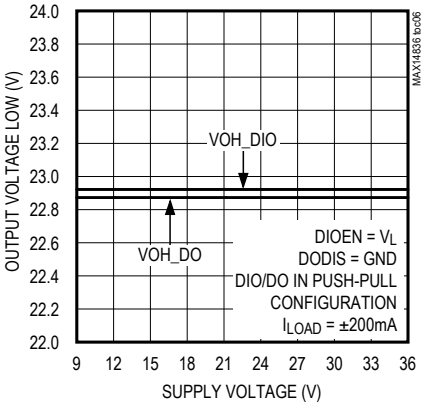
DIO DRIVER OUTPUT LOW vs. SINK CURRENT



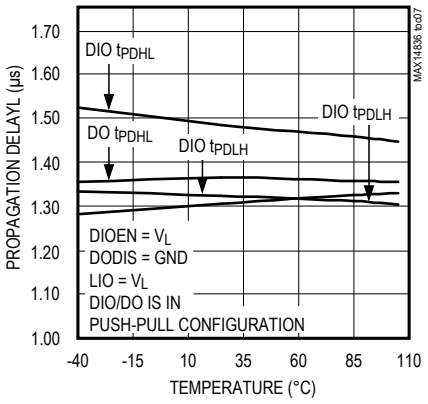
DIO/DO DRIVER OUTPUT VOLTAGE LOW vs. SUPPLY VOLTAGE



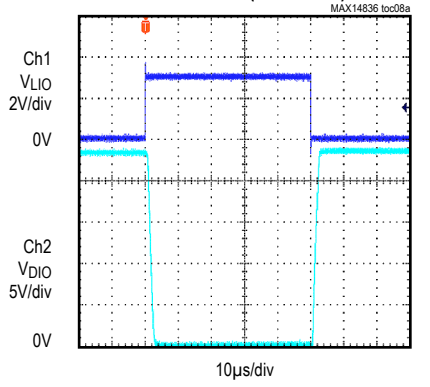
DIO/DO DRIVER OUTPUT VOLTAGE HIGH vs. SUPPLY VOLTAGE



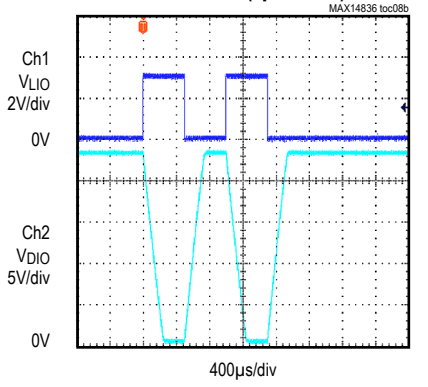
DIO/DO DRIVER PROPAGATION DELAY vs. TEMPERATURE



DIO DRIVER OUTPUT SWITCHING (1nF LOAD)



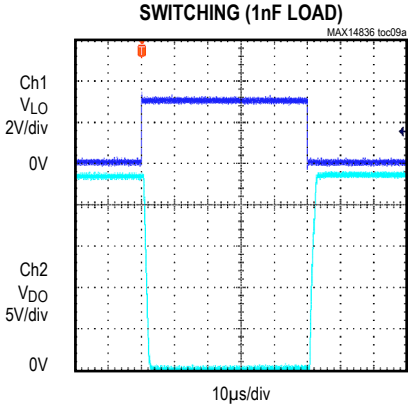
DIO DRIVER OUTPUT SWITCHING (3µF LOAD)



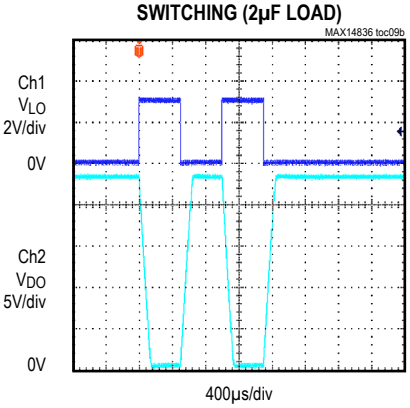
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, DIO and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

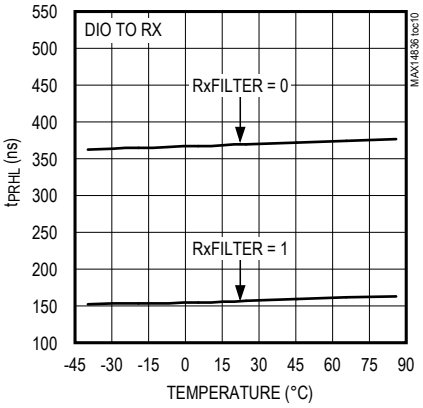
DO DRIVER OUTPUT SWITCHING (1nF LOAD)



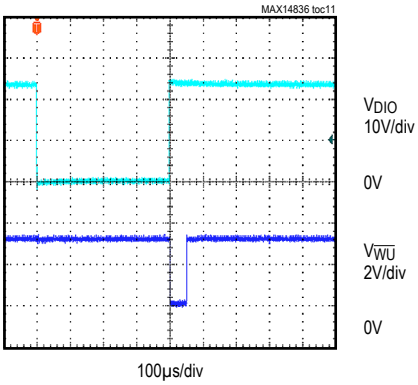
DO DRIVER OUTPUT SWITCHING (2µF LOAD)



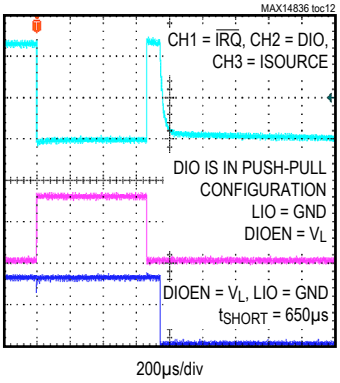
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



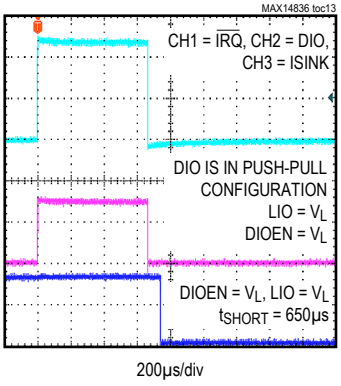
WAKE-UP DETECTION



DIO SHORT-CIRCUIT PROTECTION



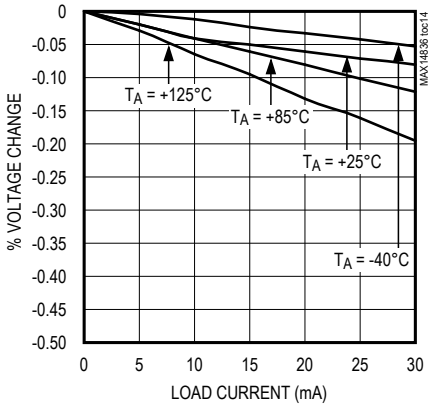
DIO SHORT-CIRCUIT PROTECTION



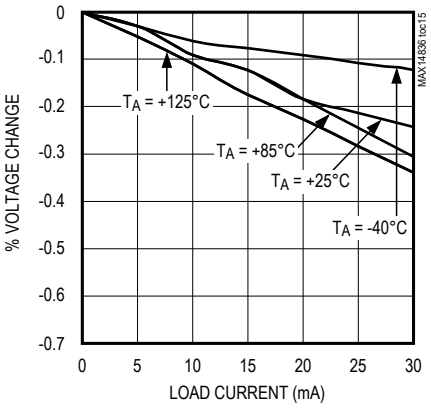
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, DIO and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

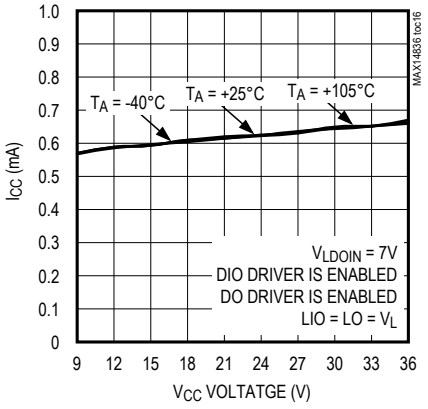
V_5 LOAD REGULATION



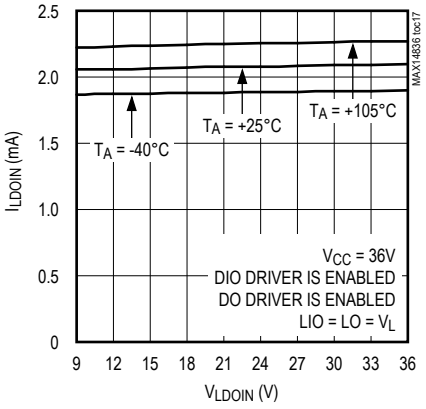
LDO33 LOAD REGULATION



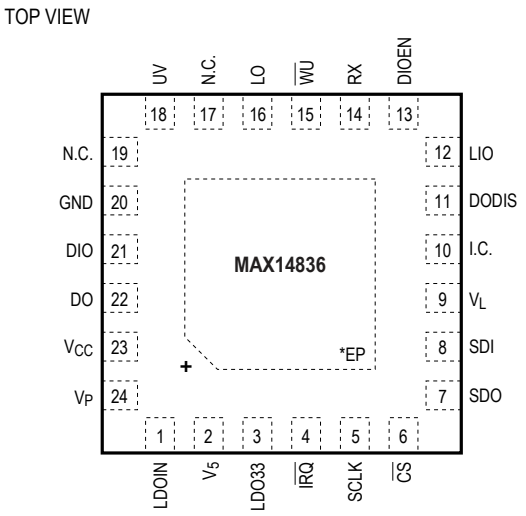
V_{CC} SUPPLY CURRENT vs. V_{CC} VOLTAGE



I_{LDOIN} SUPPLY CURRENT vs. I_{LDOIN} VOLTAGE



Pin Configuration



TQFN
(4mm × 4mm)

*CONNECT EXPOSED PAD TO GND.

Pin Description

PIN	NAME	FUNCTION
1	LDOIN	5V Linear Regulator Input. Bypass LDOIN to GND with a 0.1µF ceramic capacitor.
2	V_5	5V Power-Supply Input and 5V Linear Regulator Output. Bypass V_5 to GND with a 0.1µF ceramic capacitor for 10mA load capability. Add the recommended compensation network to increase the source capability to 30mA. See the *5V and 3.3V Linear Regulators* section for more information.
3	LDO33	3.3V Linear Regulator Output. Bypass LDO33 to GND with a 1µF ceramic capacitor.
4	$\overline{IRQ}$	Active-Low Interrupt Request Output. $\overline{IRQ}$ is a push-pull output referenced to V_L.
5	SCLK	SPI Clock Input
6	$\overline{CS}$	Active-Low SPI Chip-Select Input

Pin Description (continued)

PIN	NAME	FUNCTION
7	SDO	SPI Serial-Data Output
8	SDI	SPI Serial-Data Input
9	V_L	Logic-Level Supply Input. V_L defines the logic levels on all the logic inputs and outputs. Bypass V_L to GND with a 0.1µF ceramic capacitor.
10	I.C.	Internally Connected. Connect to V_L or leave unconnected. It is recommended to connect to V_L.
11	DODIS	DO Driver Disable Input. Drive DODIS low to enable the DO driver. Drive DODIS high to disable the DO drive.
12	LIO	DIO Input. The logic on the DIO output is the inverse logic level of the signals on the LIO inputs.
13	DIOEN	DIO Driver Enable. Drive DIOEN high to enable the DIO transmitter. DIOEN is referenced to VL
14	RX	DIO Output. RX is the inverse logic level of DIO. RX is always high when the RxDis bit in the DIOConfig register is set to 1.
15	$\overline{WU}$	Active-Low Wake-Up Output. $\overline{WU}$ is a push-pull output referenced to V_L. $\overline{WU}$ pulses low for 50µs (typ) when a valid wake-up pulse is detected on the DIO line.
16	LO	Logic Input of the DO Output. LO is the logic input that drives DO. LO is referenced to V_L.
17, 19	N.C.	Not Connected. Leave N.C. unconnected.
18	UV	Open-Drain Undervoltage Indicator Output. In case of an undervoltage, the UV open-drain transistor is off.
20	GND	Ground
21	DIO	Driver Input/Output. Drive DIOEN high to enable the DIO driver. The logic on the DIO output is the inverse logic level of the signals on the LIO. RX is the logic inverse of DIO. The DIO driver output level can be set by the LIO input or programmed by the Q bit. The level on DIO can be read by the RX output or the $\overline{Q}$Lvl bit.
22	DO	24V Logic-Level Digital Output. DO is the inverse logic level of the LO input and can be digitally-controlled through the DIOConfig register.
23	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
24	V_P	Protected 24V Supply Output. V_P is one diode drop below V_{CC}. V_P is reverse-polarity protected and can be used as a 24V protected supply to the sensor.
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX14836 is a dual-sensor driver. The device contains two 24V digital outputs. Two internal linear regulators generate common sensor voltages.

The device detects short-circuit wake-up conditions on the DIO line and generates a wake-up signal on the $\overline{WU}$ output. The DIO and DO drivers are independently-configurable to any one of three driver output types: push-pull, high-side (pnp), or low-side (npn).

The device is configured and monitored through an SPI™ interface. Extensive alarms are available through SPI.

24V Interface

The device features an IO transceiver interface capable of operating with voltages up to 36V. This is the 24V interface and includes the DIO input/output, the logic-level digital output (DO).

Configurable Drivers

The device features selectable push-pull, high-side (pnp), or low-side (npn) switching drivers at DIO and DO.

Set the DIO_N/P and DIO_PP bits in the DIOConfig register to select the driver mode for the DIO driver. When configured as a push-pull output, DIO switches between V_P and ground. Set the DIO_PP bit to 1 to select push-pull operation at DIO. Set the DIO_PP bit to 0 to configure the DIO output for open-drain operation. The DIO_N/P bit selects npn or pnp operation when DIO is configured as an open-drain output.

Set the DoN/P and DoPP bits in the DOConfig register to select the driver mode for the DO output. When configured as a push-pull output, DO switches between V_{CC} and ground. Set the DoPP bit to 1 for push-pull operation. The DoN/P bit selects npn or pnp operation when DO is configured as an open-drain output. Set the DoPP bit to 0 to select high-side or low-side operation at DO.

DIO Driver and Receiver

The DIOEN input enables the DIO driver. Drive DIOEN high to enable the DIO driver. Drive DIOEN low to disable the driver.

The device's DIO driver is specified for 200mA to drive current to large capacitive loads of up to 3µF and dynamic impedances like incandescent lamps.

The DIO receiver is always on. Disable the RX output through the RxDis bit in the DIOConfig register. Set the RxDis bit to 1 to set the RX output high. Set the RxDis bit to 0 for normal receive operation.

The DIO receiver has an analog lowpass filter to reduce high-frequency noise present on the line. Set the RxFilter bit in the DIOConfig register to 0 to set the filter corner frequency to 250kHz (typ). Set the RxFilter bit to 1 to set the corner frequency of the filter to 500MHz (typ). Noise filter is present on the DIO receiver and controlled simultaneously by the RxFilter bit.

DIO Fault Detection

The device registers a DIOFault condition when it detects a short circuit for longer than 650µs (typ). A short condition exists when DIO driver's V_{OH} or V_{OL} exceeds 2.8V (typ).

When a DIOFault error occurs, the DIOFault and DIOFaultInt bits are set, $\overline{IRQ}$ asserts, and the driver is turned off 650µs (typ) blanking time after the start of the fault condition.

When a short-circuit event occurs on DIO, the driver enters autoretry mode. In autoretry mode, the device periodically checks whether the short is still present and attempts to correct the driver output. Autoretry attempts last for 770µs (typ) and occur every 26ms (typ).

DO Fault Detection

The device registers a DoFault event when a short-circuit is present at the DO output for 440µs. A short condition exists when the DO driver's V_{OH} or V_{OL} exceeds the 2.8V (typ). When a short-circuit condition is detected, the DO driver enters autoretry mode. In autoretry mode, the device periodically checks whether the overcurrent is still present. Autoretry attempts last for 440µs (typ) and occur every 26ms (typ). When a DoFault error is detected, the DoFault and DoFaultInt bits are set, $\overline{IRQ}$ asserts, and the driver is turned off 440µs (typ) after the start of the DO faults.

Reverse-Polarity Protection

The device is protected against reverse-polarity connections on V_{CC}, DIO, DO, DI, and GND. Any combination of these pins can be connected to DC voltages up to 40V (max). A short to 40V results in a current flow of less than 500µA.

Ensure that the maximum voltage between any of these pins does not exceed 40V.

5V and 3.3V Linear Regulators

The device includes two internal regulators to generate 5V (V_5) and 3.3V (LDO33). LDO5 is specified for 10mA total external load current (i.e., LDO33 + V_5) when bypassed with a 0.1µF capacitor to ground. Add the compensation network shown in Figure 5 to draw up to 30mA of total external load current from the 5V LDO. LDO33 is specified at 20mA. The input of V_5 (LDOIN) can be powered from V_P, the protected 24V supply output, or to another voltage in the 7V to 36V range.

If the external circuits that are powered by the linear regulators require an input bypass capacitance larger than 100nF for 5V or 1µF for 3.3V, a compensation network must be added on V_5 and/or LDO33. The compensation network consists of a 10Ω series resistor and a capacitor equal to the value required by the external circuit, as shown in Figure 6. The capacitors C33 and C5 in Figure 6 represent the capacitance required by the external circuits. Figure 6 does not show any protection diodes for simplicity.

When the internal 5V LDO is not used, V_5 becomes the supply input for the internal analog and digital functions and, therefore, has to be supplied externally so that the MAX14836 operates normally. The 5V LDO can be disabled by connecting LDOIN to V_5. Apply an external voltage of 4.75V to 5.25V to V_5 when the LDO is disabled.

Use the LDO33Dis bit in the Mode register to disable LDO33. See the *Mode Register [R1, R0] = [1,1]* section for more information. V_5 and LDO33 are not protected against short circuits.

Power-Up

If V_L is connected to V5 or to LDO33, the DIO and DO driver outputs and the UV output are high-impedance when V_{CC}, V_5, V_L, and/or LDO33 voltages are below their respective undervoltage thresholds during power-up. If V_L is not connected to V_5 or to LDO33, V_L needs to be powered up before or simultaneously with V_5 or LDO33 in order to ensure that the DO output is high impedance at power-up. UV goes low and the drivers are enabled when all these voltages exceed their respective undervoltage-lockout thresholds.

The drivers are automatically disabled if V_{CC}, V_5, or V_L falls below its threshold.

Undervoltage Detection

The device monitors V_{CC}, V_5, V_L, and optionally LDO33 for undervoltage conditions. UV is high-impedance when any monitored voltage falls below its UVLO threshold.

V_{CC}, V_5, and V_L undervoltage detection cannot be disabled. When V_{CC} falls below the V_{CCUVLO} threshold, the UV24 and UV24Int bits are set, UV asserts high, and $\overline{IRQ}$ asserts low.

The SPI register contents are unchanged while V_5 is present, regardless of the state of V_{CC} and LDO33. The SPI interface is not accessible and $\overline{IRQ}$ is not available when UV is asserted due to a V_5 or V_L undervoltage event.

When the internal 3.3V LDO regulator voltage (V_{LDO33}) falls below the LDO33 undervoltage lockout threshold, the UV33Int bit in the Status register is set and $\overline{IRQ}$ asserts. UV asserts if the UV33En bit in the Mode register is set to 1.

The UV output deasserts once the undervoltage condition is removed. However, bits in the Status register and the $\overline{IRQ}$ output are not cleared until the Status register has been read.

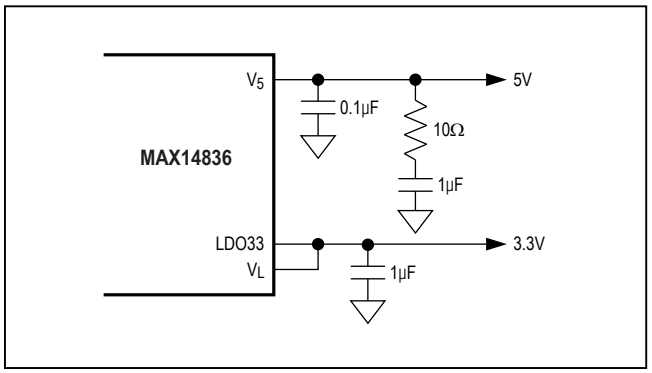


Figure 5. V_5 Compensation Network

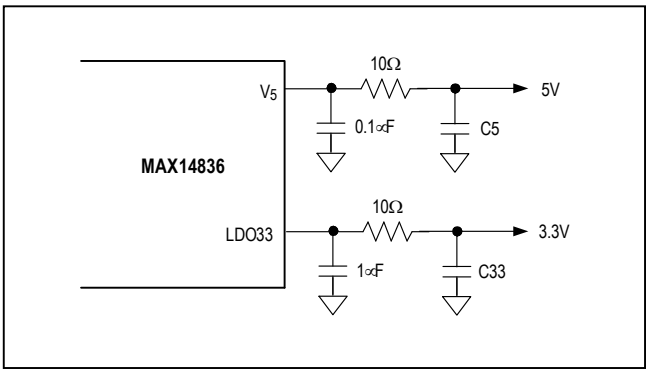


Figure 6. Larger Bypass Capacitance for Powering External Circuits

Wake-Up Detection

The device detects a wake-up condition on the DIO line in push-pull, high-side (pnp), or low-side (npn) operation modes. A wake-up condition is detected when the DIO output is shorted for 410µs (typ). $\overline{WU}$ pulses low for 50µs (typ) when the device detects a wake-up pulse on DIO (Figure 3).

Set the WuIntEn bit in the Mode register to set the WuInt bit in the Status register and generate an interrupt on $\overline{IRQ}$ when a wake-up pulse is detected. WuInt is set and $\overline{IRQ}$ asserts immediately after DIO is released when WuIntEn = 1.

Thermal Protection and Considerations

The internal LDOs and drivers can generate more power than the package for the devices can safely dissipate. Ensure that the driver and LDO loading is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{DIO} + P_{DO} + P_5 + P_{LDO33} + P_Q$$

where P_{DIO} is the power generated in the DIO driver, P_{DO} is the power dissipated by the DO driver, P_5 and P_{LDO33} are the power generated by the LDOs, P_Q is the quiescent power generated by the MAX14836.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mW) due to the DIO driver:

$$P_{DIO} = [I_{DIO}(max)] \times [V_{O\_}(max)]$$

where $V_{O\_}$ = the larger of V_{OL_DIO} and V_{OH_DIO}

(See the *Typical Operating Characteristics* on page 11.)

Calculate the internal power dissipation of the DO driver using the following equation:

$$P_{DO} = [I_{DO}(max)] \times [V_{O\_}(max)]$$

Calculate the power dissipation in the 5V LDO (V_5) using the following equation:

$$P_5 = (V_{LDOIN} - V_5) \times I_5$$

where I_5 $V_{O\_}$ includes the I_{LDO33} current sourced from LDO33.

Calculate the power dissipated in the 3.3V LDO (LDO33) using the following equation:

$$P_{LDO33} = 1.7V \times I_{LDO33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_Q = I_{CC}(max) \times V_{CC}(max)$$

Overtemperature Warning

Bits in the Status and Mode registers are set when the temperature of the device exceeds +125°C (typ). The OTempInt bit in the Status register is set and $\overline{IRQ}$ asserts when the OTemp bit in the Mode register is set. Read the Status register to clear the OTempInt bit and $\overline{IRQ}$.

The OTemp bit is cleared when the die temperature falls to +102°C.

The device continues to operate normally unless the die temperature reaches the +165°C thermal-shutdown threshold, when the device enters thermal shutdown.

Thermal Shutdown

All regulators and the DIO and DO output drivers are automatically switched off when the internal die temperature exceeds the +165°C (typ) thermal-shutdown threshold. SPI communication is available, and register content is maintained, during a thermal shutdown event.

Register Functionality

The devices have four 8-bit-wide registers for configuration and monitoring (Table 1).

Table 1. Register Summary

REGISTER	R1	R0	D7	D6	D5	D4	D3	D2	D1	D0	READ/ WRITE
Status	0	0	WuInt	DoFaultInt	—	$\overline{Q}$Lvl	DIOFaultInt	UV33Int	UV24Int	OTempInt	Read only
DIOConfig	0	1	RxFilter	—	DIO_N/P	DIO_PP	DIODEn	Q	RxDis	—	R/W
DOConfig	1	0	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	—	—	R/W
Mode	1	1	RST	WuIntEn	DoFault	DIOFault	UV24	OTemp	UV33En	LDO33Dis	R/W

R1/R0 = Register address.

— Writing to registers has no effect.

Status Register [R1, R0] = [0,0]

BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	WuInt	DoFaultInt	ResVD	$\overline{Q}$Lvl	DIOFaultInt	UV33Int	UV24Int	OTempInt
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	X	X	0	0	0	0
RESET UPON READ	Yes	Yes	No	No	Yes	Yes	Yes	Yes

X = Unknown. These bits are dependent on the DIO input.
ResVD = reserved

The Status register reflects the logic levels of DIO and shows the source of interrupts that DIOFault cause an $\overline{IRQ}$ hardware interrupt. The $\overline{IRQ}$ interrupt is asserted when an alarm condition (OTemp, UV33, UV24, DIOFault, DoFault, WuI) is detected. All bits in the Status register are read-only. The interrupt bits return to the default state after the Status register is read. If a DIO or DO fault condition persists, the associated interrupt bits are immediately set after the Status register is read.

BIT	NAME	DESCRIPTION
D7	WuInt	**Wake-Up Interrupt Request.** WuInt is set when a wake-up request pulse is detected on DIO and the WuIntEn bit in the Mode register is set. $\overline{IRQ}$ asserts when WuInt is set to 1. Read the Status register to clear the WuInt bit and deassert $\overline{IRQ}$.
D6	DoFaultInt	**DO Fault Interrupt.** DoFaultInt interrupt bit and DoFault bit (in the Mode register) are set when a fault condition occurs on the DO driver output. The device registers a fault condition when a short-circuit or voltage fault is detected on DO (see the *DO Fault Detection* section for more information). $\overline{IRQ}$ asserts when DoFaultInt is 1. Read the Status register to clear the DoFaultInt bit and deassert $\overline{IRQ}$. If the DoFault is still present during the next autoretry cycle, the DoFaultInt bit and $\overline{IRQ}$ is set again.
D5	ResVD	Reserved

BIT	NAME	DESCRIPTION
D4	$\overline{Q}$Lvl	**DIO Logic Level.** The $\overline{Q}$Lvl bit is the inverse of the logic level at DIO. $\overline{Q}$Lvl is 1 when the DIO input level is low (< 5.2V) and is 0 when the DIO logic level is high (> 8V) (Table 3). $\overline{Q}$Lvl remains active when the DIO receiver is disabled (RxDis = 1). $\overline{Q}$Lvl does not affect $\overline{IRQ}$. $\overline{Q}$Lvl is not changed when the Status register is read.
D3	DIOFaultInt	**DIO Fault Interrupt.** The DIOFaultInt interrupt bit and DIOFault bit (in the Mode register) are set when a short circuit or voltage fault occurs on the DIO driver output (see the *DIO Fault Detection* section for more information). $\overline{IRQ}$ asserts when DIOFault is 1. Read the Status register to clear the DIOFaultInt bit and deassert $\overline{IRQ}$. If DIO fault is still present during the next autoretry cycle, the DIOFault bit and $\overline{IRQ}$ is set again.
D2	UV33Int	**Internal 3.3V LDO (LDO33) Undervoltage Warning.** Both the UV33Int interrupt bit and the UV33En bit (in the Mode register) are set when V_{LDO33} falls below the 2.4V LDO33 undervoltage threshold. If UV33En is set in the Mode register, $\overline{IRQ}$ asserts low when the UV33Int bit is 1. Read the Status register to clear the UV33Int bit and deassert $\overline{IRQ}$. Set the UV33En bit to 1 in the Mode register to enable undervoltage monitoring for UV33Int. When enabled, UV asserts high when the UV33Int bit is 1. UV deasserts when V_{LDO33} rises above the LDO33 undervoltage threshold.
D1	UV24Int	**V_{CC} Undervoltage Interrupt.** The UV24Int interrupt bit and the UV24 bit (in the Mode register) are set when the V_{CC} voltage falls below the 6V undervoltage threshold. $\overline{IRQ}$ asserts low when the UV24Int bit is 1. Read the Status register to clear the UV24Int bit and deassert $\overline{IRQ}$. V_{CC} undervoltage detection cannot be disabled.
D0	OTempInt	**Overtemperature Warning.** The OTempInt interrupt bit and the OTemp bit (in the Mode register) are set when a high-temperature condition is detected by the devices. OTemp is set when the temperature of the die exceeds +125°C (typ). OTempInt is set and $\overline{IRQ}$ asserts when the OTemp bit is 1. The OTempInt bit is cleared and $\overline{IRQ}$ deasserts when the Status register is read. Once cleared, OTempInt is not reset if the die temperature remains above the thermal-warning threshold and does not fall below +102°C.

Table 2. DO Driver Enable, Disable

DODIS Pin	DOEn Bit	DO State
Low	x	Enabled
High	0	Disabled
High	1	Enabled

X = Don't care.

Table 3. $\overline{Q}$Lvl and RX Output

V_{DIO} (V)	$\overline{Q}$Lvl BIT	RX OUTPUT
< 5.2	1	High
> 8	0	Low

DIOConfig Register [R1, R0] = [0,1]

BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RxFilter	—	DIO_N/P	DIO_PP	DIODEn	Q	RxDis	—
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0

Use the DIOConfig register to control the DIO driver and receiver parameters. All bits in the DIOConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	RxFilter	**DIO Receiver Filter Control.** The DIO receiver has an all-analog lowpass filter to reduce high-frequency noise on the receiver input. Set the RxFilter bit to 0 to set the filter corner frequency to 500kHz. Set the RxFilter bit to 1 to set the filter corner frequency to 1MHz. Noise filters on C/Q and DI are controlled simultaneously by the RxFilter bit.
D6	—	**Writing to register has no effect.**
D5	DIO_N/P	**DIO Driver npn/pnp Mode.** The DIO_N/P bit selects between low-side (npn) and high-side (pnp) modes when the DIO driver is configured as an open-drain output (DIO_PP = 0). Set DIO_N/P to 1 to configure the driver for low-side (npn) operation. Set DIO_N/P to 0 for high-side (PNP) operation.
D4	DIO_PP	**DIO Driver Push-Pull Operation.** Set DIO_PP to 1 to enable push-pull operation on the DIO driver. The DIO output is open-drain when DIO_PP is 0.
D3	DIODEn	**DIO Driver Enable/Disable.** Set the DIODEn bit to 1 to enable the DIO driver. Set DIODEn to 0 for hardware (DIOEN) control. See Table 4.
D2	Q	**DIO Driver Output Logic.** The Q bit can be used to program the C/Q output driver through software. The DIO driver must be enabled and LIO must be high to control the DIO driver through the Q bit (Figure 7). DIO has the same logic polarity as the Q bit. Set the Q bit to 0 to control the DIO driver with LIO. The DIO driver output state depends on the DIO_PP and DIO_N/P bits as shown in Table 5. Note that Table 5 assumes that the C/Q driver is enabled (DIOEN = V_L or DIODEn = 1).
D1	RxDis	**DIO Receiver Enable/Disable.** Set the RxDis bit to 1 to disable the DIO receiver. The RX output is high when RxDis is 1.
D0	—	**Writing ro register has no effect.**

Table 4. DIODEn and DIOEN DIO Driver Control

DIODEn	DIOEN	DIO DRIVER
0	Low	Disabled
X	High	Enabled
1	X	Enabled

X = Don't care.

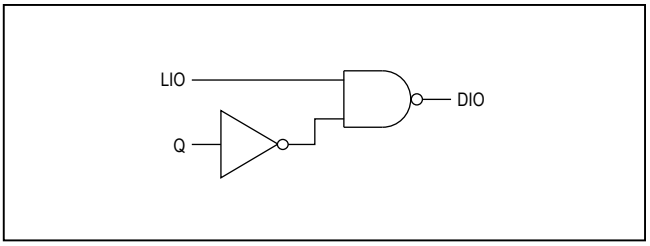


Figure 7. Equivalent DIO Logic

Table 5. DIO Driver Output State

LIO (SEE NOTE)	Q	DIO_PP	DIO_N/P	DIO CONFIGURATION	DIO STATE
High	1	0	0	pnp, open-drain	On, DIO is high
High	0	0	0	pnp, open-drain	Off, DIO is high-impedance
High	1	0	1	npn, open-drain	Off, DIO is high-impedance
High	0	0	1	npn, open-drain	On, DIO is low
High	1	1	X	Push-pull	High
High	0	1	X	Push-pull	Low

Note: *LIO = V_L.*

X = Don't care.

DOConfig Register [R1, R0] = [1,0]

BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	—	—
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0

Use the DOConfig register to control DO interface. All bits in the DOConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	DoInv	**DO Output Polarity.** Set the DoInv bit to 1 to invert the logic of the DO output. This bit also works in conjunction with the DoAv (Table 6). DO tracks the LIO input with the opposite polarity when both the DoAv and DoInv bits are set.
D6	DoAv	**DO Antivalent Operation.** Set the DoAv bit to 1 to enable antivalent output operation on DO. DO tracks the LIO and input (and the Q bit) when DoAv is 1 (Table 6). The LO input and the DoBit are ignored when the DoAv bit is 1.
D5	DoN/P	**DO Driver npn/pnp Operation.** The DoN/P bit selects between low-side (npn) and high-side (pnp) modes when the DO driver is configured as an open-drain output (DoPP = 0). Set DoN/P to 1 to configure the driver for low-side (npn) operation. Set DoN/P to 0 for high-side (pnp) operation.
D4	DoPP	**DO Driver Push-Pull Operation.** Set the DoPP bit to 1 to configure the DO driver output for push-pull operation. DO is an open-drain output when DoPP is 0.
D3	DoEn	**DO Driver Enable/Disable.** Set the DoEn bit to 1 to enable the DO driver. The DO driver is high-impedance when DoEn is 0.
D2	DoBit	**DO Driver Output Logic.** The DoBit bit can be used to program the DO output driver through software. Drive LO high to activate DoBit programming (Figure 8). The DO output state is given in Table 7. Note that Table 7 assumes that the DoInv bit is 0.
D1	—	**Writing to register has no effect.**
D0	—	**Writing to register has no effect.**

Table 6. DoAv and DoInv Operation

DoAv	DoInv	LIO (Note 1)	LO (Note 1)	DO (Note 2)	DIO (Note 2)
0	0	Low	Low	High	High
0	0	Low	High	Low	High
0	0	High	Low	High	Low
0	0	High	High	Low	Low
0	1	Low	Low	Low	High
0	1	Low	High	High	High
0	1	High	Low	Low	Low
0	1	High	High	High	Low
1	0	Low	Low	Low	High
1	0	Low	High	Low	High
1	0	High	Low	High	Low
1	0	High	High	High	Low
1	1	Low	Low	High	High
1	1	Low	High	High	High
1	1	High	Low	Low	Low
1	1	High	High	Low	Low

Note 1: Low is when V_{LIO}, OR V_{LO} = 0V; high is when V_{LIO}, V_{TXQ}, or V_{LO} = V_L.

Note 2: Low is when DIO or DO < 5.2V; high is when DIO or DO > 8V.

Table 7. DO Output Programmed by DoBit

LO	DoBit	DoPP	DoN/P	DO CONFIGURATION	DO STATE
High	0	1	X	Push-pull	Low
High	1	1	X	Push-pull	High
High	0	0	0	pnp	Off, DO is high-impedance
High	1	0	0	pnp	On, DO is high
High	0	0	1	npn	On, DO is low
High	1	0	1	npn	Off, DO is high-impedance
Low	X	X	X	See Table 6	See Table 6

X = Don't care.

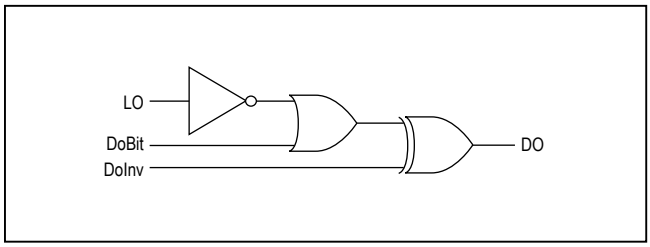


Figure 8. Equivalent DO Logic

Mode Register [R1, R0] = [1,1]

BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	WuIntEn	DoFault	DIOFault	UV24	OTemp	UV33En	LDO33Dis
READ/WRITE	R/W	R/W	R	R	R	R	R	R/W
POR STATE	0	0	0	0	0	0	0	0

Use the Mode register to reset the MAX14836 and manage the 3.3V LDO. The Mode register has bits that represent the current status of fault conditions. When writing to the Mode register, the contents of the fault indication bits (bits 2 to 5) do not change.

BIT	NAME	DESCRIPTION
D7	RST	**Register Reset.** Set RST to 1 to reset all registers to their default power-up state. Then set RST to 0 for normal operation. The Status register is cleared and $\overline{IRQ}$ deasserts (if asserted) when RST = 1. Interrupts are not generated while RST = 1.
D6	WuIntEn	**Wake-Up Interrupt Enable.** Set WuIntEn to 1 to enable wake-up interrupt generation. When WuIntEn is set, the WuInt bit in the Status register is set and $\overline{IRQ}$ asserts when a valid wake-up condition is detected. The DIO driver must be enabled for wake-up detection. The state of WuIntEn does not affect the WU output. See the *Wake-Up Detection* section for more information.
D5	DoFault	**DO Fault Status.** The DoFault bit is set when a short-circuit or voltage fault occurs at the DO driver output (see the *DO Fault Detection* section for more information). The DoFault and DoFaultInt bits are both set when a fault occurs on DO. In every autoretry fault-detect cycle, the DOFault bit is 0 during the blanking time. DoFault is cleared when the fault is removed.
D4	DIOFault	**DIO Fault Status.** The DIOFault bit is set when a short-circuit or voltage fault occurs at the C/Q driver output (see the *DIO Fault Detection* section for more information). The DIOFault and DIOFaultInt bits are both set when a fault occurs on DIO. In every autoretry fault-detect cycle, the DOFault bit is 0 during the blanking time. In every autoretry fault-detect cycle, the DIOFault bit is 0 during the blanking time. DIOFault is cleared when the fault is removed.
D3	UV24	**V_{CC} Undervoltage Condition.** Both the UV24 and the UV24Int bits are set when V_{CC} falls below V_{CCUVLO}. UV24 is cleared when V_{CC} rises above the V_{CC} threshold. V_5 must be present for V_{CC} undervoltage monitoring
D2	OTemp	**Temperature Warning.** The OTemp bit is set when a high-temperature condition occurs on the devices. Both the OTempInt interrupt in the Status register and the OTemp bit are set when the junction temperature of the die rises to above +125°C (typ). The OTemp bit is cleared when the junction temperature falls below +102°C (typ).
D1	UV33En	**LDO33 UV Enable.** Set the UV33En bit to 1 to assert the UV output when LDO33 voltage falls below the 2.4V (typ) undervoltage lockout threshold. The UV33En bit does not affect the UV33Int bit in the Status register; $\overline{IRQ}$ asserts when V_{LDO33} falls below $V_{LDO33UVLO}$ regardless of the state of UV33En.
D0	LDO33Dis	**LDO33 Enable/Disable.** Set LDO33Dis to 1 to disable the 3.3V linear regulator (LDO33).

SPI Interface

The device communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs—clock (SCLK), chip-select ($\overline{CS}$), and data in (SDI)—and one output, data out (SDO). The maximum SPI clock rate for the device is 12MHz. The SPI interface complies with clock polarity CPOL = 0 and clock phase CPHA = 0 (see Figure 9 and Figure 10).

The SPI interface is not available when V_5 or V_L are not present.

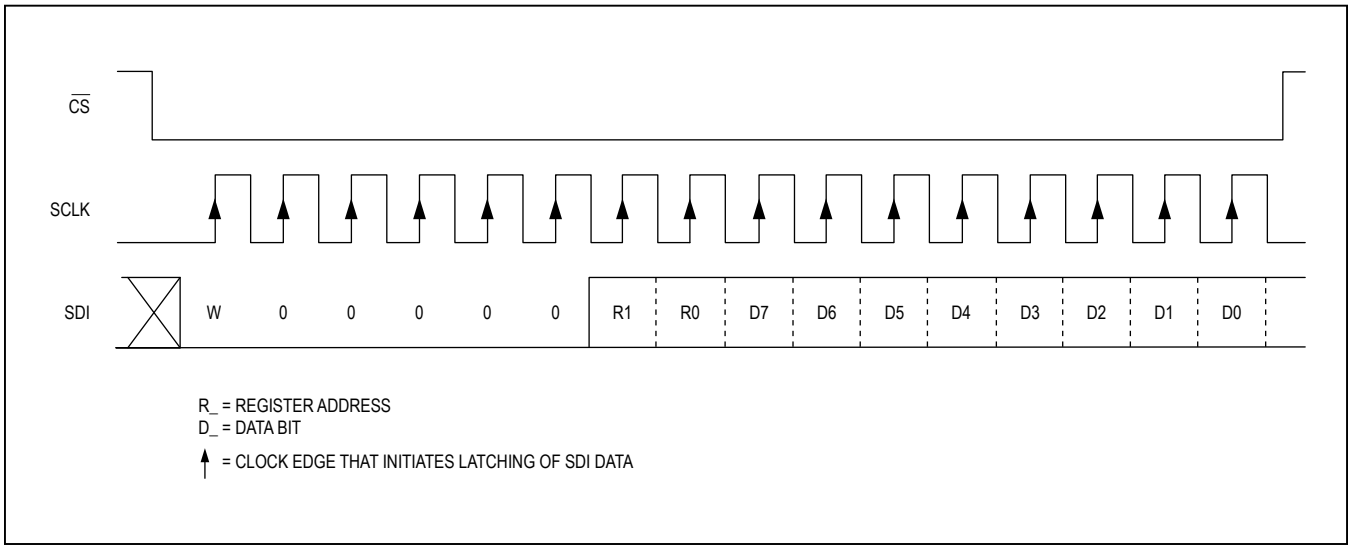


Figure 9. SPI Write Cycle

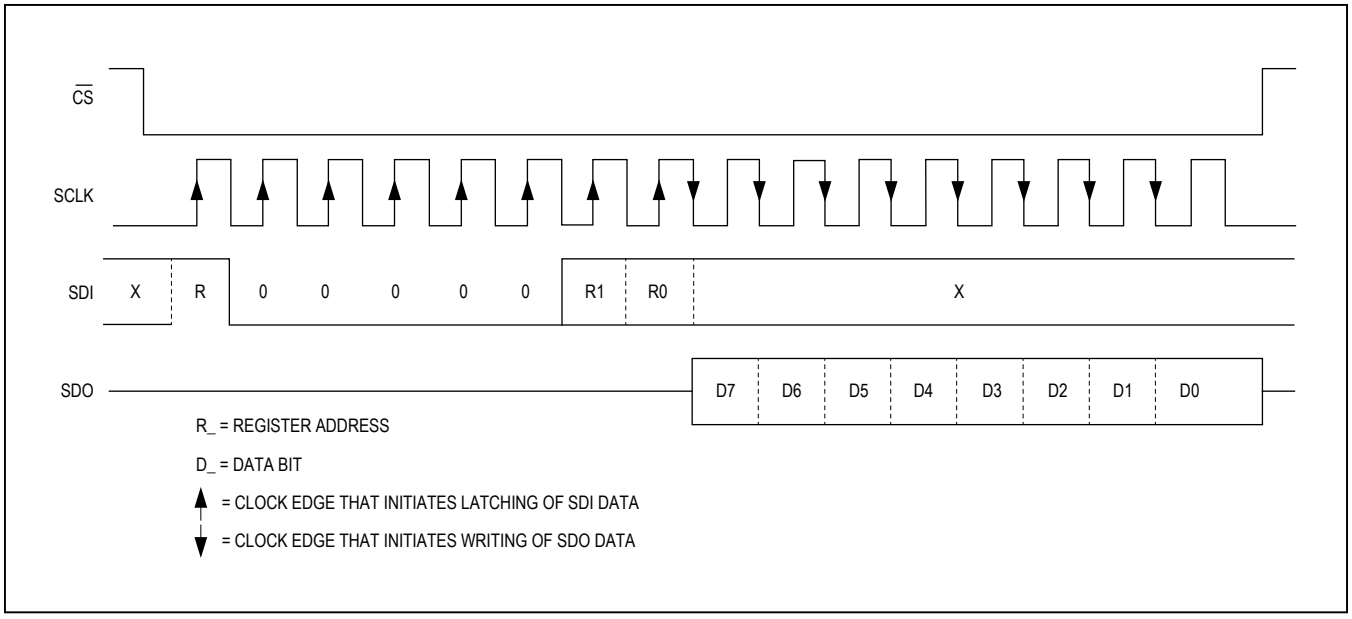


Figure 10. SPI Read Cycle

Applications Information

UART Interfacing

The logic levels of the microcontroller interface I/Os (LIO, DODIS, DIOEN, and RX) are defined by V_L.

Transient Protection

Inductive load-switching, surges, and bursts create high transient voltages. DIO and DO should be protected against high overvoltage and undervoltage transients. Positive voltage transients on DIO and DO must be limited to +55V relative to GND and negative voltage transients must be limited to -55V (relative to V_{CC}) on DO. Figure 11 shows suitable protection using TVS diodes to meet both the IEC 61000-4-2 ESD and IEC 61000-4-5 surge testing. Other protection schemes may also be suitable.

The external TVS diodes can be biased via the internal VP diode, or by using an external diode, as shown in Figure 12. The scheme shown in Figure 12 has the benefit of not supplying the sensor power supply when the external 24V L+ supply is not present and an external voltage is applied to DIO or DO.

The device has to be protected against transients that occur during hot-plugging of the L+ sensor supply (VCC input). This is achieved by placing a 10Ω resistor with 1µF capacitor before LDOIN and connecting an RC between the sensor supply input and the VCC pin, as shown in Figure 11. The RC time constant of the filter on VCC should be larger or equal to 0.8µs. In case that V_L is supplied by V_5 and the bypass capacitor on V_5 is 100nF, the 10Ω resistor in series with LDOIN is not needed.

Optional External Powering

The MAX14836 is powered by V_{CC} and V_5. V_L is a reference voltage input to set the logic levels of the microcontroller interface. The logic and SPI interface are operational when V_5 and V_L are present even if V_{CC} is not present.

The V_P output provides a reverse-polarity-protected voltage one diode drop below V_{CC} and can be used for supplying external circuitry, like power supplies. The current drawn from V_P cannot exceed 50mA. Be aware that capacitance on V_P can cause transient currents at power-up equal to C x dV_{CC}/dt.

V_5 is typically powered by the internal 5V regulator, but can alternatively be powered by an external 5V regulator. When powering V_5 externally, connect LDOIN to V_5 (Figure 12). This configuration disables operation of the internal 5V regulator and reduces power consumption.

When an external 5V regulator is used to power V_5, the V_5 bypass capacitance is determined by that regulator, and is not limited to 100nF.

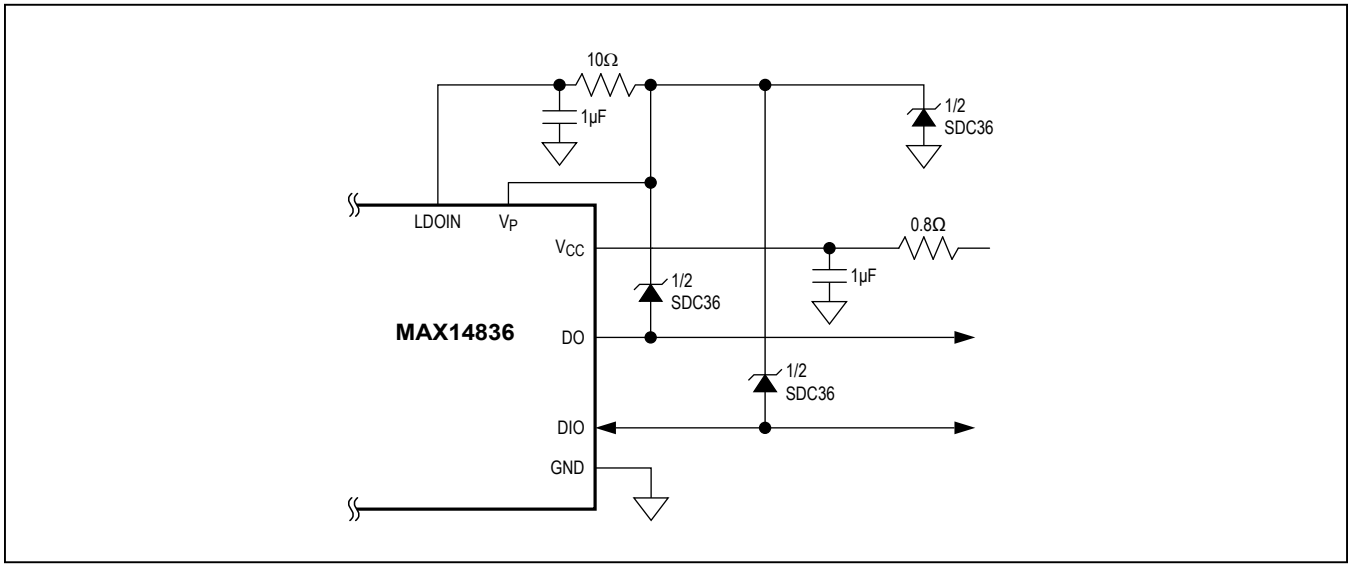


Figure 11. MAX14836 Operating Circuit with TVS Protection

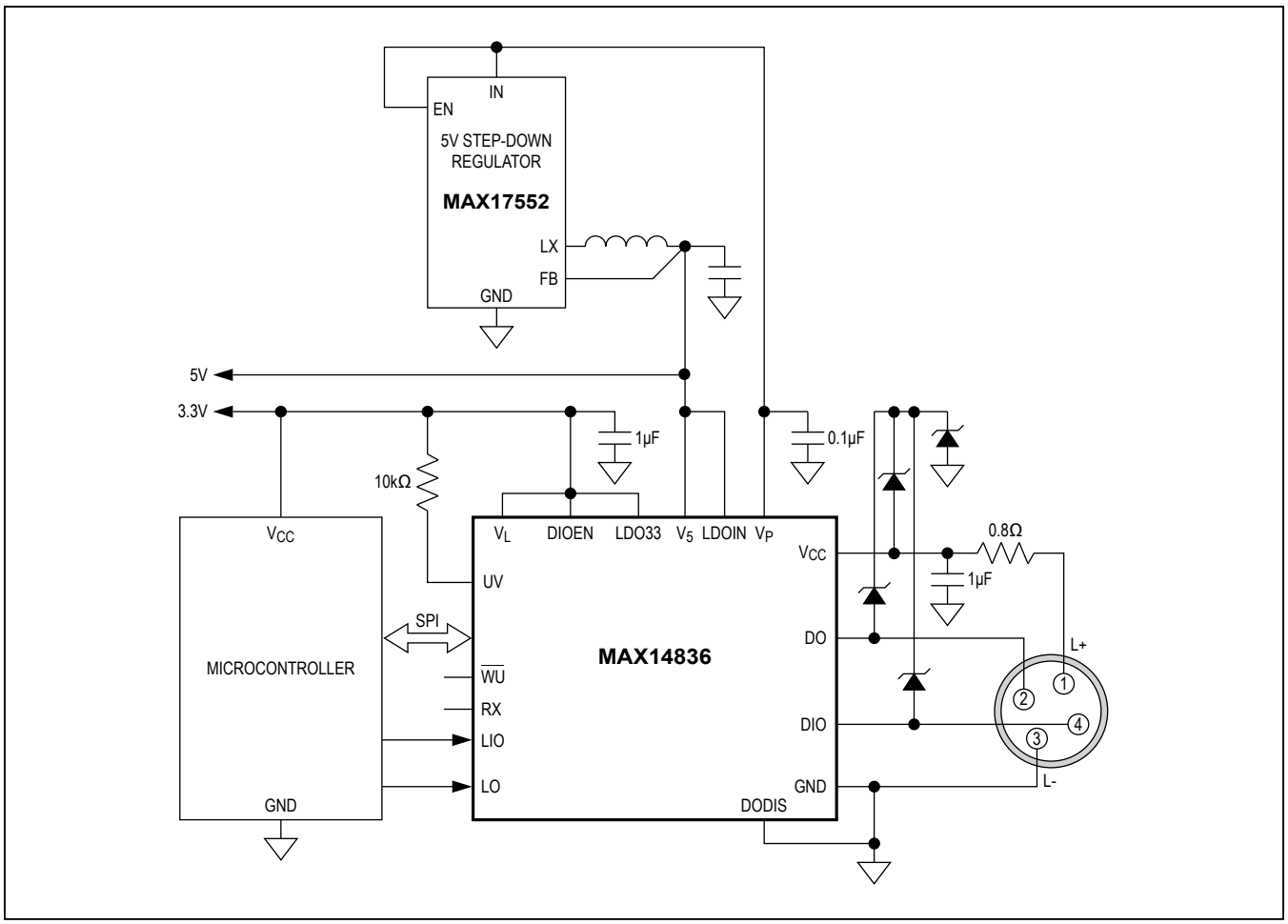


Figure 12. Using an Optional External Supply to Power the MAX14836

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14836GTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	5/14	Added RC filter need and application information and circuit for larger LDO bypass capacitor.	7
2	9/14	Updated *Features and Benefits* section, *Typical Application Circuit*, *AC Electrical Characteristics* table, *Power-Up* section, and corrected figure references	1, 7, 16, 20, 23

