# Z8430/Z84C30 NMOS/CMOS Z80 ®CTC Counter/Timer Circuit

## FEATURES

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors. (1.5 mV @ 1.5V)
- **NMOS version for** cost sensitive **performance solutions.**
- **CMOS version for the designs** requiring low power consumption
- **NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz.**
- CMOS Z84C3006 - DC to 6.17 MHz, Z84C3008 - DC to 8 MHz, Z84C3010 - DC to 10 MHz
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- **6 MHz version supports 6.144 MHz CPU clock operation.**

## GENERAL DESCRIPTION

**The Z80 CTC, hereinafter referred to as Z80 CTC or CTC, four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.**

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

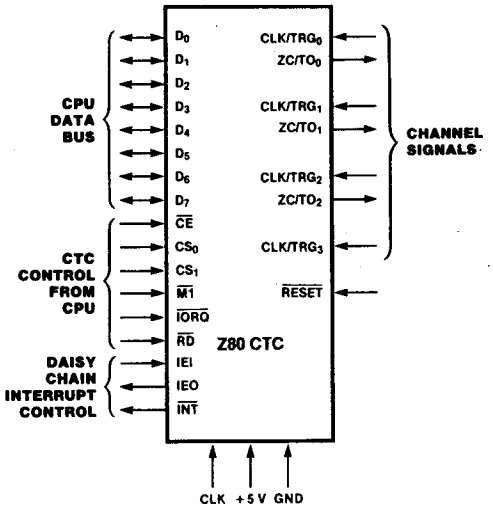



**Figure 1. Pin Functions**

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

**The Z80 CTC requires a single +5%V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin** LOFP **(Figures 2a, 2b, and 2c). Note that the** LOFP **package is only available for CMOS versions.**

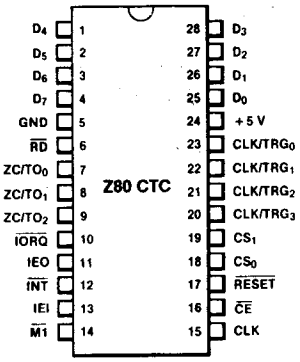



**Figure 22a. Pin Assignments**

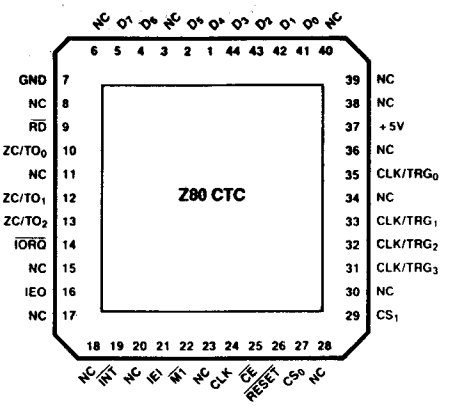



**Figure 2b. 44-pin Chip Carrier, Pin Assignments**

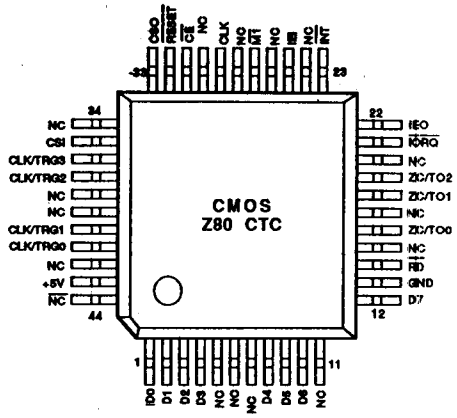



Figure 2C. 44-Pin LQFP Pin Assignments

## FUNCTIONAL DESCRIPTION

The Z80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

**The timer mode determines time intervals as small as 2 µs(8 MHz), 3 µs (6 MHz), or 4 µs (4MHz) without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.**

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256), and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count. The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output; interrupt request is the only output available from Channel 3.

The second output is Interrupt Request ($\overline{INT}$), which occurs if the channel has its interrupt enabled during programming. When the Z80 CPU acknowledges Interrupt Request, the Z80 CTC places an interrupt vector on the data bus.

The four channels of the Z80 CTC are fully prioritized and fit into four contiguous slots in a standard Z80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

## INTERNAL STRUCTURE

The CTC has four major elements, as shown in Figure 3.

- CPU bus I/O
- Channel control logic
- Interrupt logic
- Counter/timer circuits

**CPU Bus I/O.** The CPU bus I/O circuit decodes the address inputs, and interfaces the CPU data and control signals to the CTC for distribution on the internal bus.

**Internal Control Logic.** The CTC internal control logic controls overall chip operating functions such as the chip enable, reset, and read/write logic.

**Interrupt Logic.** The interrupt control logic ensures that the CTC interrupts interface properly with the Z80 CPU interrupt system. The logic controls the interrupt priority of the CTC as a function of the IEI signal. If IEI is High, the CTC has priority. During interrupt processing, the interrupt logic holds IEO Low, which inhibits the interrupt operation on lower priority devices. If the IEI input goes Low, priority is relinquished and the interrupt logic drives IEO Low.

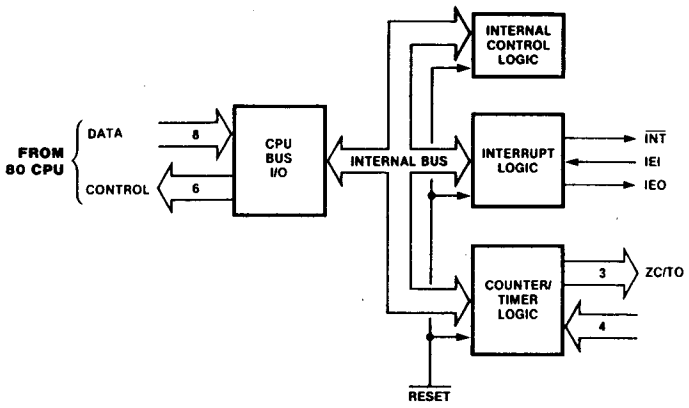



**Figure 3. Functional Block Diagram**

If a channel is programmed to request an interrupt, the interrupt logic drives IEO Low at the zero count, and generates an $\overline{INT}$ signal to the Z80 CPU. When the Z80 CPU responds with interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$), then the interrupt logic arbitrates the CTC internal priorities, and the interrupt control logic places a unique interrupt vector on the data bus.

If an interrupt is pending, the interrupt logic holds IEO Low. When the Z80 CPU issues a Return From Interrupt (RETI) instruction, each peripheral device decodes the first byte ($ED_{16}$). If the device has a pending interrupt, it raises IEO (High) for one $\overline{M1}$ cycle. This ensures that all lower priority devices can decode the entire RETI instruction and reset properly.

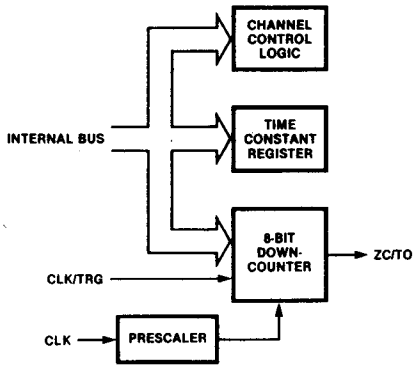



**Figure 4. Counter/Timer Block Diagram**

**Counter/Timer Circuits.** The CTC has four independent counter/timer circuits, each containing the logic shown in Figure 4.

**Channel Control Logic.** The channel control logic receives the 8-bit channel control word when the counter/timer channel is programmed. The channel control logic decodes the control word and sets the following operating conditions:

- Interrupt enable (or disable)
- Operating mode (timer or counter)
- Timer mode prescaler factor (16 or 256)
- Active slope for CLK/TRG input
- Timer mode trigger (automatic or CLK/TRG input)
- Time constant data word to follow
- Software reset

**Time Constant Register.** When the counter/timer channel is programmed, the time constant register receives and stores an 8-bit time constant value, which can be anywhere from 1 to 256 (0 = 256). This constant is automatically loaded into the down-counter when the counter/timer channel is initialized, and subsequently after each zero count.

**Prescaler.** The prescaler, which is used only in timer mode, divides the system clock frequency by a factor of either 16 or 256. The prescaler output clocks the down-counter during timer operation. The effect of the prescaler on the down-counter is a multiplication of the system clock period by 16 or 256. The prescaler factor is programmed by bit 5 of the channel control word.

**Down-Counter.** Prior to each count cycle, the down-counter is loaded with the time constant register contents. The counter is then decremented one of two ways, depending on operating mode:

- By the prescaler output (timer mode)
- By the trigger pulses into the CLK/TRG input (counter mode)

Without disturbing the down-count, the Z80 CPU can read the count remaining at any time by performing an I/O read operation at the port address assigned to the CTC channel. When the down-counter reaches the zero count, the ZC/TO output generates a positive-going pulse. When the interrupt is enabled, zero count also triggers an interrupt request signal ($\overline{INT}$) from the interrupt logic.

## PROGRAMMING

Each Z80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 1 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed to Channel 0, and identified by a 0 in bit 0.

**Addressing.** During programming, channels are addressed with the channel select pins $CS_1$ and $CS_2$. A 2-bit binary code selects the appropriate channel as shown in the following table.

| Channel | $CS_1$ | $CS_0$ |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**Reset.** The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and $D_0$-$D_7$ go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits $D_1$ and $D_2$ set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if $D_3 = 0$, operation is triggered automatically when the time constant word is loaded.

**Channel Control Word Programming.** The channel control word is shown in Figure 5. It sets the modes and parameters described below.

*Interrupt Enable.* $D_7$ enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

*Mode.* $D_6$ selects either timer or counter operating mode.

*Prescaler Factor. (Timer Mode Only).* $D_5$ selects factor—either 16 or 256.

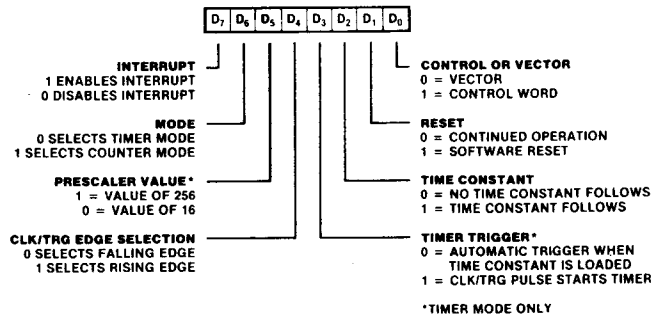



**Figure 5. Channel Control Word**

*Clock/Trigger Edge Selector.* $D_4$ selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

*Timer Trigger (Timer Mode Only).* $D_3$ selects the trigger mode for timer operation. When $D_3$ is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse ($T_2$) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When $D_3$ is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse ($T_2$) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede $T_2$ by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle ($T_3$).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

*Time Constant.* A 1 in $D_2$ indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in $D_2$ indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with $D_2$ set.

*Software Reset.* Setting $D_1$ to 1 causes a software reset, which is described in the Reset section.

*Control Word.* Setting $D_0$ to 0 identifies the word as a control word.

**Time Constant Programming.** Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that $00_{16}$ is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (CLK)
- The prescaler factor (P), which multiplies the interval by either 16 or 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of CLK x P x T. The minimum timer resolution is 16 x CLK (4μs with a 4MHz clock). The maximum timer interval is 256 x CLK x 256 (16.4 ms with a 4MHz clock). For longer intervals timers may be cascaded.

**Interrupt Vector Programming.** If the Z80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z80 CPU. To do so, the Z80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z80 CTC Channel 0. Note that $D_0$ of the vector word is always zero, to distinguish the vector from a channel control word. $D_1$ and $D_2$ are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

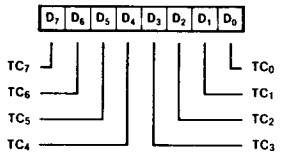



**Figure 6. Time Constant Word**

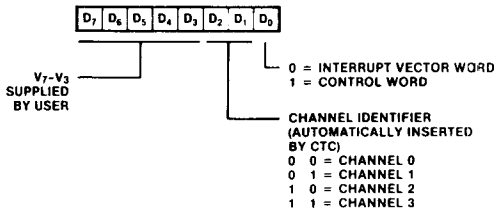



**Figure 7. Interrupt Vector Word**

## PIN DESCRIPTION

**$\overline{CE}$.** *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the downcounter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

**CLK.** *System Clock* (input). Standard single-phase Z80 system clock.

**$CLK/TRG_0$-$CLK/TRG_3$.** *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z80 CTC channels. In counter mode, every active edge on this pin decrements the downcounter. In timer mode, an active edge starts the timer.

**$CS_0$-$CS_1$.** *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to $A_0$ and $A_1$).

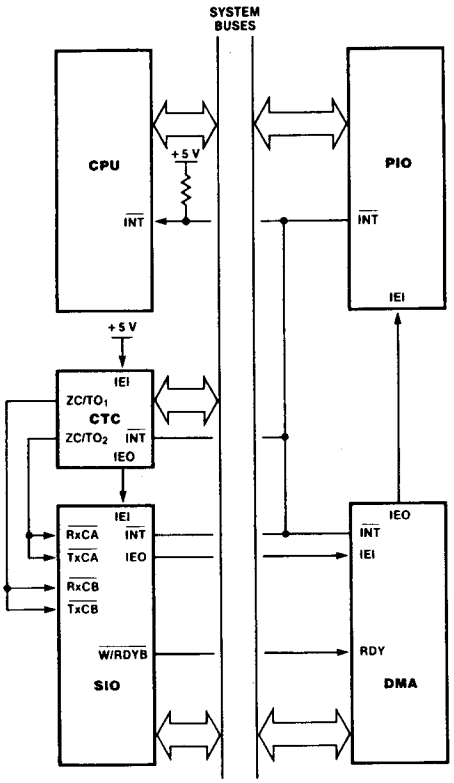



**Figure 8. A Typical Z80 Environment**

**$D_0$-$D_7$.** *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z80 CPU and the Z80 CTC.

**IEI.** *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z80 CPU.

**IEO.** *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z80 CPU is not servicing an interrupt from any Z80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

**$\overline{INT}$.** *Interrupt Request* (output, open drain, active Low). Low when any Z80 CTC channel that has been programmed to enable interrupts as a zero-count condition in its downcounter.

**$\overline{IORQ}$.** *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z80 CPU and the Z80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z80 CTC does not receive a specific write signal; rather, it internally generates is own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$, and $\overline{RD}$ are active; the contents of the downcounter are read by the Z80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z80 data bus.

**$\overline{M1}$.** *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z80 CPU is acknowledging an interrupt. The Z80 CTC then places an interupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

**$\overline{RD}$.** *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z80 CPU and the Z80 CTC.

**$\overline{RESET}$.** *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the interrupt outputs go inactive; IEO reflects IEI; $D_0$-$D_7$ go to the high-impedance state.

**$ZC/TO_0$-$ZC/TO_2$.** *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the downcounter decrements to zero.

## TIMING

**Read Cycle Timing.** Figure 9 shows read cycle timing. This cycle reads the contents of a down-counter without disturbing the count. During clock cycle $T_2$, the Z80 CPU initiates a read cycle by driving the following inputs Low: $\overline{RD}$, $\overline{IORQ}$, and $\overline{CE}$. A 2-bit binary code at inputs $CS_1$ and $CS_0$ selects the channel to be read. $\overline{M1}$ must be High to distinguish this cycle from an interrupt acknowledge.

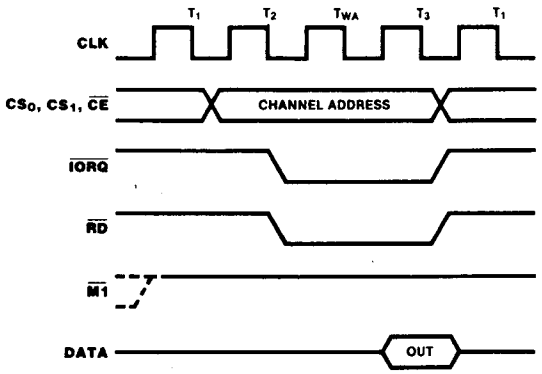



**Figure 9. Read Cycle Timing**

**Write Cycle Timing.** Figure 10 shows write cycle timing for loading control, time constant, or vector words.

The CTC does not have a write signal input, so it generates one internally when the read ($\overline{RD}$) input is High during $T_1$. During $T_2$ $\overline{IORQ}$ and $\overline{CE}$ inputs are Low. $\overline{M1}$ must be High to distinguish a write cycle from an interrupt acknowledge. A 2-bit binary code at inputs $CS_1$ and $CS_0$ selects the channel to be addressed, and the word being written is placed on the Z80 data bus. The data word is latched into the appropriate register with the rising edge of clock cycle $T_3$.

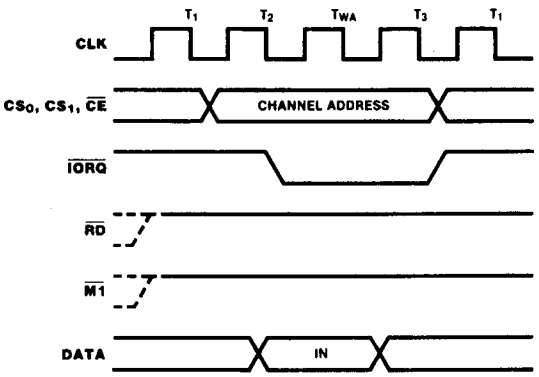



**Figure 10. Write Cycle Timing**

**Timer Operation.** In the timer mode, a CLK/TRG pulse input starts the timer (Figure 11) on the second succeeding rising edge of CLK. The trigger pulse is asynchronous, and it must have a minimum width. A minimum lead time (210 ns) is required between the active edge of the CLK/TRG and the next rising edge of CLK to enable the prescaler on the following clock edge. If the CLK/TRG edge occurs closer than this, the initiation of the timer function is delayed one clock cycle. This corresponds to the start-up timing discussed in the programming section. The timer can also be started automatically if so programmed by the channel control word.

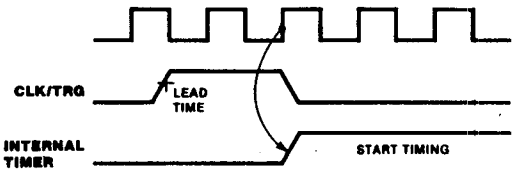



**Figure 11. Timer Mode Timing**

**Counter Operation.** In the counter mode, the CLK/TRG pulse input decrements the downcounter. The trigger is asynchronous, but the count is synchronized with CLK. For the decrement to occur on the next rising edge of CLK, the trigger edge must precede CLK by a minimum lead time as shown in Figure 12. If the lead time is less than specified, the count is delayed by one clock cycle. The trigger pulse must have a minimum width, and the trigger period must be at least twice the clock period. If the trigger repetition rate is faster than 1/3 the clock frequency, then TsCTR(Cs), AC Characteristics Specification 26, must be met.

The ZC/TO output occurs immediately after zero count, and follows the rising CLK edge.

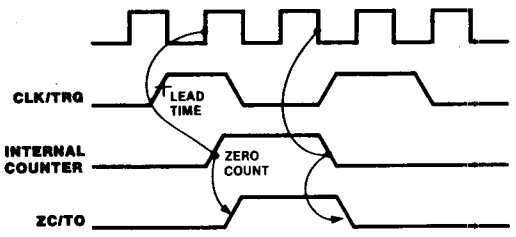



**Figure 12. Counter Mode Timing**

## INTERRUPT OPERATION

The Z80 CTC follows the Z80 system interrupt protocol for nested priority interrupts and return from interrupt, wherein the interrupt priority of a peripheral is determined by its location in a daisy chain. Two lines—IEI and IEO—in the CTC connect it to the system daisy chain. The device closest to the +5V supply has the highest priority (Figure 13). For additional information on the Z80 interrupt structure, refer to the *Z80 CPU Product Specification* and the *Z80 CPU Technical Manual.*

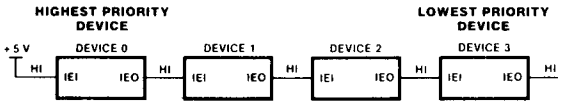



**Figure 13. Daisy-Chain Interrupt Priorities**

Within the Z80 CTC, interrupt priority is predetermined by channel number: Channel 0 has the highest priority, and Channel 3 the lowest. If a device or channel is being serviced with an interrupt routine, it cannot be interrupted by a device or channel with lower priority until service is complete. Higher priority devices or channels may interrupt the servicing of lower priority devices or channels.

A Z80 CTC channel may be programmed to request an interrupt every time its downcounter reaches zero. Note that the CPU must be programmed for interrupt mode 2. Some time after the interrupt request, the CPU sends an interrupt acknowledge. The CTC interrupt control logic determines the highest priority channel that is requesting an interrupt. Then, if the CTC IEI input is High (indicating that it has priority within the system daisy chain) it places an 8-bit interrupt vector on the system data bus. The high-order five bits of this vector were written to the CTC during the programming process; the next two bits are provided by the CTC interrupt control logic as a binary code that identifies the highest priority channel requesting an interrupt; the low-order bit is always zero.

**Interrupt Acknowledge Timing.** Figure 14 shows interrupt acknowledge timing. After an interrupt request, the Z80 CPU sends an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). All channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active—about two clock cycles earlier than $\overline{IORQ}$. $\overline{RD}$ is High to distinguish this cycle from an instruction fetch.

The CTC interrupt logic determines the highest priority channel requesting an interrupt. If the CTC interrupt enable input (IEI) is High, the highest priority interrupting channel within the CTC places its interrupt vector on the data bus when $\overline{IORQ}$ goes Low. Two wait states ($T_{WA}$) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.

**Return from Interrupt Timing.** At the end of an interrupt service routine the RETI (Return From Interrupt) instruction initializes the daisy chain enable lines for proper control of nested priority interrupt handling. The CTC decodes the 2-byte RETI code internally and determines whether it is intended for a channel being serviced. Figure 15 shows RETI timing.

If several Z80 peripherals are in the daisy chain, IEI settles active (High) on the chip currently being serviced when the opcode $ED_{16}$ is decoded. If the following opcode is $4D_{16}$, the peripheral being serviced is released and its IEO becomes active. Additional wait states are allowed.

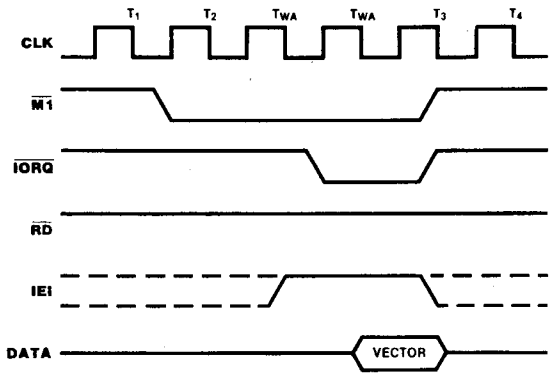



**Figure 14. Interrupt Acknowledge Timing**

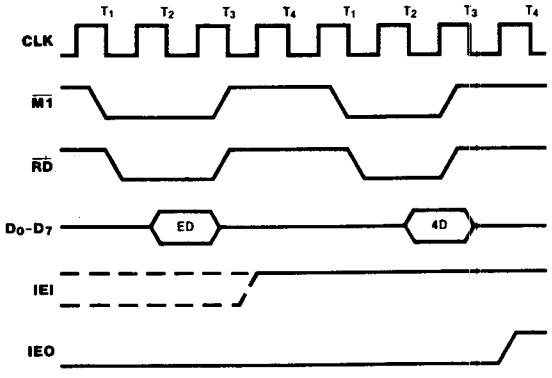



**Figure 15. Return From Interrupt Timing**

## ABSOLUTE MAXIMUM RATINGS

Voltages on $V_{CC}$ with respect to $V_{SS}$ . . . . . – 0.3V to + 7.0V
Voltages on all inputs with respect to $V_{SS}$ . . . . . – 0.3V to $V_{CC}$ + 0.3V
Storage Temperature . . . . . – 65 °C to + 150 °C

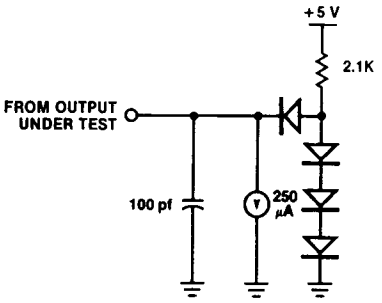
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only: operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin. Available operating temperature range is:

- **S = 0°C to +70°C, $V_{CC}$ Range**
  NMOS: +4.75V ≤ $V_{CC}$ ≤ +5.25V
  CMOS: +4.50V ≤ $V_{CC}$ ≤ +5.50V
- E= -40°C to 100°C, +4.50V ≤ $V_{CC}$ ≤ +5.50V

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.




## DC CHARACTERISTICS (Z84C30/CMOS Z80 CTC)

$V_{CC}$=5.0V ± 10%, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{ILC}$ | Clock Input Low Voltage | -0.3 | +0.45 | V | |
| $V_{IHC}$ | Clock Input High Voltage | $V_{CC}$-0.6 | $V_{CC}$+0.3 | V | |
| $V_{IL}$ | Input High Voltage | 2.2 | $V_{CC}$ | V | |
| $V_{IH}$ | Input Low Voltage | -0.3 | 0.8 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{LO}$=2.0mA |
| $V_{OH1}$ | Output High Voltage | 2.4 | | V | $I_{OH}$=-1.6mA |
| $V_{OH2}$ | Output High Voltage | $V_{CC}$-0.8 | | V | $I_{OH}$=-250µA |
| $I_{LI}$ | Input Leakage Current | -10 | 10 | µA | $V_{IN}$=0.4V to $V_{CC}$ |
| $I_{LO}$ | 3-state Output Leakage Current in Float | -10 | 10 | µA | $V_{OUT}$=0.4V to $V_{CC}$ |
| $I_{CC1}$ | Power Supply Current - 4MHz | | 7 [1] | mA | $V_{CC}$=5V |
| | - 6MHz | | 8 [1] | mA | CLK=4,6,8,10MHz |
| | - 8MHz | | 10 [1] | mA | $V_{IH}$=$V_{CC}$-0.2V |
| | - 10MHz | | 12 [1] | mA | $V_{IL}$=0.2V |
| $I_{CC2}$ | Standby Supply Current | | 10 | µA | $V_{CC}$=5V<br>CLK=(0)<br>$V_{IH}$=$V_{CC}$-0.2V<br>$V_{IL}$=0.2V |
| $I_{OHD}$ | Darlington Drive Current | -1.5 | -5.0 | mA | $V_{OH}$=1.5V<br>REXT=1.1K ohm |

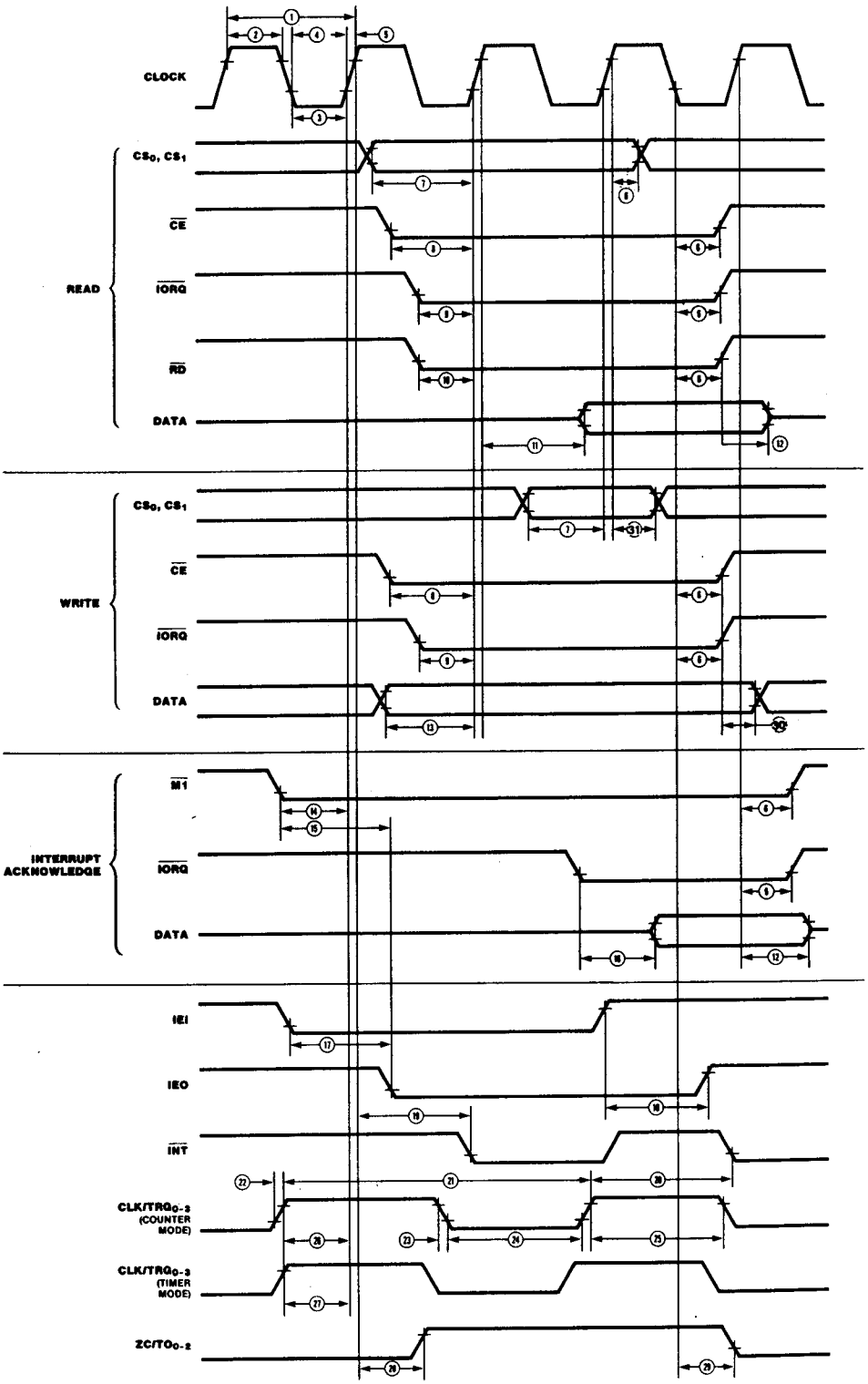
**Note:** [1] Measurements made with outputs floating.

## CAPACITANCE

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| CLK | Clock Capacitance | **10** | pf |
| $C_{IN}$ | Input Capacitance | **10** | pf |
| $C_{OUT}$ | Output Capacitance | 15 | pf |

$T_A$ = 25°C, f = 1 MHz
Unmeasured pins returned to ground.

## AC CHARACTERISTICS (Z84C30/CMOS Z80 CTC)



## AC CHARACTERISTICS (Z84C30/CMOS Z80 CTC Continued)

| No | Symbol | Parameter | Z84C3004 * Min | Z84C3004 * Max | Z84C3006 Min | Z84C3006 Max | Z84C3008 Min | Z84C3008 Max | Z84C3010 Min | Z84C3010 Max | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TcC | Clock Cycle Time | 250 | [1] | 162 | [1] | 125 | [1] | 100 | [1] | |
| 2 | TwCh | Clock pulse Width (High) | 110 | DC | 65 | DC | 55 | DC | 42 | DC | |
| 3 | TwCl | Clock pulse Width (Low) | 110 | DC | 65 | DC | 55 | DC | 42 | DC | |
| 4 | TfC | Clock Fall Time | | 30 | | 20 | | 10 | | 10 | |
| 5 | TrC | Clock Rise Time | | 30 | | 20 | | 10 | | 10 | |
| 6 | Th | All Hold Times | 0 | | 0 | | 0 | | 0 | | |
| 7 | TsCS(C) | /CS to Clock Rise Setup Time | 160 | | 100 | | 50 | | 35 | | |
| 8 | TsCE(C) | /CE to Clock Rise Setup Time | 150 | | 100 | | 50 | | 35 | | |
| 9 | TsIO(C) | /IORQ to Clock Rise Setup Time | 115 | | 70 | | 40 | | 35 | | |
| 10 | TsRD(C) | /RD Fall to Clock Rise Setup Time | 115 | | 70 | | 40 | | 35 | | |
| 11 | TdC(DO) | Clock Rise to Data Out Float Delay | 200 | | 130 | | 90 | | 90 | | [2] |
| 12 | TdRIr (DOz) | /RD, /IORQ rising to Data Outime Float Delay | | 50 | | 40 | | 40 | | 40 | |
| 13 | TsDI (C) | Data In to Clock rising set-up | 50 | | 40 | | 30 | | 30 | | |
| 14 | TsM1(C) | /M1 to Clock Rise Setup Time | 90 | | 70 | | 50 | | 40 | | |
| 15 | TdM1(IEO) | /M1 Fall to IEO Fall Delay (Interrupt Immediately Preceding /M1 Fall) | | 190 | | 130 | | 90 | | 70 | [3] |
| 16 | TdIO(DIO) | /IORQ Fall to Data Out Delay (/INTACK Cycle) | | 160 | | 110 | | 80 | | 80 | [2,6] |
| 17 | TdIEI(IEOf) | IEI Fall to IEO Fall Delay | | 130 | | 100 | | 70 | | 70 | [3] |
| 18 | TdIEI(IEOr) | IEI Rise to IEO Rise Delay (After ED Decode) | | 160 | | 110 | | 70 | | 70 | [3] |
| 19 | TdC(INT) | Clock Rise to /INT Fall Delay | (TcC+140) | | (TcC+120) | | (TcC+100) | | (TcC+80) | | [4] |
| 20 | TdCLK(INT) | CLK/TRG Rise to /INT Fall Delay | | | | | | | | | |
| | | TsCTR(C) Satisfied | (19)+(26) | | (19)+(26) | | (19)+(26) | | (19)+(26) | | [5] |
| | | TsCTR(C) Not Satisfied | (1)+(19)+(26) | | (1)+(19)+(26) | | (1)+(19)+(26) | | (1)+(19)+(26) | | [5] |
| 21 | TcCTR | CLK/TRG Cycle Time | (2TcC) | | (2TcC) | | (2TcC) | | (2TcC) | | [5] |
| 22 | TrCTR | CLK/TRG Rise Time | | 50 | | 40 | | 30 | | 30 | |
| 23 | TfCTR | CLK/TRG Fall Time | | 50 | | 40 | | 30 | | 30 | |
| 24 | TwCTRh | CLK/TRG Width (Low) | 200 | | 120 | | 90 | | 90 | | |
| 25 | TwCTRl | CLK/TRG Width (High) | 200 | | 120 | | 90 | | 90 | | |
| 26 | TsCTR(Cs) | CLK/TRG Rise to Clock Rise Setup Time for Immediate Count | 210 | | 150 | | 110 | | 90 | | [5] |
| 27 | TsCTR(Ct) | CLK/TRG Rise to Clock Rise Setup Time for Enabling of Prescaler On Following Clock Rise | 210 | | 150 | | 110 | | 90 | | [4] |

* 4 MHz Z84C30 is obsoleted and replaced by 6 MHz

**Z84C30 AC CHARACTERISTICS (Continued)**

| No | Symbol | Parameter | Z84C3004* Min | Z84C3004* Max | Z84C3006 Min | Z84C3006 Max | Z84C3008 Min | Z84C3008 Max | Z84C3010 Min | Z84C3010 Max | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 28 | TdC(ZC/TOr) | Clock Rise to ZC/TO Rise Delay | | 190 | | 140 | | 100 | | 80 | |
| 29 | TdC(ZC/TOf) | Clock Fall to ZC/TO Fall Delay | | 190 | | 140 | | 100 | | 80 | |
| 30 | ThRIr(D) | /CE, /IORQ Rise to Data Hold | 20 | | 20 | | 10 | | 10 | | |
| 31 | ThC(CS) | Clock Rise to /CS Hold | 20 | | 20 | | 10 | | 10 | | |

* RESET must be active for a minimum of 3 clock cycles.
Units in Nanoseconds

**Notes:**
[1] TcC = TwCh + TwCl + TrC + TfC.
[2] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.
[3] Increase delay by 2nS for each 10pF increase in loading, 100pF max.
[4] Timer mode.
[5] Counter mode.
[6] 2.5TcT > (N-2)TdIEI(IEOf) + TdM1(IEO) + TsIEI(IO) + TTL Buffer Delay, if any.

* 4 MHz Z84C30 is obsoleted and replaced by 6 MHz

## DC CHARACTERISTICS (Z8430/NMOS Z80 CTC)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{ILC}$ | Clock Input Low Voltage | −0.3[c] | +0.45[a] | V | |
| $V_{IHC}$ | Clock Input High Voltage | $V_{CC}$ −0.6[a] | $V_{CC}$ +0.3[b] | V | |
| $V_{IL}$ | Input Low Voltage | −0.3[c] | +0.8[a] | V | |
| $V_{IH}$ | Input High Voltage | +2.2[a] | $V_{CC}$[b] | V | |
| $V_{OL}$ | Output Low Voltage | | +0.4[a] | V | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ | Output High Voltage | +2.4[a] | | V | $I_{OH}$ = −250 μA |
| $I_{CC}$ | Power Supply Current: | | +120[a] | mA | |
| $I_{LI}$ | Input Leakage Current | | ±10[a] | μA | $V_{IN}$ = 0.4 to $V_{CC}$ |
| $I_{LO}$ | 3-State Output Leakage Current in Float | | ±10[a] | μA | $V_{OUT}$ = 0.4 to $V_{CC}$ |
| $I_{OHD}$ | Darlington Drive Current | −1.5[a] | | mA | $V_{OH}$ = 1.5V<br>$R_{EXT}$ = 390Ω |

## CAPACITANCE

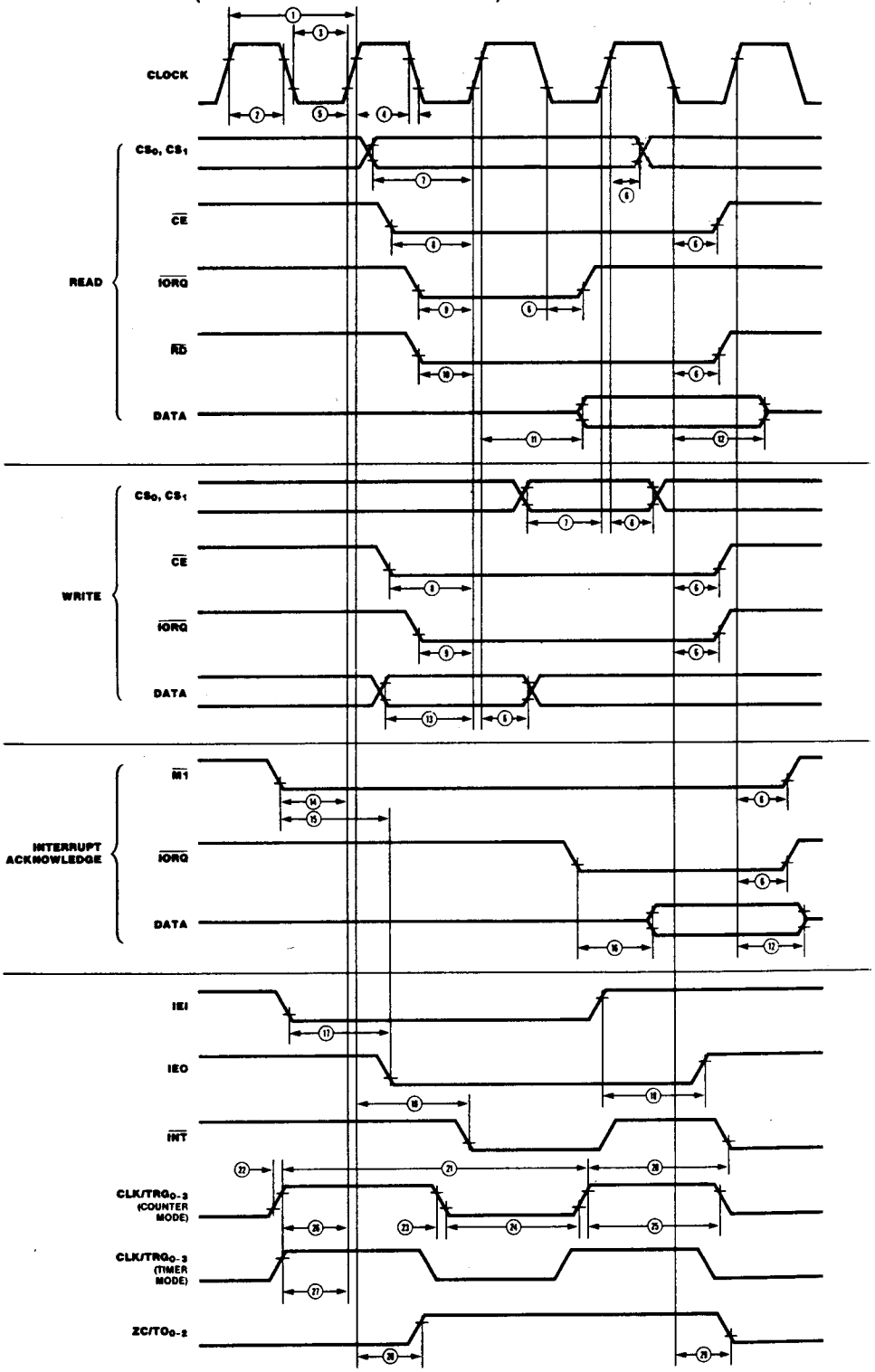
| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| CLK | Clock Capacitance | 20[c] | pf |
| $C_{IN}$ | Input Capacitance | 5[c] | pf |
| $C_{OUT}$ | Output Capacitance | 15[c] | pf |

$T_A$ = 25°C, f = 1 MHz
Unmeasured pins returned to ground.

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by characterization/design

## AC CHARACTERISTICS (Z8430/NMOS Z80 CTC Continued)



## AC CHARACTERISTICS (Z8430/NMOS Z80 CTC)

| Number | Symbol | Parameter | Z0843004 Min | Z0843004 Max | Z0843006 Min | Z0843006 Max | Notes† |
|---|---|---|---|---|---|---|---|
| 1 | TcC | Clock Cycle Time | 250 | [1] | 162 | [1] | |
| 2 | TwCh | Clock Width (High) | 105 | 2000 | 65 | 2000 | |
| 3 | TwCl | Clock Width (Low) | 105 | 2000 | 65 | 2000 | |
| 4 | TfC | Clock Fall Time | | 30 | | 20 | |
| 5 | TrC | Clock Rise Time | | 30 | | 20 | |
| 6 | Th | All Hold Times | 0 | | 0 | | |
| 7 | TsCS(C) | CS to Clock ↑ Setup Time | 160 | | 100 | | |
| 8 | TsCE(C) | $\overline{CE}$ to Clock ↑ Setup Time | 150 | | 100 | | |
| 9 | TsIO(C) | $\overline{IORQ}$ ↓ to Clock ↑ Setup Time | 115 | | 70 | | |
| 10 | TsRD(C) | $\overline{RD}$ ↓ to Clock ↑ Setup Time | 115 | | 70 | | |
| 11 | TdC(DO) | Clock ↑ to Data Out Delay | | 200 | | 130 | [2] |
| 12 | TdC(DOz) | Clock ↓ to Data Out Float Delay | | 110 | | 90 | |
| 13 | TsDI(C) | Data In to Clock ↑ Setup Time | 50 | | 40 | | |
| 14 | TsM1(C) | $\overline{M1}$ to Clock ↑ Setup Time | 90 | | 70 | | |
| 15 | TdM1(IEO) | $\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt immediately preceding M1) | | 190 | | 130 | [3] |
| 16 | TdIO(DOI) | $\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle) | | 160 | | 110 | [2] |
| 17 | TdIEI(IEOf) | IEI ↓ to IEO ↓ Delay | | 130 | | 100 | [3] |
| 18 | TdIEI(IEOr) | IEI ↑ to IEO ↑ Delay (After ED Decode) | | 160 | | 110 | [3] |
| 19 | TdC(INT) | Clock ↑ to $\overline{INT}$ ↓ Delay | | (1) + 140 | | (1) + 120 | [4,6] |
| 20 | TdCLK(INT) | CLK/TRG ↑ to $\overline{INT}$ ↓ | | | | | |
| | | tsCTR(C) satisfied | | (19) + (26) | | (19) + (26) | [5,6] |
| | | tsCTR(C) not satisfied | | (1) + (19) + (26) | | (1) + (19) + (26) | [5,6] |
| 21 | TcCTR | CLK/TRG Cycle Time | 2TcC | | 2TcC | | [5] |
| 22 | TrCTR | CLK/TRG Rise Time | | 50 | | 40 | |
| 23 | TfCTR | CLK/TRG Fall Time | | 50 | | 40 | |
| 24 | TwCTRl | CLK/TRG Width (Low) | 200 | | 120 | | |
| 25 | TwCTRh | CLK/TRG Width (High) | 200 | | 120 | | |

NOTES:

[1] TcC = TwCh + TwCl + TrC + TfC.

[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines.

[3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum.

[4] Timer mode

[5] Counter mode.

[6] Parenthetical numbers reference the table number of a parameter. e.g., (1) refers to TcC.

† 2.5 TcC > (n – 2) TDIEI(IEOf) + TDM1(IEO) + TsIEI(IO) + TTL buffer delay, if any. $\overline{RESET}$ must be active for a minimum of 3 clock cycles. Units are nanoseconds unless otherwise specified.

## AC CHARACTERISTICS (Z8430/NMOS Z80 CTC Continued)

| Number | Symbol | Parameter | Z0843004 Min | Z0843004 Max | Z0843006 Min | Z0843006 Max | Notes† |
|---|---|---|---|---|---|---|---|
| 26 | TsCTR(Cs) | CLK/TRG ↑ to Clock ↑ Setup Time for Immediate Count | 210 | | 150 | | [5] |
| 27 | TsCTR(Ct) | CLK/TRG ↑ to Clock ↑ Setup Time for enabling of Prescaler on following clock ↑ | 210 | | 150 | | [4] |
| 28 | TdC(ZC/TOr) | Clock ↑ to ZC/TO ↑ Delay | | 190 | | 140 | |
| 29 | TdC(ZC/TOf) | Clock ↓ to ZC/TO ↓ Delay | | 190 | | 140 | |

NOTES:

[1] TcC = TwCh + TwCl + TrC + TfC.

[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines.

[3] Increase delay by 2 ns for each 10 pf increase in loading. 100 pf maximum.

[4] Timer mode

[5] Counter mode.

[6] Parenthetical numbers reference the table number of a parameter. e.g., (1) refers to TcC.

† 2.5 TcC > (n – 2) TDIEI(IEOf) + TDM1(IEO) + TslEI(IO) + TTL buffer delay, if any. $\overline{\text{RESET}}$ must be active for a minimum of 3 clock cycles. Units are nanoseconds unless otherwise specified.