

SPECIFICATION

Product Type : EPD

Model Number : 2.13inch e-Paper (B)

Description : Screen Size: 2.13"
Color: Black, White and Red
Display Resolution: 212*104



Waveshare Electronics

Waveshare Electronics Room 813, Dynamic World Building,
Zhenhua Rd, Futian District, Shenzhen China

Website: www.waveshare.com

Revision History

| Rev. | Issued Date | Revised Contents |
|------|-------------|---|
| 1.0 | Jun.01.2015 | Preliminary |
| 1.1 | Jun.09.2015 | 1. In part 4: Modify the mechanical drawing of EPD module. |
| 1.2 | Jun.17.2015 | 1. In part 7-2): Modify Image update Time at 25°C from 8~12S to 12~15S. |
| 1.3 | Jul.21.2015 | 1. In part 4: Modify the Mechanical Drawing of EPD module. |
| 1.4 | Jul.23.2015 | 1. In part 9-1): Add the panel's storage and transportation conditions. 2. In part 9-1): Add the panel's operation conditions. 3. In part note 9-2: Modify each update interval time should be minimum at 150 seconds to 180 seconds. 4. In part 12: Delete block diagram. |
| 1.5 | Aug.24.2015 | 1. In part 8: Modify typical operating sequence. |
| 1.6 | Sep.18.2015 | 1. Modify Part Number. |
| 1.7 | Nov.07.2015 | 1. In part 11: Modify T=40°C, RH=80% for 168 hrs to 240 hrs. |
| 2.0 | Feb.27.2017 | 1. In part 7-5: Modify Reference Circuit. |

TECHNICAL SPECIFICATION

CONTENTS

| NO. | ITEM | PAGE |
|-----|---|------|
| - | Cover | 1 |
| - | Revision History | 2 |
| - | Contents | 3 |
| 1 | Application | 4 |
| 2 | Features | 4 |
| 3 | Mechanical Specifications | 4 |
| 4 | Mechanical Drawing of EPD module | 5 |
| 5 | Input/Output Terminals | 6 |
| 6 | Command Table | 8 |
| 7 | Electrical Characteristics | 26 |
| 8 | Typical Operating Sequence | 34 |
| 9 | Optical Characteristics | 38 |
| 10 | Handling, Safety and Environment Requirements | 40 |
| 11 | Reliability test | 41 |
| 12 | Point and line standard | 43 |
| 13 | Packing | 44 |

1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 2.13" active area contains 212×104 pixels, and has 1-bit white/black and 1-bit red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

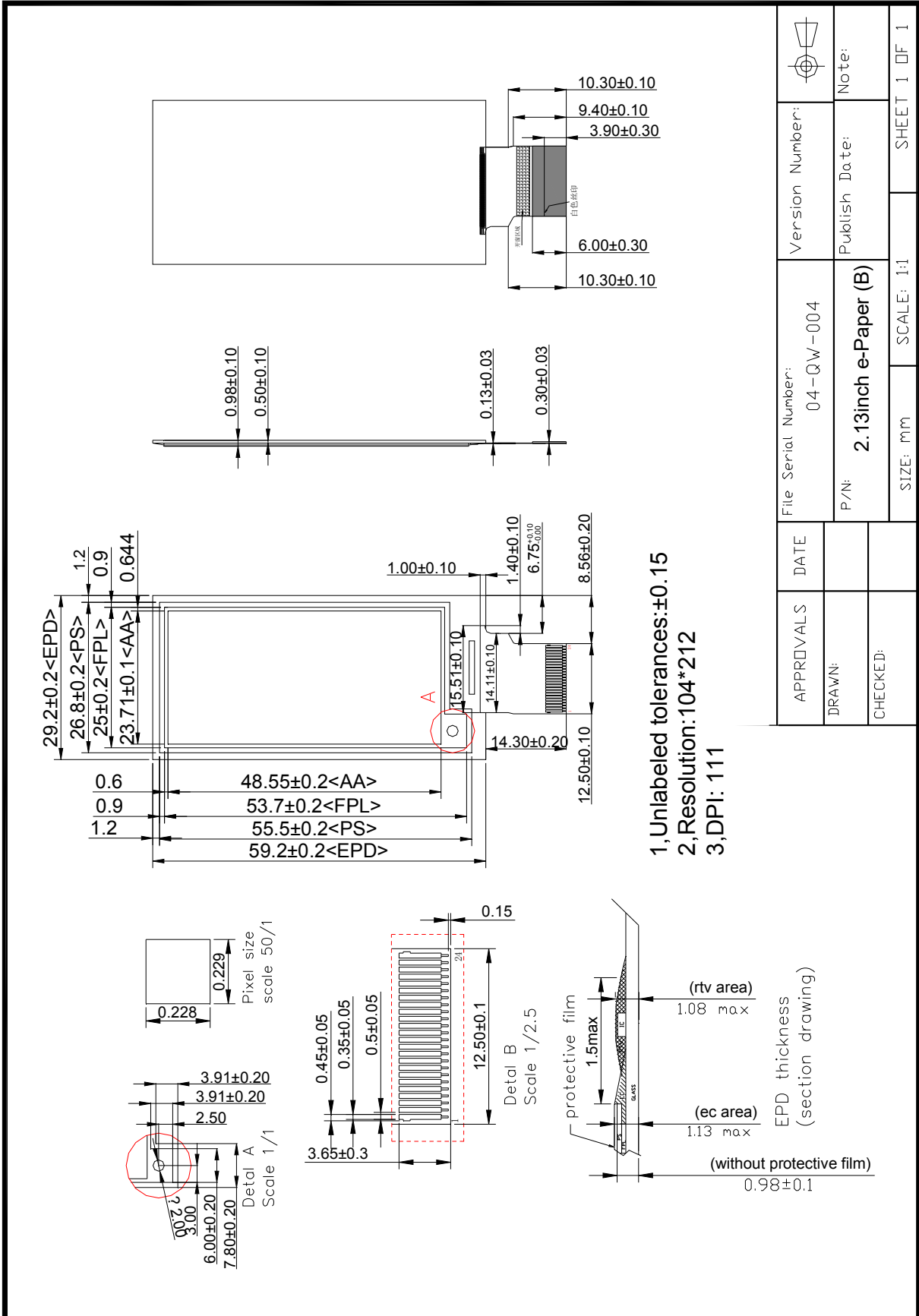
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I²C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

3. Mechanical Specifications

| Parameter | Specifications | Unit | Remark |
|---------------------|---------------------------|-------|----------|
| Screen Size | 2.13 | Inch | |
| Display Resolution | 212(H)×104(V) | Pixel | Dpi: 111 |
| Active Area | 48.55(H)×23.71(V) | mm | |
| Pixel Pitch | 0.229×0.228 | mm | |
| Pixel Configuration | Square | | |
| Outline Dimension | 59.2(H)×29.2 (V) ×0.98(D) | mm | |
| Weight | 4±0.5 | g | |

4. Mechanical Drawing of EPD module



5. Input/Output Terminals

5-1) Pin out List

| Pin # | Type | Single | Description | Remark |
|-------|------|--------|--|-----------|
| 1 | | NC | No connection and do not connect with other NC pins | Keep Open |
| 2 | O | GDR | N-Channel MOSFET Gate Drive Control | |
| 3 | O | RESE | Current Sense Input for the Control Loop | |
| 4 | C | VGL | Negative Gate driving voltage | |
| 5 | C | VGH | Positive Gate driving voltage | |
| 6 | O | TSCL | I ² C Interface to digital temperature sensor Clock pin | |
| 7 | I/O | TSDA | I ² C Interface to digital temperature sensor Date pin | |
| 8 | I | BS1 | Bus selection pin | Note 5-5 |
| 9 | O | BUSY | Busy state output pin | Note 5-4 |
| 10 | I | RES # | Reset | Note 5-3 |
| 11 | I | D/C # | Data /Command control pin | Note 5-2 |
| 12 | I | CS # | Chip Select input pin | Note 5-1 |
| 13 | I/O | D0 | serial clock pin (SPI) | |
| 14 | I/O | D1 | serial data pin (SPI) | |
| 15 | I | VDDIO | Power for interface logic pins | |
| 16 | I | VCI | Power Supply pin for the chip | |
| 17 | | VSS | Ground | |
| 18 | C | VDD | Core logic power pin | |
| 19 | C | VPP | Power Supply for OTP Programming | |
| 20 | C | VSH | Positive Source driving voltage | |
| 21 | C | PREVGH | Power Supply pin for VGH and VSH | |
| 22 | C | VSL | Negative Source driving voltage | |
| 23 | C | PREVGL | Power Supply pin for VCOM, VGL and VSL | |
| 24 | C | VCOM | VCOM driving voltage | |

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

| BS1 | MPU Interface |
|------------|--|
| L | 4-lines serial peripheral interface (SPI) |
| H | 3-lines serial peripheral interface (SPI) – 9 bits SPI |

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|---|-----|-----|----|----|----|----|----|----|----|----|--------------------------|--------------------------------------|-----|
| 1 | Panel Setting (PSR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 00h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | RES[1:0],REG,KW/R,UD,SHL,SHD_N,RST_N | 0Fh |
| 2 | Power Setting (PWR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 01h | |
| | | 0 | 1 | - | - | - | - | - | - | # | # | # | VDS_EN,VDG_EN | 03h |
| | | 0 | 1 | - | - | - | - | - | - | # | # | # | VCOM_HV,VGHL_LV[1:0] | 00h |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | VDH[5:0] | 26h |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | VDL[5:0] | 26h |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | VDHR[5:0] | 03h |
| 3 | Power OFF(POF) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | 02h | |
| 4 | Power OFF Sequence Setting(PFS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | 03h | |
| | | 0 | 1 | - | - | # | # | - | - | - | - | - | T_VDS_OF | 00h |
| 5 | Power ON(PON) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | 04h | |
| 6 | Power ON Measure(PMES) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | 05h | |
| 7 | Booster Soft Start(BTST) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | 06h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | BT_PHA[7:0] | 17h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | BT_PHB[7:0] | 17h |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | BT_PHC[5:0] | 17h |
| 8 | Deep Sleep | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | 07h | |
| | | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | Check code | A5h |
| 9 | Display Start Transmission 1(DTM1, white/black Data) (x-byte command) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | B/W Pixel Data (160×296) | 10h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | KPXL[1:8] | 00h |
| | | 0 | 1 | .. | .. | .. | .. | .. | .. | .. | .. | .. | .. | ... |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | KPXL[n-1:n] | 00h |
| 10 | Data Stop | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 11h | |
| | | 1 | 1 | # | - | - | - | - | - | - | - | - | | 00h |
| 11 | Display Refresh(DRF) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | 12h | |
| 12 | Display Start Transmission 2(DTM2, Red Data) (x-byte command) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Red Pixel Data(160×296) | 13h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | RPXL[1:8] | 00h |
| | | 0 | 1 | .. | .. | .. | .. | .. | .. | .. | .. | .. | .. | .. |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | RPXL[n-1:n] | 00h |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default |
|----|--|-----|-----|----|----|----|----|----|----|----|----|-------------------|---------|
| 13 | VCOM LUT(LUTC) (45-byte command, structure of bytes 2~7 repeated) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | 20h |
| 14 | W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | 21h |
| 15 | B2W LUT (LUTBW / LUTR) (43-byte command, structure of bytes 2~7 repeated 7 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | 22h |
| 16 | W2B LUT (LUTWB / LUTW) (43-byte command, structure of bytes 2~7 repeated 7 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | 23h |
| 17 | B2B LUT (LUTBB / LUTB) (43-byte command, structure of bytes 2~7 repeated 7 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | | 24h |
| 18 | PLL control(PLL) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 30h |
| | | 0 | 1 | - | - | # | # | # | # | # | # | M[2:0],N[2:0] | 3Ch |
| 19 | Temperature Sensor Calibration (TSC) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | 40h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | LM[10:3]/TSR[7:0] | 00h |
| | | 1 | 1 | # | # | # | - | - | - | - | - | LM[2:0]/- | 00h |
| 20 | Temperature Sensor Selection (TSE) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | | 41h |
| | | 0 | 1 | # | - | - | - | # | # | # | # | TSE,TO[3:0] | 00h |
| 21 | Temperature Sensor Write (TSW) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | | 42h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | WATTR[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | WMSB[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | WLSB[7:0] | 00h |
| 22 | Temperature Sensor Read (TSR) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | | 43h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | RMSB[7:0] | 00h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | RLSB[7:0] | 00h |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|--------------------------------------|-----|-----|----|----|----|----|----|----|----|----|----------------------------|---|-----|
| 23 | Vcom and data interval setting (CDI) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | | 50h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | VBD[1:0],DDX[1:0],CDI[3:0] | D7h | |
| 24 | Lower Power Detection (LPD) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | | 51h | |
| | | 1 | 1 | - | - | - | - | - | - | - | # | LPD | 01h | |
| 25 | TCON setting (TCON) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | | 60h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | S2G[3:0],G2S[3:0] | 22h | |
| 26 | Resolution setting (TRES) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | | 61h | |
| | | 0 | 1 | # | # | # | # | # | 0 | 0 | 0 | HRES[7:3] | 00h | |
| | | 0 | 1 | - | - | - | - | - | - | - | - | # | VRES[8:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | | 00h |
| 27 | Get Status (FLG) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | | 71h | |
| | | 1 | 1 | - | # | # | # | # | # | # | # | # | PTL_FLAG,P ² C_BUSY,DATA_FLAG,PON,POF,BUSY | 02h |
| 28 | Auto Measurement Vcom | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 80h | |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | AMVT[1:0], XON,AMVS, AMV,AMVE | 10h |
| 29 | Read Vcom Value(VV) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 81h | |
| | | 1 | 1 | - | - | # | # | # | # | # | # | # | VV[5:0] | 00h |
| 30 | VCM_DC Setting (VDCS) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | 82h | |
| | | 0 | 1 | - | - | # | # | # | # | # | # | # | VDCS[5:0] | 00h |
| 31 | Partial Window (PTL) | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | 90h | |
| | | 0 | 1 | # | # | # | # | # | 0 | 0 | 0 | HRST[7:3] | 00h | |
| | | 0 | 1 | # | # | # | # | # | 1 | 1 | 1 | HRED[7:3] | 07h | |
| | | 0 | 1 | - | - | - | - | - | - | - | - | # | VRST[8:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | | 00h |
| | | 0 | 1 | - | - | - | - | - | - | - | - | # | VRED[8:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | | 00h |
| | | 0 | 1 | - | - | - | - | - | - | - | - | # | PT_SCAN | 01h |
| 32 | Partial In (PTIN) | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 91h | |
| 33 | Partial Out (PTOUT) | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | 92h | |
| 34 | Program Mode (PGM) | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | A0h | |
| | | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Check code = A5h | A5h | |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default |
|----|------------------------------|-----|-----|----|----|----|----|----|----|----|----|------------------------|---------|
| 35 | Active Progmming (APG) | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | A1h |
| 36 | Read OTP (ROTP) | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | A2h |
| | | 1 | 1 | - | - | - | - | - | - | - | - | Read Dummy | N/A |
| | | 1 | 1 | # | # | # | # | # | # | # | # | Data of Address = 000h | N/A |
| | | 1 | 1 | .. | .. | .. | .. | .. | .. | .. | .. | .. | N/A |
| | | 1 | 1 | # | # | # | # | # | # | # | # | Data of address = n | N/A |
| 37 | Power Saving (PWS) | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | | E3h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | VCOM_W[3:0],SD_W[3:0] | 00h |

(1) Panel Setting (PSR) (Register: R00H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|-----|-----|------|------|--------|-----|----|-----|-------|-------|
| Setting the panel | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | RES1 | RES0 | REG_EN | BWR | UD | SHL | SHD_N | RST_N |

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.

01b: 96x252 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.

10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.

11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.

REG_EN: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

BWR: Black / White / Red

0: Pixel with B/W/Red. (Default)

1: Pixel with B/W.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → ... → G0

1: Scan up. (default) First line to last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift direction

0: Shift left First data to last data: Sn-1 → Sn-2 → Sn-3 → ... → S0

1: Shift right. (default) First data to last data: S0 → S1 → S2 → ... → Sn-1

SHD_N: Booster Switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.

1: Booster ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N: Soft Reset

1: No effect (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V

When RST_N become LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) Power Setting (PWR) (R01H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------------------|-----|-----|----|----|-----------|----|----|---------|--------------|--------|
| Selecting Internal/External Power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | 0 | 1 | - | - | - | - | - | - | VDS_EN | VDG_EN |
| | 0 | 1 | - | - | - | - | - | VCOM_HV | VGHL_LV[1:0] | |
| | 0 | 1 | - | - | VDH[5:0] | | | | | |
| | 0 | 1 | - | - | VDL[5:0] | | | | | |
| | 0 | 1 | - | - | VDHR[5:0] | | | | | |

VDS_EN: Source power selection

0: External source power from VDH/VDL pins

1: Internal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection

0: External gate power from VGH/VGL pins

1: Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

| VGHL_LV | VGHL voltage level |
|-------------|--------------------|
| 00(Default) | VGH=16V,VGL= -16V |
| 01 | VGH=15V,VGL= -15V |
| 10 | VGH=14V,VGL= -14V |
| 11 | VGH=13V,VGL= -13V |

VDH[5:0]: Internal VDH power selection for B/W pixel.(Default value: 100110b)

| VDH | VDH_V | VDH | VDH_V |
|--------|-------|----------|-------|
| 000000 | 2.4V | ... | ... |
| 000001 | 2.6V | 100110 | 10.0V |
| 000010 | 2.8V | 100111 | 10.2V |
| 000011 | 3.0V | 101000 | 10.4V |
| 000100 | 3.2V | 101001 | 10.6V |
| 000101 | 3.4V | 101010 | 10.8V |
| 000110 | 3.6V | 101011 | 11.0V |
| 000111 | 3.8V | (others) | 11.0V |

VDL[5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

| VDL | VDL_V | VDL | VDL_V |
|--------|-------|----------|--------|
| 000000 | -2.4V | ... | ... |
| 000001 | -2.6V | 100110 | -10.0V |
| 000010 | -2.8V | 100111 | -10.2V |
| 000011 | -3.0V | 101000 | -10.4V |
| 000100 | -3.2V | 101001 | -10.6V |
| 000101 | -3.4V | 101010 | -10.8V |
| 000110 | -3.6V | 101011 | -11.0V |
| 000111 | -3.8V | (others) | -11.0V |

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

| VDHR | VDHR_V | VDHR | VDHR_V |
|--------|--------|----------|--------|
| 000000 | 2.4V | ... | ... |
| 000001 | 2.6V | 100110 | 10.0V |
| 000010 | 2.8V | 100111 | 10.2V |
| 000011 | 3.0V | 101000 | 10.4V |
| 000100 | 3.2V | 101001 | 10.6V |
| 000101 | 3.4V | 101010 | 10.8V |
| 000110 | 3.6V | 101011 | 11.0V |
| 000111 | 3.8V | (others) | 11.0V |

(3) Power OFF (PWR) (R02H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|----|----|----|----|----|----|----|----|
| Turning OFF the power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF. Source Driver output and Vcom will remain as previous condition, which may have 2 condition: 0V or floating.

(4) Power off sequence setting (PFS) (R03H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|----|----------------|----|----|----|----|----|
| Setting Power OFF sequence | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 1 | - | - | T_VDS_OFF[1:0] | - | - | - | - | - |

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) Power ON (PON) (R04H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------|-----|-----|----|----|----|----|----|----|----|----|
| Turning ON the Power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

After the Power ON command, the driver will be powered ON following the Power ON Sequence. Refer to the Power ON Sequence section. In the sequence, temperature sensor will be activated for one time sensing before enabling booster.

(6) Power ON Measure (PMES) (R05H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------|-----|-----|----|----|----|----|----|----|----|----|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| Starting data transmission | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | 0 | 1 | BT_PHA7 | BT_PHA6 | BT_PHA5 | BT_PHA4 | BT_PHA3 | BT_PHA2 | BT_PHA1 | BT_PHA0 |
| | 0 | 1 | BT_PHB7 | BT_PHB6 | BT_PHB5 | BT_PHB4 | BT_PHB3 | BT_PHB2 | BT_PHB1 | BT_PHB0 |
| | 0 | 1 | - | - | BT_PHC5 | BT_PHC4 | BT_PHC3 | BT_PHC2 | BT_PHC1 | BT_PHC0 |

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
 100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

| | | | | |
|-------------|--|------------------|-------------------------|------------------------------|
| | 00b: 10mS | 01b: 20mS | 10b: 30mS | 11b: 40mS |
| BTPHB[5:3]: | Driving strength of phase B | | | |
| | 000b: strength 1 | 001b: strength 2 | 010b: strength 3 | 011b: strength 4 |
| | 100b: strength 5 | 101b: strength 6 | 110b: strength 7 | 111b: strength 8 (strongest) |
| BTPHB[2:0]: | Minimum OFF time setting of GDR in phase B | | | |
| | 000b: 0.27uS | 001b: 0.34uS | 010b: 0.40uS | 011b: 0.54uS |
| | 100b: 0.80uS | 101b: 1.54uS | 110b: 3.34uS | 111b: 6.58uS |
| BTPHC[5:3]: | Driving strength of phase C | | | |
| | 000b: strength 1 | 001b: strength 2 | 010b: strength 3 | 011b: strength 4 |
| | 100b: strength 5 | 101b: strength 6 | 110b: strength 7 | 111b: strength 8 (strongest) |
| BTPHC[2:0]: | Minimum OFF time setting of GDR in phase C | | | |
| | 000b: 0.27uS | 001b: 0.34uS | 010b: 0.40uS | 011b: 0.54uS |
| | 100b: 0.80uS | 101b: 1.54uS | 110b: 3.34uS | 111b: 6.58uS |

(8) Deep Sleep (DSLPL) (R07H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|----|----|----|----|----|----|
| Deep Sleep | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|------------|------------|------------|------------|------------|------------|------------|----------|
| Starting data transmission | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | Pixel1 | Pixel2 | Pixel3 | Pixel4 | Pixel5 | Pixel6 | Pixel7 | Pixel8 |
| | 0 | 1 | .. | .. | .. | .. | .. | .. | .. | .. |
| | 0 | 1 | Pixel(n-7) | Pixel(n-6) | Pixel(n-5) | Pixel(n-4) | Pixel(n-3) | Pixel(n-2) | Pixel(n-1) | Pixel(n) |

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes "OLD" data to SRAM.

In B/W/Red mode, this command writes "B/W" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|-----------|----|----|----|----|----|----|----|
| Stopping data transmission | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | Data_flag | - | - | - | - | - | - | - |

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY signal will become “0”.

(11) Display Refresh (DRF) (R12H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|-----|-----|----|----|----|----|----|----|----|----|
| Refreshing the display | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY signal will become “0” and the refreshing of panel starts.

(12) Data Start Transmission 2 (DTM2) (R13H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|------------|------------|------------|------------|------------|------------|------------|----------|
| Starting data transmission | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | 0 | 1 | Pixel1 | Pixel2 | Pixel3 | Pixel4 | Pixel5 | Pixel6 | Pixel7 | Pixel8 |
| | 0 | 1 | .. | .. | .. | .. | .. | .. | .. | .. |
| | 0 | 1 | Pixel(n-7) | Pixel(n-6) | Pixel(n-5) | Pixel(n-4) | Pixel(n-3) | Pixel(n-2) | Pixel(n-1) | Pixel(n) |

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

(13) VCOM LUT (LUTC) (R20H)

This command builds Look-up Table for VCOM

(14) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White.

(15) B2W LUT (LUTBW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White.

(16) W2B LUT (LUTWB/LUTW) (R23H)

This command builds Look-up Table for White - to- Black.

(17) B2B LUT (LUTBB / LUTB) (R24H)

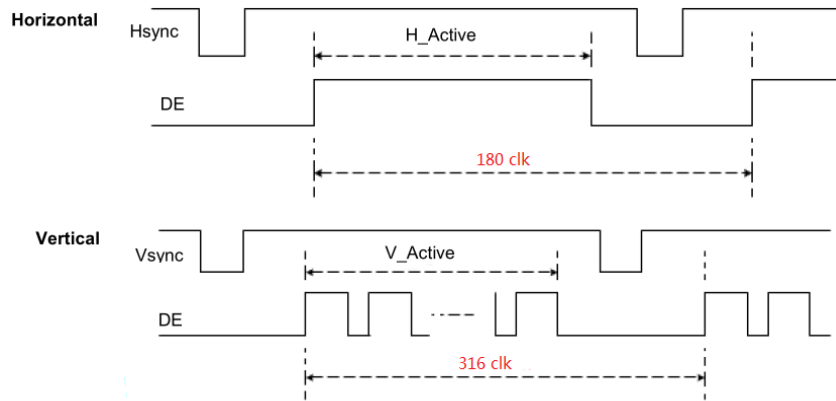
This command builds Look-up Table for Black - to- Black.

(18) PLL Control (PLL) (R30H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----|-----|----|----|--------|----|----|--------|----|----|
| Controlling PLL | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | - | - | M[2:0] | | | N[2:0] | | |

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

| M | N | Frame Rate | M | N | Frame Rate | M | N | Frame Rate | M | N | Frame Rate |
|---|---|------------|---|---|------------|---|---|------------|---|---|-----------------|
| 1 | 1 | 29 Hz | 3 | 1 | 86 Hz | 5 | 1 | 150 Hz | 7 | 1 | 200 Hz |
| | 2 | 14 Hz | | 2 | 43 Hz | | 2 | 72 Hz | | 2 | 100 Hz |
| | 3 | 10 Hz | | 3 | 29 Hz | | 3 | 48 Hz | | 3 | 67 Hz |
| | 4 | 7 Hz | | 4 | 21 Hz | | 4 | 36 Hz | | 4 | 50 Hz (Default) |
| | 5 | 6 Hz | | 5 | 17 Hz | | 5 | 29 Hz | | 5 | 40 Hz |
| | 6 | 5 Hz | | 6 | 14 Hz | | 6 | 24 Hz | | 6 | 33Hz |
| | 7 | 4 Hz | | 7 | 12Hz | | 7 | 20 Hz | | 7 | 29 Hz |
| 2 | 1 | 57 Hz | 4 | 1 | 114 Hz | 6 | 1 | 171 Hz | | | |
| | 2 | 29 Hz | | 2 | 57 Hz | | 2 | 86 Hz | | | |
| | 3 | 19 Hz | | 3 | 38 Hz | | 3 | 57 Hz | | | |
| | 4 | 14 Hz | | 4 | 29Hz | | 4 | 43 Hz | | | |
| | 5 | 11 Hz | | 5 | 23 Hz | | 5 | 34 Hz | | | |
| | 6 | 10 Hz | | 6 | 19 Hz | | 6 | 29 Hz | | | |
| | 7 | 8 Hz | | 7 | 16 Hz | | 7 | 24 Hz | | | |



(19) Temperature Sensor Calibration (TSC) (R40H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|-----|-----|---------|--------|--------|--------|--------|--------|--------|--------|
| Sensing Temperature | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | 1 | D10/TS7 | D9/TS6 | D8/TS5 | D7/TS4 | D6/TS3 | D5/TS2 | D4/TS1 | D3/TS0 |
| | 1 | 1 | D2 | D1 | D0 | - | - | - | - | - |

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

| TS[7:0]/D[10:3] | Temperature (°C) | TS[7:0]/D[10:3] | Temperature (°C) | TS[7:0]/D[10:3] | Temperature (°C) |
|-----------------|------------------|-----------------|------------------|-----------------|------------------|
| 1110_0111 | -25 | 0000_0000 | 0 | 0001_1001 | 25 |
| 1110_1000 | -24 | 0000_0001 | 1 | 0001_1010 | 26 |
| 1110_1001 | -23 | 0000_0010 | 2 | 0001_1011 | 27 |
| 1110_1010 | -22 | 0000_0011 | 3 | 0001_1100 | 28 |
| 1110_1011 | -21 | 0000_0100 | 4 | 0001_1101 | 29 |
| 1110_1100 | -20 | 0000_0101 | 5 | 0001_1110 | 30 |
| 1110_1101 | -19 | 0000_0110 | 6 | 0001_1111 | 31 |
| 1110_1110 | -18 | 0000_0111 | 7 | 0010_0000 | 32 |
| 1110_1111 | -17 | 0000_1000 | 8 | 0010_0001 | 33 |
| 1111_0000 | -16 | 0000_1001 | 9 | 0010_0010 | 34 |
| 1111_0001 | -15 | 0000_1010 | 10 | 0010_0011 | 35 |
| 1111_0010 | -14 | 0000_1011 | 11 | 0010_0100 | 36 |
| 1111_0011 | -13 | 0000_1100 | 12 | 0010_0101 | 37 |
| 1111_0100 | -12 | 0000_1101 | 13 | 0010_0110 | 38 |
| 1111_0101 | -11 | 0000_1110 | 14 | 0010_0111 | 39 |
| 1111_0110 | -10 | 0000_1111 | 15 | 0010_1000 | 40 |
| 1111_0111 | -9 | 0001_0000 | 16 | 0010_1001 | 41 |
| 1111_1000 | -8 | 0001_0001 | 17 | 0010_1010 | 42 |
| 1111_1001 | -7 | 0001_0010 | 18 | 0010_1011 | 43 |
| 1111_1010 | -6 | 0001_0011 | 19 | 0010_1100 | 44 |
| 1111_1011 | -5 | 0001_0100 | 20 | 0010_1101 | 45 |
| 1111_1100 | -4 | 0001_0101 | 21 | 0010_1110 | 46 |
| 1111_1101 | -3 | 0001_0110 | 22 | 0010_1111 | 47 |
| 1111_1110 | -2 | 0001_0111 | 23 | 0011_0000 | 48 |
| 1111_1111 | -1 | 0001_1000 | 24 | 0011_0001 | 49 |

(20) Temperature Sensor Enable (TSE) (R41H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------|-----|-----|-----|----|----|----|---------|----|----|----|
| Enable Temperature | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Sensor/Offset | 0 | 1 | TSE | - | - | - | TO[3:0] | | | |

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default)

1: Disable; using external sensor.

TO[3:0]: Temperature offset.

| TO[3:0] | Calculation | TO[3:0] | Calculation |
|---------|-------------|---------|-------------|
| 0000 b | 0 | 1000 | -8 |
| 0001 | 1 | 1001 | -7 |
| 0010 | 2 | 1010 | -6 |
| ... | ... | ... | ... |
| 0110 | 6 | 1110 | -2 |
| 0111 | 7 | 1111 | -1 |

(21) Temperature Sensor Write (TSW) (R42H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------------------|-----|-----|------------|----|----|----|----|----|----|----|
| Write External Temperature Sensor | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | WATTR[7:0] | | | | | | | |
| | 0 | 1 | WMSB[7:0] | | | | | | | |
| | 0 | 0 | WLSB[7:0] | | | | | | | |

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

(22) Temperature Sensor Read (TSR) (R43H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|-----|-----|-----------|----|----|----|----|----|----|----|
| Read External Temperature Sensor | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | 1 | 1 | RMSB[7:0] | | | | | | | |
| | 1 | 1 | RLSB[7:0] | | | | | | | |

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(23) VCOM And Data Interval Setting (CDI) (R50H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------------|-----|-----|----------|----|----------|----|----------|----|----|----|
| Set Interval Between Vcom and Data | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | VBD[1:0] | | DDX[1:0] | | CDI[3:0] | | | |

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

B/W/Red mode (BWR=0)

| DDX[0] | VBD[1:0] | LUT | DDX[0] | VBD[1:0] | LUT |
|--------|----------|----------|------------|----------|----------|
| 0 | 00 | Floating | 1(Default) | 00 | LUTB |
| | 01 | LUTR | | 01 | LUTW |
| | 10 | LUTW | | 10 | LUTR |
| | 11 | LUTB | | 11 | Floating |

B/W mode (BWR=1)

| DDX[0] | VBD[1:0] | LUT | DDX[0] | VBD[1:0] | LUT |
|--------|----------|-------------|------------|----------|-------------|
| 0 | 00 | Floating | 1(Default) | 00 | Floating |
| | 01 | LUTBW (1→0) | | 01 | LUTWB (1→0) |
| | 10 | LUTWB (0→1) | | 10 | LUTBW (0→1) |
| | 11 | Floating | | 11 | Floating |

DDX[1:0]: Data polarity.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.

DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

| DDX[1:0] | Data {Red, B/W} | LUT | DDX[1:0] | Data {Red, B/W} | LUT |
|-------------|-----------------|------|----------|-----------------|------|
| 00 | 00 | LUTW | 10 | 00 | LUTR |
| | 01 | LUTB | | 01 | LUTR |
| | 10 | LUTR | | 10 | LUTW |
| | 11 | LUTR | | 11 | LUTB |
| 01(Default) | 00 | LUTB | 11 | 00 | LUTR |
| | 01 | LUTW | | 01 | LUTR |
| | 10 | LUTR | | 10 | LUTB |
| | 11 | LUTR | | 11 | LUTW |

B/W mode (BWR=1)

| DDX[0] | Data {New, Old} | LUT | DDX[0] | Data {New, Old} | LUT |
|--------|-----------------|-------------|------------|-----------------|-------------|
| 0 | 00 | LUTWW (0→0) | 1(Default) | 00 | LUTBB (0→0) |
| | 01 | LUTBW (1→0) | | 01 | LUTWB (0→1) |
| | 10 | LUTWB (0→1) | | 10 | LUTBW (1→0) |
| | 11 | LUTBB (1→1) | | 11 | LUTWW (1→1) |

CDI[3:0]: Vcom and data interval

| CDI[3:0] | Vcom and Data Interval | CDI[3:0] | Vcom and Data Interval |
|----------|------------------------|----------|------------------------|
| 0000 b | 17 hsync | 0110 | 11 |
| 0001 | 16 | 0111 | 10 (Default) |
| 0010 | 15 | ... | ... |
| 0011 | 14 | 1101 | 4 |
| 0100 | 13 | 1110 | 3 |
| 0101 | 12 | 1111 | 2 |

(24) Low Power Detection (LPD) (R51H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Detect Low Power | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | - | - | - | - | - | - | - | LPD |

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Interval Low Power Detection Flag

0: Low power input (VDD < 2.5V) 1: Normal status (default)

(25) TCON Setting (TCON) (R60H)

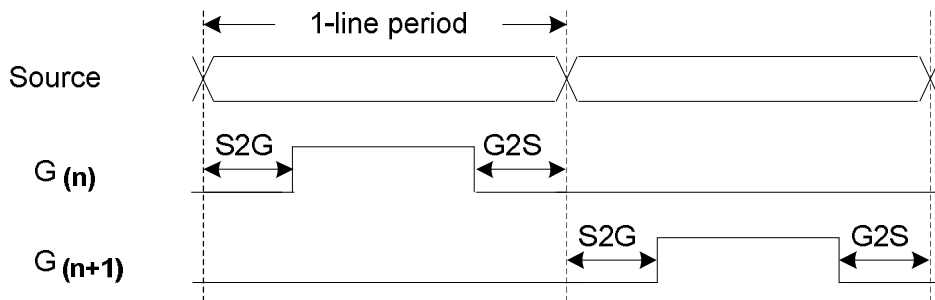
| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------------|-----|-----|----------|----|----|----|----------|----|----|----|
| Set Gate/Source Non-overlap Period | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | S2G[3:0] | | | | G2S[3:0] | | | |

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

| S2G[3:0] or G2S[3:0] | Period | S2G[3:0] or G2S[3:0] | Period |
|----------------------|-------------|----------------------|--------|
| 0000b | 4 | ... | ... |
| 0001 | 8 | 1011 | 48 |
| 0010 | 12(Default) | 1100 | 52 |
| 0011 | 16 | 1101 | 56 |
| 0100 | 20 | 1110 | 60 |
| 0101 | 24 | 1111 | 64 |

Period = 660 nS.



(26) Resolution Setting (TRES) (R61H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------------------------|-----|-----|-----------|----|----|----|----|----|----|---------|---|
| Set Display Resolution | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| | 0 | 1 | HRES[7:3] | | | | | | 0 | 0 | 0 |
| | 0 | 1 | - | - | - | - | - | - | - | VRES[8] | |
| | 0 | 0 | VRES[7:0] | | | | | | | | |

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

GD : First active gate = G0 (Fixed); LAST active gate = VRES[8:0] - 1

SD : First active source = S0 (Fixed); LAST active source = HRES[7:3]*8 - 1

| VV[5:0] | Vcom value |
|----------|------------|
| 00 0000b | -0.10 V |
| 00 0001b | -0.15 V |
| 00 0010b | -0.20 V |
| : | : |
| 11 1010b | -3.00 V |

(30) VCM_DC Setting (VDCS) (R82H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|-----------|----|----|----|----|----|
| Set VCM_DC | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | - | - | VDCS[5:0] | | | | | |

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

| VDCS[5:0] | Vcom value |
|-----------|-------------------|
| 00 0000b | -0.10 V (default) |
| 00 0001b | -0.15 V |
| 00 0010b | -0.20 V |
| : | : |
| 11 1010b | -3.00 V |

(31) Partial Window(PTL) (R90H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------|-----|-----|-----------|----|----|----|----|----|----|---------|
| Set Partial Window | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | HRST[7:3] | | | | | 0 | 0 | 0 |
| | 0 | 1 | HRED[7:3] | | | | | 1 | 1 | 1 |
| | 0 | 1 | - | - | - | - | - | - | - | VRST[8] |
| | 0 | 1 | VRST[7:0] | | | | | | | |
| | 0 | 1 | - | - | - | - | - | - | - | VRED[8] |
| | 0 | 1 | VRED[7:0] | | | | | | | |
| | 0 | 1 | - | - | - | - | - | - | - | PT_SCAN |

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(32) Partial In (PTIN) (R91H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|----|----|----|----|----|----|
| Partial In | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

This command makes the display enter partial mode.

(33) Partial Out (PTOUT) (R92H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|----|----|----|----|----|----|
| Partial In | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

This command makes the display exit partial mode and enter normal mode.

(34) Program Mode (PGM) (RA0H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------|-----|-----|----|----|----|----|----|----|----|----|
| Enter Program Mode | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excuted if check code = 0xA5.

(35) Active Program (APG) (RA1H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------|-----|-----|----|----|----|----|----|----|----|----|
| Active Program OTP | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

After this command is transmitted, the programming state machine would be activated.

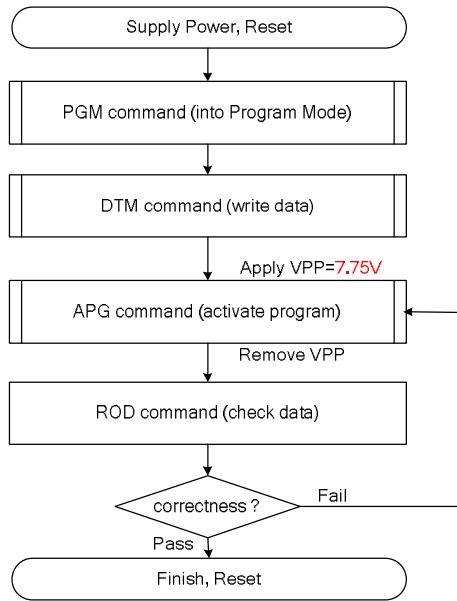
The BUSY flag would fall to 0 until the programming is completed.

(36) Read OTP Data (ROTP) (RA2H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|-----|-----|--------------------------------------|----|----|----|----|----|----|----|
| Read OTP data for check | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | 1 | 1 | Dummy | | | | | | | |
| | 1 | 1 | The data of address 0x000 in the OTP | | | | | | | |
| | 1 | 1 | The data of address 0x001 in the OTP | | | | | | | |
| | 1 | 1 | .. | | | | | | | |
| | 1 | 1 | The data of address (n-1) in the OTP | | | | | | | |
| | 1 | 1 | The data of address (n) in the OTP | | | | | | | |

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0xFFF.



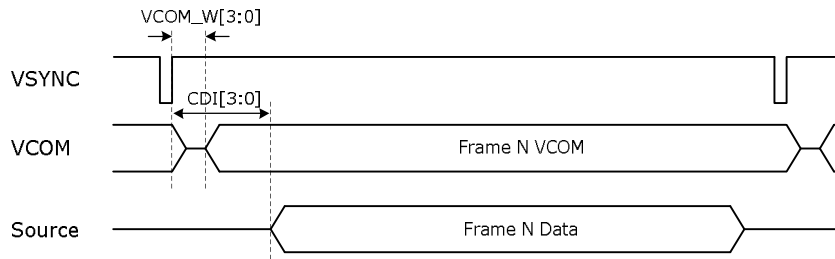
The sequence of programming OTP

(37) Power Saving (PWS) (RE3H)

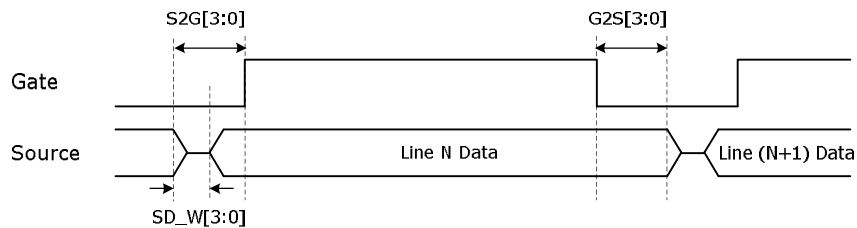
| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|-----|-----|-------------|----|----|----|-----------|----|----|----|
| Power Saving for Vcom & Source | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 1 | VCOM W[3:0] | | | | SD W[3:0] | | | |

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



7. Electrical Characteristics

7-1) Absolute maximum rating

| Parameter | Symbol | Rating | Unit |
|-----------------------|------------------|------------------------------|------|
| Logic Supply Voltage | V _{CI} | -0.3 to +6.0 | V |
| Logic Input Voltage | V _{IN} | -0.3 to V _{CI} +2.4 | V |
| Operating Temp. range | T _{OPR} | 0 to +40 | °C |
| Storage Temp. range | T _{STG} | -25 to +60 | °C |

7-2) Panel DC Characteristics

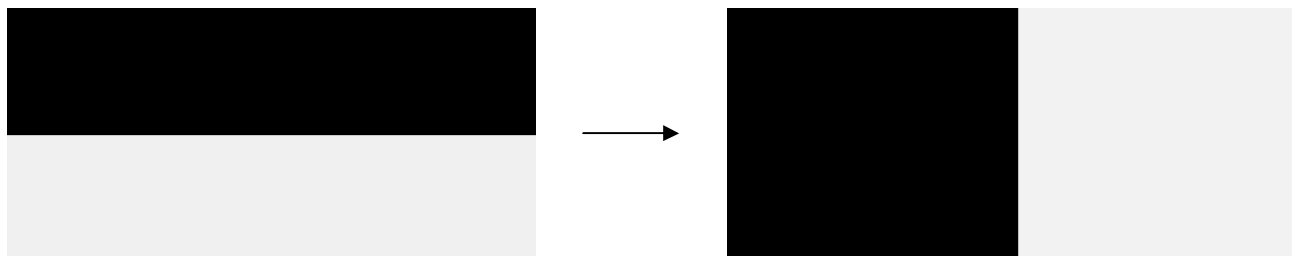
The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_A = 25°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|----------------------|---|----------------------|------|--------------------|------|
| Single ground | V _{SS} | - | - | 0 | - | V |
| Logic Supply Voltage | V _{CI} | - | 2.3 | 3.3 | 3.6 | V |
| High level input voltage | V _{IH} | Digital input pins | 0.7V _{CI} | - | V _{CI} | V |
| Low level input voltage | V _{IL} | Digital input pins | 0 | - | 0.3V _{CI} | V |
| High level output voltage | V _{OH} | Digital input pins , IOH= 400uA | V _{CI} -0.4 | - | - | V |
| Low level output voltage | V _{OL} | Digital input pins , IOL= -400uA | 0 | - | 0.4 | V |
| Image update current | I _{UPDATE} | - | - | 8 | 10 | mA |
| Standby panel current | I _{standby} | - | - | - | 5 | uA |
| Power panel (update) | P _{UPDATE} | - | - | 26.4 | 40 | mW |
| Standby power panel | P _{STBY} | - | - | - | 0.0165 | mW |
| Operating temperature | - | - | 0 | - | 40 | °C |
| Storage temperature | - | - | -25 | - | 60 | °C |
| Image update Time at 25 °C | - | - | - | 12 | 15 | Sec |
| Deep sleep mode current | I _{VCI} | DC/DC off No clock No input load Ram data not retain | - | 2 | 5 | uA |
| Sleep mode current | I _{VCI} | DC/DC off No clock No input load Ram data retain | - | 35 | 50 | uA |

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare
- V_{com} is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.3V, T_A = 25°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------|-----------------|-----|-------|-----|------|
| Internal Oscillator frequency | Fosc | VCI=2.3 to 3.6V | - | 1.625 | - | MHz |

7-3-2) MCU Interface

7-3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

| Pin Name | Data/Command Interface | | Control Signal | | |
|---------------|------------------------|------|----------------|------|------|
| | D1 | D0 | CS# | D/C# | RES# |
| Bus interface | SDIN | SCLK | CS# | D/C# | RES# |
| SPI4 | SDIN | SCLK | CS# | L | RES# |

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

| Function | CS# | D/C# | SCLK |
|---------------|-----|------|------|
| Write Command | L | L | ↑ |
| Write data | L | H | ↑ |

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-9: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

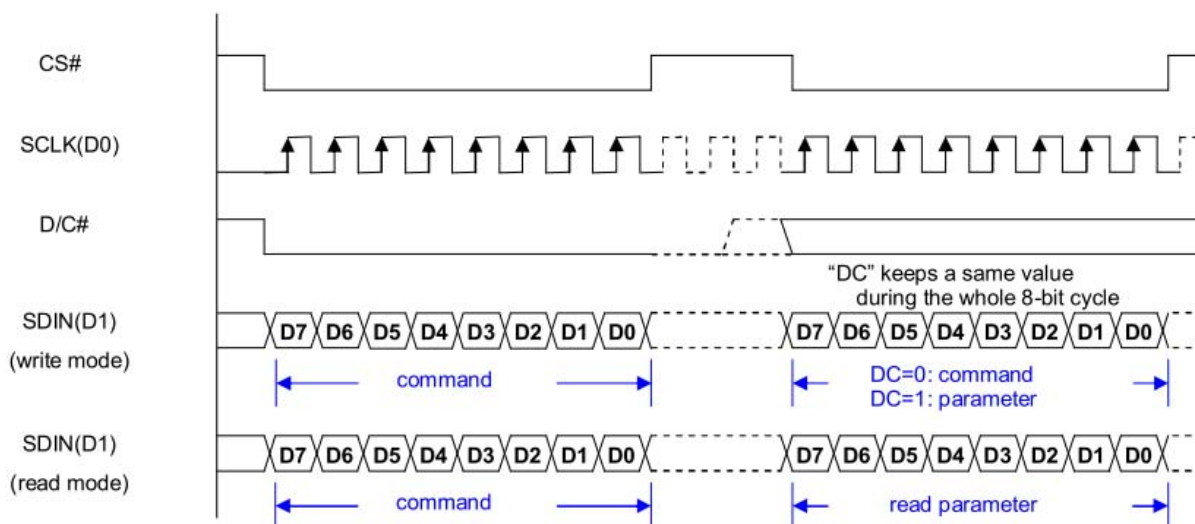


Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode

7-3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

| Function | CS# | D/C# | SCLK |
|---------------|-----|---------|------|
| Write Command | L | Tie LOW | ↑ |
| Write data | L | Tie LOW | ↑ |

Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-10: ↑stands for rising edge of signal

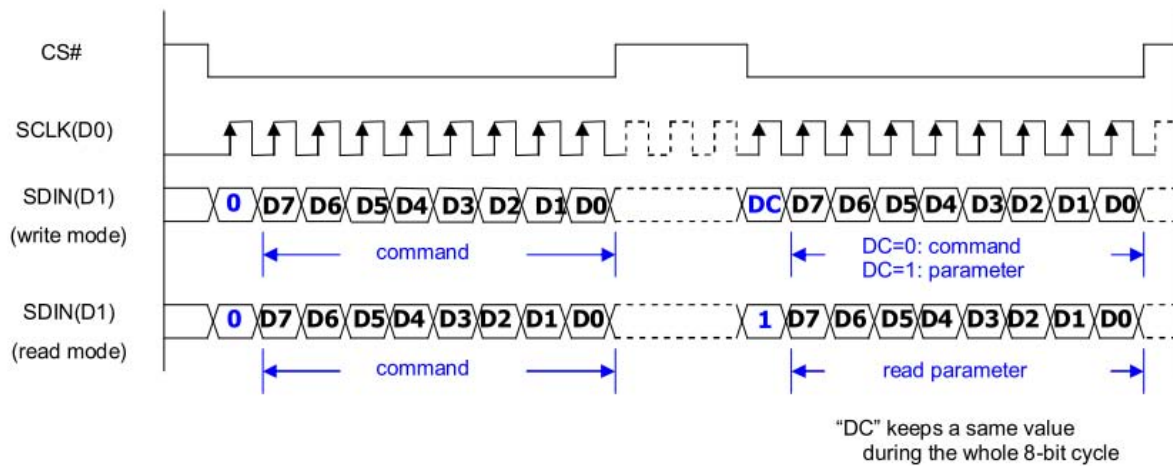
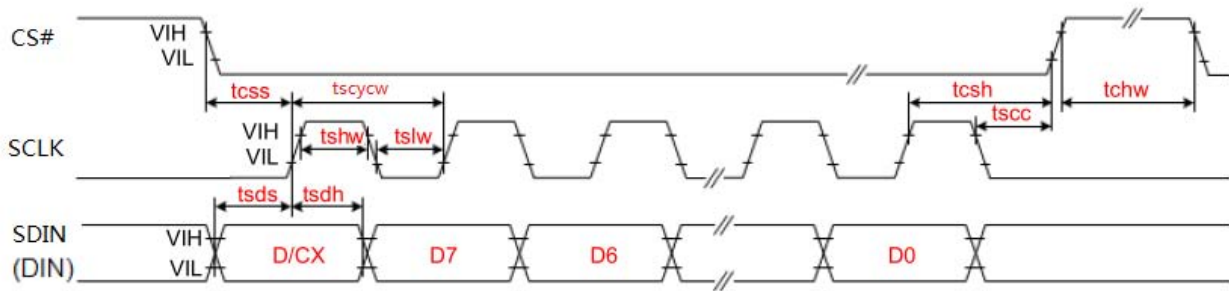
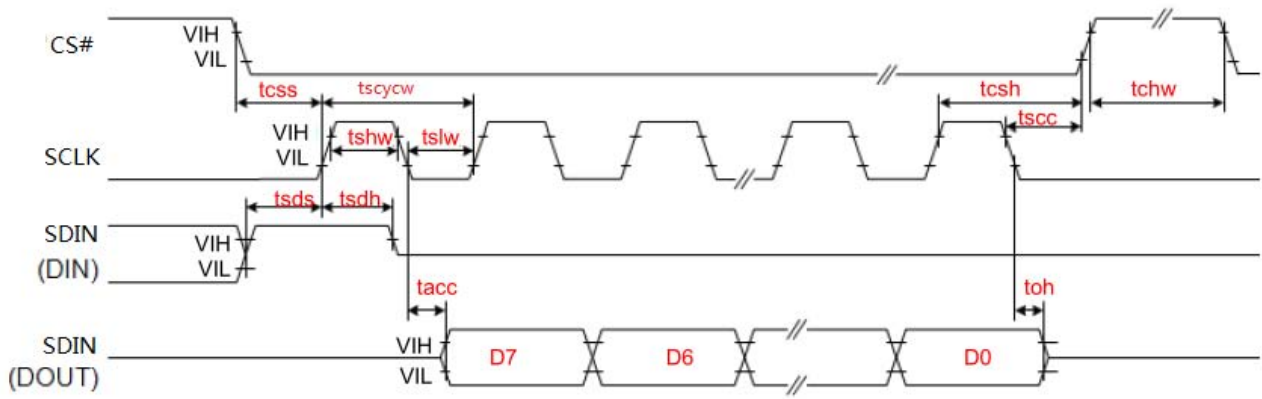


Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode

7-3-3) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

| Symbol | Signal | Parameter | Min | Typ | Max | Unit |
|--------|---------------------------|-----------------------------|-----|-----|-----|------|
| tcss | CS# | Chip Select Setup Time | 60 | - | - | ns |
| tcsh | | Chip Select Hold Time | 65 | - | - | ns |
| tscc | | Chip Select Setup Time | 20 | - | - | ns |
| tchw | | Chip Select Setup Time | 40 | - | - | ns |
| tscycw | SCLK | Serial clock cycle (write) | 100 | - | - | ns |
| tshw | | SCL “H” pulse width (write) | 35 | - | - | ns |
| tslw | | SCL “L” pulse width (write) | 35 | - | - | ns |
| tscyrc | | Serial clock cycle (Read) | 150 | - | - | ns |
| tshr | | SCL “H” pulse width (Read) | 60 | - | - | ns |
| tslr | | SCL “L” pulse width (Read) | 60 | - | - | ns |
| tsds | SDIN (DIN) SDIN (DOUT) | Data setup time | 30 | - | - | ns |
| tsdh | | Data hold time | 30 | - | - | ns |
| tacc | | Access time | - | - | 10 | ns |
| toh | | Output disable time | 15 | - | - | ns |

7-4) Power Consumption

| Parameter | Symbol | Conditions | TYP | Max | Unit | Remark |
|---------------------------------------|--------|------------|------|--------|------|--------|
| Panel power consumption during update | - | 25°C | 26.4 | 40 | mW | - |
| Power consumption in standby mode | - | 25°C | - | 0.0165 | mW | - |

7-5) Reference Circuit

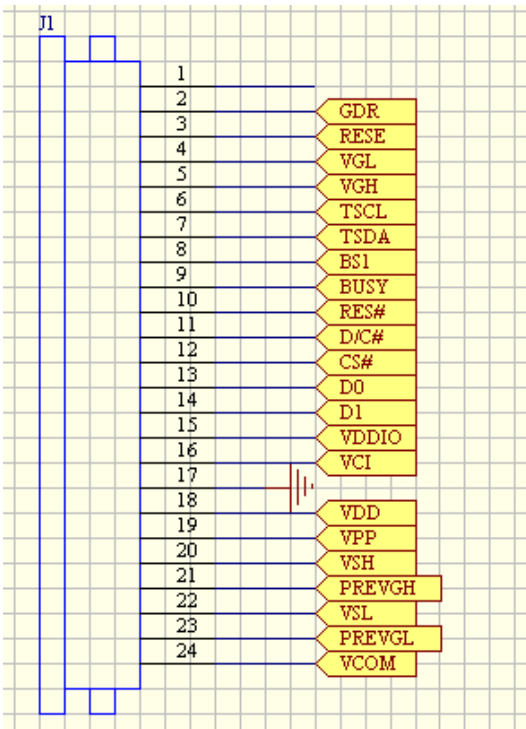


Figure . 7-5 (1)

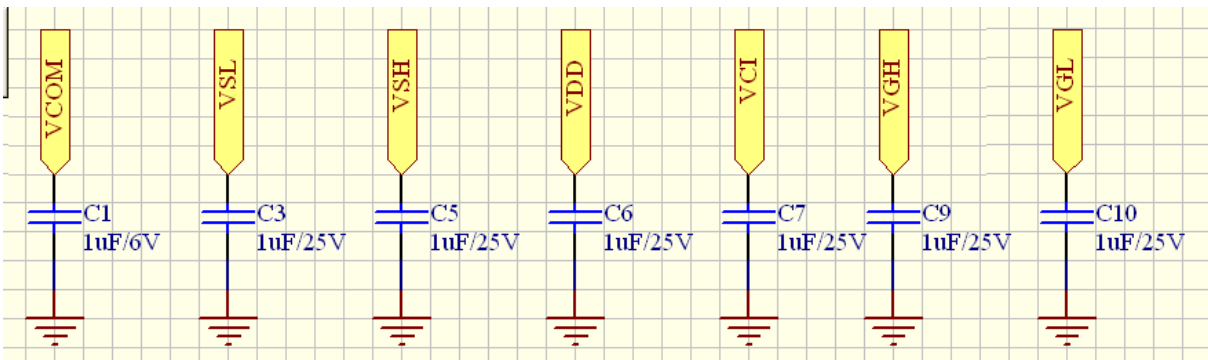


Figure . 7-5 (2)

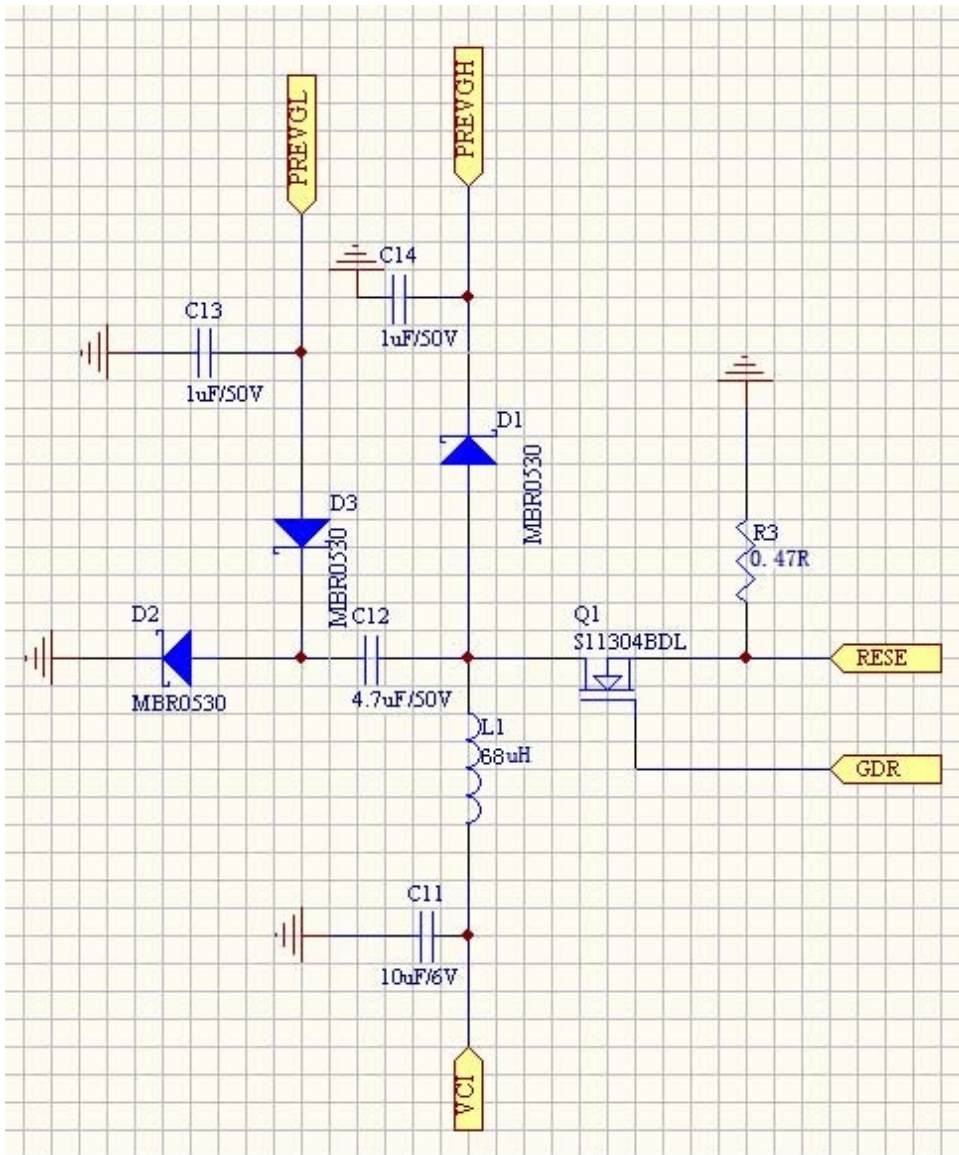


Figure . 7-5 (3)

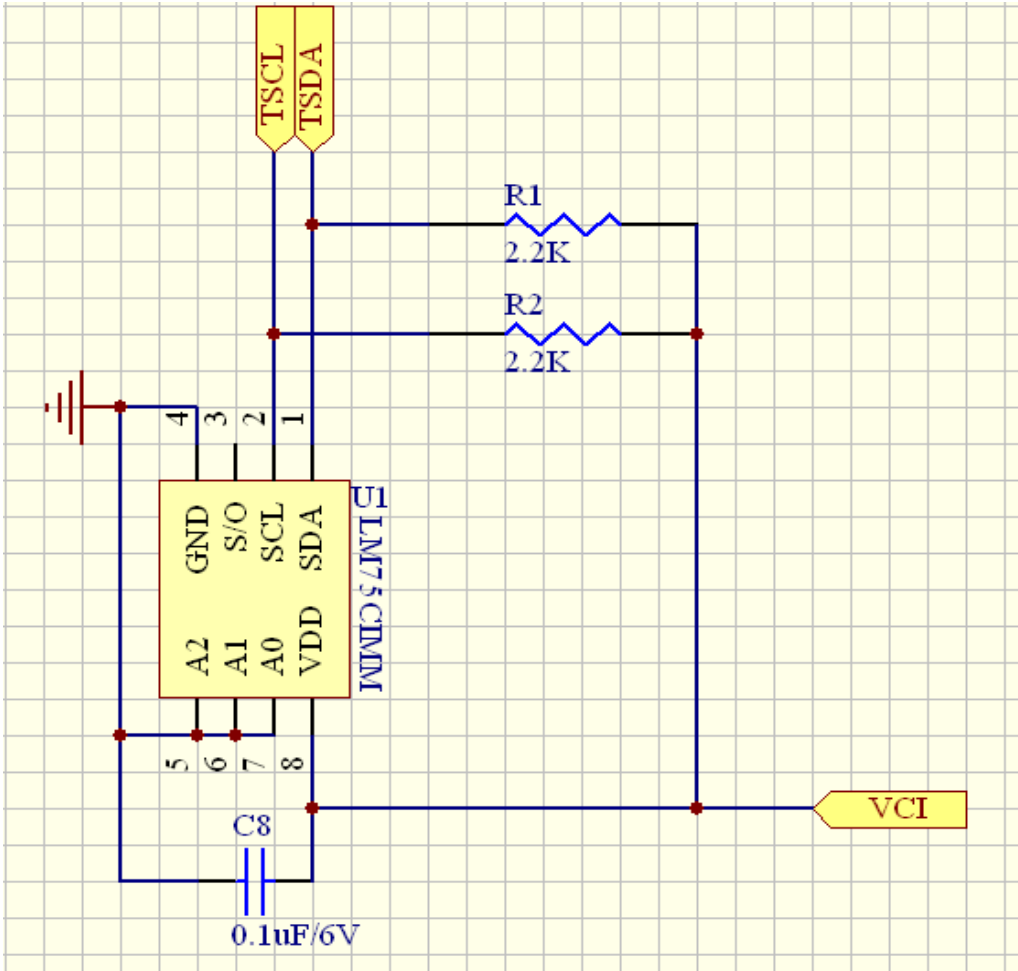
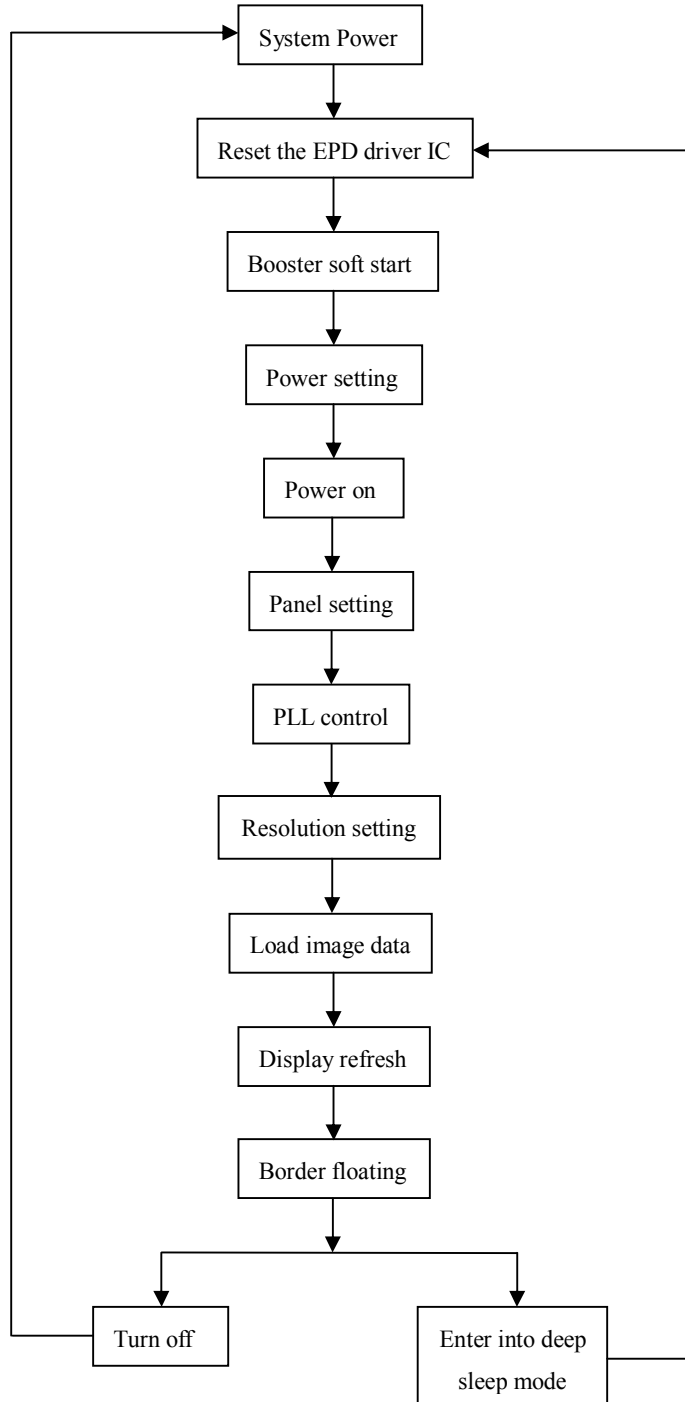


Figure . 7-5 (4)

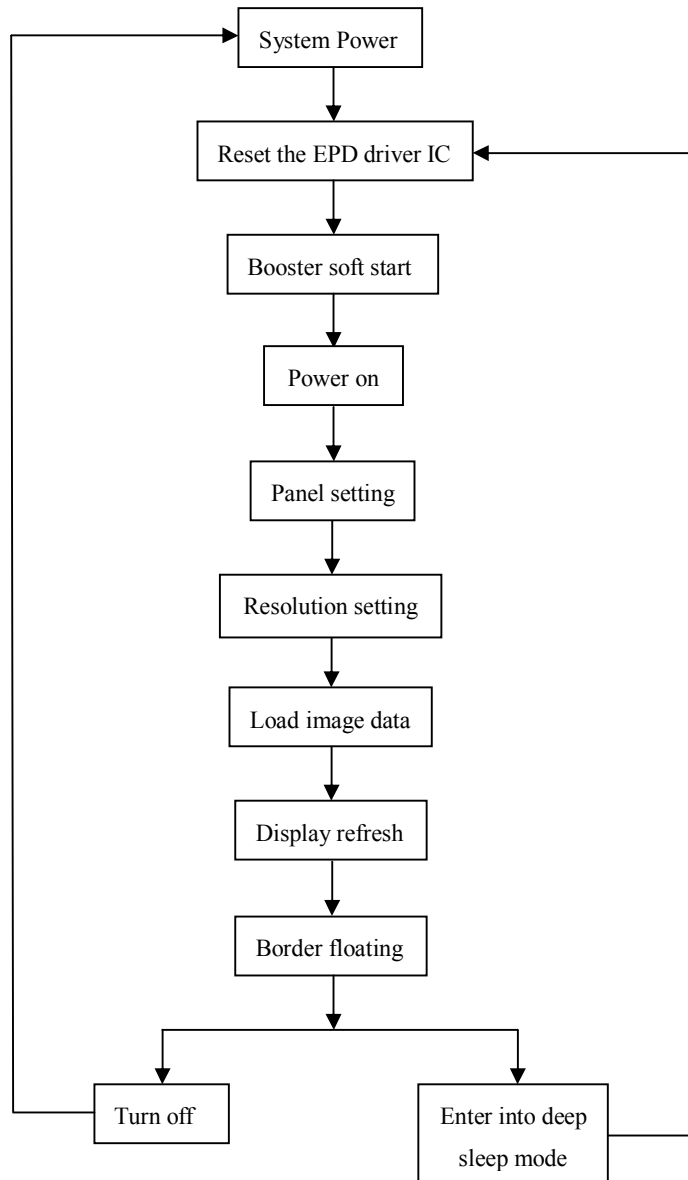
8. Typical Operating Sequence

8.1) Normal Operation Flow

1. BWR mode & LUT form Register

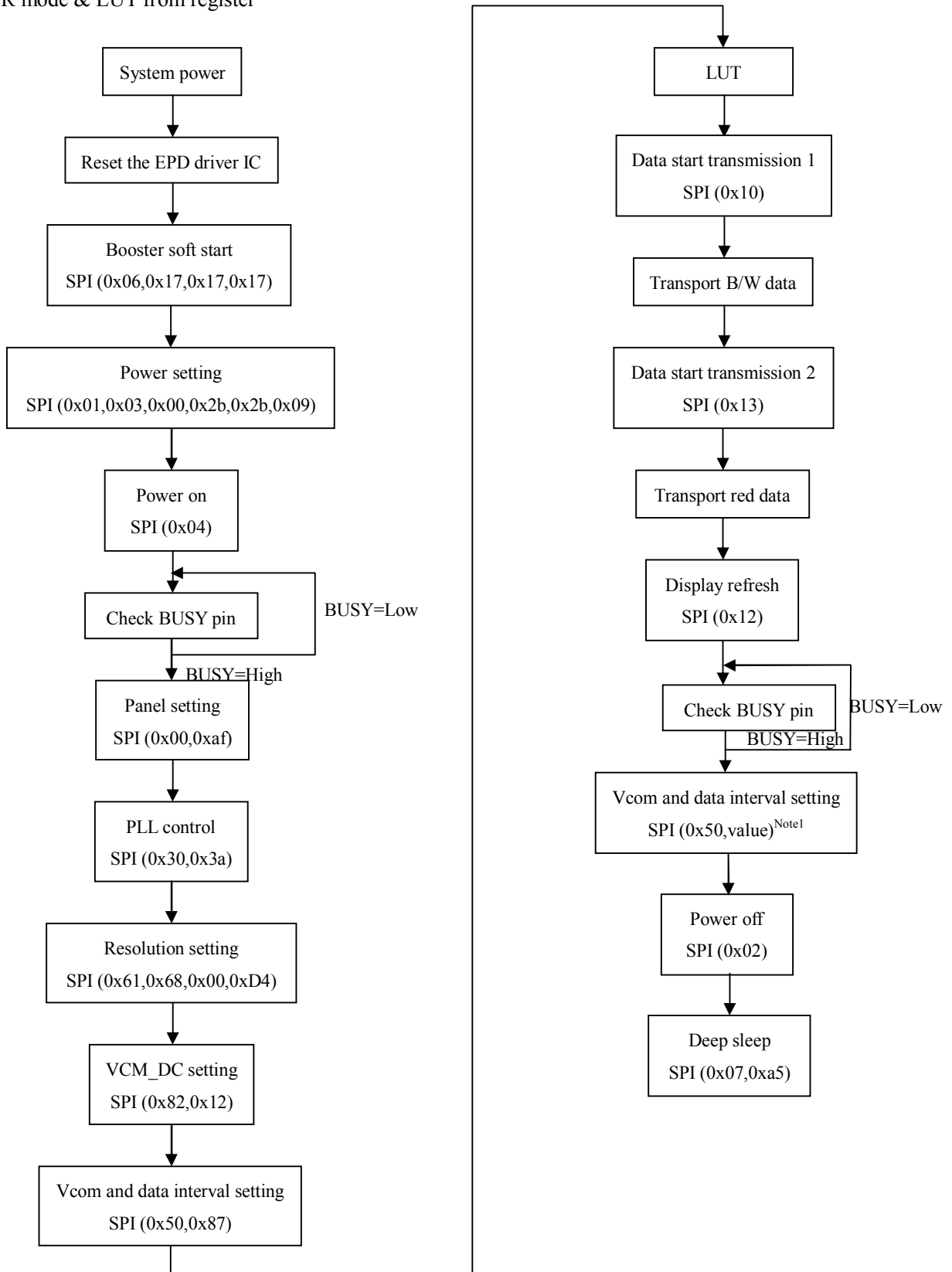


2. BWR mode & LUT form OTP



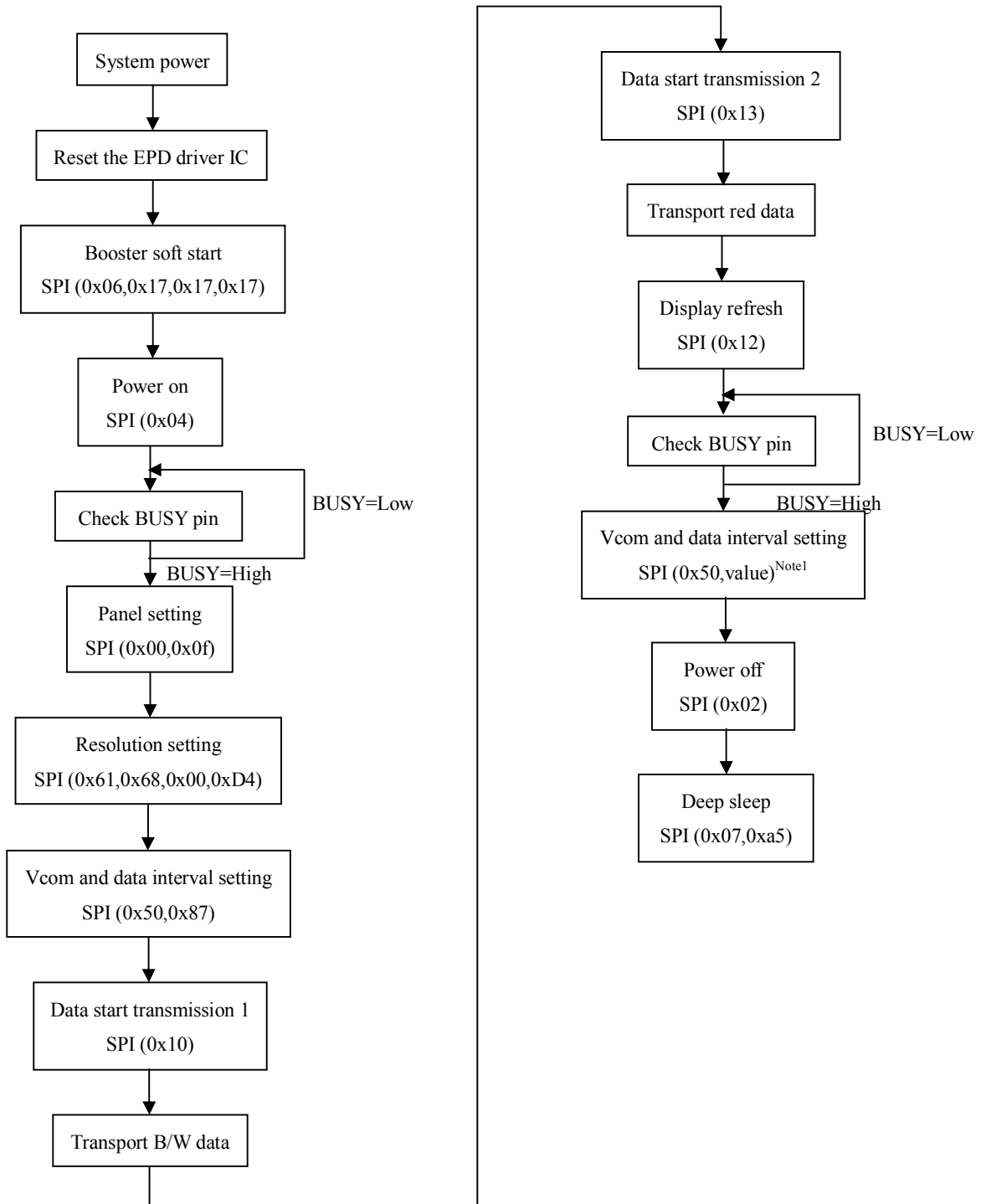
8.2) Reference Program Code

1. BWR mode & LUT from register



Note1: Set border to floating.

2. BWR mode & LUT from OTP



Note1: Set border to floating.

9. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYPE | MAX | UNIT | Note |
|--------------|----------------|----------------------------|-----|---|-----|------|----------|
| R | Reflectance | White | 30 | 35 | - | % | Note 9-1 |
| Gn | 2Grey Level | - | - | $DS + (WS-DS) \times n(m-1)$ | - | L* | - |
| CR | Contrast Ratio | indoor | 8 | | - | - | - |
| Panel's life | | 0°C~40°C | | 1000000 times or 5 years | | | Note 9-2 |
| Panel | Image Update | Storage and transportation | | Update the white screen | | | |
| | Update Time | Operation | | Suggest update once every 24 hours or at least 10 days to update again. | | | |

WS : White state, DS : Dark state

Gray state from Dark to White : DS、WS

m : 2

Note 9-1: Luminance meter: Eye – One Pro Spectrophotometer

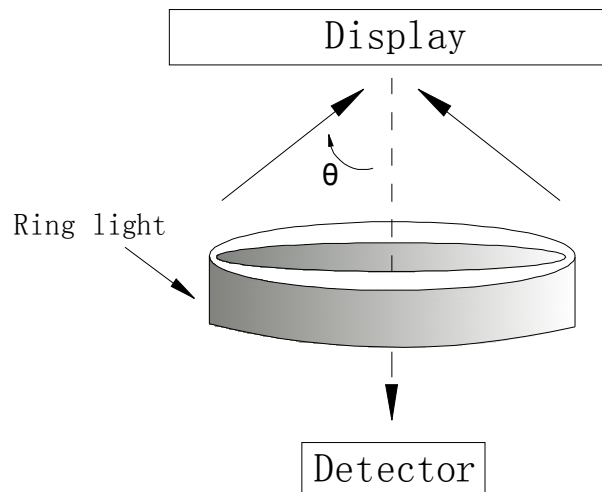
Note 9-2: Panel life will not guaranteed when work in temperature below 0 degree or above 40 degree. Each update interval time should be minimum at 180 seconds.

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance Rd: dark reflectance

$$CR = R1/Rd$$

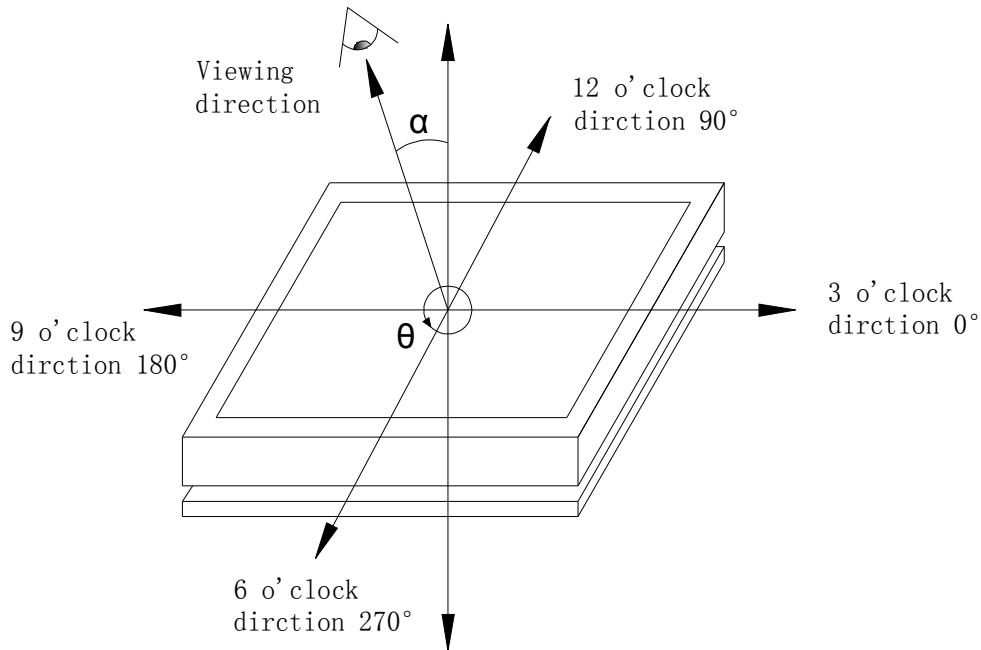


9-3) Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9-4) Bi-stability

The Bi-stability standard as follows:

| Bi-stability | Result | | |
|-----------------------------|--------------------------|-----|-----|
| | | AVG | MAX |
| 24 hours Luminance drift | White state ΔL^* | - | 3 |
| | Black state ΔL^* | - | 3 |

10. Handling, Safety And Environmental Requirements

| WARNING |
|--|
| <p>The display glass may break when it is dropped or bumped on a hard surface. Handle with care.</p> <p>Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.</p> |

| CAUTION |
|--|
| <p>The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.</p> <p>Disassembling the display module can cause permanent damage and invalidate the warranty agreements.</p> |

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status | |
|---|---|
| Product specification | The data sheet contains final product specifications. |
| Limiting values | |
| <p>Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).</p> <p>Stress above one or more of the limiting values may cause permanent damage to the device.</p> <p>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</p> | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

| Product Environmental certification |
|--|
| RoHS |

11. Reliability test

| | TEST | CONDITION | METHOD | REMARK |
|---|---|--|---|---|
| 1 | High-Temperature Operation | T = 40°C, RH=35%, for 240 hrs | When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp. | When experiment finished, the EPD must meet electrical and optical performance standards. |
| 2 | Low-Temperature Operation | T = 0°C for 240 hrs | When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab. | When experiment finished, the EPD must meet electrical and optical performance standards. |
| 3 | High-Temperature Storage | T = +60°C, RH= 35%, for 240 hrs Test in white pattern | When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp. | When experiment finished, the EPD must meet electrical and optical performance standards. |
| 4 | Low-Temperature Storage | T = -25°C for 240 hrs Test in white pattern | When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab | When experiment finished, the EPD must meet electrical and optical performance standards. |
| 5 | High Temperature, High-Humidity Operation | T=+40°C, RH=80% for 240 hrs | When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA. | When experiment finished, the EPD must meet electrical and optical performance standards. |
| 6 | High Temperature, High-Humidity Storage | T=+50°C, RH=80% for240hrs Test in white pattern | When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA. | When experiment finished, the EPD must meet electrical performance standards. |
| 7 | Temperature Cycle | [-25°C 30mins]→ [+60°C, RH=35% 30mins], | 1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25°C, storage period 30 minutes. After 30 minutes, it needs 30min to | When experiment finished, the EPD must meet electrical |

| | | | | |
|----|----------------------------|--|---|--|
| | | 50cycles Test in white pattern | <p>let temperature rise to 60°C. After 30min, temperature will be adjusted to 60°C, RH=35% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25°C. One temperature cycle (2hrs) is complete.</p> <p>2. Temperature cycle repeats 70 times.</p> <p>3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB.</p> | and optical performance standards. |
| 8 | UV exposure Resistance | 765 W/m ² for 168 hrs,40°C | Standard # IEC 60 068-2-5 Sa | |
| 9 | Electrostatic discharge | Machine model: +/-250V, 0 Ω ,200pF | Standard # IEC61000-4-2 | |
| 10 | Package Vibration | 1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction | Full packed for shipment | |
| 11 | Package Drop Impact | Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each. | Full packed for shipment | |

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) There's temperature vs display quality limitation in our display module, we guarantee 1 pixel display quality from 5°C ~ 30°C, and 2 pixel display quality for 0°C ~ 5°C & 30°C ~ 40°C.

(3) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 15 mins.

12. Point and line standard

Shipment Inseption Standard

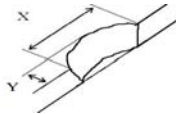
Part-A: Active area Part-B: Border area

Equipment: Electrical test fixture, Point gauge

Outline dimension:

59.2(H)*29.2(V)*0.98(D)

Unit: mm

| Environment | Temperature | Humidity | Illuminance | Distance | Time | Angle |
|------------------------|--|--------------------------|--------------------|----------|--------|-------|
| | 23±2℃ | 55±5%RH | 1200~1500Lux | 300 mm | 35 Sec | |
| Name | Causes | Spot size | | Part-A | Part-B | |
| Spot | B/W spot in glass or protection sheet, foreign mat. Pin hole | D ≤ 0.25mm | | Ignore | Ignore | |
| | | 0.25mm < D ≤ 0.4mm | | 4 | | |
| | | 0.4mm < D | | 0 | | |
| Scratch or line defect | Scratch on glass or Scratch on FPL or Particle is Protection sheet. | Length | Width | Part-A | Ignore | |
| | | L ≤ 2.0mm | W ≤ 0.2 mm | Ignore | | |
| | | 2.0 mm < L ≤ 5.0mm | 0.2 mm < W ≤ 0.3mm | 2 | | |
| | | 5.0 mm < L | 0.3mm < W | 0 | | |
| Air bubble | Air bubble | D1, D2 ≤ 0.2 mm | | Ignore | Ignore | |
| | | 0.2 mm < D1, D2 ≤ 0.35mm | | 4 | | |
| | | 0.35mm < D1, D2 | | 0 | | |
| Side Fragment |  | | | | | |
| | X ≤ 5mm, Y ≤ 1mm & display is ok, Ignore | | | | | |

Remarks: Spot define: That only can be seen under WS or DS defects.

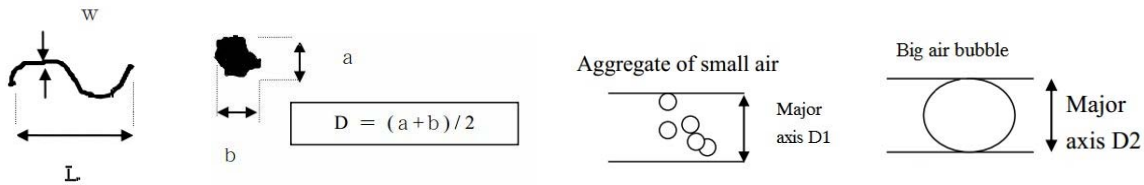
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot: $W > 1/4L$ Scratch or line defect: $W \leq 1/4L$

Definition for L/W and D (major axis)

FPC bonding area pad doesn't allowed visual inspection.



Note: AQL = 0.4

13. Packing

