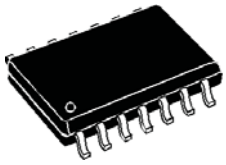
L6564H

High voltage startup transition-mode PFC

Datasheet – production data

Features

- Onboard 700 V startup source
- Fast “bi-directional” input voltage feedforward ($1/V^2$ correction)
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- AC brownout detection
- Low (≤100 µA) startup current
- 6 mA max. operating bias current
- 1% (@ T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO-14 package



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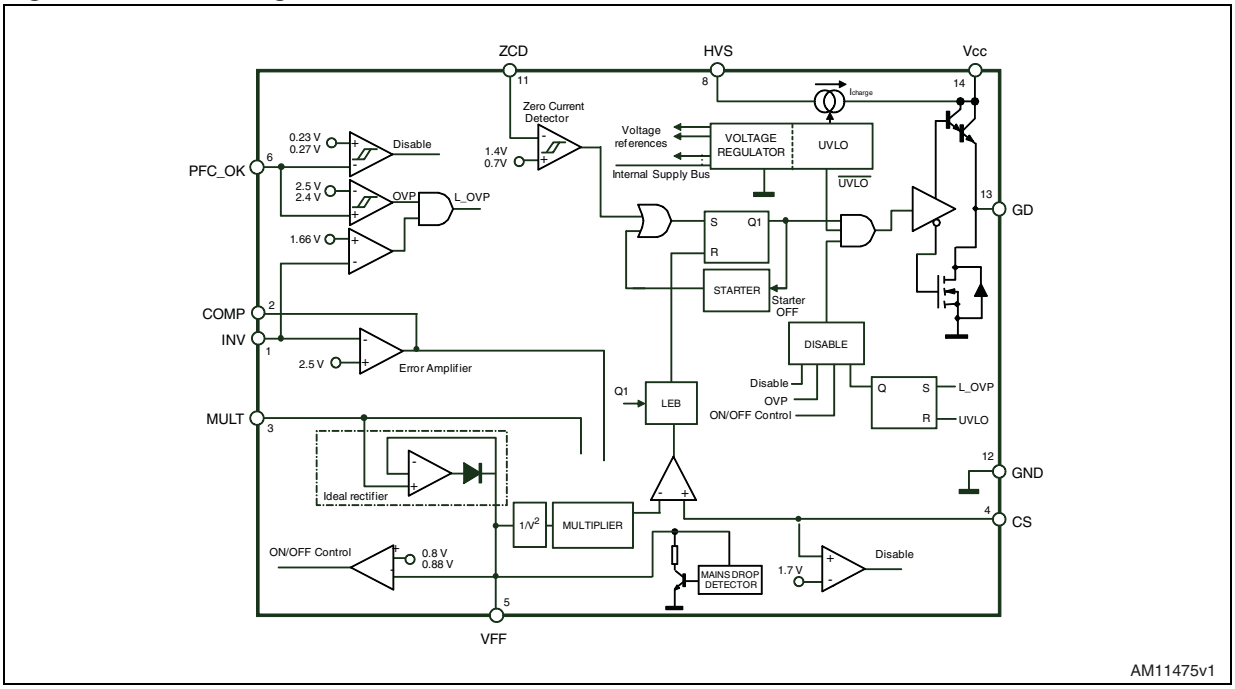
Application

- PFC pre-regulators for:
  - High-end AC-DC adapter/charger
  - IEC61000-3-2 or JEITA-MITI compliant SMPS, in excess of 400 W
  - SMPS for LED luminaires

Figure 1. Block diagram



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1 Description

The L6564H is a current-mode PFC controller operating in transition mode (TM) which embeds the same features existing in the L6564 with the addition of a high voltage startup source. These functions make the IC especially suitable for applications that must be compliant with energy saving regulations and where the PFC preregulator works as the master stage.

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @T_J = 25 °C) internal voltage reference. The loop stability is optimized by the voltage feedforward function ($1/V^2$ correction), which, in this IC, uses a proprietary technique that also considerably improves line transient response in the case of both mains drops and surges (“bi-directional”).

In addition to overvoltage protection able to control the output voltage during transient conditions, the IC also provides protection against feedback loop failures or erroneous settings. Other onboard protection functions allow brownout conditions and boost inductor saturation to be safely handled.

The totem pole output stage, capable of a 600 mA source and 800 mA sink current, is suitable for a high power MOSFET or IGBT drive. This, combined with the other features and the possibility to operate with ST's proprietary fixed-off-time control, makes the device an excellent solution for SMPS up to 400 W that requires compliance with EN61000-3-2 and JEITA-MITI standards.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HVS}	8	Voltage range (referred to ground)	-0.3 to 700	V
I_{HVS}	8	Output current	Self-limited	I_{HVS}
V_{CC}	14	IC supply voltage (Icc ≤ 20 mA)	Self-limited	V
---	1, 3, 6	Max. pin voltage (Ipin ≤1 mA)	Self-limited	V
---	2, 4, 5	Analog inputs and outputs	-0.3 to 8	V
I_{ZCD}	11	Zero current detector max. current	-10 (source) 10 (sink)	mA
VFF pin	5	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” acceptance criteria: “normal performance”	+/- 1750	V
Other pins	1 to 4 6, 8, 11 to 14		+/- 2000	V

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction-to-ambient	120	°C/W
Ptot	Power dissipation @T_A = 50 °C	0.75	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Pin connection

Figure 2. Pin connection

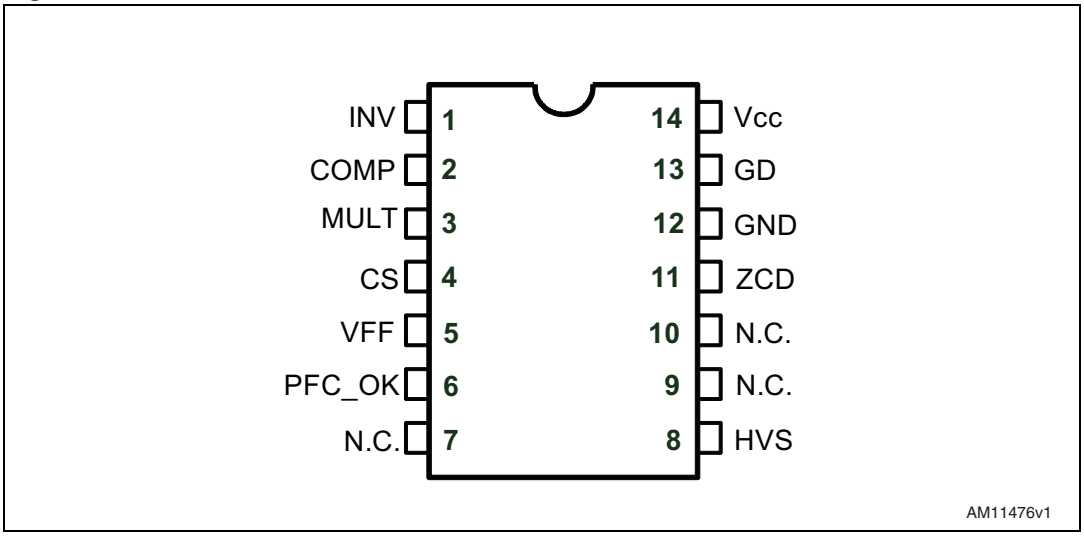


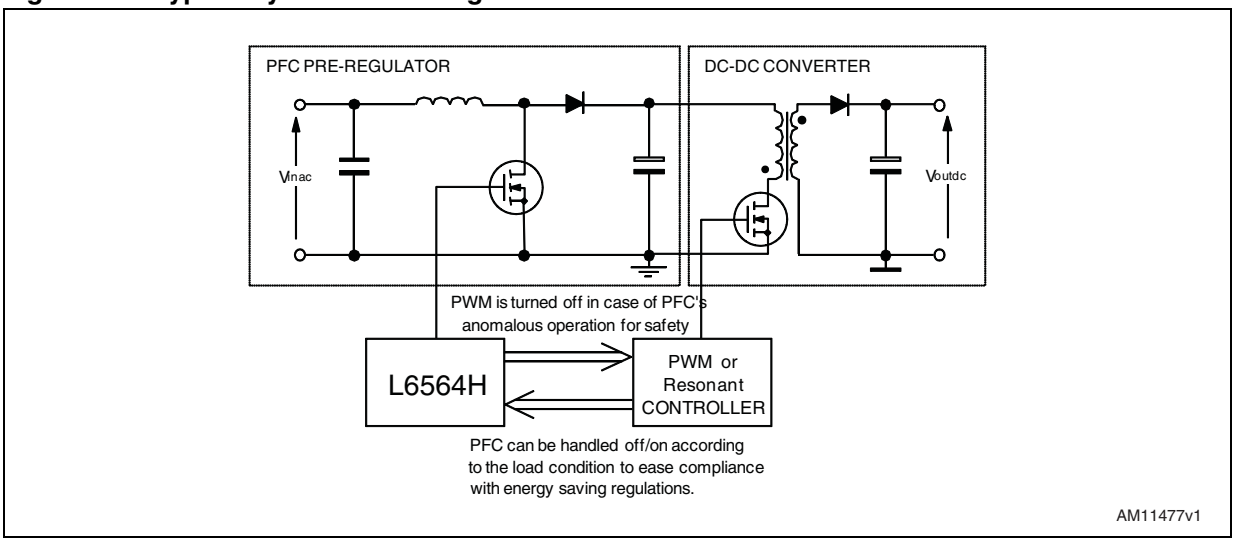
Table 3. Pin description

n°	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD. To avoid an uncontrolled rise of the output voltage at zero load, when the voltage on the pin falls below 2.4 V the gate driver output is inhibited (burst-mode operation).
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET turn-off. A second comparison level at 1.7 V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage on the MULT pin (3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND but with a resistor ranging from 100 KΩ (minimum) to 2 MΩ (maximum).

Table 3. Pin description (continued)

n°	Name	Function
6	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V, the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if at the same time the voltage of the INV pin falls below 1.66 V, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling V_{CC}. bringing its value lower than 6 V before moving up to the turn-on threshold. If the voltage on this pin is brought below 0.23 V, the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can be used as a remote on/off control input.
7	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
8	HVS	High voltage startup. The pin, able to withstand 700 V, is to be tied directly to the rectified mains voltage. A 1 mA internal current source charges the capacitor connected between the V_{CC} pin (14) and the GND pin (12) until the voltage on the V_{CC} pin reaches the startup threshold, it is then shut down. Normally, the generator is re-enabled when the V_{CC} voltage falls below 6 V to ensure a low power throughput during short-circuit. Otherwise, when a latched protection is tripped the generator is re-enabled as V_{CC} reaches the UVLO threshold to keep the latch supplied.
9	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
10	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
11	ZCD	Boost inductor demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET turn-on.
12	GND	Ground. Current return for both the signal part of the IC and the gate driver.
13	GD	Gate driver output. The totem pole output stage is able to drive Power MOSFETs and IGBTs with a peak current of 600 mA source and 800 mA sink. The high level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages.
14	V_{CC}	Supply voltage of both the signal part of the IC and the gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.

Figure 3. Typical system block diagram



4 Electrical characteristics

(T_J = -25 to 125 °C, V_{CC}= 12 V, C_O = 1 nF between pin GD and GND, C_{FF} = 1 µF and R_{FF} = 1 MΩ between pin VFF and GND; unless otherwise specified.)

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	10.3		22.5	V
V_{CCOn}	Turn-on threshold	(1)	11	12	13	V
V_{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
$V_{CCrestart}$	V_{CC} for resuming from latch	OVP latched	5	6	7	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener voltage	Icc = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, V_{CC} = 10 V		90	150	µA
I_q	Quiescent current	After turn-on, V_{MULT} = 1 V		4	5	mA
I_{CC}	Operating supply current	@ 70 kHz		5	6.0	mA
I_{qdis}	Idle state quiescent current	V_{PFC_OK}> $V_{PFC\_OK\_S}$ AND V_{INV}<V_{FFD}		180	280	µA
		V_{PFC_OK}<$V_{PFC\_OK\_D}$		1.5	2.2	mA
I_q	Quiescent current	V_{PFC_OK}>$V_{PFC\_OK\_S}$ OR V_{COMP} < 2.3 V		2.2	3	mA
High voltage startup generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700			V
$V_{HVstart}$	Start voltage	IV_{CC} < 100 µA	65	80	100	V
I_{charge}	V_{CC} charge current	V_{HV} > $V_{Hvstart}$, V_{CC}> 3 V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	V_{HV} > $V_{Hvstart}$, V_{CC}> 3 V			1.6	mA
		V_{HV} > $V_{Hvstart}$, V_{CC} = 0			0.8	
$I_{HV, OFF}$	OFF-state leakage current	V_{HV} = 400 V			40	µA
$V_{CCrestart}$	V_{CC} restart voltage	V_{CC} falling	5	6	7	V
		(1) IC latched off	8.7	9.5	10.3	
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V		-0.2	-1	µA
V_{MULT}	Linear operation range		0 to 3			V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5		V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} = 0 to 0.4 V, V_{VFF} = 1 V V_{COMP} = upper clamp	1.33	1.66		V/V
K_M	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.375	0.45	0.525	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.3 V < V_{CC} < 22.5 V (2)	2.455		2.545	
	Line regulation	V_{CC} = 10.3 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 4 V		-0.2	-1	µA
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	8	9		V
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	2	4		mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Burst-mode voltage	(1)	2.3	2.4	2.5	
	Lower clamp voltage	I_{SINK} = 0.5 mA (1)	2.1	2.25	2.4	
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			1	µA
t_{LEB}	Leading edge blanking		100	150	250	ns
$td_{(H-L)}$	Delay to output		100	200	300	ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = upper clamp, V_{MULT} =1 V, V_{VFF} = 1 V	1.0	1.08	1.16	V
Vcs_{ofst}	Current sense offset	V_{MULT} = 0, V_{VFF} = 3 V		40	70	mV
		V_{MULT} = 3 V, V_{VFF} = 3 V		20		
Boost inductor saturation detector						
V_{CS_th}	Threshold on current sense	(1)	1.6	1.7	1.8	V
I_{INV}	E/A input pull-up current	After V_{CS} > V_{CS_th}, before restarting	5	10	13	µA
PFC_OK functions						
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.6 V		-0.1	-1	µA
$V_{PFC\_OK\_C}$	Clamp voltage	I_{PFC_OK} = 1 mA	9	9.5		V
$V_{PFC\_OK\_S}$	OVP threshold	(1) voltage rising	2.435	2.5	2.565	V
$V_{PFC\_OK\_R}$	Restart threshold after OVP	(1) voltage falling	2.34	2.4	2.46	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{PFC\_OK\_D}$	Disable threshold	(1) voltage falling	0.12		0.35	V
$V_{PFC\_OK\_D}$	Disable threshold	(1) voltage falling T_J = 25 °C	0.17	0.23	0.29	V
$V_{PFC\_OK\_E}$	Enable threshold	(1) voltage rising	0.15		0.38	V
$V_{PFC\_OK\_E}$	Enable threshold	(1) voltage rising T_J = 25 °C	0.21	0.27	0.32	V
V_{FFD}	V_{INV} feedback failure detection threshold (V_{INV} falling)	$V_{PFC\_OK} > V_{PFC\_OK\_S}$	1.61	1.66	1.71	V
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7		V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)		1.1	1.4	1.9	V
V_{ZCDT}	Triggering voltage (negative-going edge)		0.5	0.7	0.9	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V			1	µA
I_{ZCDsrc}	Source current capability		-2.5	-4		mA
I_{ZCDsnk}	Sink current capability		2.5	5		mA
Startup timer						
t_{START_DEL}	Startup delay	First cycle after wake-up	25	50	75	µs
t_{START}	Timer period		75	150	300	µs
		Restart after $V_{CS} > V_{CS\_th}$	150	300	600	
Voltage feedforward						
V_{VFF}	Linear operation range		1		3	V
ΔV	Dropout V_{MULTpk}-V_{VFF}	V_{CC}< V_{CCOn}			800	mV
		V_{CC} > or = to V_{CCOn}			20	
ΔV_{VFF}	Line drop detection threshold	Below peak value	40	70	100	mV
ΔV_{VFF}	Line drop detection threshold	Below peak value T_J = 25 °C	50	70	90	mV
R_{DISCH}	Internal discharge resistor	T_J = 25 °C	7.5	10	12.5	kΩ
			5		20	
V_{DIS}	Disable threshold	(1) voltage falling	0.745	0.8	0.855	V
V_{EN}	Enable threshold	(1) voltage rising	0.845	0.88	0.915	V
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.8	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_f	Voltage fall time			30	60	ns
t_r	Voltage rise time			45	110	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; V_{CC} = 20 V	10	12	15	V
	UVLO saturation	V_{CC}= 0 to V_{CCOn}, I_{sink}= 2 mA			1.1	V

1. Parameters tracking each other.
2. The multiplier output is given by:

$$V_{cs} = V_{CS\_Ofst} + K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$$

5 Typical electrical performance

Figure 4. IC consumption vs. V_{CC}

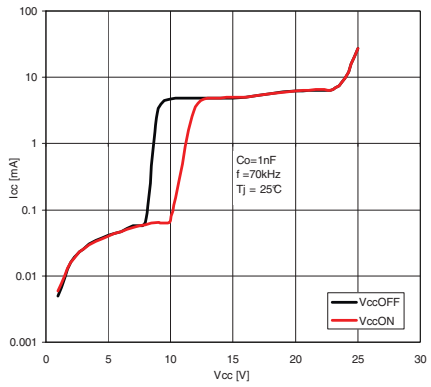


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Figure 5. IC consumption vs. T_J

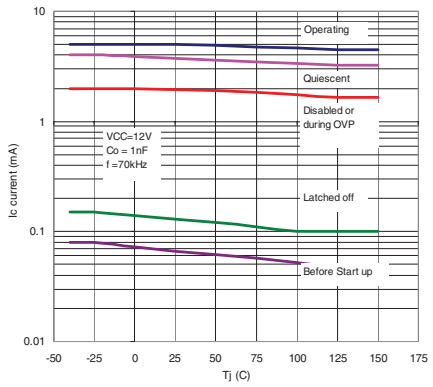

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Figure 6. V_{CC} Zener voltage vs. T_J

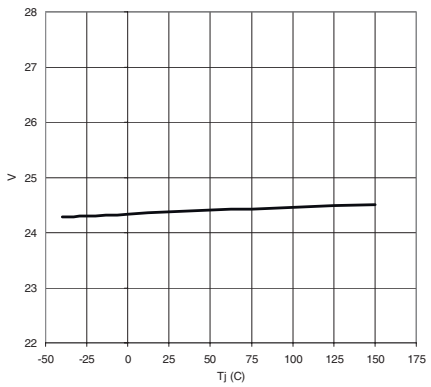

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Figure 7. Startup and UVLO vs. T_J

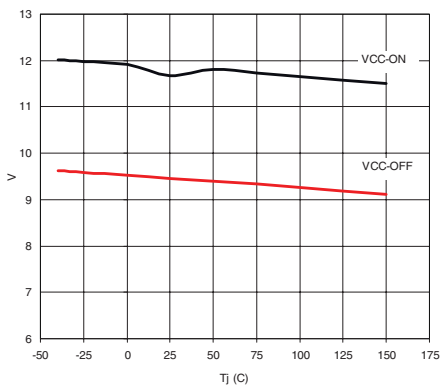

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Figure 8. Feedback reference vs. T_J

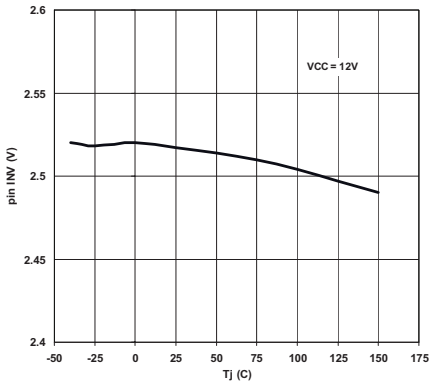

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Figure 9. E/A output clamp levels vs. T_J

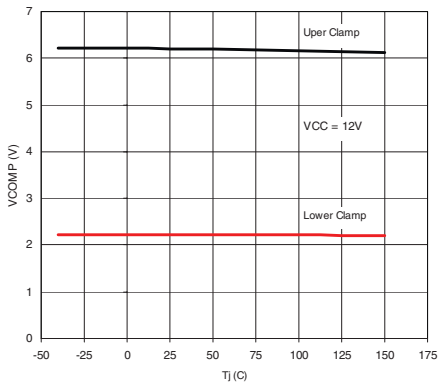

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Figure 10. UVLO saturation vs. T_J

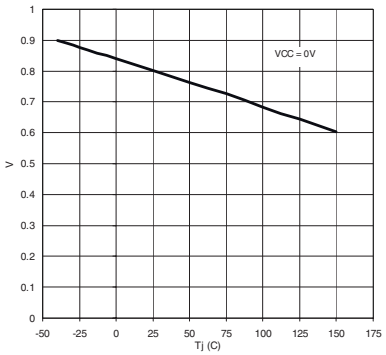

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Figure 11. OVP levels vs. T_J

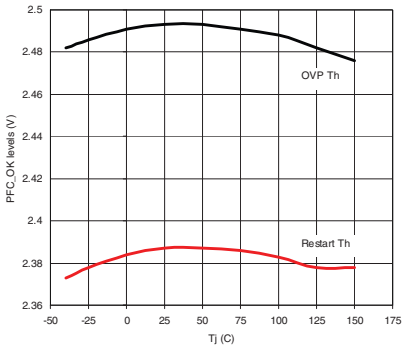

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Figure 12. Inductor saturation threshold vs. T_J

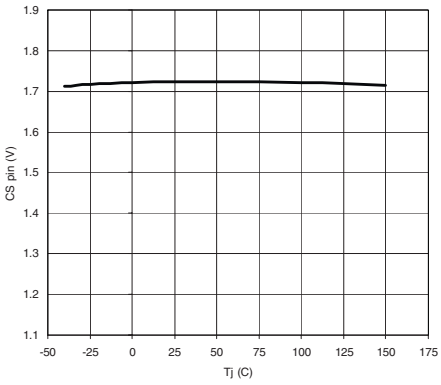

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Figure 13. Vcs clamp vs. T_J

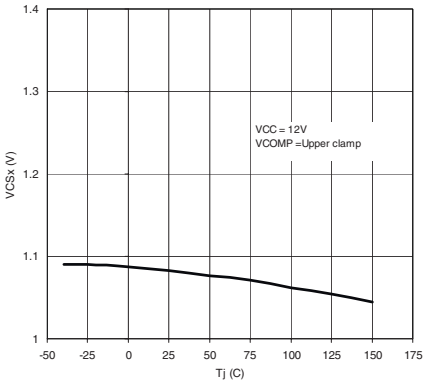

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Figure 14. ZCD sink/source capability vs. T_J

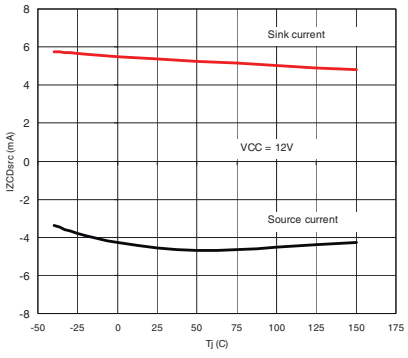

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Figure 15. ZCD clamp level vs. T_J

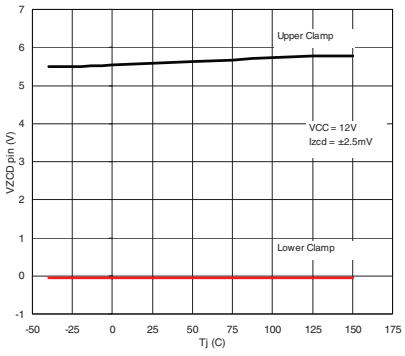

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Figure 16. R discharge vs. T_J

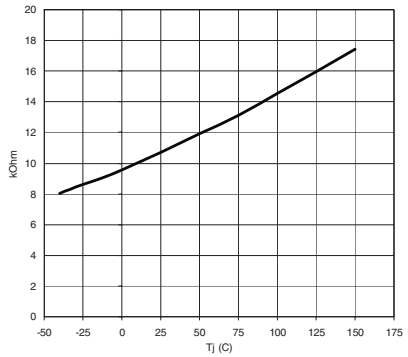

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Figure 17. Line drop detection threshold vs. T_J

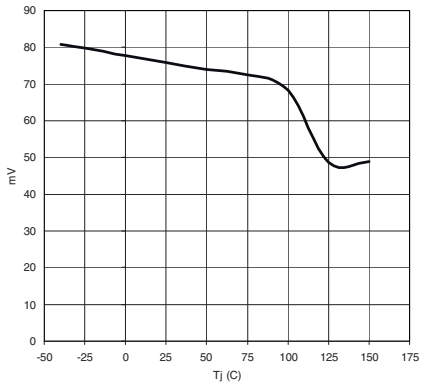

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Figure 18. V_{MULTpk} - V_{VFF} dropout vs. T_J

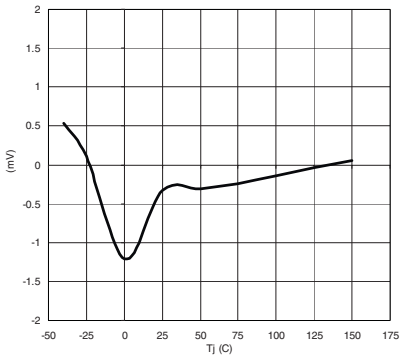

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Figure 19. PFC_OK threshold vs. T_J

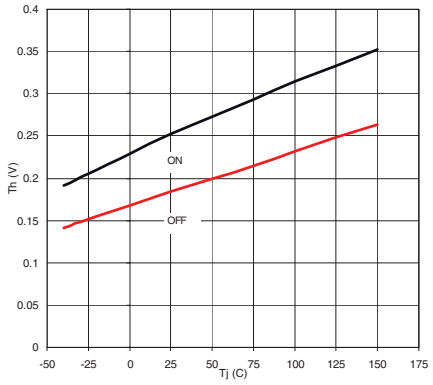

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Figure 20. PFC_OK FFD threshold vs. T_J

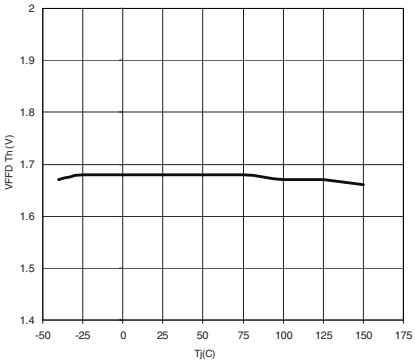

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Figure 21. Multiplier characteristics @V_{FF}=1 V

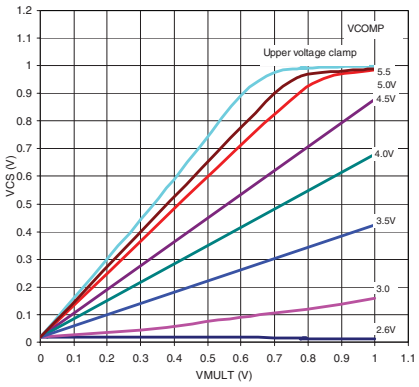

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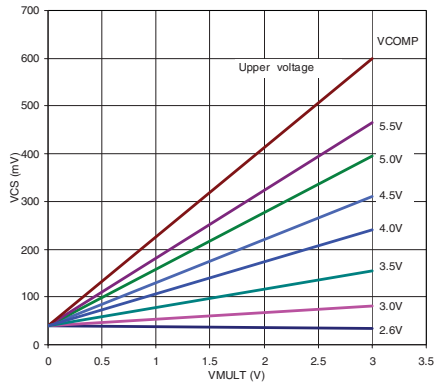
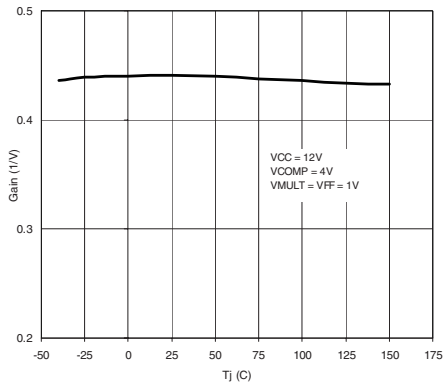
Figure 22. Multiplier characteristics @V_{FF}=3 V



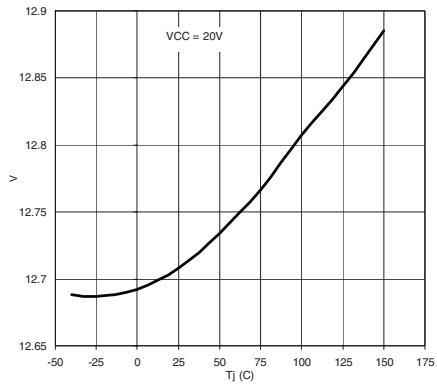
AM11450v1

Figure 23. Multiplier gain vs. T_J



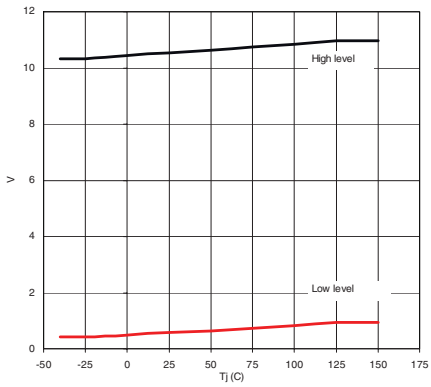
AM11451v1

Figure 24. Gate drive clamp vs. T_J



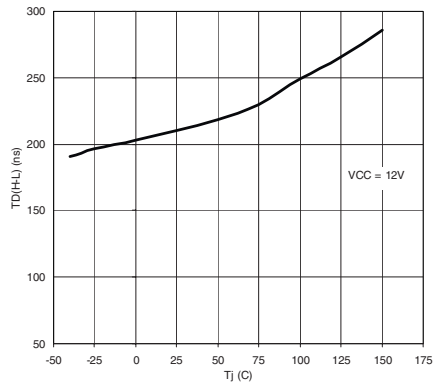
AM11452v1

Figure 25. Gate drive output saturation vs. T_J



AM11453v1

Figure 26. Delay to output vs. T_J



AM11454v1

Figure 27. Startup timer period vs. T_J

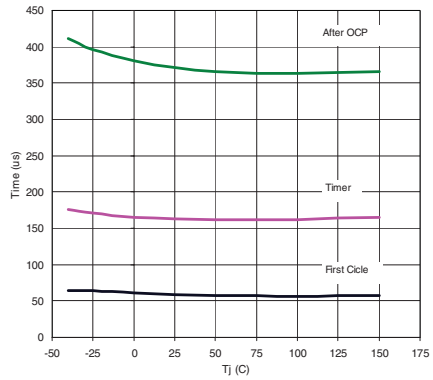


Figure 28. HV start voltage vs. T_J

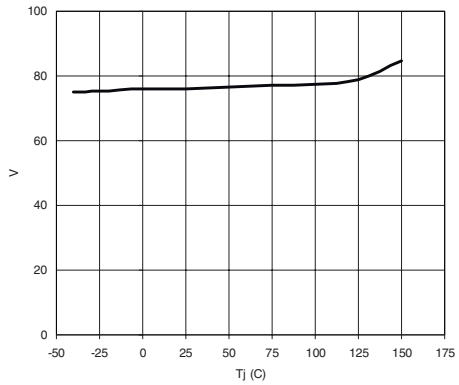


Figure 29. V_{CC} restart voltage vs. T_J

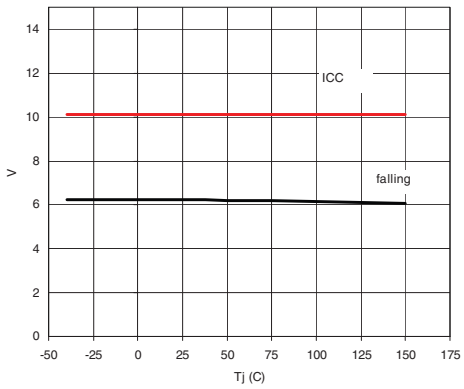
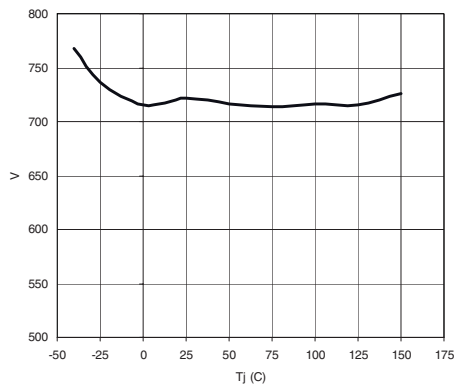


Figure 30. HV breakdown voltage vs. T_J



6 Application information

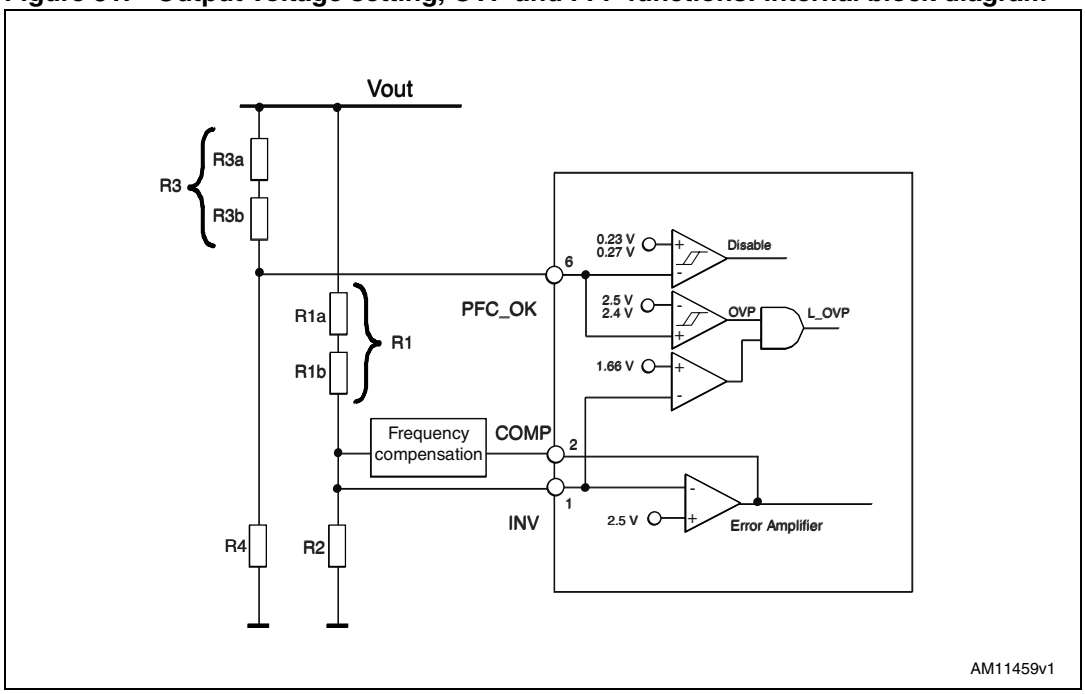
6.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage V_o of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. A pin of the device (PFC_OK) has been dedicated to monitor the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 31*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum V_o that can be expected.

Example 1: V_o = 400 V, V_{OX} = 434 V. Select: R3 = 8.8 MΩ; then: R4 = 8.8 MΩ·2.5/(434-2.5) = 51 kΩ

When this function is triggered, the gate drive activity is immediately stopped until the voltage on the PFC_OK pin drops below 2.4 V. Note that R1, R2, R3 and R4 can be selected without any constraints. The unique criterion is that both dividers must sink a current from the output bus which needs to be significantly higher than the bias current of both INV and PFC_OK pins.

Figure 31. Output voltage setting, OVP and FFP functions: internal block diagram



6.2 Feedback failure protection (FFP)

The OVP function described above handles “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. If the overvoltage is generated by a feedback disconnection, for instance when the upper resistor of the output divider (R1) fails to open, the comparator detects the voltage at the INV pin. If the voltage is lower than 1.66 V and the OVP is active, the FFP is triggered, the gate drive activity is

immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA, and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the V_{CC} voltage of the L6564H goes below 6 V.

The PFC_OK pin doubles its function as a not-latched IC 'disable': a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

Note that these functions offer complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK voltage divider in a short condition or open, or the PFC_OK pin left floating, results in shutting down the IC and stopping the pre-regulator.

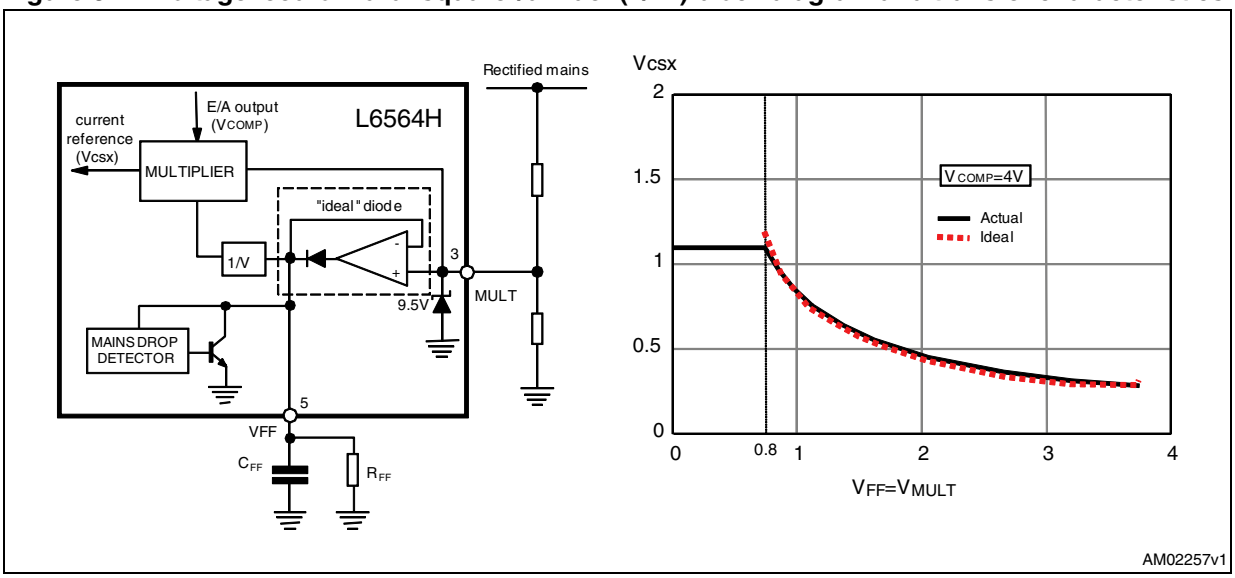
6.3 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to a large trade-off in the design.

For example, setting the gain of the error amplifier to get f_c = 20 Hz @ 264 Vac means having $f_c \approx$ 4 Hz @ 88 Vac, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feedforward can compensate for the gain variation with the line voltage and allow the minimizing of all the issues mentioned above. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 32*).

Figure 32. Voltage feedforward: squarer/divider ($1/V^2$) block diagram and transfer characteristics



In this way a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which significantly improves dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated is affected by a considerable amount of ripple at twice the mains frequency which causes distortion of the current reference (resulting in high HD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6564H realizes a new voltage feedforward that, with a technique that makes use of just two external parts, strongly minimizes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor R_{FF}, both connected from the VFF pin (#5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (#3). In this way, in the case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode; in the case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges C_{FF} avoiding a long settling time before reaching the new voltage level. The discharge of C_{FF} is stopped as its voltage equals the voltage on the MULT pin or if the voltage on the VFF pin falls below 0.88 V, to prevent the “brownout protection” function from being improperly activated (see *Section 6.6: Power management/housekeeping functions*).

As a result of the VFF pin functionality, an acceptably low steady-state ripple and low current distortion can be achieved with a limited undershoot or overshoot on the pre-regulator output.

The twice-mains-frequency ($2 \cdot f_L$) ripple appearing across C_{FF} is triangular with a peak-to-peak amplitude that, with good approximation, is given by:

$$\Delta V_{FF} = \frac{2\,V_{MULTpk}}{1 + 4 f_L R_{FF} C_{FF}}$$

where f_L is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its $2 \cdot f_L$ component, is:

$$D_3\% = \frac{100}{2\pi\, f_L R_{FF} C_{FF}}$$

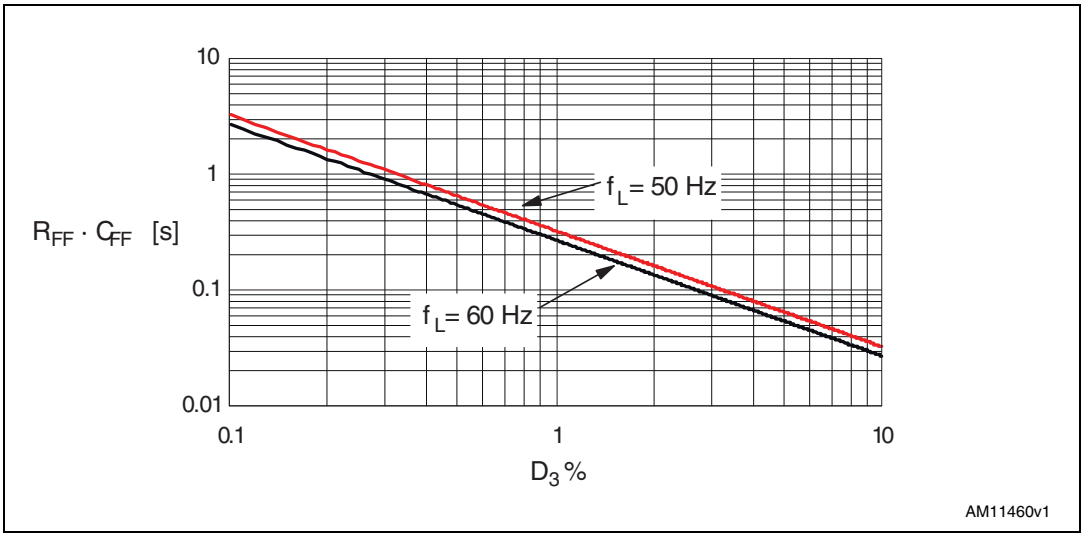
Figure 33 shows a diagram that helps in choosing the time constant $R_{FF} \cdot C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion. Note that there is a minimum value for the time constant $R_{FF} \times C_{FF}$ below which improper activation of the VFF fast discharge may occur. In fact, the twice-mains frequency ripple across C_{FF} under steady-state conditions must be lower than the minimum line drop detection threshold (DVVFF_min = 40 mV). Therefore: must be lower than the minimum line drop detection threshold (ΔV_{FF_min} = 40 mV).

So:

$$R_{FF} \quad C_{FF} > \frac{2\frac{V_{MULTpk\_max}}{\Delta V_{VFF\_min}} - 1}{4 f_{L\_min}}$$

Always connect R_{FF} and C_{FF} to the pin, the IC does not work properly if the pin is either left floating or connected directly to ground.

Figure 33. R_{FF}·C_{FF} as a function of 3rd harmonic distortion introduced in the input current



6.4 THD optimizer circuit

The L6564H is provided with a special circuit that reduces the conduction dead-angle occurring at the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (total harmonic distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 34 shows the internal block diagram of the THD optimizer circuit.

Figure 34. THD optimizer circuit

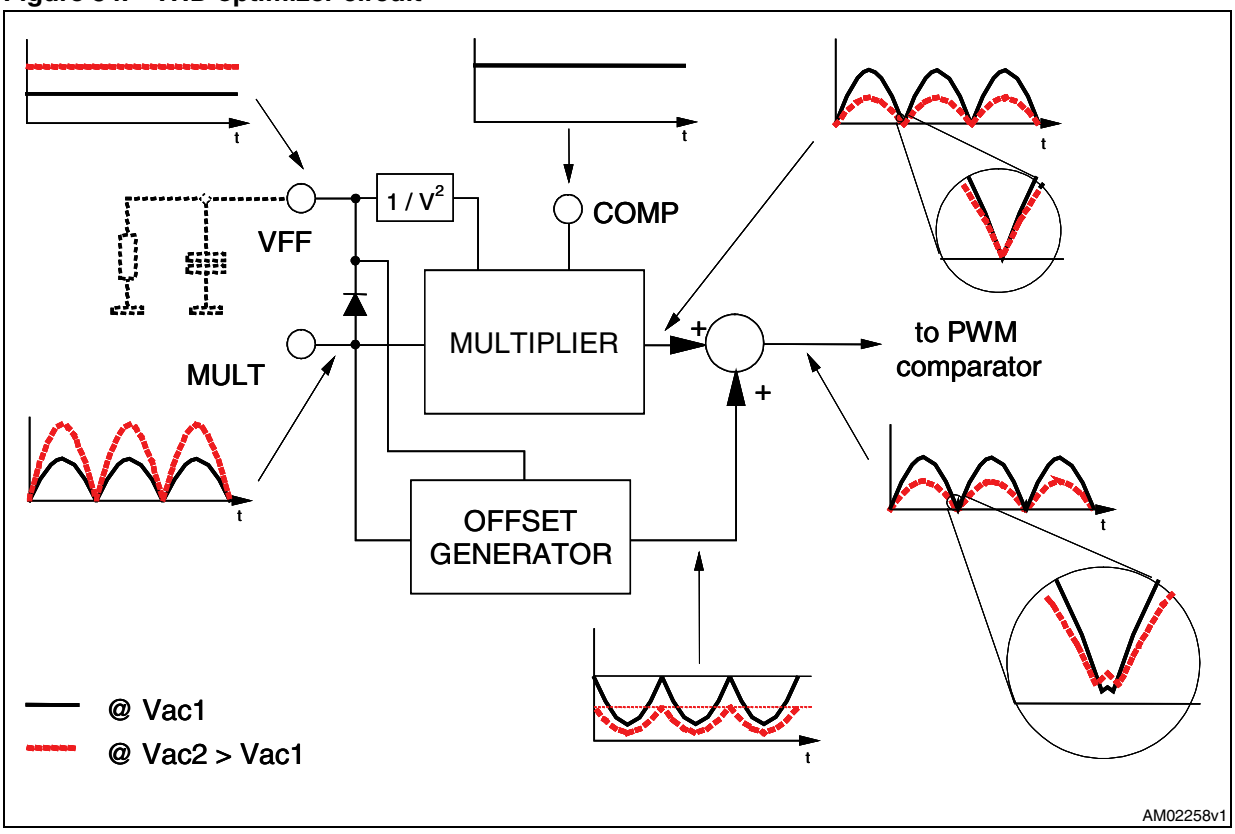
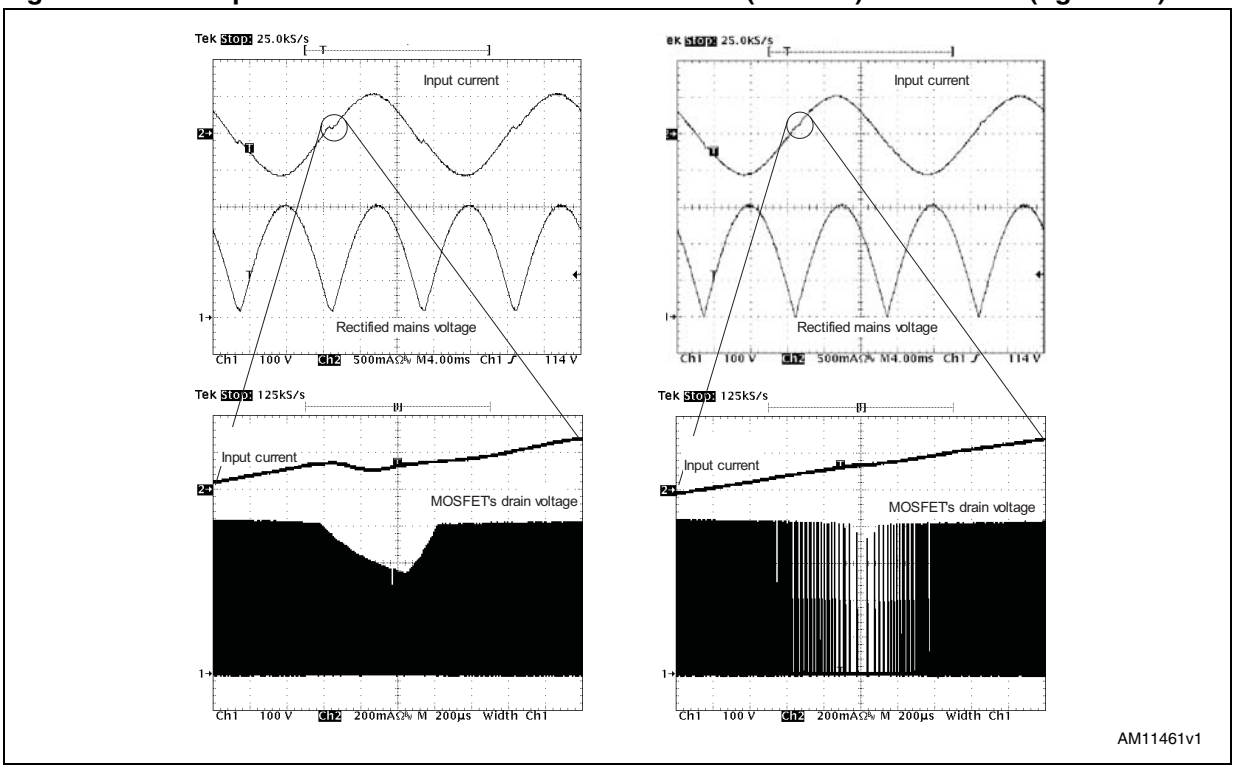


Figure 35. THD optimization: standard TM PFC controller (left side) and L6564H (right side)



Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the VFF pin (see *Section 6.3*) so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer worsens.

The effect of the circuit is shown in *Figure 35*, where the key waveforms of a standard TM PFC controller are compared to those of this chip.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - therefore reducing the effectiveness of the optimizer circuit.

6.5 Inductor saturation detection

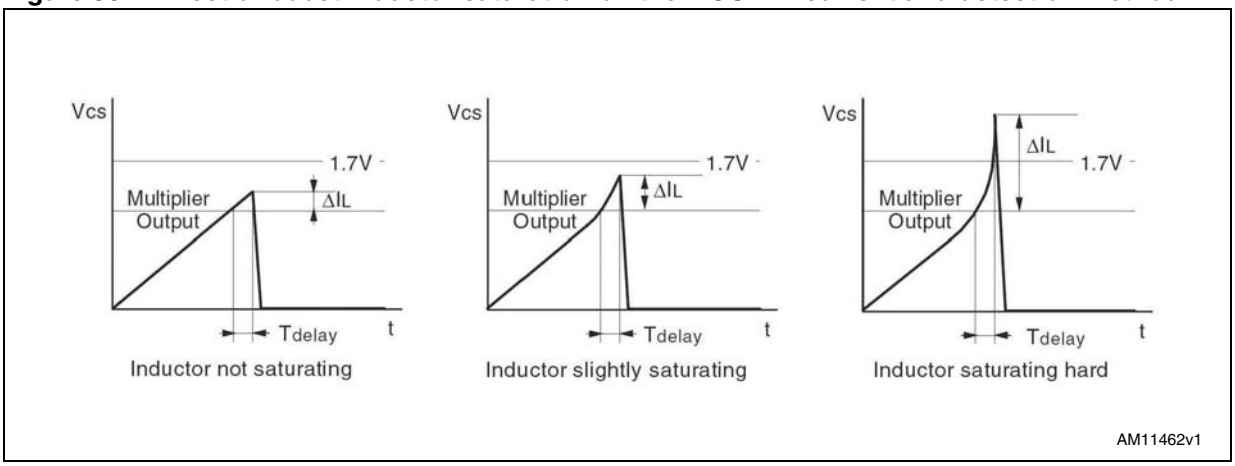
The boost inductor's hard saturation may be a fatal event for a PFC pre-regulator: the current up-slope becomes so large (50-100 times steeper, see *Figure 36*) that during the current sense propagation delay the current may reach abnormally high values. The voltage drop caused by this abnormal current on the sense resistor reduces the gate-to-source voltage, so that the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after few switching cycles.

However, in some applications such as AC-DC adapters, where the PFC pre-regulator is turned off at light load for energy saving reasons, even a well-designed boost inductor may

occasionally slightly saturate when the PFC stage is restarted because of a larger load demand. This happens when the restart occurs at an unfavorable line voltage phase, i.e. when the output voltage is significantly below the rectified peak voltage. As a result, in the boost inductor, the inrush current coming from the bridge rectifier adds to the switched current and, furthermore, there is little or no voltage available for demagnetization.

To cope with a saturated inductor, the L6564H is provided with a second comparator on the current sense pin (CS, pin 4) that stops the IC if the voltage, normally limited within 1.1 V, exceeds 1.7 V. After that, the IC attempts to restart through the internal starter circuitry; the starter repetition time is twice the nominal value to guarantee lower stress for the inductor and boost diode. Hence, system safety is considerably increased.

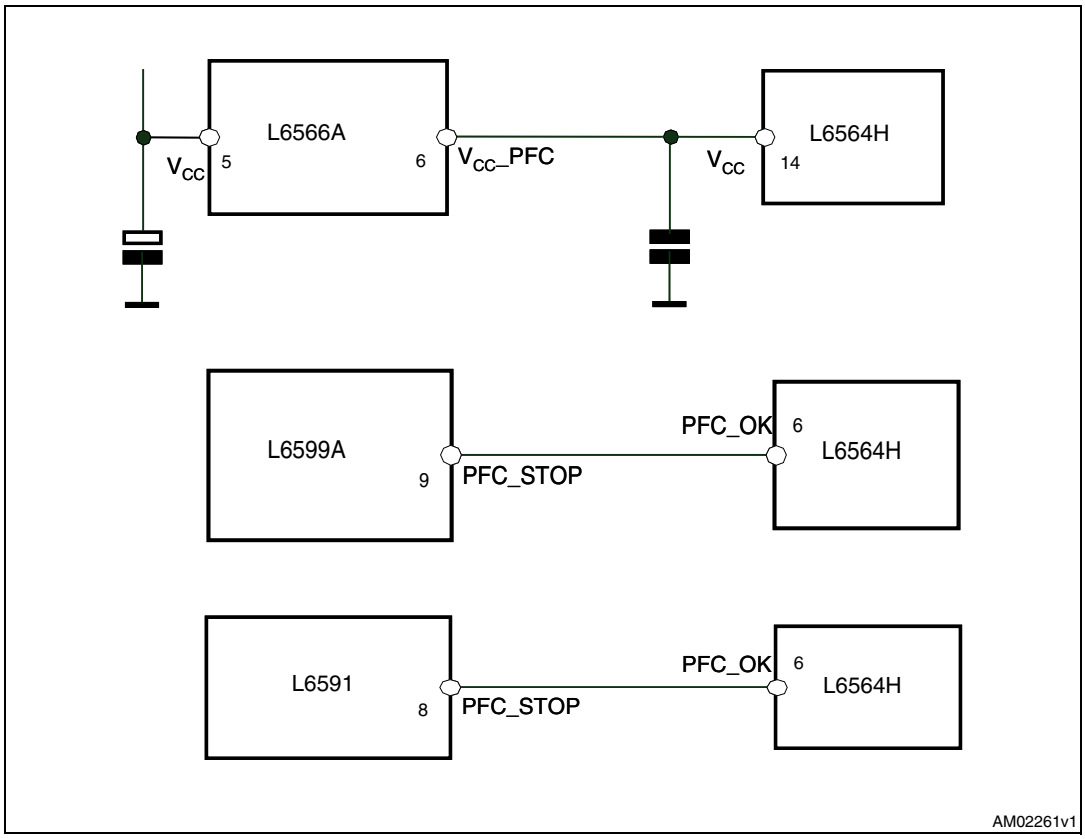
Figure 36. Effect of boost inductor saturation on the MOSFET current and detection method



6.6 Power management/housekeeping functions

A communication line with the control IC of the cascaded DC-DC converter can be established via the disable function included in the PFC_OK pin (see *Section 6.2* for more details). This line is typically used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6564H in case of light load and to minimize the no-load input consumption. Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. Interface circuits are shown in *Figure 37*. Needless to say, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage.

Figure 37. Interface circuits that let the DC-DC converter's controller IC disable the L6564H

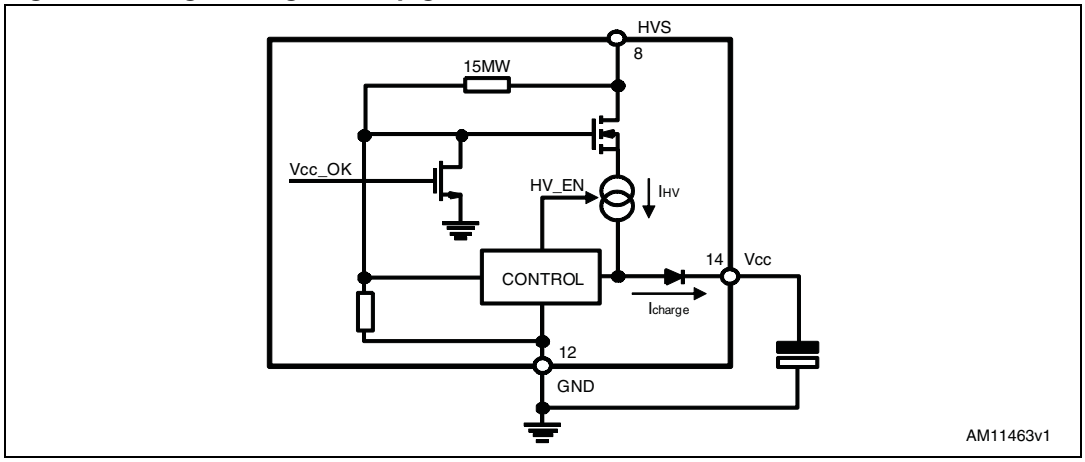


Another function available is the brownout protection which is basically a not-latched shutdown function that is activated when a condition of mains undervoltage is detected. This condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to function in open loop and this may be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power-down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shut down the unit in case of brownout. The brownout threshold is internally fixed at 0.8 V and is sensed on the VFF pin (#5) during the voltage falling and an 80 mV threshold hysteresis prevents rebounding at input voltage turn-off. In *Table 5* it is possible to find a summary of all of the above mentioned working conditions that cause the device to stop operating.

7 High voltage startup generator

Figure 38 shows the internal schematic of the high voltage startup generator (HV generator). It is made up of a high voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

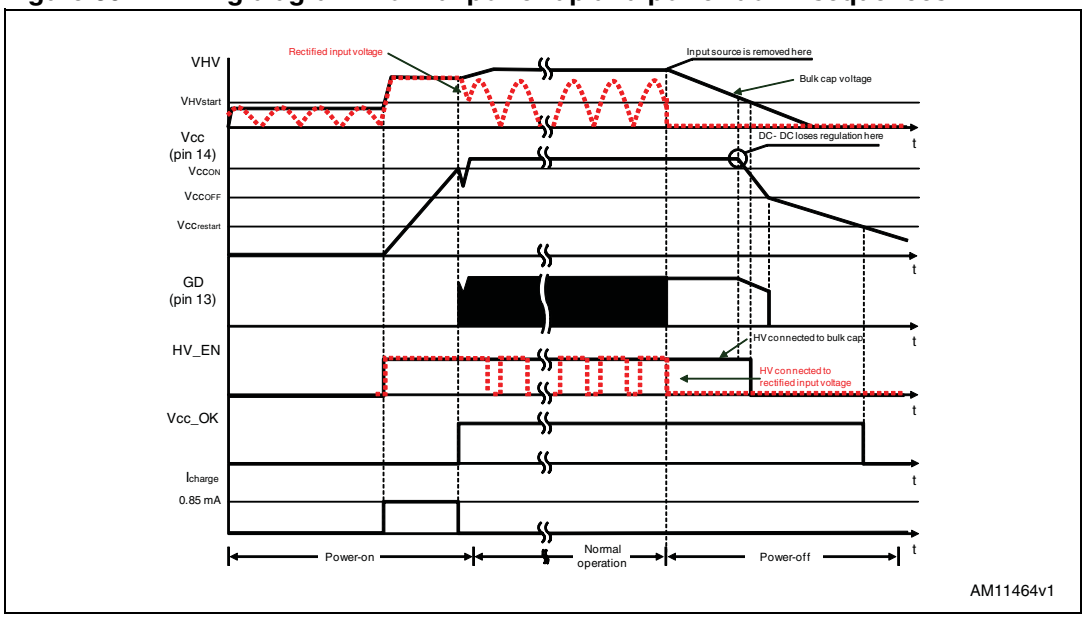
Figure 38. High voltage startup generator: internal schematic



The HV generator is physically located on a separate chip, made with BCD offline technology able to withstand 700 V, controlled by a low voltage chip, where all of the control functions reside.

With reference to the timing diagram of *Figure 39*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus device consumption, charges the bypass capacitor connected from the V_{CC} pin (14) to ground and causes its voltage to rise almost linearly.

Figure 39. Timing diagram: normal power-up and power-down sequences



As the V_{CC} voltage reaches the startup threshold (12 V typ.) the low voltage chip starts operating and the HV generator is cut off by the V_{CC}_OK signal asserted high. The device is powered by the energy stored in the V_{CC} capacitor until the self-supply circuit (we assume that it is made with an auxiliary winding in the transformer of the cascaded DC-DC converter and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MΩ resistor (≈ 10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard startup circuit made with external dropping resistors.

At converter power-down the DC-DC converter loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. V_{CC} then drops and stop IC activity as it falls below the UVLO threshold (9.5 V typ.). The V_{CC}_OK signal is de-asserted as the V_{CC} voltage goes below a threshold $V_{CCrestart}$ located at about 6 V. The HV generator can now restart. However, if Vin < $V_{HVstart}$, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see *Section 6.6: Power management/housekeeping functions*) is not used.

If the device detects a fault due to feedback failure, the internal $V_{CCrestart}$ is brought up to over the V_{CCOff} (turn-off threshold). As a result, shown in *Figure 40*, the voltage at the V_{CC} pin oscillates between its turn-on and turn-off thresholds until the HV bus is recycled and drops below the startup threshold of the HV generator.

The high voltage startup circuitry is capable of guaranteeing a safe behavior in case of short-circuit present on the DC-DC output when the V_{CC} of both controllers are generated by the same auxiliary inding. *Figure 41* shows how the PFC manages the V_{CC} cycling and the associated power transfer. At short-circuit the auxiliary circuit is no longer able to sustain the V_{CC} which starts dropping; reaching its V_{CCOff} threshold the IC stops switching, reduces consumption and drops more until the $V_{CCrestart}$ threshold is tripped. Now, the high voltage startup generator restarts and when the V_{CC} again crosses its turn-on threshold the IC starts switching. In this manner the power is transferred from mains to PFC output only during a short time for each trep cycle.

Figure 40. High voltage startup behavior during latch-off protection

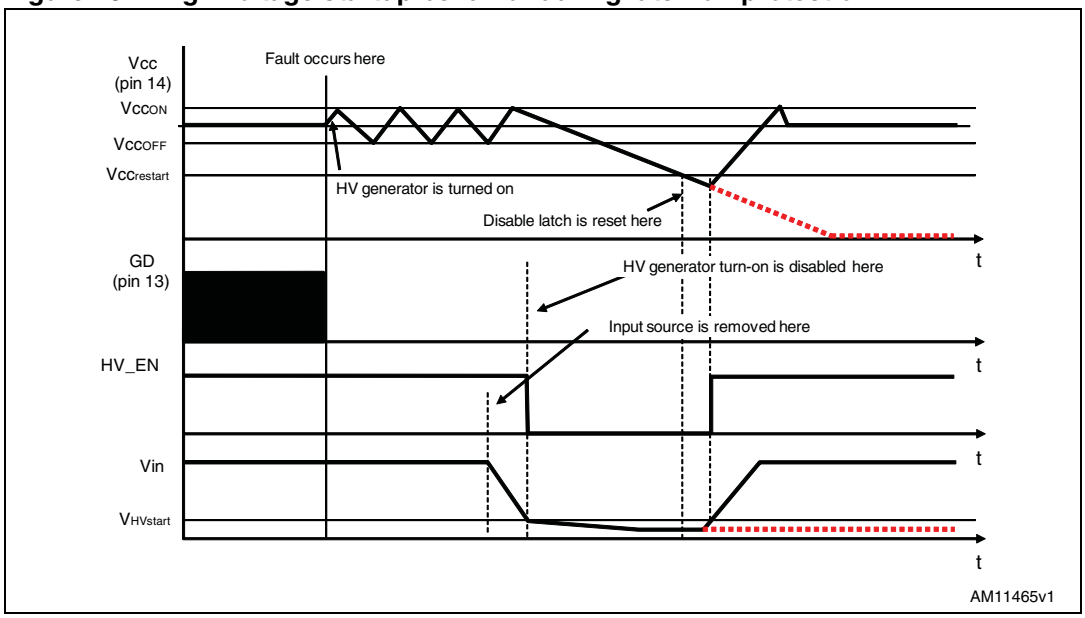


Figure 41. High voltage startup managing the DC-DC output short-circuit

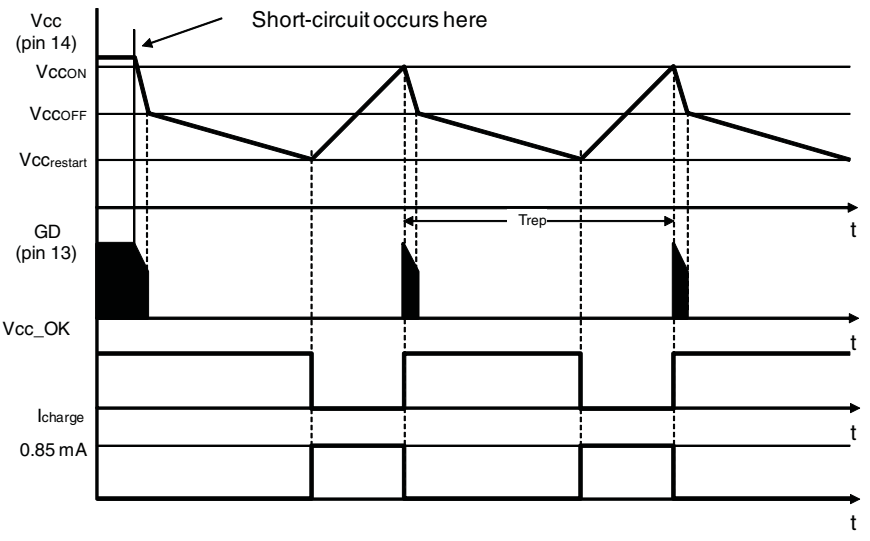


Table 5. Summary of L6564H idle states

Condition	Caused or revealed by	IC behavior	Restart condition	Typical IC consumption
UVLO	$V_{CC} < V_{CCOff}$	Disabled	$V_{CC} > V_{CCOn}$	90 µA
Feedback disconnected	PFC_OK > $V_{PFC\_OK\_S}$ and INV < 1.66 V	Latched	$V_{CC} < V_{CCrestart}$ then $V_{CC} > V_{CCOn}$	180 µA
Standby	PFC_OK < $V_{PFC\_OK\_D}$	Stop switching	PFC_OK > $V_{PFC\_OK\_E}$	1.5 mA
AC brownout	RUN < VDIS	Stop switching	RUN > V_{EN}	1.5 mA
OVP	PFC_OK > $V_{PFC\_OK\_S}$	Stop Switching	PFC_OK < $V_{PFC\_OK\_R}$	2.2 mA
Low consumption	COMP < 2.4 V	Burst mode	COMP > 2.4 V	2.2 mA
Saturated boost inductor	Vcs > V_{CS_th}	Doubled T_{start}	Auto restart	2.2 mA

8 Application examples and ideas

Figure 42. Demonstration board EVL6564H - 100 W, wide-range mains: electrical schematic

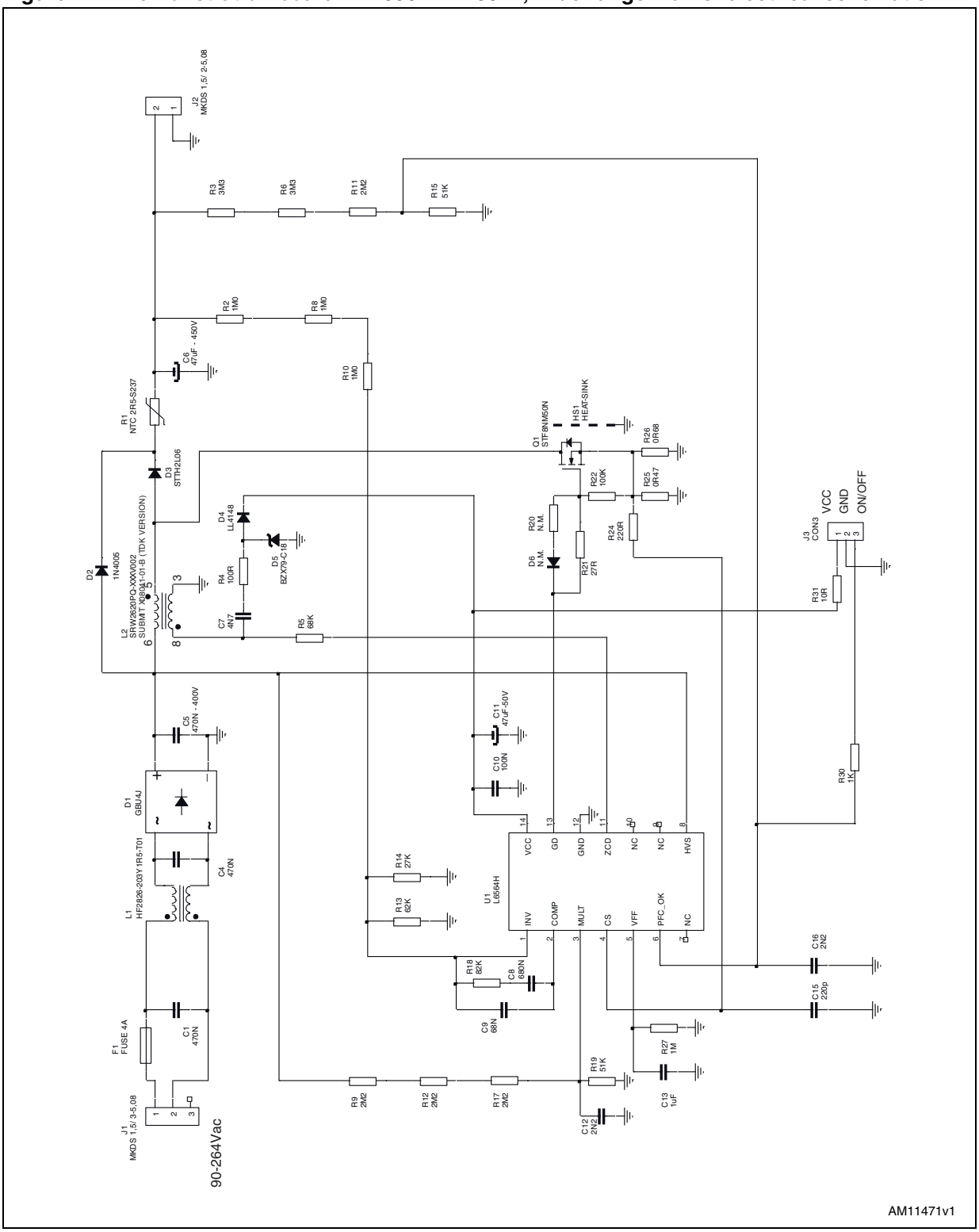


Figure 43. EVL6564H demonstration board: compliance to EN61000-3-2 standard

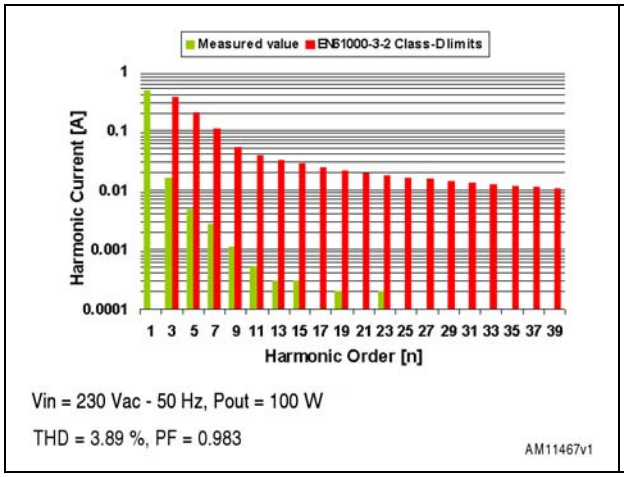


Figure 44. EVL6564H demonstration board: compliance to JEITA-MITI standard

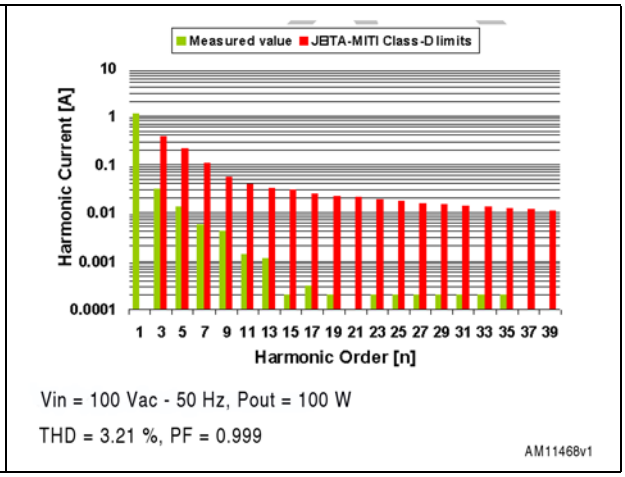


Figure 45. EVL6564H demonstration board: input current waveform @230 V -50 Hz - 100 W load

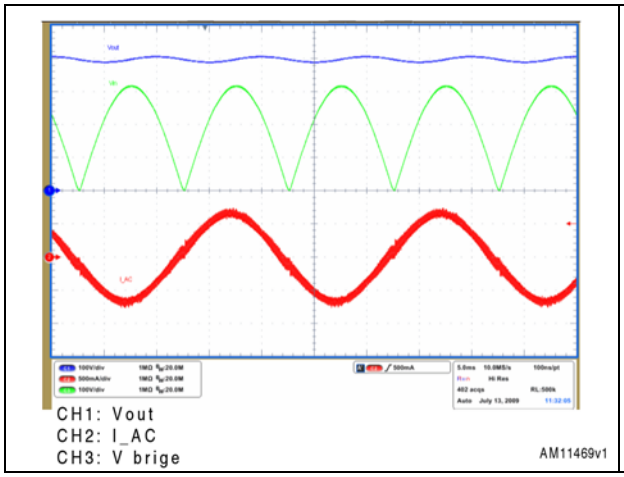
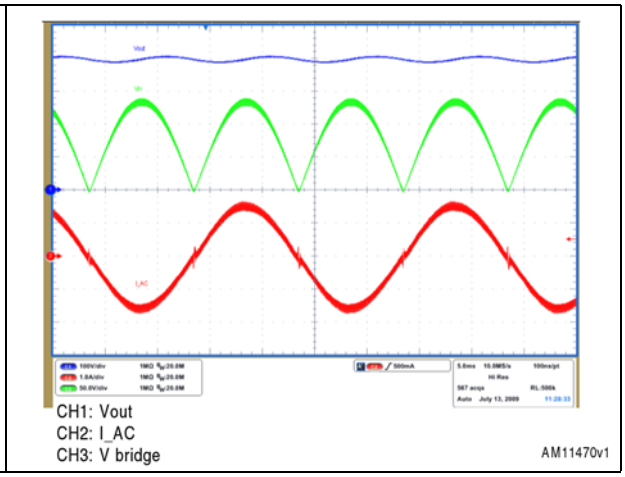


Figure 46. EVL6564H demonstration board: input current waveform @100 V - 50 Hz - 100 W load



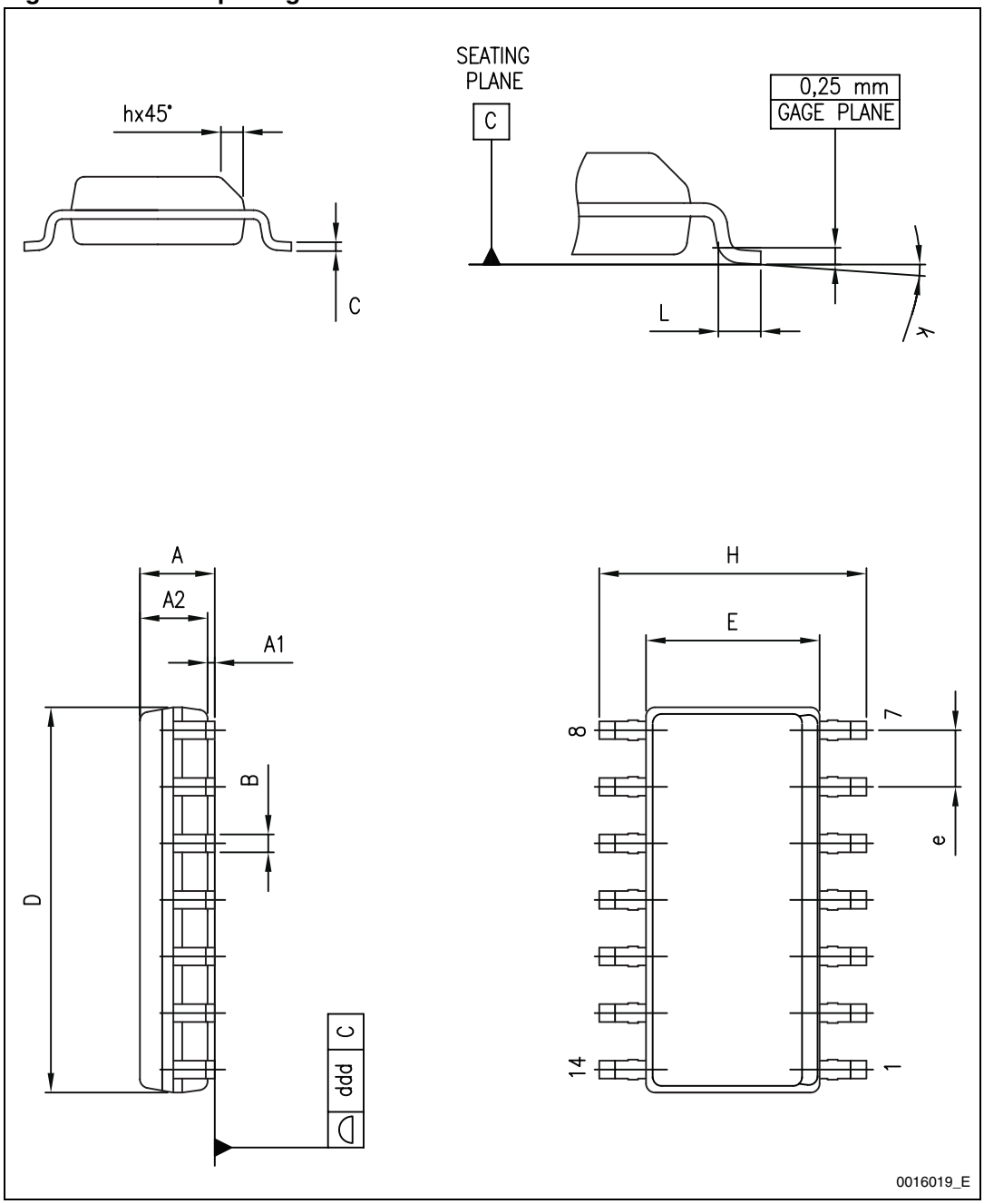
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 6. SO-14 mechanical data

Dim.	Databook (mm.)		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
K	0		8
e		0.40	
ddd			0.10

Figure 47. SO-14 package dimensions



10 Ordering codes

Table 7. Ordering information

Order codes	Package	Packing
L6564H	SO-14	Tube
L6564HTR		Tape and reel

11 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Apr-2012	1	Initial release.
07-Jun-2012	2	Datasheet promoted from preliminary data to production data.

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