TLE 8088 EM

Engine management IC for Small Engines

Data Sheet

Rev 1.0, 2012-10-01

Automotive Power

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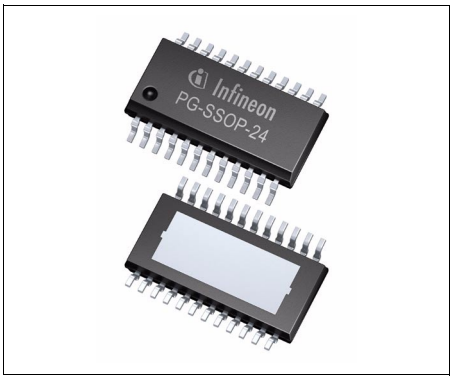
1 Overview



PG-SSOP-24

Features

- Supply 5 V (±2%), 250mA
  - Over-temperature and Over-current Protection
- Watchdog and Reset Function
- K-Line Transceiver
- 1 low side driver for inductive loads with maximum operation current of 2.6A including over-temperature, over-current protection and open load/short to GND in off diagnosis
- 1 low side driver for resistive loads with maximum operation current of 3A including over-temperature and over-current protection
- Small Package PG-SSOP-24 Exposed Pad
- Temperature Range: -40°C to 150°C
- Green Product (RoHS compliant)
- AEC Qualified

Description

TLE8088EM is an engine management IC based on Infineon Smart Power Technology (SPT). It is protected by embedded protection functions and integrates a Power Supply, K-line and power stages to drive different loads in an Engine Management System. It is designed to provide a compact and cost optimized solution for Engine Management and Powertrain Systems. It is specially suitable for one cylinder motorcycle engine management system.

Type	Package	Marking
TLE8088EM	PG-SSOP-24	TLE8088EM

2 Block Diagram

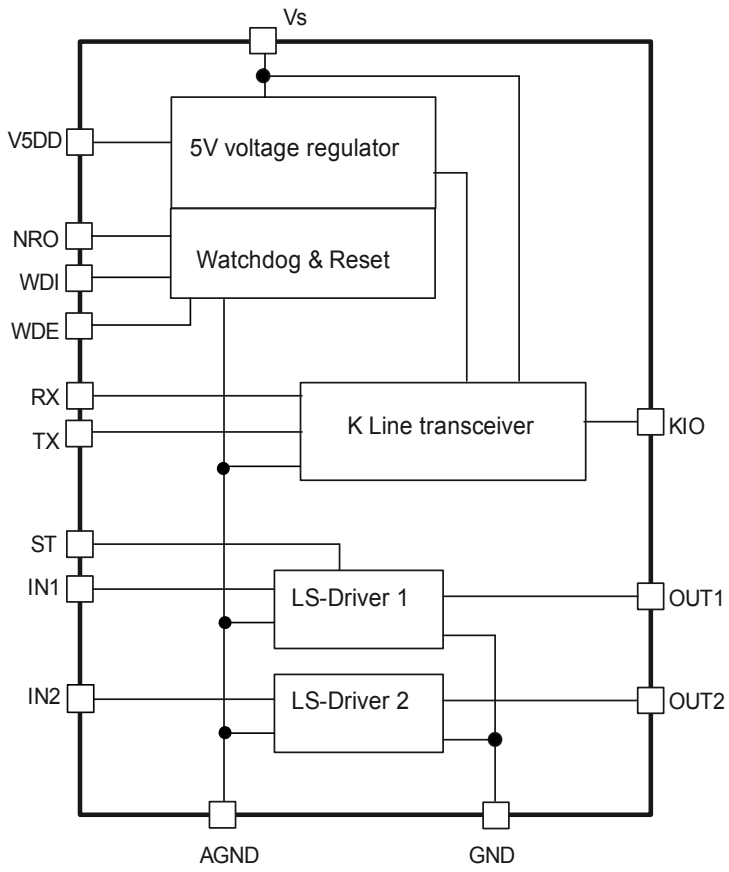


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

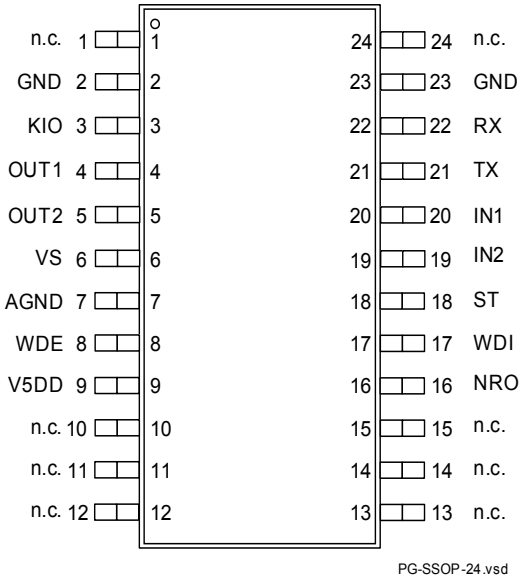


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	n.c.	Not connected
2	GND	Power Ground
3	KIO	K-Line bus connection
4	OUT1	Output channel 1
5	OUT2	Output channel 2
6	VS	Battery voltage: 100nF ceramic capacitor directly connected at the IC to ground
7	AGND	Analog ground: should be connected to the system logic ground
8	WDE	Watchdog enable: active high, internal pull up
9	V5DD	5V supply output: connected to external blocking capacitor.
10	n.c.	Not connected
11	n.c.	Not connected
12	n.c.	Not connected
13	n.c.	Not connected
14	n.c.	Not connected
15	n.c.	Not connected
16	NRO	Reset output: open drain, active low
17	WDI	Watchdog input: trigger input for watchdog pulses
18	ST	Status signal: output diagnostic signal
19	IN2	Control Input Channel 2: internal pull down

Pin	Symbol	Function
20	IN1	Control Input Channel 1: internal pull down
21	TX	Logic level input for data to be transmitted on the K-Line bus KIO
22	RX	Logic output of data received from the K-Line bus KIO.
23	GND	Power Ground
24	n.c.	Not connected
	Exposed pad	should be connected to GND and to the ground plane of the ECU

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Continuous Voltage on pin Vs	V_S	-0.3	40	V	
4.1.2	Continuous Voltage on pin OUT1	V_{OUT1}	-0.3	30	V	IN1=0V
4.1.3	Continuous Voltage on pin OUT2, KIO	$V_{OUT2, KIO}$	-0.3	35	V	IN2=0V TX=V5DD
4.1.4	IN1, IN2, V5DD, RxD, TxD, ST, NRO, WDI, WDE	V_x	-0.3	5.5	V	2)
Temperatures						
4.1.5	Junction Temperature	T_j	-40	150	°C	–
4.1.6	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.7	ESD Resistivity to GND, Vs, K-LINE, OUT1,2	V_{ESD}	-4	4	kV	HBM[3)]
4.1.8	ESD Resistivity to GND, other pins	V_{ESD}	-2	2	kV	HBM[3)]
4.1.9	Electro Static Discharge Voltage “Charged Device Model - CDM”	V_{ESD}	-500	500	V	All Pins CDM[4)]
4.1.10	Electro Static Discharge Voltage “Charged Device Model - CDM”	V_{ESD}	-750	750	V	Pin 1, 12, 13, 24 (corner pins) CDM[4)]

1) Not subject to production test, specified by design
2) For outputs no short circuit is allowed
3) ESD susceptibility, HBM according to EIA/JESD 22-A114B (1.5KOhm, 100pF)
4) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101-C

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage	V_S	6	18	V	–
4.2.2	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	6.3	9	K/W	Measured to exposed pad [1]
4.3.2	Junction to Ambient	R_{thJA}	–	29	–	K/W	[1] [2]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

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5 Voltage Regulator

5.1 Voltage Regulator

The TLE8088EM integrates a voltage regulator for load currents up to **250**mA. The voltage applied to pin **VS** is regulated at pin **V5DD** to 5.0 V with a precision of ±2%. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470nF. The voltage regulator features under-voltage reset, power on reset and watchdog. It is protected against over-current, short circuit and over temperature conditions.

The low-side switch function and the K-line transceiver are independent of the reset and watchdog signals.

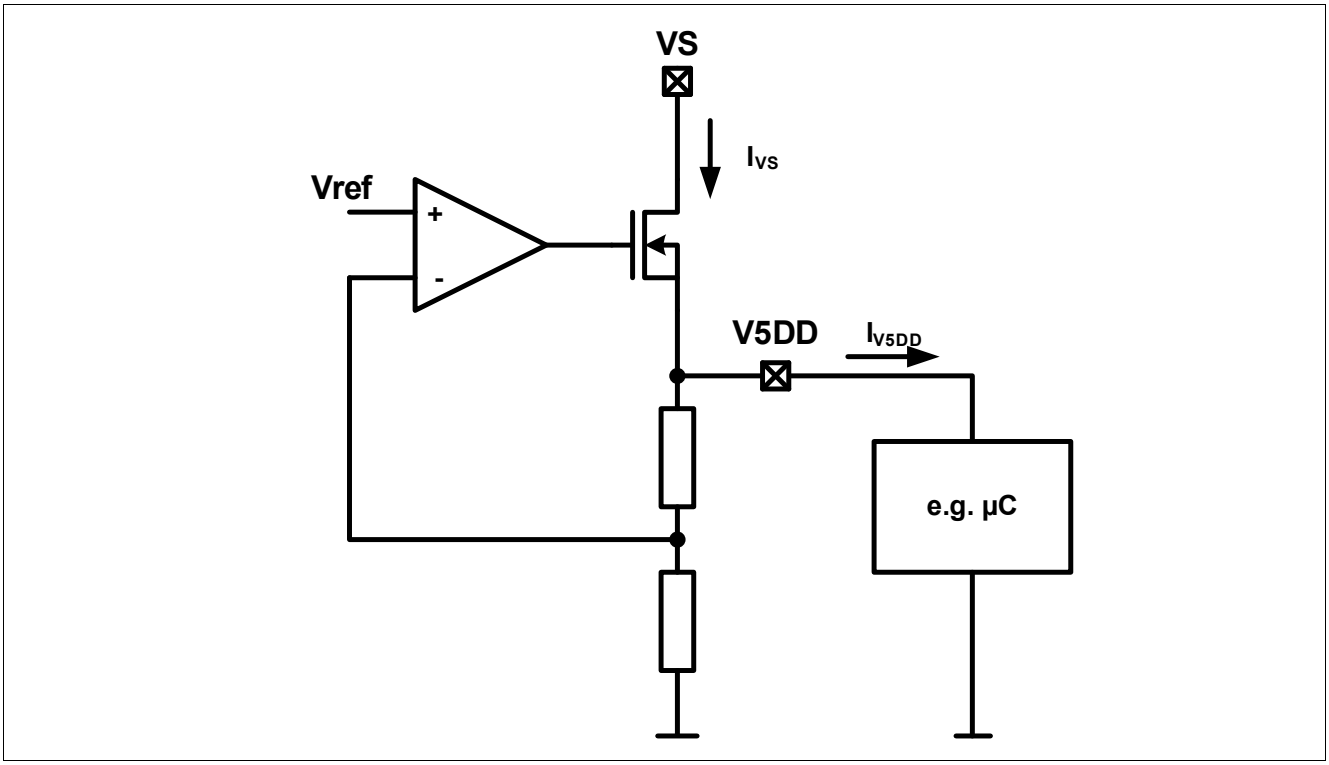


Figure 3 5V Supply

5.2 Power On Reset and Reset Output

Reset output is an open drain output. When the level of V_{V5DD} reaches the reset threshold V_{RT}, the signal at NRO remains low for the power-on reset delay time T_{RD}. The reset function and timing is illustrated in **Figure 4**. The reset reaction time t_{RR} avoids wrong triggering caused by short “glitches” on the V5DD-line. In case of V5DD power down ($V_{V5DD} < V_{RT}$ for $t > t_{RR}$) a logic low signal is generated at the pin NRO to reset an external micro controller. The level of the reset threshold for increasing V_{V5DD} is for the hysteresis (V_{RH}) higher than the level for decreasing V_{V5DD}.

The reset and watchdog signals are for external use and do not affect the state of the channels and K-line transceiver. The correct functionality of the devices is ensured by an independent voltage monitoring circuitry.

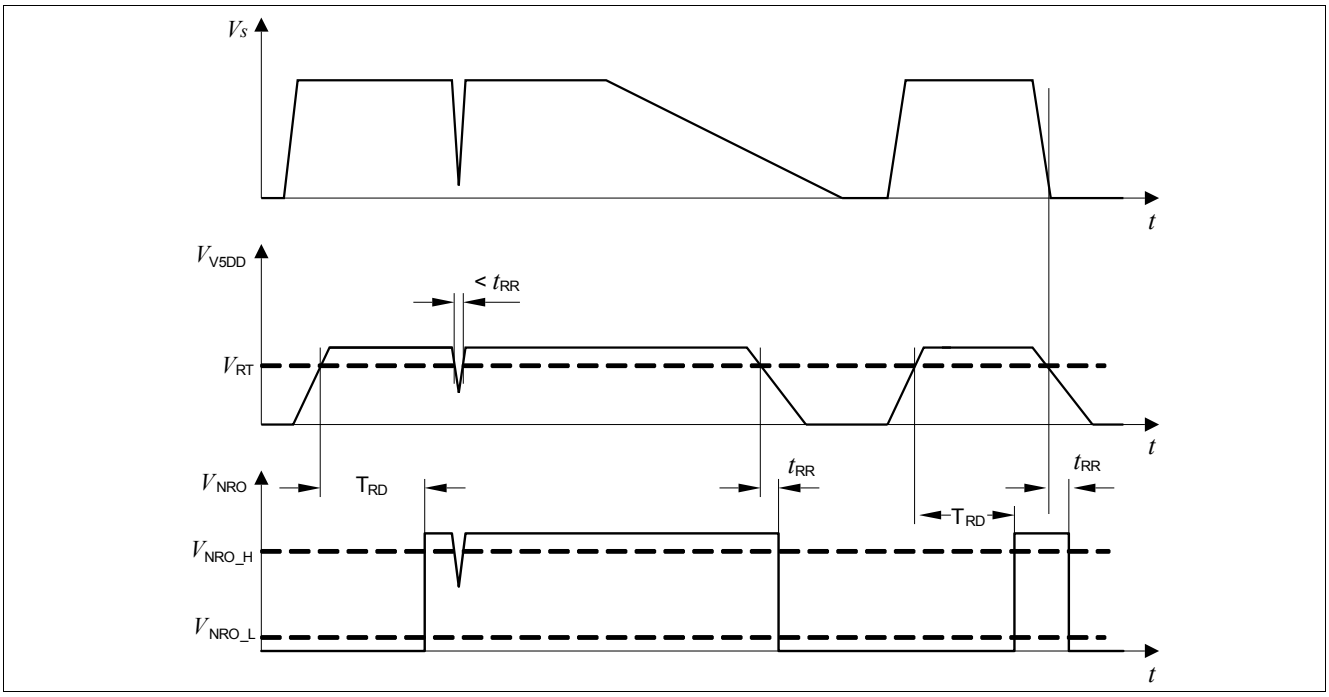


Figure 4 Reset Function and Timing Diagram

5.3 Watchdog Operation

After power on, the reset output signal at the NRO pin is kept LOW for the power-on reset delay time T_{RD} of typ. 15ms. With the LOW to HIGH transition of the signal at NRO the micro controller reset is released.

The TLE8088EM integrates a watchdog function. If WDE is connected to low, the watchdog function is disabled. If the WDE is connected to 5V or left open, the watchdog function is enabled. A pull up current source is integrated in the WDE pin.

After the activation of the watchdog function, the timing of the signal on WDI from the micro-controller must correspond the WD-Period $T_{WD,p}$ specified in the electrical characteristics. A Re-Trigger of the WD-Period is done with a HIGH-to-LOW transition at the WDI-pin within the time $T_{WD,p}$.

A HIGH to LOW transition of the watchdog trigger signal on pin WDI is taken as a trigger. To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period t_{sam} typ. 64µs) are decoded as a valid trigger, see **Figure 6**. A reset is generated (NRO goes LOW) for the time T_{WR} if there is no trigger pulse during the Watchdog Period as shown in **Figure 5**.

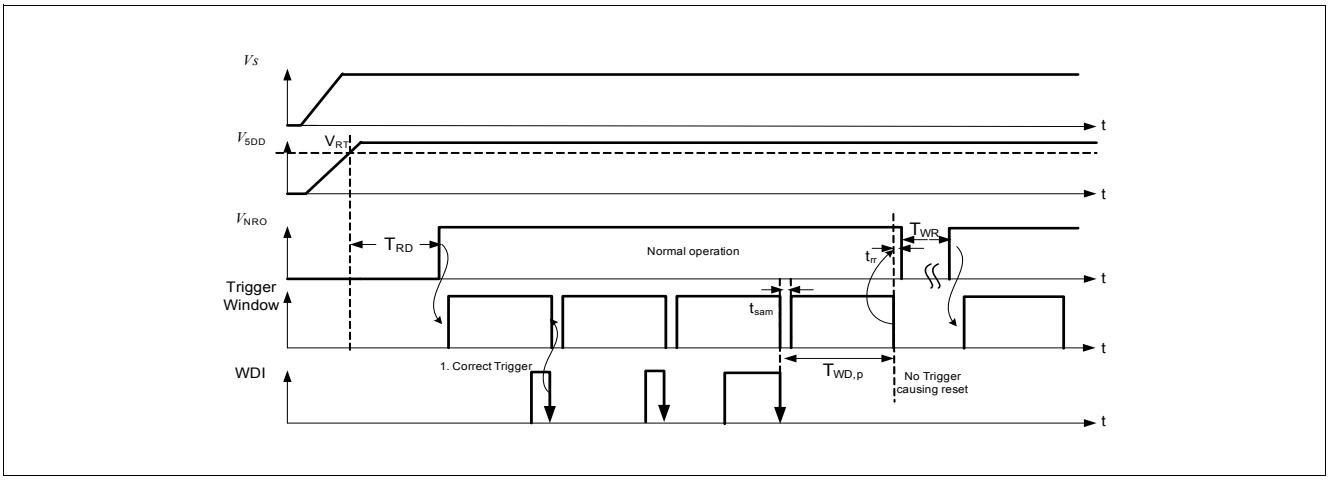


Figure 5 Watchdog Timing Diagram

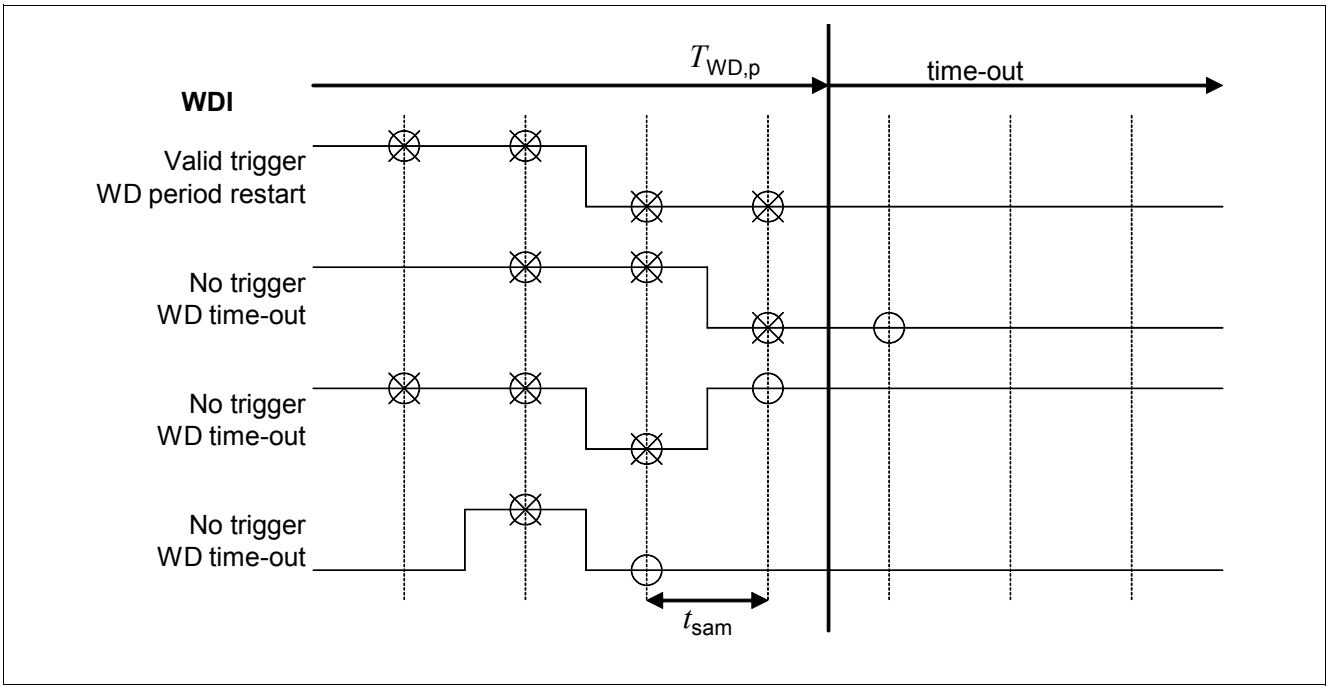


Figure 6 Watchdog valid trigger

Electrical Characteristics: Voltage Regulator

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output V5DD							
5.3.1	Output Voltage	V_{V5DD}	4.90	5.00	5.10	V	0mA < I_{V5DD} < 150mA 6V < V_s < 18V
5.3.2	Output Voltage	V_{V5DD}	4.90	5.00	5.10	V	0mA < I_{V5DD} < 250mA 6V < V_s < 18V [1]
5.3.3	Output Current Limitation	I_{V5DD}	250	–	650	mA	V_{V5DD} = 0V, 6V < V_s < 18V
5.3.4	Load Regulation	$\Delta V_{V5DD,Lo}$	–	–	20	mV	1 mA < I_{V5DD} < 150mA
5.3.4a	Load Regulation	$\Delta V_{V5DD,Lo}$	–	–	50	mV	1 mA < I_{V5DD} < 250mA [1]
5.3.5	Line Regulation	$\Delta V_{V5DD,Li}$	–	–	10	mV	I_{V5DD} = 1 mA; 10 V < V_s < 18V
5.3.6	Power Supply Rejection Ratio	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp [1]
5.3.7	Output Capacitor	C_Q	470	–	–	nF	[1]
		$ESR(C_Q)$	–	–	10	Ω	
5.3.8	Low Drop Voltage	V_{V5DD}	4.80	–	–	V	I_{V5DD} = 1mA V_S =5V
5.3.9			4.40	–	–	V	I_{V5DD} = 150mA V_S =5V; after device ramp-up (V_S >9V)
5.3.9a			4.15	–	–	V	I_{V5DD} = 250mA V_S =5V; after device ramp-up (V_S >9V) [1]
Current Consumption							
5.3.10	Quiescent Current	I_q	–	–	4	mA	I_{V5DD} = 0A; CH1,CH2 off, K-Line off
WDE							
5.3.11	Low Level Input Voltage	$V_{IN,L}$	–	–	1.00	V	–
5.3.12	High Level Input Voltage	$V_{IN,H}$	2.00	–	–	V	–
5.3.13	Hysteresis WDE	$V_{IN,HYS}$	50	–	250	mV	[1]
5.3.14	Input Pull Up Current	$I_{IN\_PU\_L}$	-20	-50	-100	µA	V_{IN} =0V
		$I_{IN\_PU\_H}$	-2.40	–	–	µA	V_{IN} =4.4V
Watchdog Input WDI							
5.3.15	Low Level Input Voltage	$V_{IN,L}$	–	–	1.00	V	
5.3.16	High Level Input Voltage	$V_{IN,H}$	2.00	–	–	V	
5.3.17	Input Voltage Hysteresis	$V_{IN,HYS}$	50	–	250	mV	[1]

Electrical Characteristics: Voltage Regulator (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.18	Input Pull Down Current	$I_{IN\_PD\_H}$	20	50	100	µA	V_{IN} =5V
		$I_{IN\_PD\_L}$	2.40	–	–	µA	V_{IN} =0.6V
5.3.19	Watchdog Sampling Time	t_{sam}	40	64	130	µs	
5.3.20	Watchdog Period	$T_{WD,p}$	50	60	70	ms	
5.3.21	Watchdog Reset Time	T_{WR}	120	240	360	µs	
Reset Output NRO							
5.3.22	Output Voltage Reset Switching Threshold	V_{RT}	4.00	4.25	4.50	V	V_{V5DD} decreasing
5.3.23	Reset Hysteresis	V_{RH}	10	–	150	mV	
5.3.24	Low Level Output Voltage	$V_{NRO,L}$	–	–	1.10	V	I_{NRO}=1mA
5.3.25	Leakage Current	$I_{NRO,LK}$	–	–	1	µA	V_{RT} = 5V
5.3.26	Power-on Reset Delay Time	T_{RD}	10	15	20	ms	
5.3.27	Reset Reaction Time	t_{RR}	1	4	8	µs	–
Over Temperature Protection							
5.3.28	Over-temperature	T_{OT}	150	–	200	°C	1)
5.3.29	Over-temperature Hysteresis	T_{OTH}	–	20	–	°C	1)

1) Not subject to production test, specified by design.

6 Power Drivers

6.1 Low-Side Drivers

The power stages are built by N-channel power MOSFET transistors. The channels are universal multi channel switches but mostly suitable to be used in Engine Management Systems. Within an Engine Management System, the best fit of the channels to the typical loads is:

- Channel 1 for injector, valves or similar sized solenoids with a maximum operation current requirement of 2.6A
- Channel 2 for malfunction indication lamps or other resistive loads with a maximum current requirement of 3A

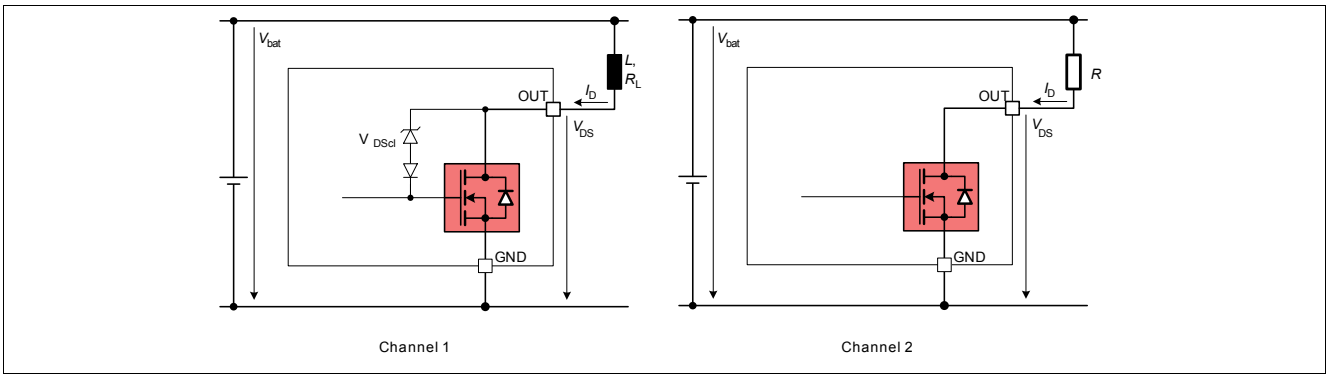


Figure 7 Low-side Switches

Channel 1 has open load detection in off state. If an open load condition persists for a time longer than the filter time t_d, an open load will be detected and the ST pin set to low. On the rising edge of the IN1 signal the ST pin will be released after the time $t_{ST,clear}$, see **Figure 9**.

In over-current situation channel 1 will be switched off and kept latched. Additionally the ST signal will be set to low after the settling time $t_{ST,set,OC}$. On the falling edge of the IN1 signal the ST pin will be released after the time $t_{ST,clear}$, see **Figure 10**. Therefore channel 1 can be switched on again by toggling the IN1 pin.

During an over-temperature event the ST signal is set to low and will turn back to high if the failure condition is disappeared (see **Table 1**).

Table 1 Truth Table for Diagnostics of CH1

Open Load	Over Current	Over Temperature	ST	Status
0	0	0	1	Normal operation
1	x	x	0	Failure detected
x	1	x	0	Failure detected and latched Channel 1 is switched off
x	x	1	0	Failure detected and channel 1 is switched off

Failure Situation	ST
0 = Situation doesn’t exist	1 = Normal operation
1 = Situation exists	0 = Failure detected
X = 0 or 1	

In over-current situation the channel 2 will be switched off, and after typ. 4ms the channel will be switched on again. Channel 2 is also over-temperature protected. In over-temperature situation channel 2 will be switched off and will restart if the junction temperature falls by thermal shutdown hysteresis T_{OTH}.

6.2 Electrical Characteristics

Electrical Characteristics

V_S = 13.5 V, T_j = -40 °C to +150 °C: All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Channel Resistance							
6.2.1	On State Resistance CH1	R_{DSon}	–	0.60	0.70	Ω	I_{Dnom}=1.3A; T_j =150°C
6.2.2	On State Resistance CH2	R_{DSon}	–	1.10	1.20	Ω	I_{Dnom}=0.3A; T_j=150°C
Input Characteristics							
6.2.3	Parallel Input Pin Low level IN1,IN2	$V_{IN,L}$	–	–	1.00	V	–
6.2.4	Parallel Input Pin High level IN1,IN2	$V_{IN,H}$	2.00	–	–	V	–
6.2.5	Parallel Input Pin Hysteresis IN1,IN2	$V_{IN,HYS}$	50	–	250	mV	1)
6.2.6	Parallel Input Pin Input Pull Down Current IN1, IN2	$I_{IN\_PD\_H}$	20	50	100	µA	V_{IN}=5V
		$I_{IN\_PD\_L}$	2.40	–	–	µA	V_{IN}=0.6V
Clamping Voltage							
6.2.7	Output Clamping Voltage CH1	V_{DScl}	30	35	40	V	I_{OUT1}=0.02A
Leakage Currents							
6.2.8	Output Leakage Current in Off Mode, CH1	I_{Doff}	–	–	3	µA	V_{DS}=13.5V; T_j=150°C 1) 2)
6.2.9	Output Leakage Current in Off Mode, CH2	I_{Doff}	–	–	3	µA	V_{DS}=13.5V; T_j=150°C 1)
Timing							
6.2.10	Turn-on Delay Time CH1	t_{dON}	–	0.25	1	µs	V_s = 13.5V, I_{DS1} = 1.3A, resistive load 1) 3)
6.2.11	Turn-on Delay Time CH2	t_{dON}		0.15	1.2	µs	V_s = 13.5V, I_{DS2} = 0.3A, resistive load 1)
6.2.12	Turn-off Delay Time CH1	t_{dOFF}	–	0.65	1.5	µs	V_s = 13,5V, I_{DS1}= 1.3A, resistive load 1)
6.2.13	Turn-off Delay Time CH2	t_{dOFF}	–	0.35	1.5	µs	V_s = 13.5V, I_{DS2} = 0.3A, resistive load 1)
6.2.14	Turn-on Time CH1	t_{sON}	–	0.45	1.2	µs	V_s = 13.5V, I_{DS1} = 1.3A, resistive load 1)

Electrical Characteristics (cont'd)

V_S = 13.5 V, T_j = -40 °C to +150 °C: All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.2.15	Turn-on Time CH2	t_{sON}	–	0.20	1	µs	V_s = 13.5V, I_{DS2} = 0.3A, resistive load 1)
6.2.16	Turn-off Time CH1	t_{sOFF}	–	0.40	1.2	µs	V_s = 13.5V, I_{DS1} = 1.3A, resistive load 1)
6.2.17	Turn-off Time CH2	t_{sOFF}	–	0.20	1	µs	V_s = 13.5V, I_{DS2} = 0.3A, resistive load 1)
Over Current Protection							
6.2.18	Output Current Switch Off Threshold CH1	I_{DS_OC}	2.6	–	5	A	6V < V_S < 18V
6.2.19	Output Current Switch off Threshold CH2	I_{DS_OC}	3.0	–	6.5	A	6V < V_S < 18V
6.2.20	Off Time of CH2 in Current Switch Off	t_{off}	3	–	8	ms	–
6.2.21	Current Switch off Filter Time CH1, CH2	t_{CL_f}	0.5	–	3	µs	–
Open Load Diagnosis for CH 1 in OFF state							
6.2.22	Open Load Detection Threshold Voltage for CH 1	V_{DSol}	2.00	2.80	3.20	V	–
6.2.23	Output pull-down Diagnosis Current	I_{Dpd}	50	100	150	µA	V_{DS} = 13.5 V
6.2.24	Open Load Diagnosis Delay Time	t_d	100	–	200	µs	–
Status Signal							
6.2.25	Low level output voltage	V_{OUT_L}	–	–	0.4	V	I_{NRO}=100µA
6.2.26	High level output voltage	V_{OUT_H}	V_{5DD} – 0.4	–	–	V	I_{NRO}=–100µA
6.2.27	Status settling time after Over Current	$t_{ST,set,OC}$	–	–	20	µs	1)
6.2.28	Status Clear Time	$t_{ST,clear}$	–	–	20	µs	1)
Over Temperature Protection							
6.2.29	Over temperature	T_{OT}	150	–	200	°C	1)
6.2.30	Over temperature hysteresis	T_{OTH}	–	20	–	°C	1)

1) Not subject to production test, specified by design.
2) in OFF mode open load diagnosis pull down current active
3) Definition see **Figure 8**

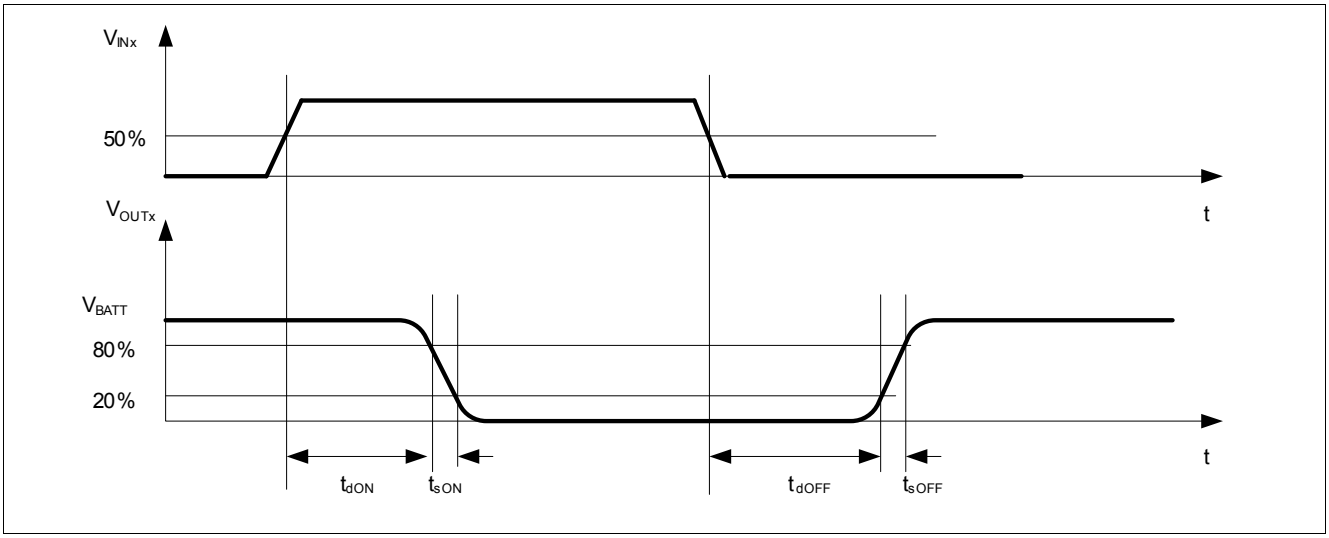


Figure 8 Timing

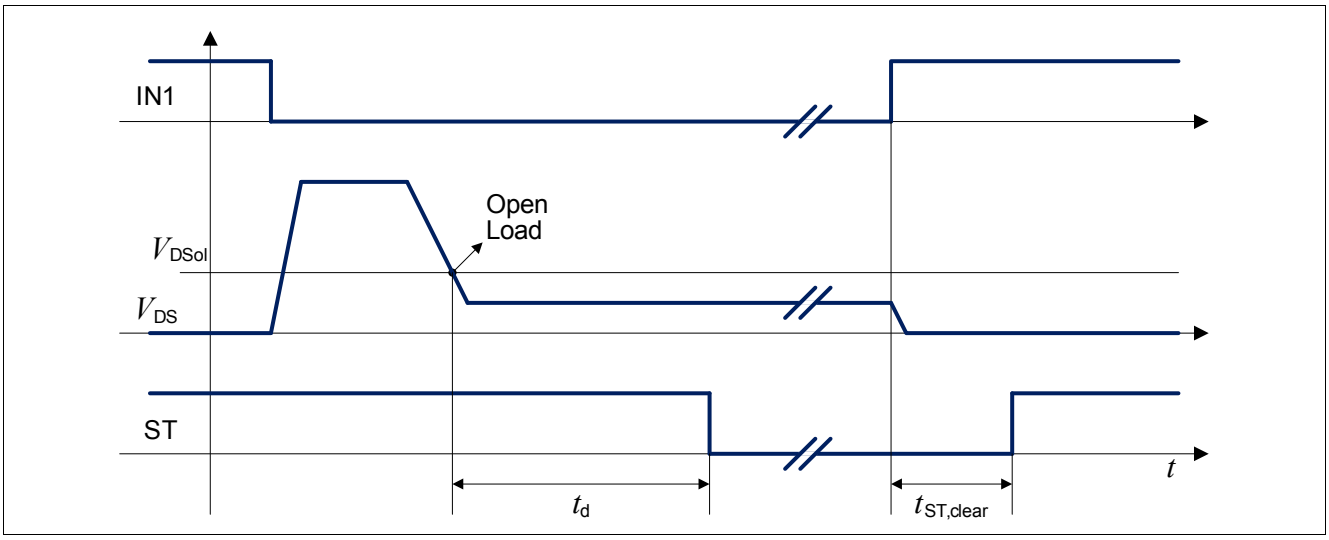


Figure 9 Open Load Detection

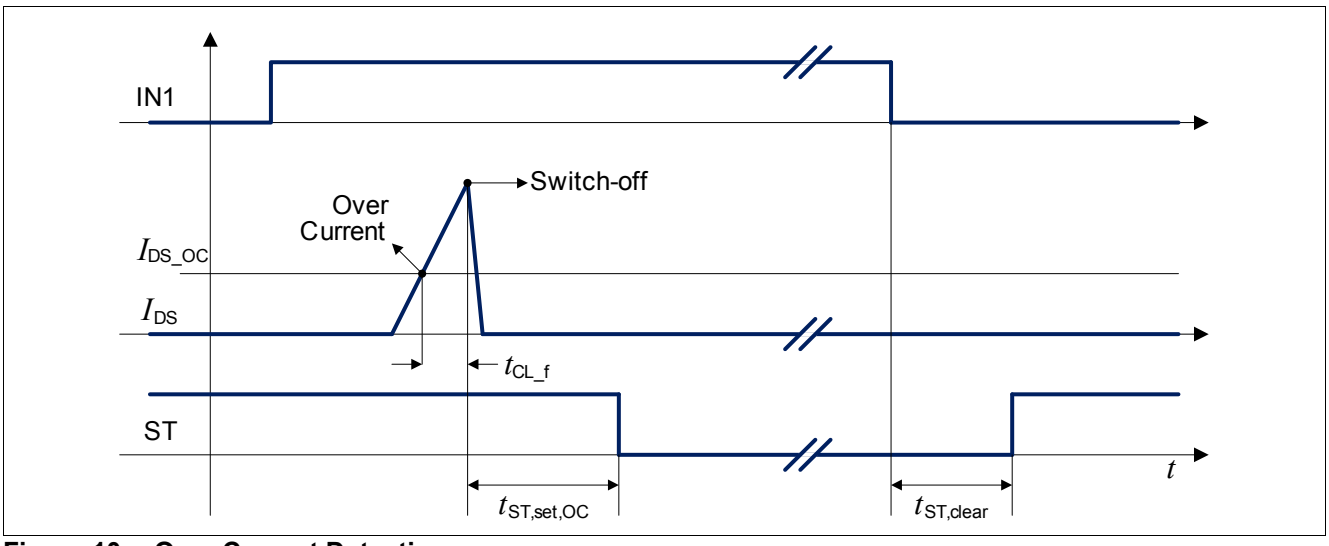


Figure 10 Over Current Detection

7 K-Line

7.1 K-Line

The K-Line module is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing. It is designed to interface between the vehicles via the special ISO K-line and meets the ISO norm 9141 specification. The device's K line bus driver's output is protected against bus shorts.

K-Line module transforms 5.0V micro-controller logic signals to battery level logic signals and vice versa. The over current limitation limits the current to a specified limit. In case of over-temperature on OUT1 the low-side switch and the output stage KIO will be switched off and can only be re-activated if the temperature has decreased below the minimum hysteresis value.

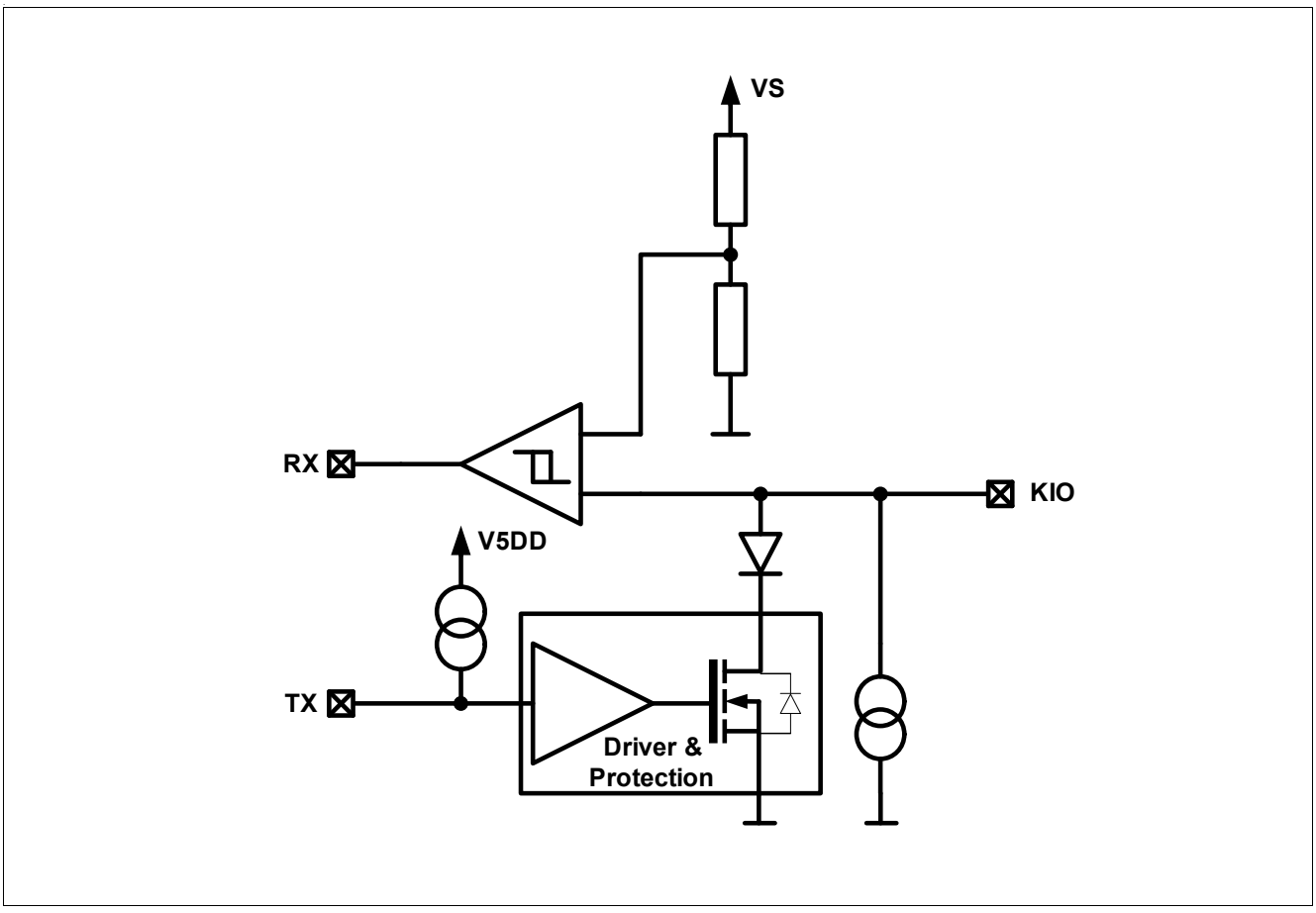


Figure 11 K-Line

Electrical Characteristics: K-Line

Table 2 Electrical Characteristics: K-Line

V_S = 13.5 V, T_j = -40 °C to +150 °C: All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Output RX							
7.1.1	Low Level Output Voltage	$V_{RX,L}$	–	–	0.4	V	I_{RX}=100µA
7.1.2	High Level Output Voltage	$V_{RX,H}$	V_{5DD}-0.4	–	–	V	I_{RX}=-100µA
Input TX							
7.1.3	Input Pin Low level	$V_{TX,L}$		–	1.00	V	–
7.1.4	Input Pin High level	$V_{TX,H}$	3.20	–		V	–
7.1.5	Input Pin Hysteresis	$V_{TX,HYS}$	280	500	700	mV	1)
7.1.6	Input Pin Pull Up Current	I_{IN_PU}	-70	–	-150	µA	VTX=0
KIO input / Output							
7.1.7	Low Level Output Voltage	$V_{KIO,L}$	–	–	1.4	V	TX=low, R_{KIO}=480Ω
7.1.8	Current Limitation	$I_{KIO(lim)}$	40	–	140	mA	
7.1.9	Output Pull-Down current	$I_{KIO,PD}$	5	–	15	µA	TX=high
KIO Input Comparator							
7.1.10	Input Low Voltage	V_{IN_L}	–	–	0.4*V_s	V	–
7.1.11	Input High Voltage	V_{IN_H}	0.6*V_s	–	–	V	–
7.1.12	Input Threshold Hysteresis	V_{IN_Hys}	0.02*V_s	–	0.175*V_s	V	–
Transfer characteristics KIO->RX and TX->KIO							
CRX=25pF; RKIO=540Ω; CKIO<=1.3nF; Vs=13.5V							
7.1.13	Transmission Frequency KIO->RX	f_{RKIO}	–	–	500	kHz	C_{KIO}=0pF
7.1.14	Transmission Frequency TX->KIO	f_{TKIO}	–	–	100	kHz	–
7.1.15	Off Delay / Rise Time KIO->RX	t_{drR}	0.05	–	0.5	µs	$C_{RX,load}$=1.6pF 2)
7.1.16	Off Delay / Rise time TX->KIO	t_{drT}	0.05	–	0.5	µs	$C_{KIO,load}$=1.6pF 1) 2)
7.1.17	On Delay / Fall time KIO->RX	t_{dfR}	0.05	–	0.5	µs	$C_{RX,load}$=1.6pF 2)
7.1.18	On Delay / Fall time TX->KIO	t_{dfT}	0.05	–	0.5	µs	$C_{KIO,load}$=1.6pF 2)

1) Not subject to production test, specified by design.

2) For definition see **Figure 12**

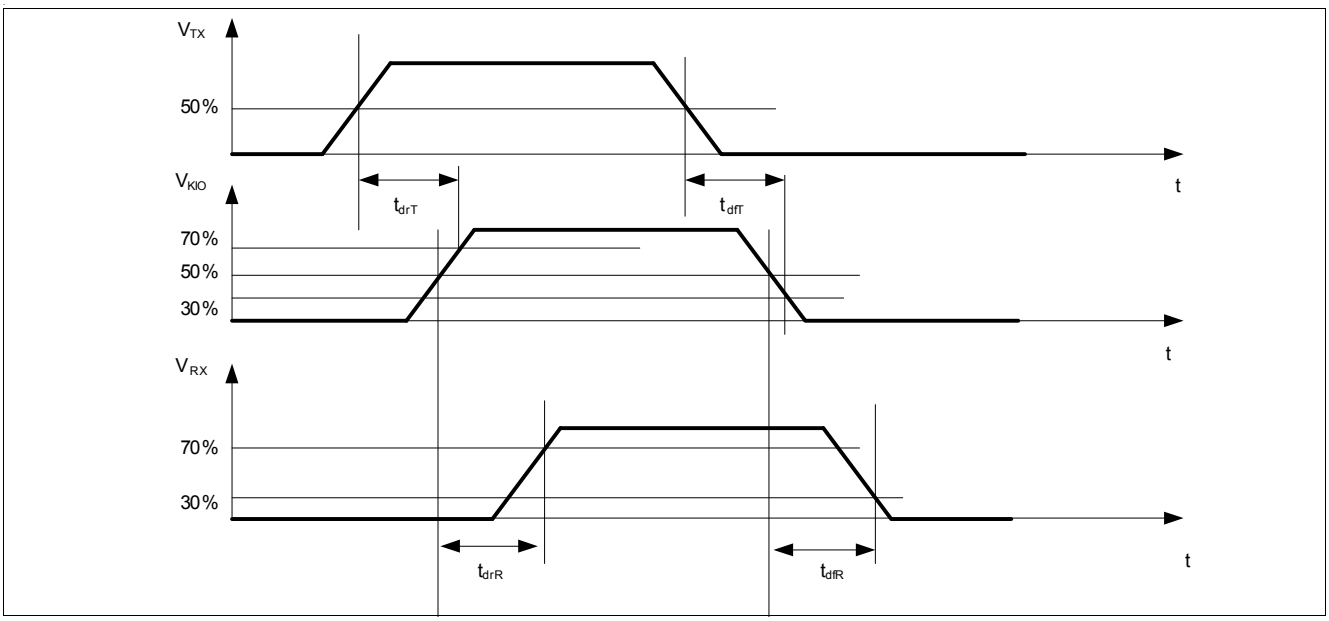
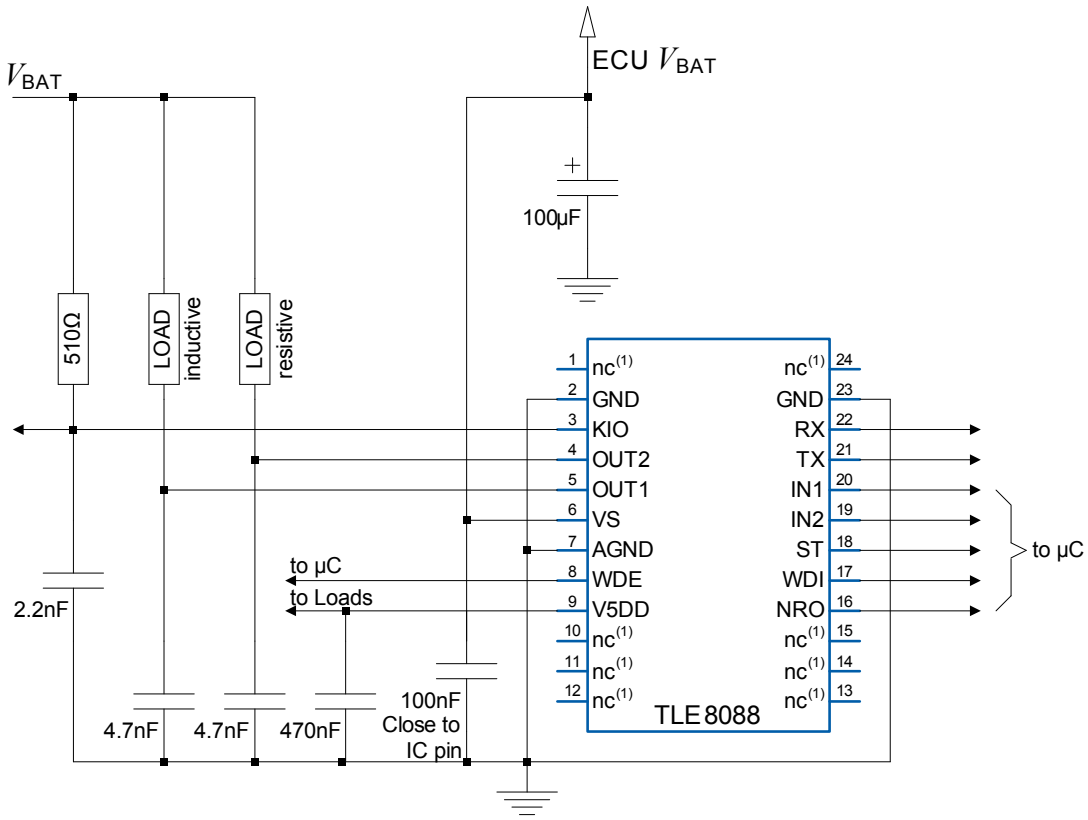


Figure 12 Transfer characteristics

8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.



(1) Pins marked as not connected (nc) are internally not bonded. Related pads can be used for facilitating the PCB routing.

Figure 13 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

8.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

9 Package Outlines

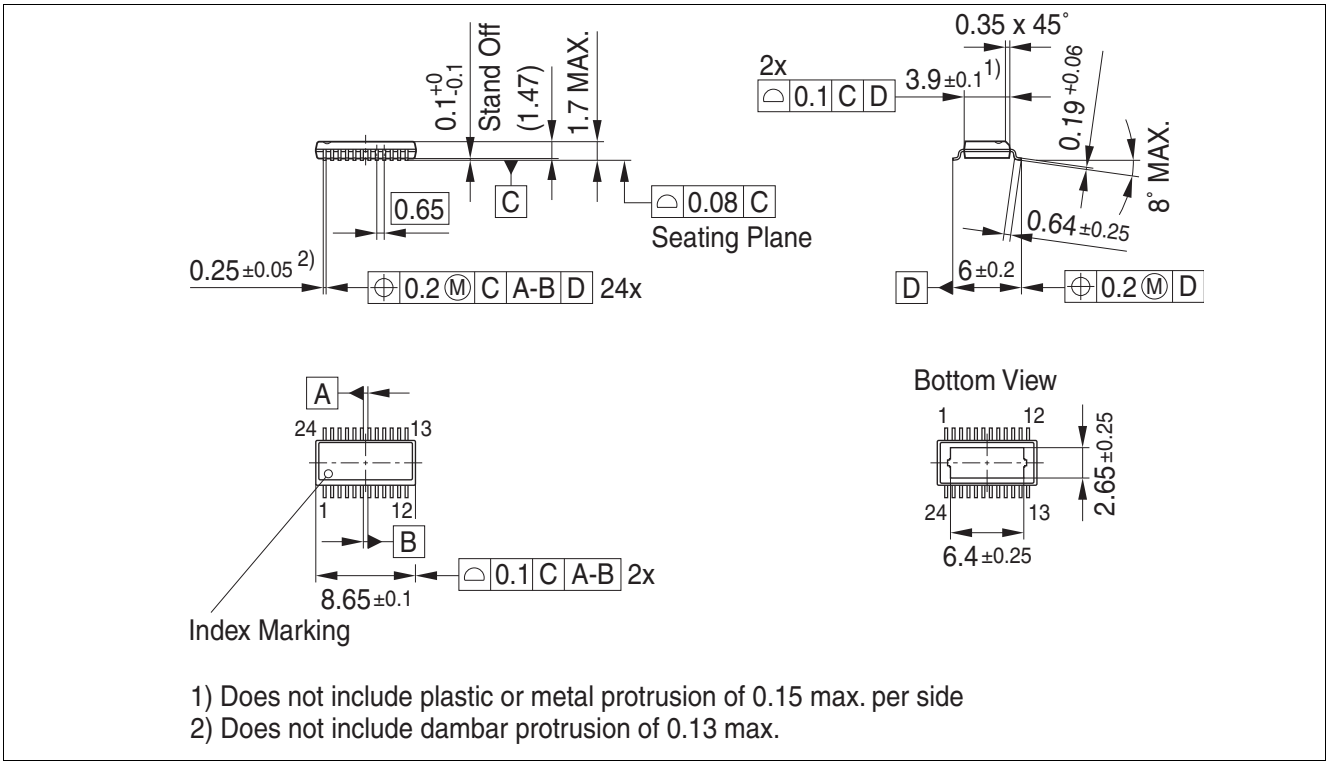


Figure 14 PG-SSOP-24

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.0	**2012-10-01**	Data Sheet Release

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