

Brief Description

The ZSPM2000 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies. The ZSPM2000 includes a high-speed MOSFET driver for a synchronous step-down converter in a single-rail and single-phase configuration.

The ZSPM2000 integrates a digital control loop, optimized for maximum flexibility and stability, as well as load step and steady-state performance. In addition, a rich set of protection and monitoring functions is provided. On-chip, non-volatile memory (NVM) and an I²C™ interface facilitate configuration.

IDT's PC-based Pink Power Designer™ graphical user interface (GUI) provides a user-friendly and easy-to-use interface to the device for communication and configuration. It can guide the user through the design of the digital compensator and offers intuitive configuration methods for additional features, such as protection and sequencing.

Features

- Programmable digital control loop
- Advanced digital control techniques
 - Tru-sample Technology™
 - State-Law Control™ (SLC)
 - Sub-cycle Response™ (SCR)
- Improved transient response and noise immunity
- Protection features
 - Over-current protection
 - Over-voltage protection (VIN, VOUT)
 - Under-voltage protection (VIN, VOUT)
 - Overloaded startup
 - Restart and delay
- Integrated MOSFET driver with adaptive anti-cross-conduction protection
- Fuse-based NVM for improved reliability
- Operation from a single 5V or 3.3V supply
- Optional PMBus™ address selection without external resistors

Benefits

- Fast configurability and design flexibility
- Simplified design and integration
- Reduced component count through system level integration
- Simplified monitoring for system power and thermal management
- Higher energy efficiency across all output loading conditions

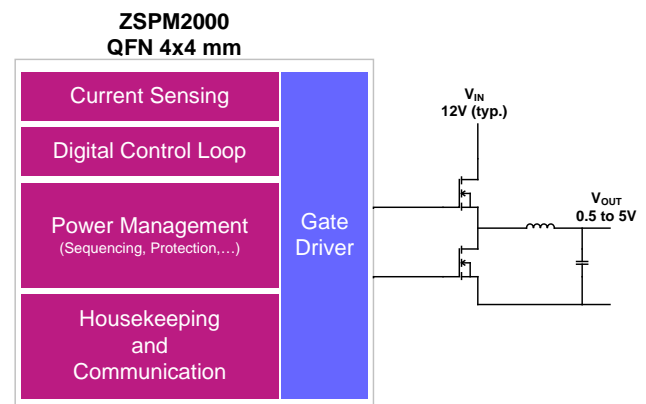
Available Support

- Evaluation Kit
- PC-based Pink Power Designer™ GUI

Physical Characteristics

- Operation temperature: -40°C to +85°C
- V_{OUT} max: 5V
- VDD50 and VDD50DRV supply: 4.75V to 5.25V
- Lead free (RoHS-compliant)

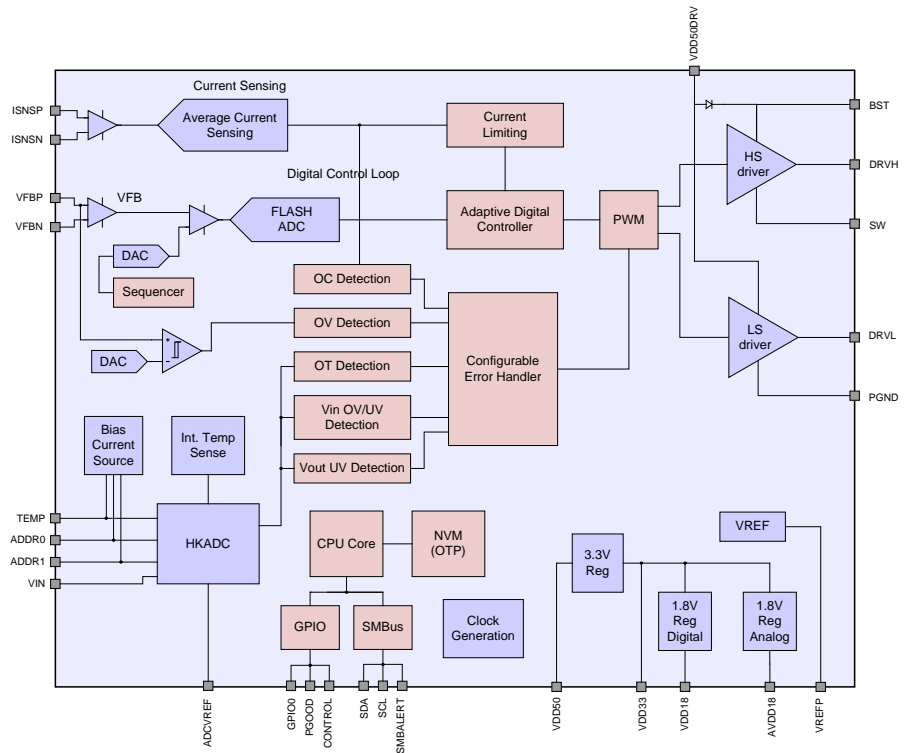
ZSPM2000 Typical Application Diagram



^{*} I²C™ is a registered trademark of NXP.

ZSPM2000 Block Diagram

- Typical Applications**
- ❖ Telecom Switches
 - ❖ Servers and Storage
 - ❖ Base Stations
 - ❖ Network Routers
 - ❖ Industrial Applications
 - ❖ Single-Rail/Single-Phase Supplies for Processors, ASICs, FPGAs, DSPs



Ordering Information

| Sales Code | Description | Package |
|----------------|---|---------|
| ZSPM2000ZI2R 1 | ZSPM2000 Lead-free QFN28 — Temperature range: -40°C to +85°C* | Reel |
| ZSPM2000-KIT01 | Evaluation Kit for ZSPM2000 with PMBus™ Communication Interface — the Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM2000 (login required; see data sheet section 9 for details) | Kit |

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1 IC Characteristics

1.1. Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------|-----------------------|---|-----|-------------------------|------------|
| Supply voltages | | | | | | |
| 5V supply voltage pins: VDD50 and VDD50DRV | V_{DD50} $V_{DD50DRV}$ | $dV/dt < 0.15V/\mu s$ | -0.3 | | 5.5 | V |
| Maximum slew rate | | | | | 0.15 | V/ μs |
| 3.3V supply voltage pin: VDD33 | V_{DD33} | | -0.3 | | 3.6 | V |
| 1.8V supply voltage pins: VDD18 and AVDD18 | V_{DD18} V_{AVDD18} | | -0.3 | | 2.0 | V |
| Digital pins | | | | | | |
| Digital I/O pins: SCL, SCA, GPIO0, SMBALERT, CONTROL, and PGOOD | | | -0.3 | | 5.5 | V |
| Analog pins | | | | | | |
| Current sensing pins: ISNSP and ISNSN | | | -0.3 | | 5.5 | V |
| Voltage feedback pins: VFBP and VFBN | | | -0.3 | | 2.0 | V |
| All other analog pins: ADCVREF, VIN, VREFP, TEMP, ADDR0, and ADDR1 | | | -0.3 | | 2.0 | V |
| MOSFET driver pins | | | | | | |
| Bootstrap supply voltage pin: BST | V_{BST} | Relative to SW | $V_{SW} - 0.3$ | | $V_{SW} + 6.5$ | V |
| | | Relative to PGND | | | 35 40.0 at < 50ns | V |
| Switching node pin: SW (bootstrap supply return) | V_{SW} | Relative to PGND | -5.0 -10.0 at < 200ns | | 35 40.0 at < 50ns | V |
| High-side driver output pin: DRVH | | Relative to BST | | | $V_{BST} + 0.3$ | V |
| | | Relative to SW | $V_{SW} - 0.3$ $V_{SW} - 2.0$ at <200ns | | | V |
| Low-side driver output pin: DRVL | | Relative to PGND | -0.3 -5.0 at < 200ns | | $V_{DD50DRV} + 0.3$ | V |
| MOSFET driver power ground pin: PGND | | | 0 | | 0 | V |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|-------------------|-------------------------|-----------------|-----|-----|-------|
| Ambient conditions | | | | | | |
| Storage Temperature Range | T _{STOR} | | -40 | | 150 | °C |
| Electrostatic Discharge Protection | ESD | JEDEC JESD22-A114 (HBM) | 1500 | | | V |
| | | JEDEC JESD22-A115 (MM) | 100 | | | V |
| Latch-Up Protection | LU | JEDEC JESD78 | Class 1 Level A | | | |
| Moisture Sensitivity Level | MSL | | 1 | | | |

1.2. Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|------------------|------------|-----|-----|-----|-------|
| Ambient conditions | | | | | | |
| Operation temperature | T _{AMB} | | -40 | | 85 | °C |

1.3. Electrical Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|------------------|------|------|------|-------|
| Supply voltages | | | | | | |
| 5V supply voltage – controller: VDD50 pin | V _{DD50} | | 4.75 | 5.0 | 5.25 | V |
| 5V supply current - controller | | VDD50=5.0V | | 23 | | mA |
| 5V supply voltage – driver: VDD50DRV pin | V _{DD50DRV} | | 4.75 | 5.0 | 5.25 | V |
| 3.3V supply voltage: VDD33 pin | V _{DD33} | | 3.0 | 3.3 | 3.6 | V |
| 3.3V supply current | | VDD50=VDD33=3.3V | | 23 | | mA |
| Internally generated supply voltages | | | | | | |
| 3.3V supply voltage: VDD33 pin | | VDD50=5.0V | 3.0 | 3.3 | 3.6 | V |
| 3.3V output current | | VDD50=5.0V | | | 2.0 | mA |
| 1.8V supply voltages: AVDD18 and VDD18 pin | | VDD50=5.0V | 1.72 | 1.80 | 1.98 | V |
| 1.8V output current | | | | | 0 | mA |
| Power on reset threshold – on: VDD33 pin | | | | 2.8 | | V |
| Power on reset threshold – off | | | | 2.6 | | V |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|------------|-----|-----|-------|-------|
| Digital IO pins (GPIO0, CONTROL, PGOOD) | | | | | | |
| Input high voltage | | VDD33=3.3V | 2.0 | | | V |
| Input low voltage | | VDD33=3.3V | | | 0.8 | V |
| Output high voltage | | VDD33=3.3V | 2.4 | | VDD33 | V |
| Output low voltage | | | | | 0.5 | V |
| Input leakage current | | | | | ±1.0 | µA |
| Output current – high | | | | | 2.0 | mA |
| Output current – low | | | | | 2.0 | mA |
| SMBus pins (SCL, SDA, SMBALERT) – open drain | | | | | | |
| Input high voltage | | VDD33=3.3V | 2.0 | | | V |
| Input low voltage | | VDD33=3.3V | | | 0.8 | V |
| Maximum bus voltage | | | | | 5.25 | V |
| Output current – low | | | | | 2.0 | mA |
| Output voltage (without external prescaler) | | | | | | |
| Set-point voltage | | | 0 | | 1.4 | V |
| Set-point resolution | | | | 1.4 | | mV |
| Set-point accuracy | | VOUT=1.4V | | 1 | | % |
| Inductor current measurement | | | | | | |
| Common mode voltage: ISNSP and ISNSN pins relative to AGND | | | 0 | | 5.0 | V |
| Differential voltage range: ISNSP to ISNSN pin | | | | | ±100 | mV |
| Accuracy | | | | 5 | | % |
| Recommended DCR sense voltage for maximum output current | | | 10 | | | mV |
| Digital pulse width modulator | | | | | | |
| Switching frequency | | | 177 | | 1000 | kHz |
| Resolution | | | | 163 | | ps |
| Frequency accuracy | | | | 2.0 | | % |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|--|-----|-----------|------|------------|
| Over-voltage protection | | | | | | |
| Reference DAC | | | | | | |
| Set-point voltage | | | 0 | | 1.58 | V |
| Resolution | | | | 25 | | mV |
| Set point accuracy | | | | 2 | | % |
| Comparator | | | | | | |
| Hysteresis | | | | 35 | | mV |
| HKADC input pins | | | | | | |
| Input voltage: TEMP, VIN, ADDR0, and ADDR1 pins | | | 0 | | 1.44 | V |
| Source impedance Vin sensing | | | | | 3 | k Ω |
| ADC resolution | | | | 0.7 | | mV |
| External temperature measurement | | | | | | |
| Supported sense elements | PN-junction | | | | | |
| Bias current for external temperature sensing: TEMP pin | | | | 60 | | μ A |
| Resolution: TEMP pin | | | | 0.32 | | K |
| Accuracy of measurement: TEMP pin | | | | \pm 5.0 | | K |
| Internal temperature measurement | | | | | | |
| Resolution | | | | 0.22 | | K |
| Accuracy of measurement | | | | \pm 5.0 | | K |
| MOSFET driver pins | | | | | | |
| Output impedance, sourcing current—DRVH pin | | $V_{BST}-V_{SW} = 5V$ | | 0.9 | 1.7 | Ω |
| Output impedance, sinking current—DRVH pin | | $V_{BST}-V_{SW} = 5V$ | | 0.7 | 1.7 | Ω |
| Rise time—DRVH pin | t_{rDRVH} | $V_{DD50DRV} = 5V$; 3nF load $V_{BST}-V_{SW} = 5V$ | | 16 | 25 | ns |
| Fall time—DRVH pin | t_{fDRVH} | $V_{DD50DRV} = 5V$; 3nF load $V_{BST}-V_{SW} = 5V$ | | 11 | 18 | ns |
| Turn-on propagation delay—DRVH pin | $t_{pdhDRVH}$ | $C_{LOAD} = 3nF$ | 10 | | 30 | ns |
| SW pin pull-down resistance | | SW to PGND | | 45 | | k Ω |
| DRVH pin pull-down resistance | | DRVH to SW $V_{BST} - V_{SW} = 0V$ | | 45 | | k Ω |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------|---------------------------------------|-----|-----|-----|------------|
| Output impedance, sourcing current—DRV L pin | | | | 0.9 | 1.7 | Ω |
| Output impedance, sinking current—DRV L pin | | | | 0.4 | 0.8 | Ω |
| DRV L rise time—DRV L pin | $t_{rDRV L}$ | $C_{LOAD} = 3nF$ | | 16 | 25 | ns |
| DRV L fall time—DRV L pin | $t_{fDRV L}$ | $C_{LOAD} = 3nF$ | | 11 | 15 | ns |
| DRV L turn-on propagation delay | $t_{pdhDRV L}$ | $C_{LOAD} = 3nF$ | 10 | | 30 | ns |
| DRV L pin pull-down resistance | $R_{DRV L-PD}$ | DRV L to PGND $V_{DD50DRV} = PGND$ | | 45 | | k Ω |
| SW node leakage current | | | | 20 | | μA |

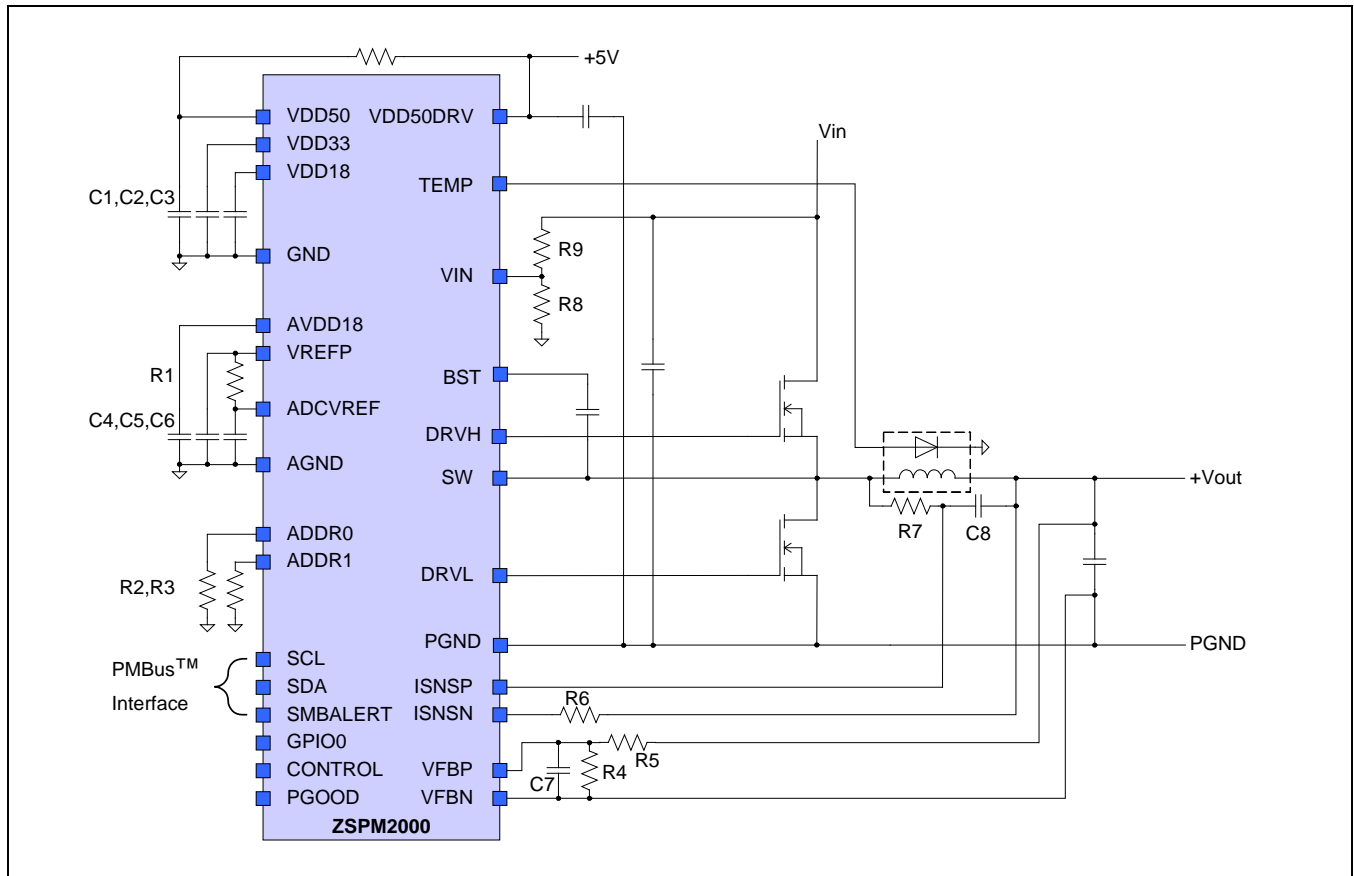
2 Product Summary

2.1 Overview

The ZSPM2000 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies supporting switching frequencies up to 1MHz. It offers a PMBus™ configurable digital power control loop incorporating output voltage sensing and average inductor current sensing, bundled with extensive fault monitoring and handling options. A high-speed MOSFET driver for a synchronous step-down converter is integrated in the ZSPM2000. The ZSPM2000 operates from a single 5V supply.

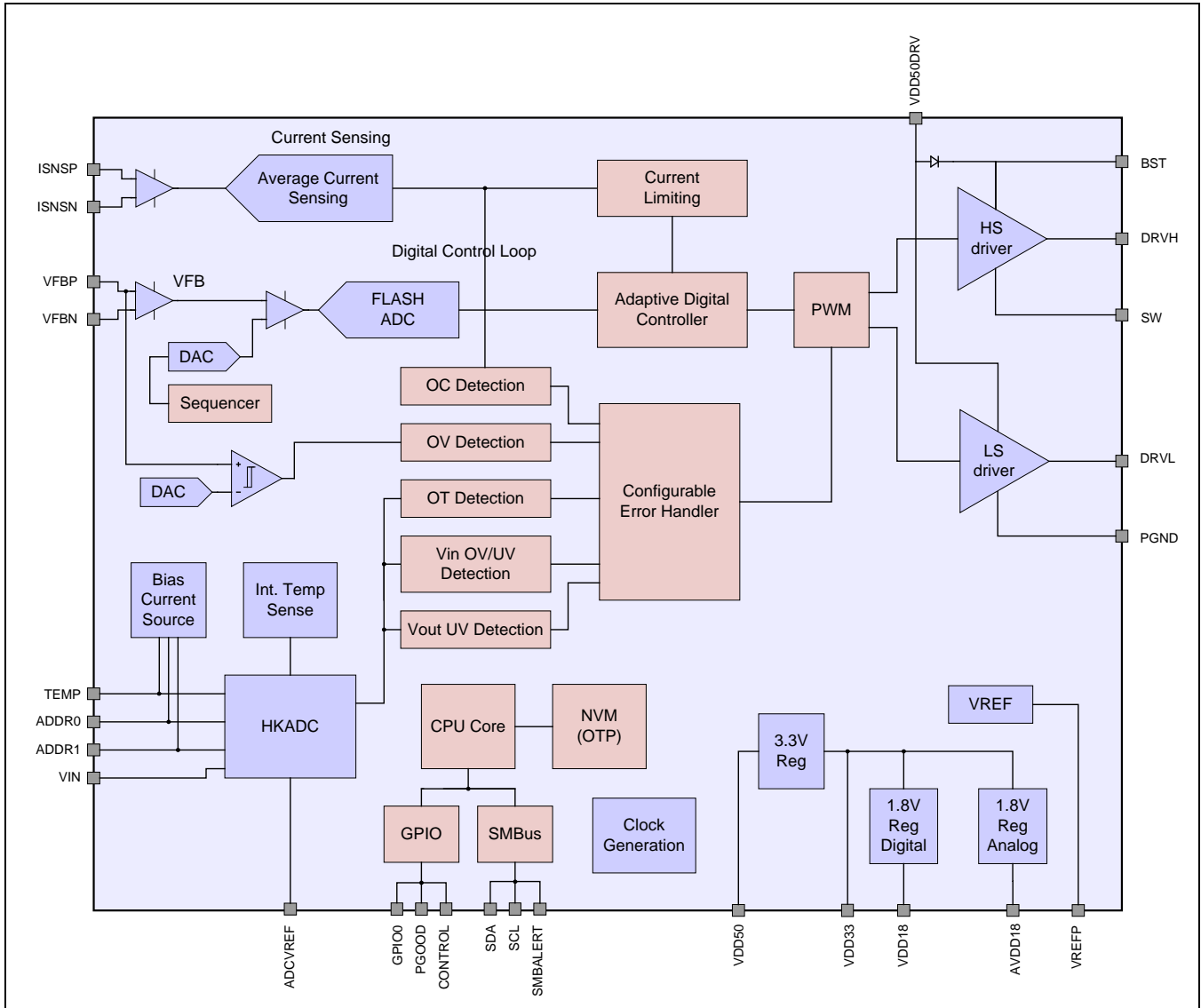
Several different functional units are incorporated in the ZSPM2000. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated, configurable error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals such as input voltage and temperature. An application-specific, low-power microcontroller is used to control the overall system. It manages configuration of the various logic units and handles the PMBus™ communication protocol. A PMBus™/SMBus/I²C™ interface is incorporated to connect with the outside world, supported by control and power-good (PGOOD) signals.

Figure 2.1 Typical Application Circuit with a 5V Supply Voltage



A high-reliability, high-temperature one-time programmable (OTP) memory is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Figure 2.2 Block Diagram



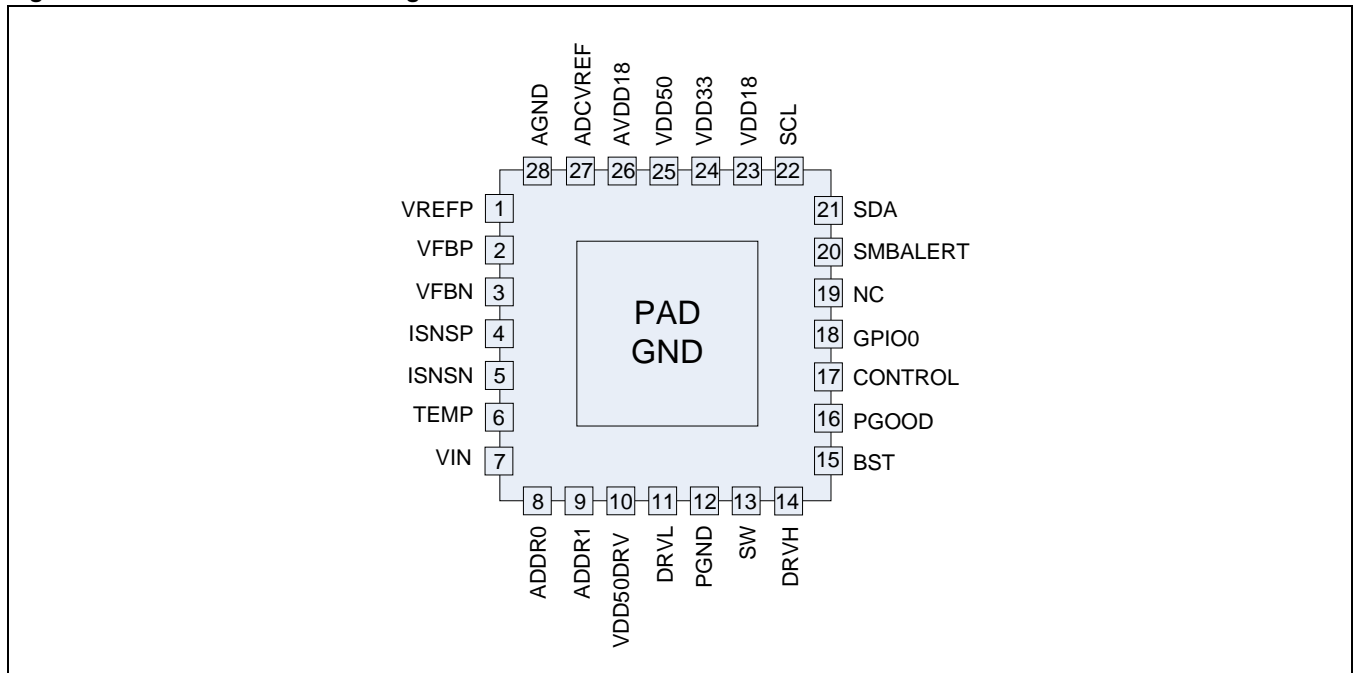
2.2. Pin Description

| Pin | Name | Direction | Type | Description |
|-----|----------|--------------|---------|---|
| 1 | VREFP | Output | Supply | Reference Terminal |
| 2 | VFBP | Input | Analog | Positive Input of Differential Feedback Voltage Sensing |
| 3 | VFBN | Input | Analog | Negative Input of Differential Feedback Voltage Sensing |
| 4 | ISNSP | Input | Analog | Positive Input of Differential Current Sensing |
| 5 | ISNSN | Input | Analog | Negative Input of Differential Current Sensing |
| 6 | TEMP | Input | Analog | Connection to External Temperature Sensing Element |
| 7 | VIN | Input | Analog | Power Supply Input Voltage Sensing |
| 8 | ADDR0 | Input | Analog | SMBus Address Selection 0 |
| 9 | ADDR1 | Input | Analog | SMBus Address Selection 1 |
| 10 | VDD50DRV | Input | Supply | 5.0 V Supply Terminal for the integrated MOSFET Driver |
| 11 | DRVL | Output | Analog | Low-Side Driver Output |
| 12 | PGND | Input | Supply | Integrated MOSFET Driver Ground |
| 13 | SW | Input | Analog | Switching Node (Bootstrap Supply Return) |
| 14 | DRVH | Output | Analog | High-Side Driver Output |
| 15 | BST | Input | Analog | Bootstrap Supply Input |
| 16 | PGOOD | Output | Digital | PGOOD Output (Internal Pull-Down) |
| 17 | CONTROL | Input | Digital | Control Input |
| 18 | GPIO0 | Input/Output | Digital | General Purpose Input/Output Pin |
| 19 | NC | | | Test pin – Do not connect |
| 20 | SMBALERT | Output | PMBus™ | SMBus Alert Output |
| 21 | SDA | Input/Output | PMBus™ | SMBus Shift Data I/O |
| 22 | SCL | Input | PMBus™ | SMBus Shift Clock Input (slave-only) |
| 23 | VDD18 | Output | Supply | Internal 1.8V Digital Supply Terminal |
| 24 | VDD33 | Output | Supply | 3.3V Supply Voltage Terminal |
| 25 | VDD50 | Input | Supply | 5.0V Supply Voltage Terminal |
| 26 | AVDD18 | Output | Supply | Internal 1.8V Analog Supply Terminal |
| 27 | ADCVREF | Input | Analog | Analog-to-Digital Converter (ADC) Reference Terminal |
| 28 | AGND | Input | Supply | Analog Ground |
| PAD | GND | Input | Supply | Exposed PAD, Digital Ground |

2.3. Available Packages

The ZSPM2000 is available in a 28-pin QFN package. The pin-out is shown in Figure 2.3. The mechanical drawing of the package can be found in Figure 7.1.

Figure 2.3 Pin-Out QFN28 Package



3 Functional Description

3.1. Power Supply Circuitry, Reference Decoupling, and Grounding

The ZSPM2000 incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external 5 V supply voltage on the VDD50DRV and VDD50 pins. The integrated MOSFET driver supply terminal VDD50DRV must be decoupled to the PGND pin (1.0 μ F minimum; 4.7 μ F recommended). Recommendation: Add a 10 Ω resistor between the VDD50DRV and VDD50 pins to provide sufficient decoupling between the pins.

Decoupling capacitors are required at the VDD50, VDD33, VDD18, and AVDD18 pins (1.0 μ F minimum; 4.7 μ F recommended). A small load current can be drawn from the VDD33 pin. For example, this can be used to supply pull-up resistors.

The reference voltages required for the analog-to-digital converters (ADCs) are generated within the ZSPM2000. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7 μ F capacitor is required at the VREFP pin and a 100nF capacitor at ADCVREF pin. The two pins should be connected with approximately 50 Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections are available on the outside of the package. Recommendation: Tie the AGND and the PAD together while separating the ground loop for the driver ground (PGND). Also use a single tie point close to the ZSPM2000 to tie the two ground connections together.

3.2. Reset/Start-up Behavior

The ZSPM2000 employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage, the ZSPM2000 begins the internal start-up process. Upon its completion, the device is ready for operation.

3.3. Digital Power Control

3.3.1. Overview

The digital power control loop consists of the integral parts required for the control functionality of the ZSPM2000. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM, which controls the drive signals to the power stage.

3.3.2. Switching Frequency

The ZSPM2000 supports the switching frequencies listed in Table 3.1.

Table 3.1 Supported Switching Frequencies

| Supported Switching Frequencies | | | |
|---------------------------------|----------|----------|----------|
| 1000kHz | 571.4kHz | 400.0kHz | 266.6kHz |
| 800kHz | 500.0kHz | 333.3kHz | 222.0kHz |
| 666.6kHz | 444.4kHz | 285.7kHz | 177.0kHz |

3.3.3. Output Voltage Feedback

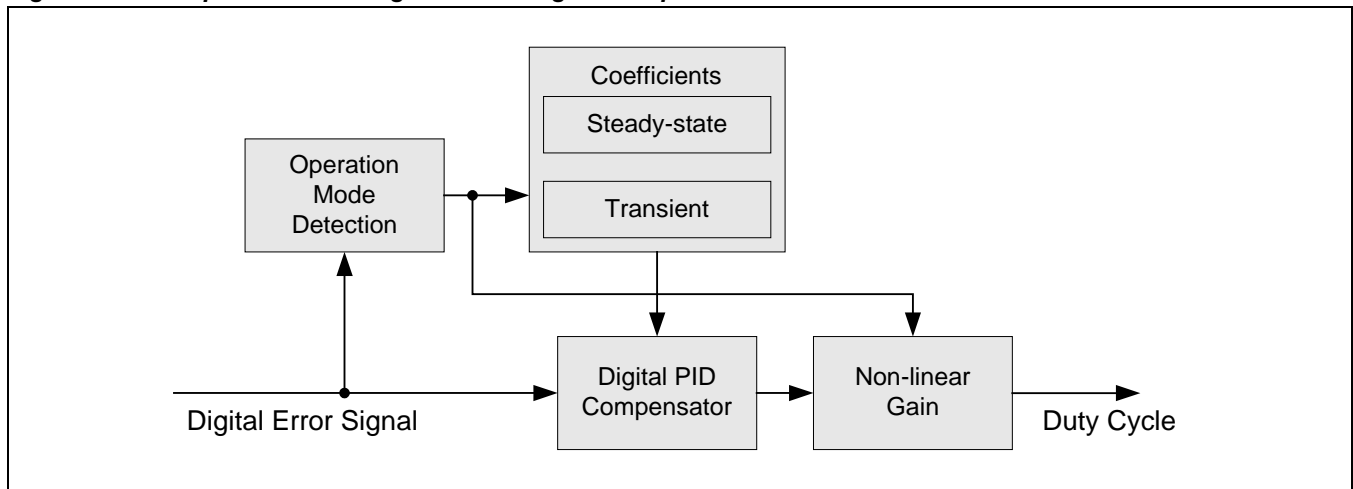
The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

Although the reference DAC generates a voltage up to 1.44V, keeping the voltage on the feedback pin (VFBP) at approximately 1.20V is recommended to guarantee sufficient headroom. If a larger output voltage is required, an external feedback divider is required.

3.3.4. Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. This digital control loop works as a voltage-mode controller using a PID-type compensation. The basic structure of the controller is shown in Figure 3.1. The proprietary State-Law™ Control (SLC) concept features two parallel compensators for steady-state operation and fast transient operation. The coefficients for the two modes can be derived using the Pink Power Designer™ graphical user interface (GUI). The ZSPM2000 implements fast, reliable switching between the different compensation modes in order to ensure good transient performance and a quiet steady state. This allows tuning the compensators individually for the respective needs; i.e., quiet steady-state and fast transient performance.

Figure 3.1 Simplified Block Diagram of the Digital Compensation



Additionally, three different techniques are used to improve transient performance further. Tru-sample Technology™ is used to acquire fast, accurate, and continuous information about the output voltage so that the ZSPM2000 can react quickly to any change in output voltage. Tru-sample Technology™ reduces phase-lag caused by sampling delays, reduces noise sensitivity, and improves transient performance.

The Sub-cycle Response™ (SCR) technique, a method to drive the DPWM asynchronously during load transients, allows limiting the maximum deviation of the output voltage and allows recharging the output capacitors faster.

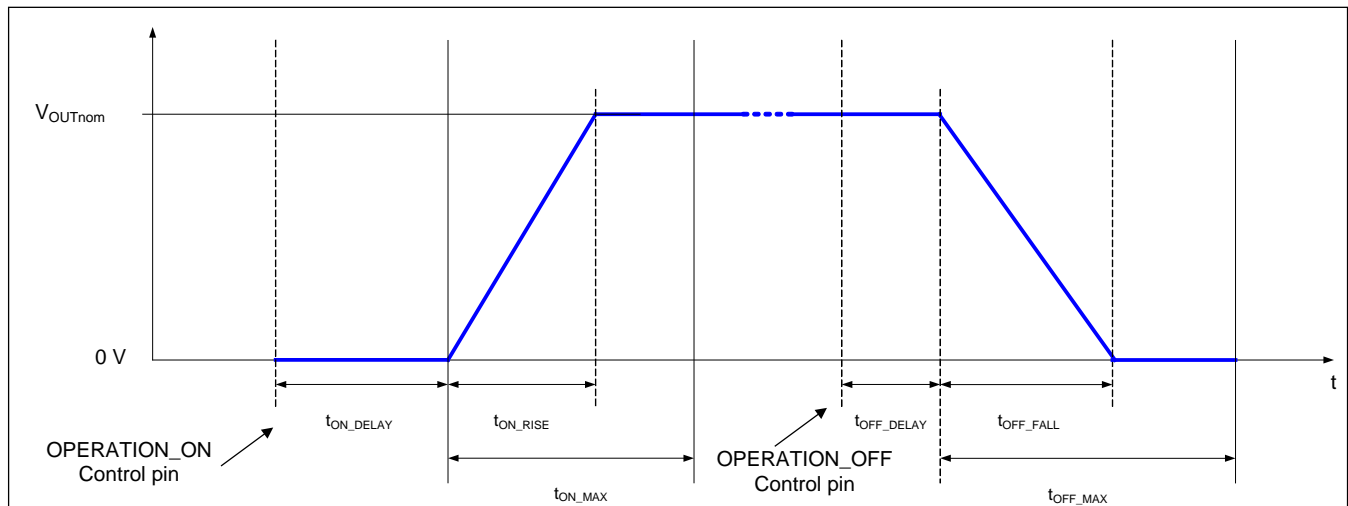
A non-linear gain adjustment is used during large load transients to boost the loop gain and reduce the settling time.

The DPWM supports switching frequencies up to 1MHz with a resolution of approximately 163ps. The minimum on-time and the maximum off-time of the modulation signal can be configured so that the ZSPM2000 can match the external power MOSFETs optimally. The functionality of the synchronous MOSFET driver is described in section 6.

3.3.5. Power Sequencing and the CONTROL Pin

The ZSPM2000 supports power sequencing features including ramp up/down and delays programmable via the Pink Power Designer™ GUI. The typical sequence of events is shown in Figure 3.2 and follows the PMBus™ standard. The individual values can be configured using the appropriate configuration setting. Three different configuration options are supported to turn on the output of the ZSPM2000. The device can be configured to turn on immediately after POR, on an OPERATION_ON command, or on an edge on the CONTROL pin.

Figure 3.2 Power Sequencing

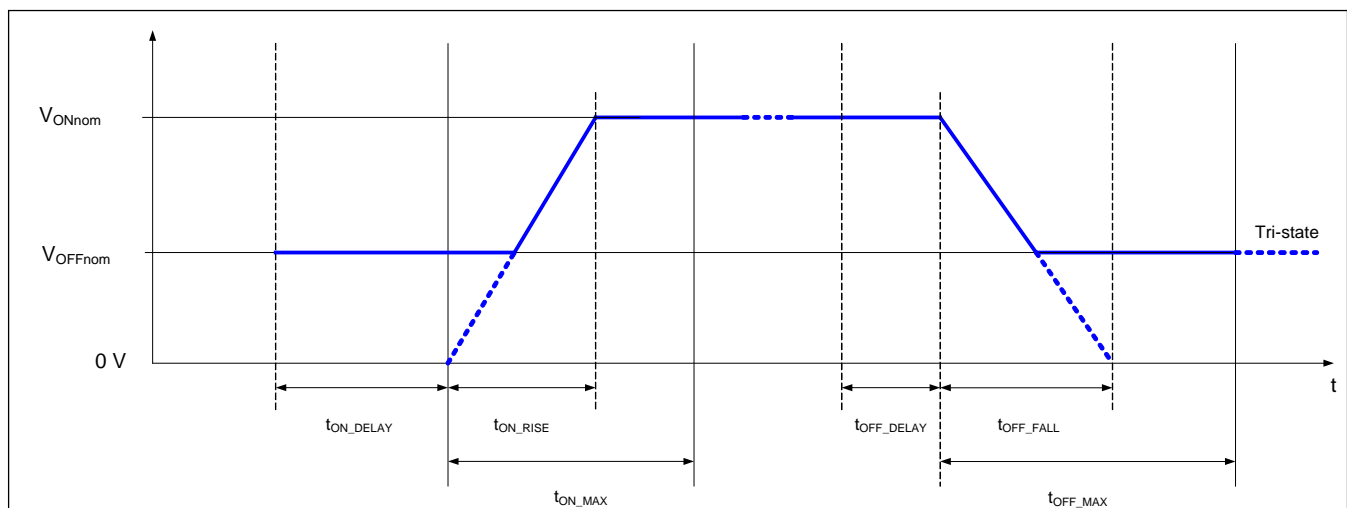


3.3.6. Pre-biased Start-up and Soft Stop

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

The ZSPM2000 also supports pre-biased off, i.e. the output voltage is not ramped down to zero and instead remains at a predefined level (V_{OFF_nom}). This value can be configured via the Pink Power Designer™ graphical user interface (GUI). After receiving the shutdown command, via PMBus™ or the CONTROL pin, the ZSPM2000 ramps down the value to the predefined value. Once the value is reached the MOSFET driver will be put into tri-state mode. Both gate drive outputs will be pulled low in the tri-state mode.

Figure 3.3 Power Sequencing with Non-zero Off Voltage

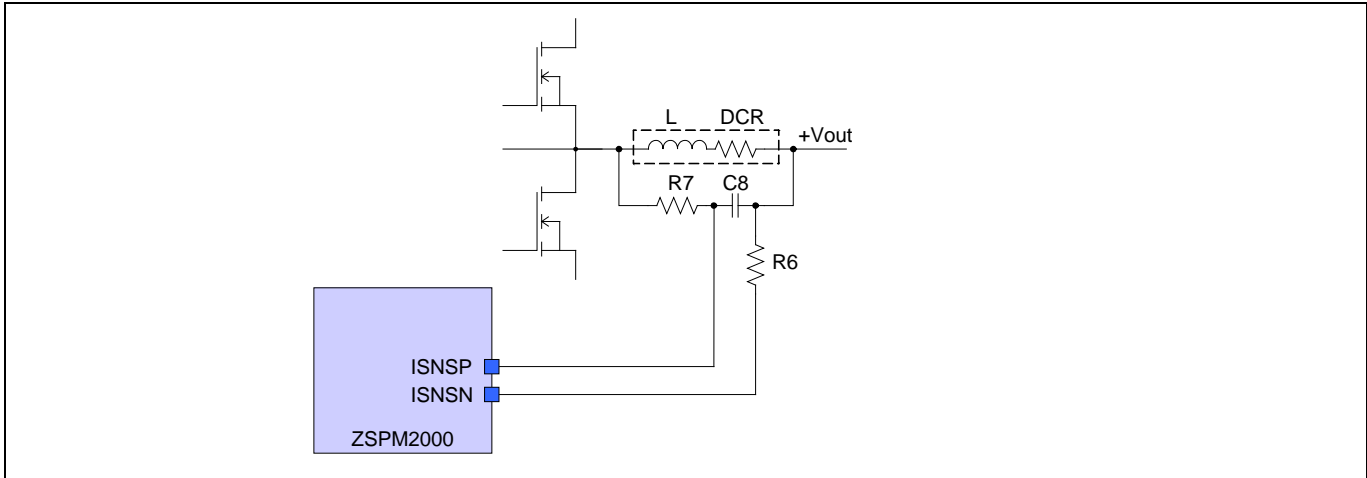


3.3.7. Current Sensing

The ZSPM2000 offers cycle-by-cycle average current sensing with configurable over-current protection. A dedicated ADC is used to provide fast and accurate current information over the switching period. The acquired information is compared with configurable current thresholds to report warning and error levels to the user. DCR current sensing across the inductor or across a dedicated shunt resistor is supported. Additionally, the device uses DCR temperature compensation via an external temperature sense element. This increases the accuracy of the current sense method by counteracting the significant change of the DCR over temperature.

To acquire accurate current information, the selection of the current sensing circuit is of critical importance. The schematic of the required current sensing circuitry is shown in Figure 3.4 for the widely-used DCR current-sensing method, which uses the parasitic resistance of the inductor to acquire the current information. The principle is based on a matched time-constant between the inductor and the low-pass filter comprising R7 and C8. The two resistors R6 and R7 should be matched fairly well in order to provide good DC voltage rejection; .i.e. to reduce the influence of the output voltage level in the current measurement.

Figure 3.4 Inductor Current Sensing Using the DCR Method



Alternatively, a simple shunt resistor can be used to measure the inductor current. The value of this resistor should be selected so that the voltage range between the pins is within the specifications given in section 1.

End-of-line calibration is supported so that the ZSPM2000 can achieve improved accuracy over the full output current range. The full calibration method is detailed in *ZSPM2000 Application Note—Programming and Calibration* (see section 9). This allows the user to correct mismatches between the nominal DCR value used to configure the device and the actual DCR value in the application caused by effects such as manufacturing variations. The calibration range is limited to $\pm 50\%$ of the nominal DCR.

Additionally, in order to improve the accuracy of the current measurement challenged by the temperature coefficient of the inductor's DCR, the ZSPM2000 features temperature compensation via external temperature sensing. The temperature of the inductors is measured with an external temperature sense element placed close to the inductor. This information is used to adapt the gain of the current sense path to compensate for the increase in actual DCR.

3.3.8. Temperature Measurement

The ZSPM2000 features two independent temperature measurement units for internal and external temperature. The internal temperature sensing measures the temperatures inside the ZSPM2000. The external temperature sense element should be placed close to the inductor to measure its temperature. A PN-junction is used as an external temperature sense element. Small-signal transistors, such as the 3904, are widely used for this application. The configuration of the sensitivity and the offset is required in the Pink Power Designer™ GUI. A temperature calibration via the Pink Power Designer™ or as part of the end-of-line calibration during production is highly recommended.

3.4. Fault Monitoring and Response Generation

The ZSPM2000 monitors various signals during operation. Depending on the selected configuration, it can respond to events generated by these signals. A wide range of options is configurable via the Pink Power Designer™ GUI. Typical monitoring within the ZSPM2000 is a three-step process. First, an event is detected via a configurable set of thresholds. This event is then digitally filtered before the ZSPM2000 reacts with a configurable response. For all monitored signals, a warning and a fault threshold can be configured. If enabled, a warning sets a status flag (see sections 4.7.6 through 4.7.11), but does not trigger a response; whereas a fault also generates a response.

Each warning and fault event can be individually enabled. The assertion of the SMBALERT signal can also be configured to individual needs. An overview of the options and configuration is given in Table 3.2.

Table 3.2 Fault Configuration Overview

| Signal | Response Type | Delay Resolution | Maximum Delay |
|---------------------------------|-----------------|------------------|---------------|
| Output Over-Voltage Fault | Low impedance* | 500µs | 90ms |
| Output Under-Voltage Fault | Low-impedance* | 500µs | 90ms |
| Input Over-Voltage Fault | High-impedance* | 500µs | 90ms |
| Input Under-Voltage Fault | High-impedance* | 500µs | 90ms |
| Over-Current Fault | Low-impedance* | 500µs | 90ms |
| External Over-Temperature Fault | Soft-Off* | 5ms | 900ms |
| Internal Over-Temperature Fault | Soft-Off* | 5ms | 900ms |

* The default options shown can be changed via the Pink Power Designer™ GUI.

The ZSPM2000 supports different response types individually configurable for each fault. The “low-impedance” response turns off the high-side external MOSFET and enables the low-side external MOSFET. After t_{OFF_MAX} (see Figure 3.2), both MOSFETs will be turned off. Conversely, a “high-Z” response will disable both MOSFETs instantaneously. A “Soft-Off” response ramps the output voltage down similar to a power-down command. The voltage will be ramped down to the value selected for V_{OFF_nom} (see Figure 3.3). After t_{OFF_MAX} , the controller will disable the power stage by turning both switches off.

For each fault response, a delay and a retry setting can be configured via the Pink Power Designer™ GUI. If the delay value is set to non-zero, the ZSPM2000 will not respond to a fault immediately. Instead it will delay the response by the configured value and then reassess the signal. If the fault is still present, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded. The retry setting configures the number of restarts of the power converter after a fault event. This number can be between zero and seven, where a setting of seven represents an infinite retry operation. In analog controllers, this feature is also known as “hiccup mode.”

3.4.1. Output Over/Under-Voltage

To prevent damage to the load, the ZSPM2000 utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM outputs are turned off. The voltage fault level is generated by a 6-bit DAC with a reference voltage of 1.60V resulting in 25mV resolution.

Additionally, the output voltage is sampled using the HKADC and continuously compared with an output over-voltage warning threshold. If the output voltage exceeds this threshold, a warning is generated and the preconfigured actions for the SMBALERT pin are triggered.

The ZSPM2000 also monitors the output voltage with two lower thresholds. If the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated and the configured response is activated.

3.4.2. Output Current Protection and Limiting

The ZSPM2000 continuously monitors the average inductor current and utilizes this information to protect the power supply from excessive output current. Two different types of protection are configurable independently.

Output current limiting to a value configurable via the Pink Power Designer™ GUI is supported by reducing the output voltage. Additionally, the maximum output current warning and fault threshold can be used to shut down the ZSPM2000. Both features can be enabled independently. If the over-current fault threshold is chosen below the current limiting threshold, the ZSPM2000 will shut down without going into current limiting mode.

3.4.3. Over-Temperature Protection

The ZSPM2000 monitors internal and external temperature. For each, a warning and a fault level can be configured and an appropriate response can be enabled.

3.5. GPIO0 Pin Configuration

The ZSPM2000 offers a flexible configuration scheme for its digital I/O pin. This enables using the GPIO0 pin (general purpose input/output) with different functions depending on the application requirements. The configuration options are listed in Table 3.3.

Table 3.3 *GPIO0 Pin Configuration Options*

| Pin | Thermal shutdown | Hardwire Option |
|-------|---------------------|---------------------|
| GPIO0 | High and low active | High and low active |

The GPIO pin can be hardwired to be high or low, or it can be used as a thermal shutdown input. If the pin is asserted by an external source, for example the thermal shutdown flag of an external temperature sensor, the ZSPM2000 flags an external over-temperature fault and reacts accordingly.

3.6. Configuration

The ZSPM2000 incorporates two different sets of configuration parameters. The first set of configuration parameters can be configured during design time and cannot be changed during run-time. The second set of configuration parameters can be configured during design time, but can also be reconfigured during run-time using the appropriate PMBus™ command. Note that these reconfigured values are not stored in the OTP memory, so they are lost during power cycling the device.

In order to evaluate the device and its configuration on the bench, a special engineering mode is supported by the device and Pink Power Designer™ GUI; i.e. the device can be reconfigured multiple times without writing the configuration into the OTP. During this engineering mode, the device starts up after power-on reset in an unconfigured state. The Pink Power Designer™ then provides the configuration to the ZSPM2000, enabling full operation without actually configuring the OTP. The engineer can use this mode to evaluate the configuration on the bench. However, the configuration will be lost upon power-on-reset.

After the design engineer has determined the final configuration options, an OTP image can be created that is then written into the ZSPM2000. This can be either on the bench using the Pink Power Designer™ or in end-of-line testing during mass production.

4 PMBus™ Functionality

4.1. Introduction

The ZSPM2000 supports the PMBus™ protocol to enable the use of configuration, monitoring, and fault management during run-time.

The PMBus™ host controller is connected to the ZSPM2000 via the PMBus™ pins: SDA and SCL. A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The ZSPM2000 supports packet error correction (PEC) according to the PMBus™ specification.

4.2. Timing and Bus Specification

Figure 4.1 PMBus™ Timing Diagram

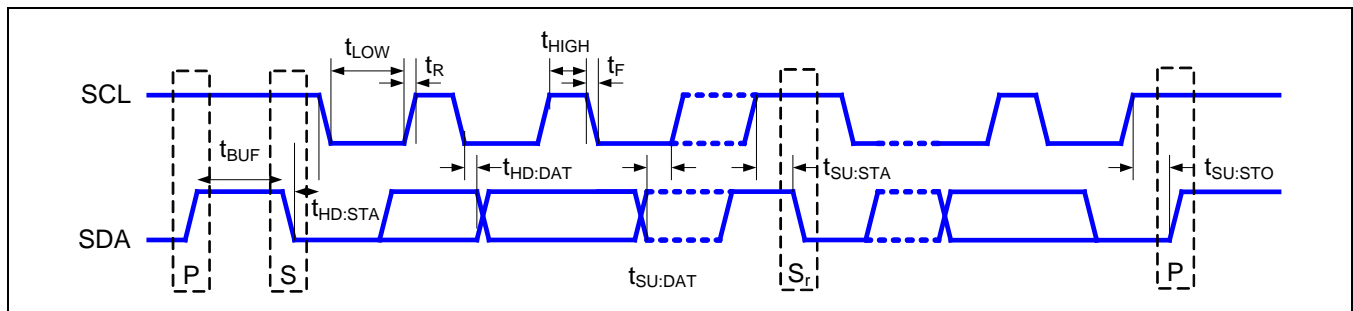


Table 4.1 PMBus™ Timing Specification

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------|------------|-----|-----|-----|---------|
| SMBus operation frequency | f_{SMB} | | 10 | 400 | 500 | kHz |
| Bus free time between start and stop | t_{BUF} | | 1.3 | | | μs |
| Hold time after start condition | $t_{HD:STA}$ | | 0.6 | | | μs |
| Repeat start condition setup time | $t_{SU:STA}$ | | 0.6 | | | μs |
| Stop condition setup time | $t_{SU:STO}$ | | 0.6 | | | μs |
| Data hold time | $t_{HD:DAT}$ | | 300 | | | ns |
| Data setup time | $t_{SU:DAT}$ | | 100 | | | ns |
| Clock low time-out | $t_{TIMEOUT}$ | | | 25 | 35 | ms |
| Clock low period | t_{LOW} | | 1.3 | | | μs |
| Clock high period | t_{HIGH} | | 0.6 | | | μs |
| Cumulative clock low extend time | $t_{LOW:SEXT}$ | | | | 25 | ms |
| Clock or data fall time | t_F | | | | 300 | ns |
| Clock or data rise time | t_R | | | | 300 | ns |

4.3. Address Selection via External Resistors

PMBus™ uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDR_x pins.

The resistor values are sensed using the internal ADC during the initialization phase, and the appropriate PMBus™ address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus™ addresses and the values of the respective required resistors are listed in Table 4.2.

Table 4.2 Supported Resistor Values for PMBus™ Address Selection

| Address (Decimal) | ADDR1 Ω | ADDR0 Ω | Address (Decimal) | ADDR1 Ω | ADDR0 Ω | Address (Decimal) | ADDR1 Ω | ADDR0 Ω | Address (Decimal) | ADDR1 Ω | ADDR0 Ω |
|-------------------|---------|---------|-------------------|---------|---------|-------------------|---------|---------|-------------------|---------|---------|
| 64 | 0 | 0 | 32 | 1.2k | 0 | 64 | 2.7k | 0 | 96 | 4.7k | 0 |
| 1* | 0 | 680 | 33 | 1.2k | 680 | 65 | 2.7k | 680 | 97* | 4.7k | 680 |
| 2* | 0 | 1.2k | 34 | 1.2k | 1.2k | 66 | 2.7k | 1.2k | 98 | 4.7k | 1.2k |
| 3* | 0 | 1.8k | 35 | 1.2k | 1.8k | 67 | 2.7k | 1.8k | 99 | 4.7k | 1.8k |
| 4* | 0 | 2.7k | 36 | 1.2k | 2.7k | 68 | 2.7k | 2.7k | 100 | 4.7k | 2.7k |
| 5* | 0 | 3.9k | 37 | 1.2k | 3.9k | 69 | 2.7k | 3.9k | 101 | 4.7k | 3.9k |
| 6* | 0 | 4.7k | 38 | 1.2k | 4.7k | 70 | 2.7k | 4.7k | 102 | 4.7k | 4.7k |
| 7* | 0 | 5.6k | 39 | 1.2k | 5.6k | 71 | 2.7k | 5.6k | 103 | 4.7k | 5.6k |
| 8* | 0 | 6.8k | 40* | 1.2k | 6.8k | 72 | 2.7k | 6.8k | 104 | 4.7k | 6.8k |
| 9 | 0 | 8.2k | 41 | 1.2k | 8.2k | 73 | 2.7k | 8.2k | 105 | 4.7k | 8.2k |
| 10 | 0 | 10k | 42 | 1.2k | 10k | 74 | 2.7k | 10k | 106 | 4.7k | 10k |
| 11 | 0 | 12k | 43 | 1.2k | 12k | 75 | 2.7k | 12k | 107 | 4.7k | 12k |
| 12* | 0 | 15k | 44 | 1.2k | 15k | 76 | 2.7k | 15k | 108 | 4.7k | 15k |
| 13 | 0 | 18k | 45 | 1.2k | 18k | 77 | 2.7k | 18k | 109 | 4.7k | 18k |
| 14 | 0 | 22k | 46 | 1.2k | 22k | 78 | 2.7k | 22k | 110 | 4.7k | 22k |
| 15 | 0 | 27k | 47 | 1.2k | 27k | 79 | 2.7k | 27k | 111 | 4.7k | 27k |
| 16 | 680 | 0 | 48 | 1.8k | 0 | 80 | 3.9k | 0 | 112 | 5.6k | 0 |
| 17 | 680 | 680 | 49 | 1.8k | 680 | 81 | 3.9k | 680 | 113 | 5.6k | 680 |
| 18 | 680 | 1.2k | 50 | 1.8k | 1.2k | 82 | 3.9k | 1.2k | 114 | 5.6k | 1.2k |
| 19 | 680 | 1.8k | 51 | 1.8k | 1.8k | 83 | 3.9k | 1.8k | 115 | 5.6k | 1.8k |
| 20 | 680 | 2.7k | 52 | 1.8k | 2.7k | 84 | 3.9k | 2.7k | 116 | 5.6k | 2.7k |
| 21 | 680 | 3.9k | 53 | 1.8k | 3.9k | 85 | 3.9k | 3.9k | 117 | 5.6k | 3.9k |
| 22 | 680 | 4.7k | 54 | 1.8k | 4.7k | 86 | 3.9k | 4.7k | 118 | 5.6k | 4.7k |
| 23 | 680 | 5.6k | 55* | 1.8k | 5.6k | 87 | 3.9k | 5.6k | 119 | 5.6k | 5.6k |
| 24 | 680 | 6.8k | 56 | 1.8k | 6.8k | 88 | 3.9k | 6.8k | 120* | 5.6k | 6.8k |
| 25 | 680 | 8.2k | 57 | 1.8k | 8.2k | 89 | 3.9k | 8.2k | 121* | 5.6k | 8.2k |
| 26 | 680 | 10k | 58 | 1.8k | 10k | 90 | 3.9k | 10k | 122* | 5.6k | 10k |
| 27 | 680 | 12k | 59 | 1.8k | 12k | 91 | 3.9k | 12k | 123* | 5.6k | 12k |
| 28 | 680 | 15k | 60 | 1.8k | 15k | 92 | 3.9k | 15k | 124* | 5.6k | 15k |
| 29 | 680 | 18k | 61 | 1.8k | 18k | 93 | 3.9k | 18k | 125* | 5.6k | 18k |
| 30 | 680 | 22k | 62 | 1.8k | 22k | 94 | 3.9k | 22k | 126* | 5.6k | 22k |
| 31 | 680 | 27k | 63 | 1.8k | 27k | 95 | 3.9k | 27k | 127* | 5.6k | 27k |

Note: The addresses marked with an asterisk () are reserved by the SMBus specification.

If only four devices are used in a system, their respective addresses can alternatively be configured without resistors by connecting the pins to GND or AVDD18 pin. The PMBus™ addresses selectable in this fashion are listed in Table 4.3.

Table 4.3 PMBus™ Address Selection without Resistors

| Address | ADDR1 | ADDR0 |
|---------|--------|--------|
| 15 | GND | AVDD18 |
| 48 | AVDD18 | GND |
| 63 | AVDD18 | AVDD18 |
| 64 | GND | GND |

4.4. Configuration Registers

The registers described in Table 4.4 are used to configure the ZSPM2000 as explained in section 3.6. Registers classified as OTP cannot be changed during run-time. Registers classified as PMBus™ can be changed during run-time with PMBus™ commands.

Table 4.4 List of Supported PMBus™ Configuration Registers

Note: See important notes at the end of the table.

| PMBus™ Parameter | Description | Data Format | Classification |
|------------------------|--|-----------------------|----------------|
| Output Voltage | | | |
| ON_OFF_CONFIG | On/off configuration | N/A | PMBus™ |
| VOUT_MODE | Exponent of the VOUT_COMMAND value | N/A | Read only |
| VOUT_COMMAND | Set output voltage | LINEAR ⁽¹⁾ | PMBus™ |
| VOUT_OV_FAULT_LIMIT | Over-voltage fault limit | N/A | OTP |
| VOUT_OV_FAULT_RESPONSE | Over-voltage fault response | N/A | OTP |
| VOUT_OV_WARN_LIMIT | Over-voltage warning level | N/A | OTP |
| VOUT_UV_WARN_LIMIT | Under-voltage warning level | N/A | OTP |
| VOUT_UV_FAULT_LIMIT | Under-voltage fault level | N/A | OTP |
| VOUT_UV_FAULT_RESPONSE | Under-voltage fault response | N/A | OTP |
| Output Current | | | |
| IOUT_OC_FAULT_LIMIT | Over-current fault limit | N/A | OTP |
| IOUT_OC_FAULT_RESPONSE | Over-current fault response | N/A | OTP |
| IOUT_OC_LV_FAULT_LIMIT | Voltage threshold during constant-current mode | N/A | OTP |
| IOUT_OC_WARN_LIMIT | Over-current warning level | N/A | OTP |

| PMBus™ Parameter | Description | Data Format | Classification |
|---|---------------------------------|-------------|----------------|
| Temperature - External | | | |
| OT_FAULT_LIMIT | Over-temperature fault level | N/A | OTP |
| OT_FAULT_RESPONSE | Over-temperature fault response | N/A | OTP |
| OT_WARN_LIMIT | Over-temperature warning level | N/A | OTP |
| Temperature - Internal | | | |
| IOT_FAULT_LIMIT | Over-temperature fault level | N/A | OTP |
| IOT_FAULT_RESPONSE | Over-temperature fault response | N/A | OTP |
| IOT_WARN_LIMIT | Over-temperature warning level | N/A | OTP |
| Input Voltage | | | |
| VIN_OV_FAULT_LIMIT | Over-voltage fault limit | N/A | OTP |
| VIN_OV_FAULT_RESPONSE | Over-voltage fault response | N/A | OTP |
| VIN_OV_WARN_LIMIT | Over-voltage warning level | N/A | OTP |
| VIN_UV_WARN_LIMIT | Under-voltage warning level | N/A | OTP |
| VIN_UV_FAULT_LIMIT | Under-voltage fault level | N/A | OTP |
| VIN_UV_FAULT_RESPONSE | Under-voltage fault response | N/A | OTP |
| Start-up Behavior / Power Sequencing | | | |
| POWER_GOOD_ON | Power good on threshold | N/A | OTP |
| POWER_GOOD_OFF | Power good off threshold | N/A | OTP |
| Output Voltage Sequencing | | | |
| TON_DELAY | Turn-on delay | N/A | OTP |
| TON_RISE | Turn-on rise time | N/A | OTP |
| TON_FAULT_MAX | Turn-on maximum fault time | N/A | OTP |
| TOFF_DELAY | Turn-off delay | N/A | OTP |
| TOFF_FALL | Turn-off fall time | N/A | OTP |
| TOFF_WARN_MAX | Turn-off maximum warning time | N/A | OTP |
| VOFF_NOM | Soft-stop off value | N/A | OTP |
| Notes: | | | |
| 1. <i>VOUT_MODE</i> is read-only for this device. | | | |

The ZSPM2000 supports the LINEAR data format according to the PMBus™ specification. Note that in accordance with the PMBus™ specification, all commands related to the output voltage are subject to the VOUT_MODE settings. Note that VOUT_MODE is read-only for the ZSPM2000.

4.5. Monitoring

The ZSPM2000 has a dedicated set of PMBus™ registers to enable advanced power management using extensive monitoring features. Different warning and error flags can be read by the PMBus™ master to ensure proper operation of the power converter or monitor the converters over its lifetime.

Table 4.5 List of Supported PMBus™ Status Registers/Commands

| PMBus™ Command | Code | Description | Data Format |
|---------------------|-------------------|---------------------------------|-------------|
| CLEAR_FAULTS | 03 _{HEX} | Clear status information | |
| STATUS_BYTE | 78 _{HEX} | Unit status byte | |
| STATUS_WORD | 79 _{HEX} | Unit status word | |
| STATUS_VOUT | 7A _{HEX} | Output voltage status | |
| STATUS_IOUT | 7B _{HEX} | Output current status | |
| STATUS_INPUT | 7C _{HEX} | Input status | |
| STATUS_TEMPERATURE | 7D _{HEX} | Temperature status | |
| STATUS_CML | 7E _{HEX} | Communication and memory status | |
| STATUS_MFR_SPECIFIC | 7F _{HEX} | Manufacturer-specific status | |
| READ_VIN | 88 _{HEX} | Input voltage read back | LINEAR |
| READ_VOUT | 8B _{HEX} | Output voltage read back | LINEAR |
| READ_IOUT | 8C _{HEX} | Output current read back | LINEAR |
| READ_TEMPERATURE_1 | 8D _{HEX} | External temperature read back | LINEAR |
| READ_TEMPERATURE_2 | 8E _{HEX} | Internal temperature read back | LINEAR |

4.6. Miscellaneous

Table 4.6 Additional Supported PMBus™ Registers

| PMBus™ Command | Code | Description | Data Length (Byte) | Values |
|----------------|-------------------|-------------------------------|--------------------|---|
| PMBUS_REVISION | 98 _{HEX} | PMBus™ revision | 1 | 11 _{HEX} |
| MFR_ID | 99 _{HEX} | Manufacturer ID | 4 | "ZMDI" (5A _{HEX} , 4D _{HEX} , 44 _{HEX} , 49 _{HEX}) |
| MFR_MODEL | 9A _{HEX} | Manufacturer model identifier | 4 | "2000" (32 _{HEX} , 30 _{HEX} , 30 _{HEX} , 30 _{HEX}) |
| MFR_REVISION | 9B _{HEX} | Manufacturer product revision | 4 | |
| MFR_SERIAL | 9E _{HEX} | Serial number | 12 | |

4.7. Detailed Description of the Supported PMBus™ Commands

4.7.1. OPERATION Command

The OPERATION command is used to turn the unit on and off in conjunction with the input from the CONTROL pin. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the CONTROL pin instructs the ZSPM2000 to change to another mode. The supported operation modes are listed in Table 4.7.

Table 4.7 Supported PMBus™ Operation Modes

| OPERATION (01 _{HEX} , read/write) | | | | | |
|--|-----------|-----------|-----------|----------------------------|--------------|
| Bits[7:6] | Bits[5:4] | Bits[3:2] | Bits[1:0] | Unit On or Off | Margin State |
| 01 | XX | XX | XX | Soft Off (With Sequencing) | N/A |
| 10 | 00 | XX | XX | On | Off |

4.7.2. ON_OFF_CONFIG Command

The ON_OFF_CONFIG command is used to configure the combination of the CONTROL pin and PMBus™ OPERATION command that turns the unit on or off. The supported configuration options are listed in Table 4.8.

Table 4.8 Supported PMBus™ ON_OFF_CONFIG Options

| ON_OFF_CONFIG (02 _{HEX} , read/write) | | |
|--|------------------|--|
| Bits | Name | Description |
| [0] | CONTROL OFF | Value ignored. Device always uses the programmed turn off delay and fall time. |
| [1] | CONTROL Polarity | 0: Active low (pull pin low to start the unit). 1: Active high (pull pin high to start the unit). |
| [2] | CONTROL Enable | 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit.* |
| [3] | OPERATION Enable | 0: Unit ignores the on/off settings in the OPERATION command. 1: Unit requires the on/off settings in the OPERATION command to start the unit*. |

* Depending on the configuration, both conditions must be in the on state in order to turn on the unit.

4.7.3. CLEAR_FAULTS Command

The CLEAR_FAULTS command is used to clear any fault bits that have been set in the status registers. Additionally, the SMBALERT signal is cleared if it was previously asserted. Note that the device resumes operation with the currently configured state after a CLEAR_FAULTS command has been issued. If a fault/warning is still present, the respective bit is set immediately again.

4.7.4. VOUT_MODE Command

The VOUT_MODE command is used to retrieve information about the data format for all output voltage related commands. Note that this is a read-only value.

| VOUT_MODE (20 _{HEX} , read only) | | |
|---|-----------|--------------------------------|
| Bits | Name | Description |
| [4:0] | PARAMETER | 2's complement of the exponent |
| [7:5] | MODE | 000: Linear data format |

4.7.5. VOUT_COMMAND Command

The VOUT_COMMAND is used to set the output voltage during run-time.

| VOUT_COMMAND (21 _{HEX} , read/write) | | |
|---|----------|---|
| Bits | Name | Description |
| [15:0] | MANTISSA | Unsigned mantissa of output voltage in V. Exponent can be retrieved via VOUT_MODE command. |

4.7.6. STATUS_BYTE Command

The STATUS_BYTE command returns a summary of the most critical faults in one byte.

| STATUS_BYTE (78 _{HEX} , read only) | | |
|---|-------------------|--|
| Bits | Name | Description |
| [0] | NONE OF THE ABOVE | A fault not listed in bits [7:1] has occurred. |
| [1] | CML | A communication fault as occurred. |
| [2] | TEMPERATURE | A temperature fault or warning has occurred. |
| [3] | VIN_UV | An input under-voltage fault has occurred. |
| [4] | IOUT_OC | An output over-current fault has occurred. |
| [5] | VOUT_OV | An output over-voltage fault has occurred. |
| [6] | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| [7] | BUSY | Not supported. |

4.7.7. STATUS_WORD Command

The STATUS_WORD command returns a summary of the device status information in two data bytes.

| STATUS_WORD (79 _{HEX} , read only) | | |
|---|-------------|--|
| Bits | Name | Description |
| [7:0] | STATUS_BYTE | See status byte (section 4.7.6). |
| [8] | UNKNOWN | Not supported |
| [9] | OTHER | Not supported |
| [10] | FANS | No supported |
| [11] | POWER_GOOD# | The POWER_GOOD signal, if present, is negated. |
| [12] | MFR | A manufacturer-specific fault or warning has occurred. |
| [13] | INPUT | An input related warning or fault has occurred. |
| [14] | IOUT/POUT | An output current or output power warning or fault has occurred. |
| [15] | VOUT | An output voltage related warning or fault has occurred. |

4.7.8. STATUS_VOUT Command

| STATUS_VOUT (7A _{HEX} , read only) | | |
|---|--------------|---|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | VOUT_UV_FLT | An output voltage under-voltage fault has occurred. |
| [5] | VOUT_UV_WARN | An output voltage under-voltage warning has occurred. |
| [6] | VOUT_OV_WARN | An output voltage over-voltage warning has occurred. |
| [7] | VOUT_OV_FLT | An output voltage over-voltage fault has occurred. |

4.7.9. STATUS_IOUT Command

| STATUS_IOUT (7B _{HEX} , read only) | | |
|---|-----------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | IOUT_OC_WARN | An over-current warning has occurred. |
| [6] | ICOUT_OC_LV_FLT | An over-current low-voltage shutdown fault has occurred. |
| [7] | IOUT_OC_FLT | An over-current fault has occurred. |

4.7.10. STATUS_INPUT Command

| STATUS_INPUT (7C _{HEX} , read only) | | |
|--|-------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | VIN_UV_FLT | An input voltage under-voltage fault has occurred. |
| [5] | VIN_UV_WARN | An input voltage under-voltage warning has occurred. |
| [6] | VIN_OV_WARN | An input voltage over-voltage warning has occurred. |
| [7] | VIN_OV_FLT | An input voltage over-voltage fault has occurred. |

4.7.11. STATUS_TEMPERATURE Command

| STATUS_TEMPERATURE (7D _{HEX} , read only) | | |
|--|--------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | | Not supported. |
| [6] | TEMP_OV_WARN | An (external) over-temperature warning has occurred. |
| [7] | TEMP_OV_FLT | An (external) over-temperature fault has occurred. |

4.7.12. STATUS_CML Command

| STATUS_CML (7E _{HEX} , read only) | | |
|--|-----------|---|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | SMBUS_FLT | SMBus™ timeout or a format error has occurred. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | PEC_FLT | A packet error check fault has occurred. |
| [6] | | Not supported. |
| [7] | CMD_FLT | An invalid or an unsupported command has been received. |

4.7.13. STATUS_MFR_SPECIFIC Command

| STATUS_MFR_SPECIFIC (80 _{HEX} , read only) | | |
|---|---------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | | Not supported. |
| [6] | ITEMP_OV_WARN | An (internal) over-temperature warning has occurred. |
| [7] | ITEMP_OV_FLT | An (internal) over-temperature fault has occurred. |

4.7.14. READ_VIN Command

| READ_VIN (88 _{HEX} , read only) | | |
|--|------|--|
| Bits | Name | Description |
| [15:0] | VIN | Input voltage in V (linear data format). |

4.7.15. READ_VOUT Command

| READ_VOUT (8B _{HEX} , read only) | | |
|---|------|---|
| Bits | Name | Description |
| [15:0] | VOUT | Output voltage in V (linear data format). Note that this command is mantissa only. |

4.7.16. READ_IOUT Command

| READ_IOUT (8C _{HEX} , read only) | | |
|---|--|--|
|---|--|--|

| Bits | Name | Description |
|--------|------|---|
| [15:0] | IOUT | Output current in amperes (linear data format). |

4.7.17. READ_TEMPERATURE1 Command

| READ_TEMPERATURE1 (8D _{HEX} , read only) | | |
|---|-------|--|
| Bits | Name | Description |
| [15:0] | TEMP1 | External temperature in °C (linear data format). |

4.7.18. READ_TEMPERATURE2 Command

| READ_TEMPERATURE2 (8E _{HEX} , read only) | | |
|---|-------|--|
| Bits | Name | Description |
| [15:0] | TEMP2 | Internal temperature in °C (linear data format). |

5 External Component Selection

5.1 Output Voltage Feedback Components

The ZSPM2000 supports direct output voltage feedback without external components up to an output voltage of 1.4V. However, adding a high-frequency low-pass filter in the sense path is highly recommended to remove high-frequency disturbances from the sense signals. Placing these components as close as possible to the ZSPM2000 is recommended. For larger output voltages, a feedback divider is required. Using resistors with small tolerances is recommended to guarantee good output voltage accuracy. Table 5.1 lists the required component values as a function of the maximum supportable output voltage. It is mandatory that the selected resistors values are configured in the Pink Power Designer™ GUI so that they can be taken into account for the configuration of the ZSPM2000.

Figure 5.1 Output Voltage Sense Circuitry

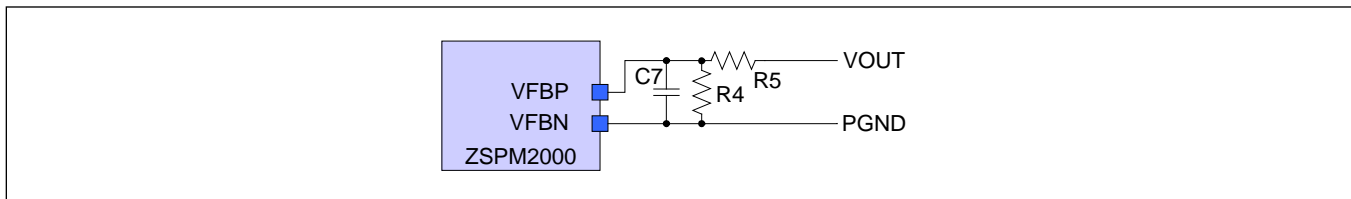
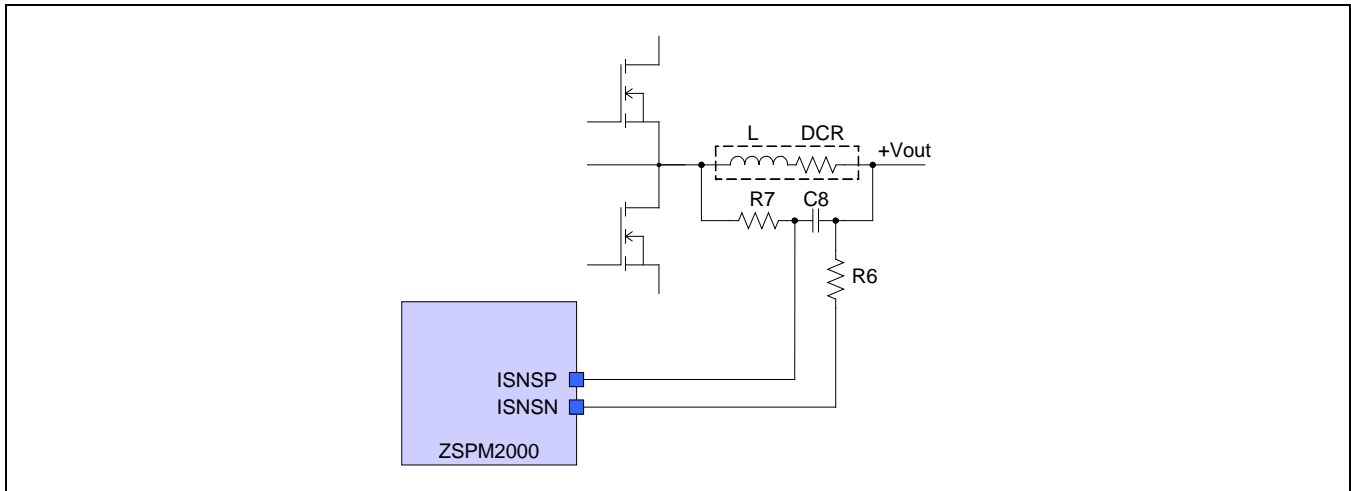


Table 5.1 Output Voltage Feedback Component Overview

| Nominal Output Voltage | Maximum Output Voltage | R4 | R5 | C7 |
|------------------------|------------------------|-------|-------|------|
| 1.20V | 1.40V | open | 1.0kΩ | 22pF |
| 1.80V | 2.1V | 1.5kΩ | 750Ω | 47pF |
| 2.50V | 2.80V | 1.0kΩ | 1.0kΩ | 47pF |
| 3.30V | 4.25V | 1.0kΩ | 2.2kΩ | 33pF |
| 5.00V | 5.00V | 1.0kΩ | 3.3kΩ | 33pF |

5.2. DCR Current Sensing Components

Figure 5.2 Inductor Current Sensing Using the DCR Method



The ZSPM2000 supports the loss-less DCR current sense method. The equivalent DC resistance (DCR) of the inductor is used to measure the inductor current without adding any additional components into the power path. The technique is based on matching the time constants of the inductor and the parallel low-pass filter. Therefore the components $R6$, $R7$, and $C8$ must be selected depending on the selected inductor. The following procedure is recommended:

- 1.) Set $R7 = 1k\Omega$
- 2.) Calculate $C8 = L / (DCR * R7)$.
- 3.) Pick capacitor $C8$ from the appropriate E-series close to $C8$.
- 4.) Recalculate $R6=R7= L / (DCR * C8)$ based on the capacitor selected for $C8$.

5.3. Input Voltage Sensing

The ZSPM2000 supports input voltage sensing for protection and monitoring. Therefore a voltage divider between the input voltage and the VIN pin is required. The recommended resistor values for different input voltage ranges can be found in Table 5.2. For different nominal input voltages, the respective component values with the maximum supported input voltage are listed. Optionally, a capacitor, typically 10nF, can be connected to the VIN pin to help improve accuracy.

Figure 5.3 Input Voltage Sense Circuitry

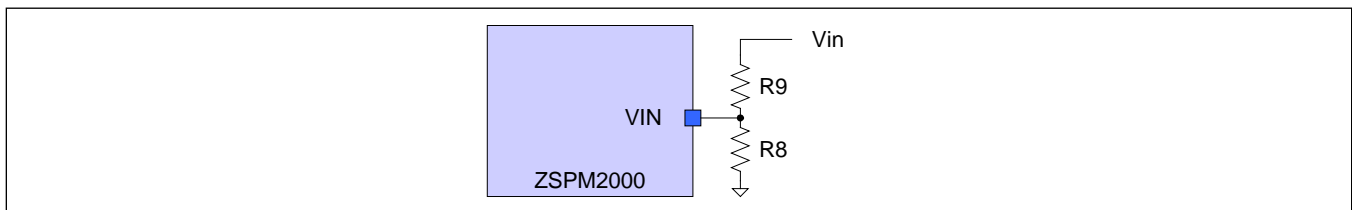


Table 5.2 Input Voltage Sense Component Overview

| Nominal Input Voltage | Maximum Input Voltage | R9 | R8 |
|-----------------------|-----------------------|---------------|---------------|
| 12V | 14.5V | 20k Ω | 2.2k Ω |
| 8.0V | 9.0V | 12k Ω | 2.2k Ω |
| 5.0V | 6.5V | 8.2k Ω | 2.2k Ω |

6 Synchronous MOSFET Driver Features

6.1. Introduction

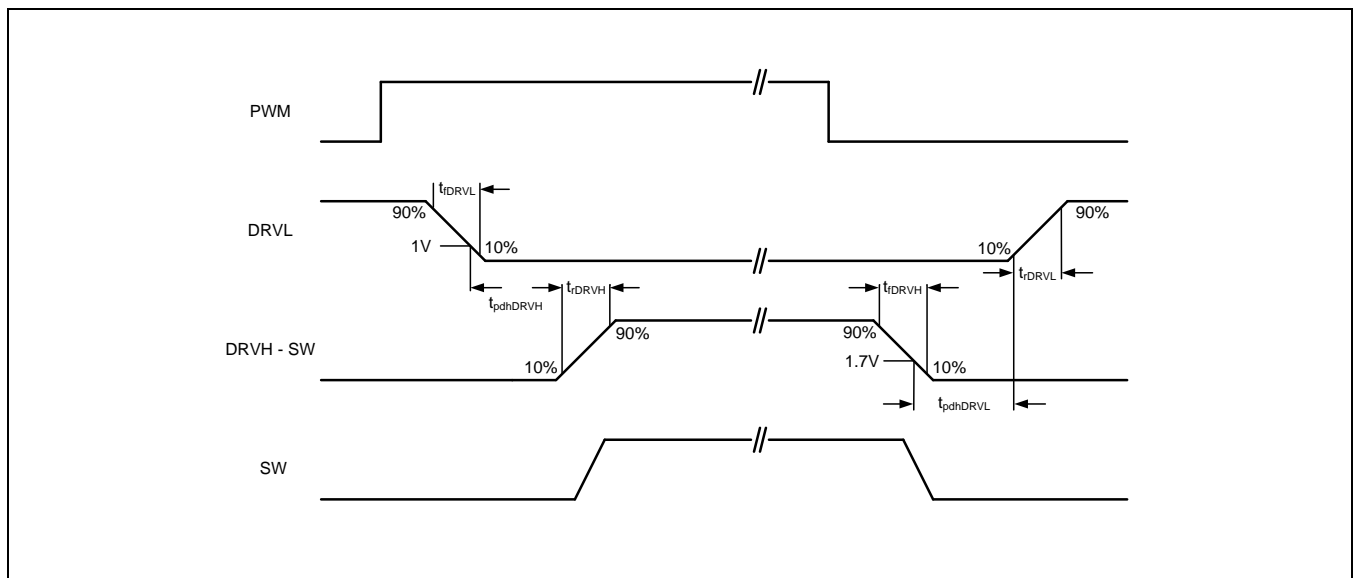
The synchronous MOSFET gate driver of the ZSPM2000 is designed to drive the N-channel MOSFETs of a low voltage step-down converter. The driver supply voltage (VDD50DRV) is 5V, and the driver is capable of driving a 3nF load. The input under-voltage lockout function guarantees the outputs are low when the supply voltage is low.

6.2. Adaptive Non-overlap Dead-Time Control

Adaptive dead-time control is used to avoid shoot-through damage of the power MOSFETs. See section 1.3 for the timing specifications for this function, which are illustrated in Figure 6.1. When the internal PWM signal pulls high, the driver will monitor the gate voltage of the low side MOSFET; i.e., the DRVL pin of the ZSPM2000. When the DRVL voltage falls below the gate threshold, DRVH will be set to high after the $t_{pdhDRVH}$ delay. When the PWM is set low, DRVH will be set low, and the driver will monitor the gate voltage of the high-side MOSFET. When the voltage between the DRVH and SW pins falls below the top gate drive threshold, DRVL will be set to high after the $t_{pdhDRVL}$ delay.

Figure 6.1 Adaptive Non-overlap Dead-Time Control Timing Diagram

Note: the PWM signal is internal.



6.3. Layout Guidelines

Layout of the point-of-load (POL) converter PCB is very important. The bootstrap (BST) pin and VDD50DRV pin decoupling capacitors should be placed as close as possible to the ZSPM2000. The VDD50DRV bypass capacitor should be connected to the PGND pin of the ZSPM2000.

Connect the PGND pin to the ground plane of the power stage. The ground plane can provide a good return path for the gate drive current and reduce the ground noise. To minimize the ground loop for the low-side MOSFET, place the PGND pin close to the source pin of the low-side MOSFET. The gate drive traces should be routed to minimize the length; the recommended minimum width is 20 mils.

7 Mechanical Specifications

Based on JEDEC MO-220. All dimensions are in millimeters.

Figure 7.1 28-Pin QFN Package Drawing

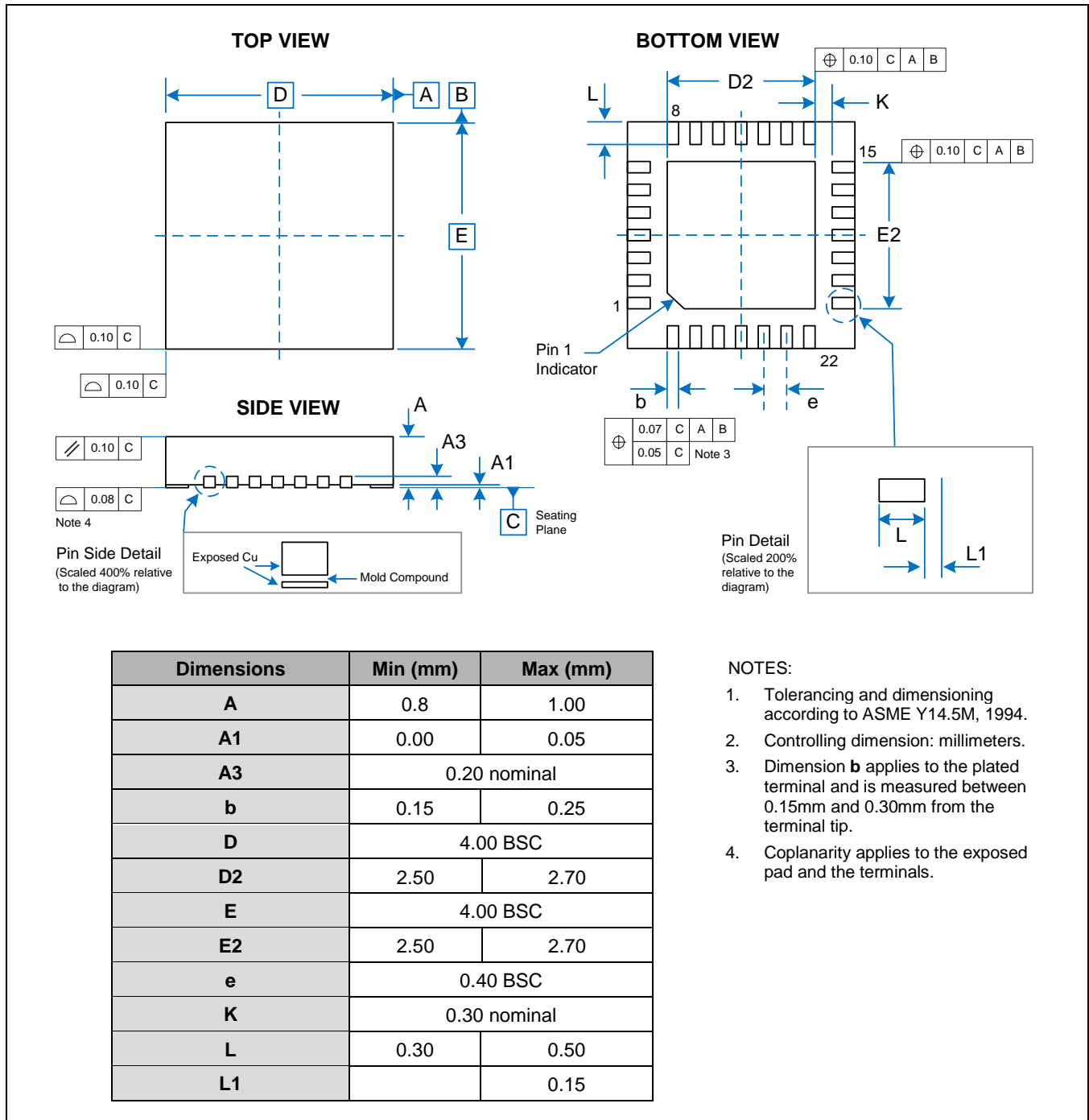


Figure 7.2 28-Pin QFN Recommended Mounting Footprint

All dimensions are in millimeters.

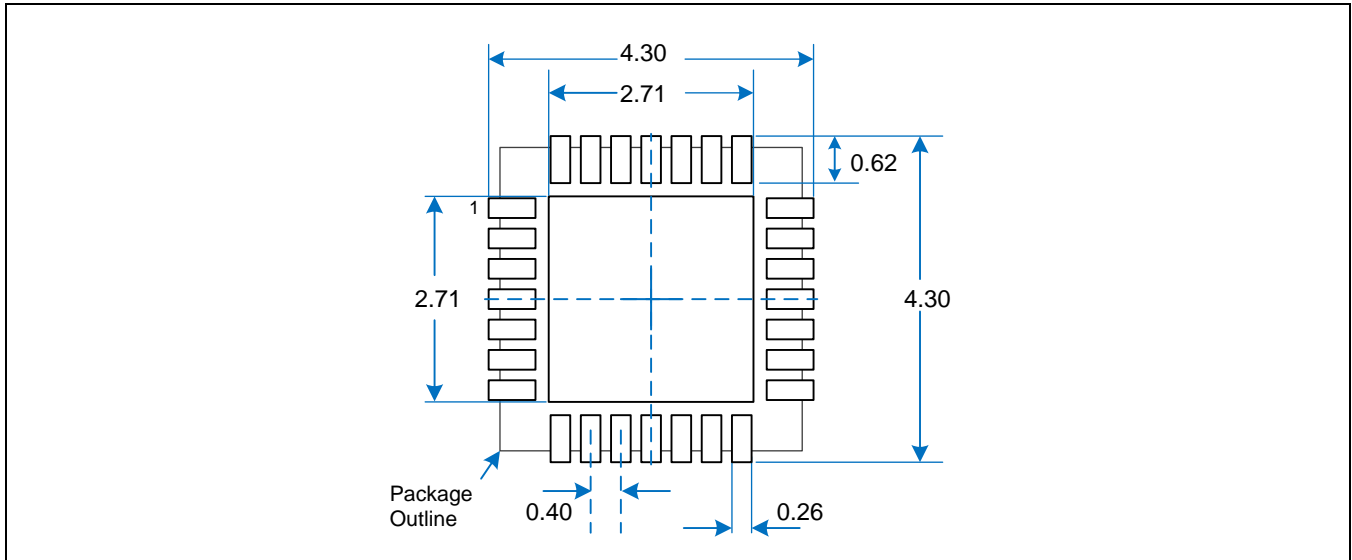
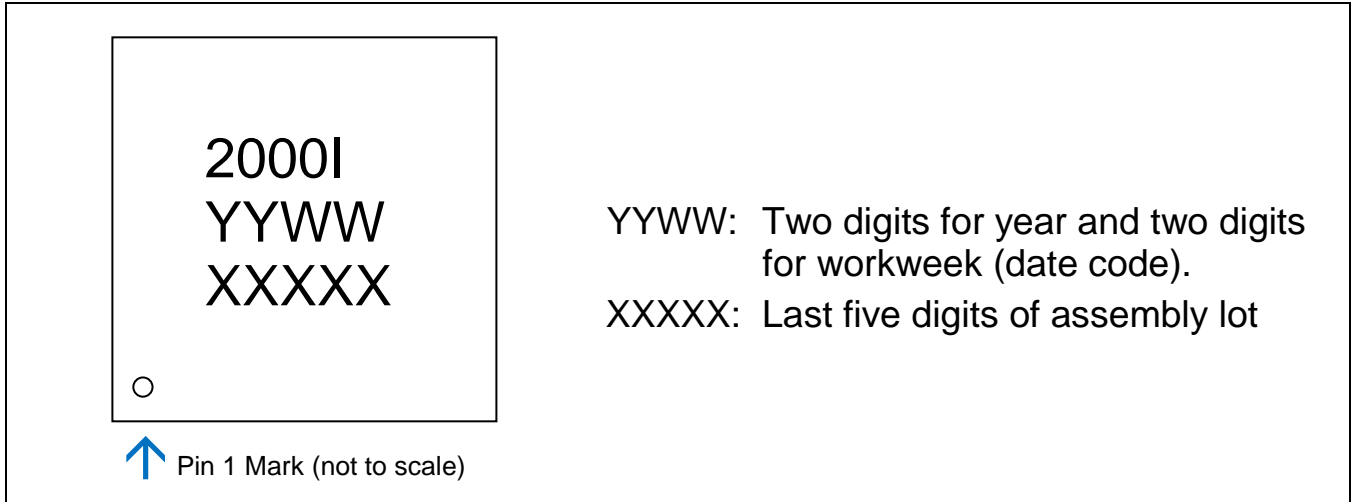


Figure 7.3 Top Marking Diagram



8 Ordering Information

Note: This product is sold under a limited license from PowerOne, Inc. related to digital power technology as set forth in U.S. Patent 7000125 and other related patents owned by PowerOne, Inc. This license does not extend to standalone power supply products.

| Product Sales Code | Description | Package |
|--------------------|---|---------|
| ZSPM2000ZI2R 1 | ZSPM2000 Lead-free QFN28 — Temperature range: -40°C to +85°C | Reel |
| ZSPM2000-KIT01 | Evaluation Kit for ZSPM2000 with PMBus™ Communication Interface — the Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM2000 (login required; see data sheet section 9 for details) | Kit |

9 Related Documents

| Document |
|---|
| ZSPM2000 Feature Sheet |
| ZSPM1000/ZSPM2000 Pink Power Designer™ Graphic User Interface (GUI) * |
| ZSPM100x/ZSPM200x Application Note—Programming and Calibration * |
| ZSPM2000-KIT01 Kit Description * |

Visit the ZSPM2000 product page www.IDT.com/ZSPM2000 or contact your nearest sales office for the latest version of these documents.

Note: Documents marked with an asterisk (*) require a free customer login account.

10 Glossary

| Term | Description |
|-------|--|
| ASIC | Application Specific Integrated Circuit |
| DCR | Equivalent DC Resistance |
| DPWM | Digital Pulse-Width Modulator |
| DSP | Digital Signal Processing |
| FPGA | Field-Programmable Gate Array |
| GPIO | General Purpose Input/Output |
| GUI | Graphical User Interface |
| HKADC | Housekeeping Analog-To-Digital Converter |
| NVM | Non-volatile Memory |
| OT | Over-Temperature |
| OTP | One-Time Programmable Memory |

| Term | Description |
|------|----------------------------------|
| OV | Over-Voltage |
| PEC | Packet Error Correction |
| PID | Proportional/Integral/Derivative |
| POL | Point-of-Load |
| SCL | Serial Clock |
| SCR | Sub-cycle Response™ |
| SDA | Serial Data |
| SLC | State-Law Control™ |
| SPM | Smart Power Management |

11 Document Revision History

| Revision | Date | Description |
|----------|-------------------|---|
| 1.00 | November 16, 2014 | First release. |
| 1.01 | March 4, 2015 | Correction for hyperlink to product page web address. Update for Korean address and sales e-mail address in contact information. |
| | January 27, 2016 | Changed to IDT branding. |



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