



BUK9640-100A

N-channel TrenchMOS logic level FET

13 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

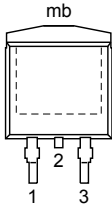
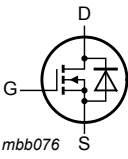
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2 ; Fig. 3		-	-	39	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	158	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C		-	-	43	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C		-	29	39	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11 ; Fig. 12		-	34	40	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 80 V; T _j = 25 °C; Fig. 13		-	20	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 39\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	-	182	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9640-100A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9640-100A	BUK9640-100A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-15	15	V

Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	158	W
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; Fig. 2; Fig. 3		-	39	A
		T _{mb} = 100 °C; V _{GS} = 5 V; Fig. 2		-	28	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Fig. 3		-	159	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	39	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	159	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 39 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped		-	182	mJ

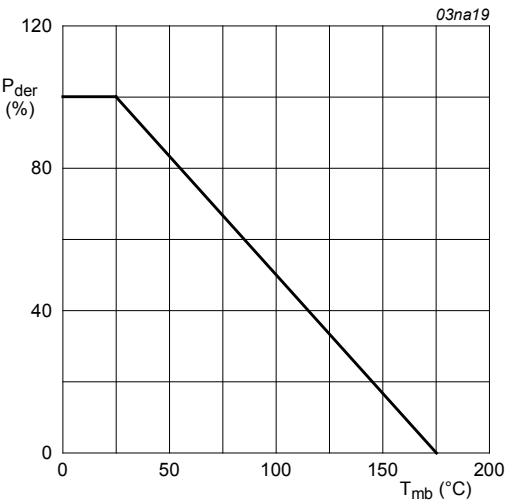


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

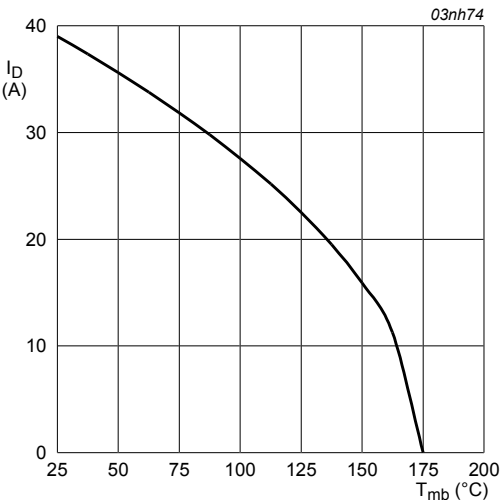


Fig. 2. Normalized continuous drain current as a function of mounting base temperature

T_{amb} = 25°C; I_{DM} is single pulse

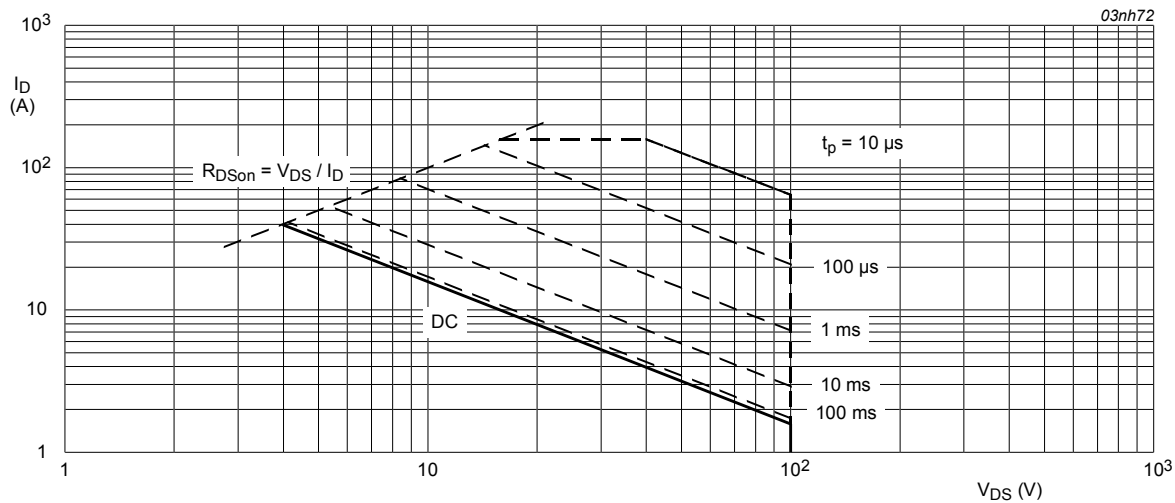


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{amb} = 25^{\circ}C$; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W

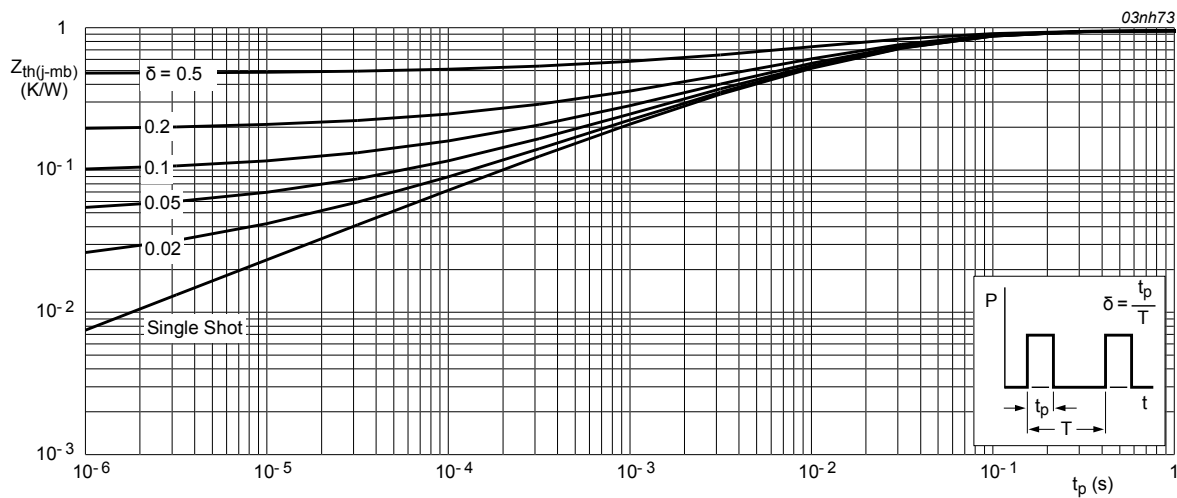


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C		100	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C		89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 10		1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10		-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C		-	0.05	10	µA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C		-	-	43	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 11 ; Fig. 12		-	-	100	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C		-	29	39	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11 ; Fig. 12		-	34	40	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 80 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 13		-	48	-	nC
Q _{GS}	gate-source charge			-	5.4	-	nC
Q _{GD}	gate-drain charge			-	20	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 14		-	2304	3072	pF
C _{oss}	output capacitance			-	222	266	pF
C _{rss}	reverse transfer capacitance			-	151	207	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C		-	20	-	ns
t _r	rise time			-	135	-	ns
t _{d(off)}	turn-off delay time			-	125	-	ns
t _f	fall time			-	90	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die; T _j = 25 °C		-	2.5	-	nH

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		from drain lead 6 mm from package to centre of die; $T_j = 25\text{ }^{\circ}\text{C}$		-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ }^{\circ}\text{C}$		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 37\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;		-	60	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	240	-	nC

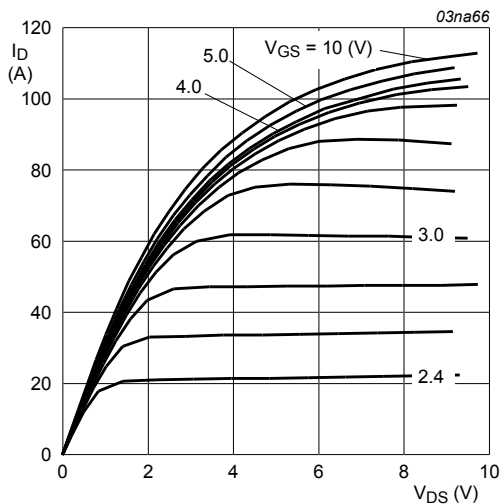


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$; $t_p = 300\mu\text{s}$

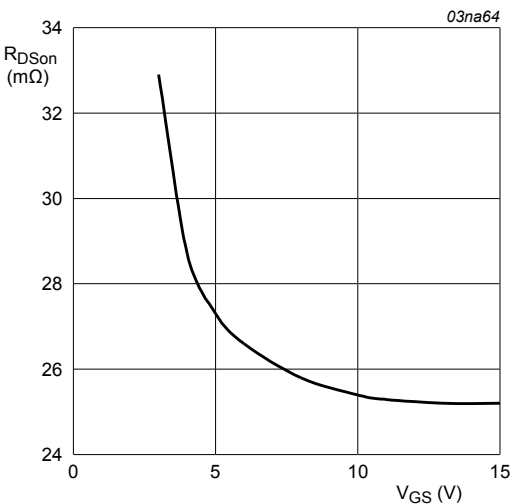
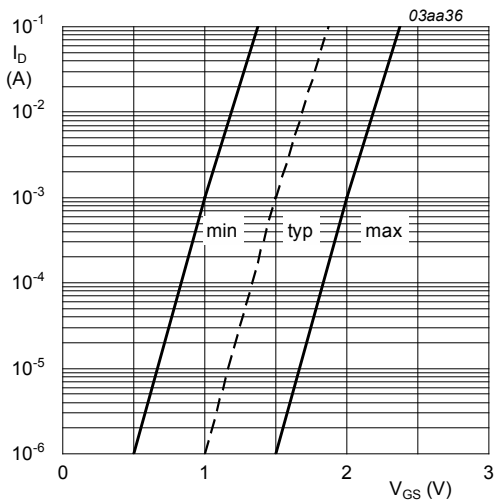


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$



$T_J = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

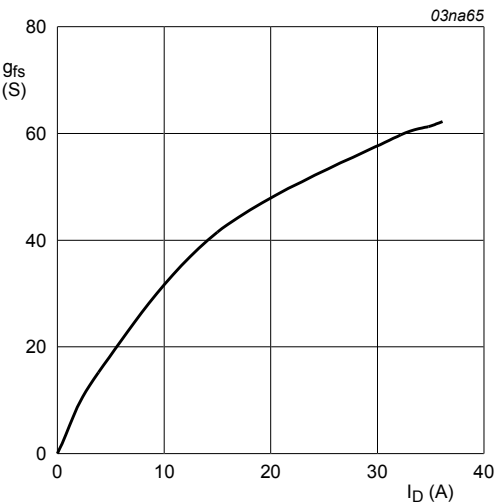


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25\text{ }^{\circ}\text{C}; V_{DS} = 25\text{ V}$

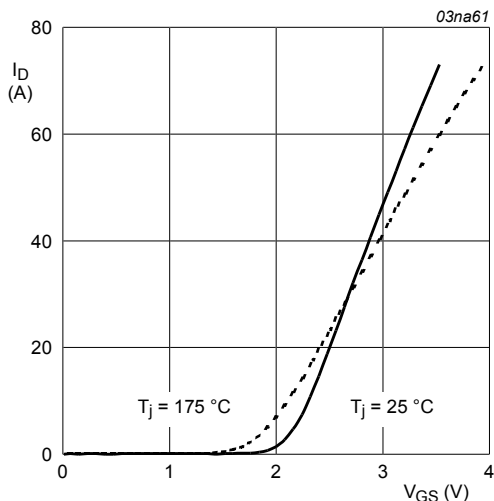


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25\text{ V}$

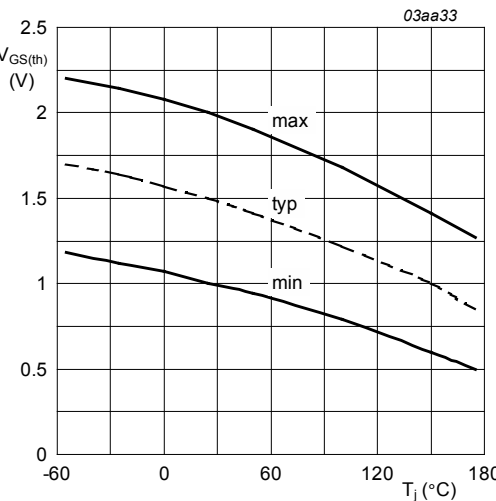


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

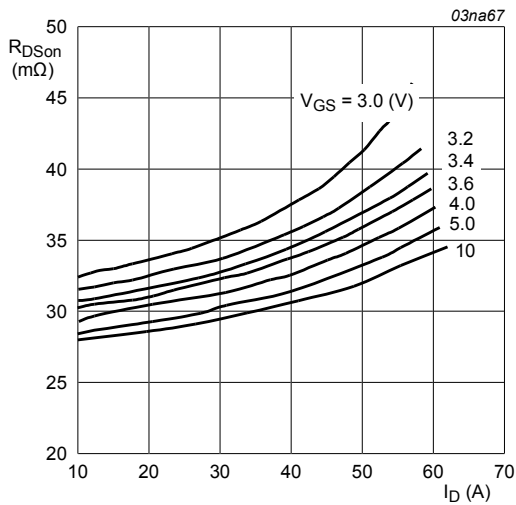


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}\text{C}$$

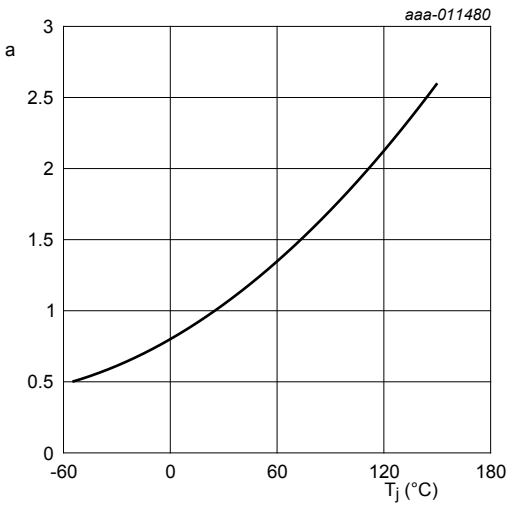


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

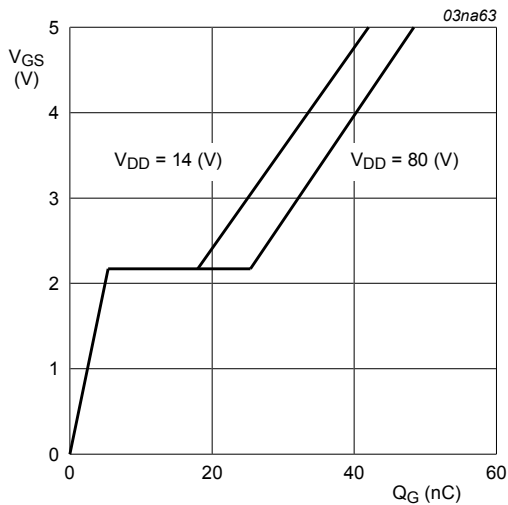


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$$

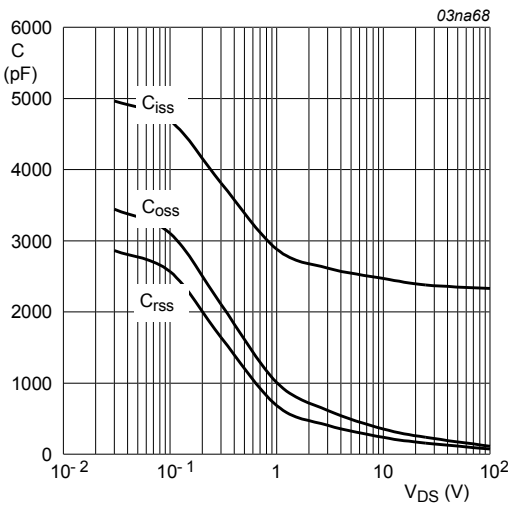


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

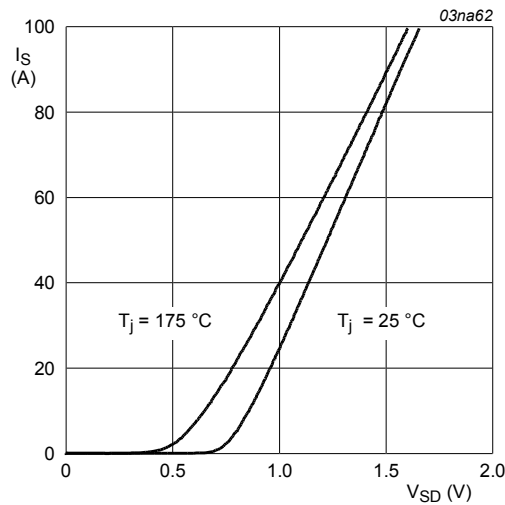


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

11. Package outline



Fig. 16. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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