

SCOPE: MICROPROCESSOR SUPERVISORY CIRCUITS

<u>Device Type</u>	<u>Generic Number</u>
01	MAX690(x)/883B
02	MAX691(x)/883B
03	MAX692(x)/883B
04	MAX693(x)/883B
05	MAX694(x)/883B
06	MAX695(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM SMD			
JA	P	GDIP1-T08 or CDIP2-T08	8 LEAD CERDIP
JE	E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP
FB	X	CDFP3-F10	10 LEAD Flatpack
LP	2	CQCC1-N20	20 Pin Leadless Chip

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)

V _{CC}	-0.3V to +6.0V
V _{BATT}	-0.3V to +6.0V
All other Inputs <u>I</u> /	-0.3V to (V _{OUT} +0.5V)

Input Current

V _{CC}	200mA
V _{BATT}	50mA
GND	20mA

Output Current

V _{OUT}	Short-circuit protected
All other outputs	20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/μs

Lead Temperature (soldering, 10 seconds) +300°C

Storage Temperature -65°C to +160°C

Continuous Power Dissipation T_A=+70°C

8 lead CERDIP(derate 8.0mW/°C above +70°C) 640mW

16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW

10 lead Flatpack(derate 5.3mW/°C above +70°C) 421mW

20 lead LCC(derate 9.1mW/°C above +70°C) 727mW

Junction Temperature T_J +150°C

Thermal Resistance, Junction to Case, Θ_{JC}:

Case Outline 8 lead CERDIP.....	55°C/W
Case Outline 16 lead CERDIP.....	50°C/W
Case Outline 10 lead Flatpack	85°C/W
Case Outline 20 leadless Chip carrier	20°C/W

Thermal Resistance, Junction to Ambient, Θ_{JA}:

Case Outline 8 lead CERDIP.....	125°C/W
Case Outline 16 lead CERDIP.....	100°C/W
Case Outline 10 lead Flatpack	190°C/W
Case Outline 20 leadless Chip carrier	110°C/W

NOTE 1: The input voltage limits on PFI and WDI may be exceeded if the input current is less than 10mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
Supply Voltage Range (V_{CC}) DASH 03 & 04	+4.5V to +5.5V
Supply Voltage Range (V_{CC}) DASH 01, 02, 05, 06	+4.75V to +5.5V

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125°C 2/ Unless otherwise specified						
BATTERY-BACKUP SWITCHING								
Operating Voltage Range	V _{CC}		1,2,3	01,02,05,06	4.75	5.5	V	
					03,04	4.5		5.5
Operating Voltage Range	V _{BATT}		1,2,3	01,02,05,06	2.0	4.25	V	
					03,04	2.0		4.0
Output Voltage	V _{OUT}	I _{OUT} =1mA	1,2,3	All	V _{CC} -0.3		V	
		I _{OUT} =50mA			V _{CC} -0.5			
Output Voltage-Battery-Backup Mode	BATT _{OUT}	I _{OUT} =250μA, V _{CC} <V _{BATT} -0.2V	1,2,3	All	VBATT-0.1		V	
Supply Current (Excludes I _{OUT})	I _{CC}	I _{OUT} =1mA	1 2,3	All		5 7	mA	
		I _{OUT} =50mA	1 2,3		10 15			
Supply Current in Battery-Backup Mode	I _{BATT}	V _{CC} =0V, V _{BATT} =2.8V	1 2,3	All		1 10	μA	
Battery Standby Current	BATT SBI	5.5V>V _{CC} >V _{BATT} +1V +=Discharge, -=Charge	1 2,3	All	-0.10 -1.00	+0.02 +0.02	μA	
Battery-Switchover, Threshold, V _{CC} to V _{BATT}	BATT SW _{TH}	Power-Up or Power-Down	1,2,3	All	-200	+200	mV	
BATT ON Output Voltage	BATT ON _{OUT}	I _{SINK} =3.2mA	1,2,3	02,04,06		0.4	V	
BATT ON Output Short-Circuit Current	BATT ON _{IOS}	BATT ON = V _{OUT} BATT ON =0V Source Current	1,2,3	02,04,06		60	mA	
					0.1	25		μA
RESET AND WATCHDOG TIMING								
Reset Voltage Threshold	R _{TH}		1,2,3	01,02,05,06	4.5	4.75	V	
				03,04	4.25	4.5		
Reset Threshold Hysteresis	RT _{HH}		1,2,3	All		250	mV	
Reset Timeout Delay	R _{DEL}	OSC SEL High, V _{CC} =5V	9 10,11	01,02 03,04	35 31	70 78	ms	
			9 10,11	05,06	140 126	280 310		

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125 °C 2/ Unless otherwise specified						
Watchdog Timeout Period, Internal Oscillator	WD _{INT}	Long Period, V _{CC} =5V		9 10,11	All	1.00 0.90	2.25 2.42	sec
		Short Period, V _{CC} =5V		9 10,11		70 62	140 154	ms
Watchdog Timeout Period, External Clock	WD _{EXT}	Long Period		9 10,11	02,04,06	3840	4097	Clock Cycles
		Short Period		9 10,11	02,04,06	768	1025	
Minimum WDI Input Pulse Width	WDI _{PW}	V _{IL} =0.4V, V _{IH} =V _{CC} (0.8)		9 10,11	All	200 300		ns
RESET Output Voltage High	R _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
RESET Output Voltage Low	R _{VOL}	I _{SINK} =1.6mA, V _{CC} =4.25V		1	All		0.4	V
		I _{SINK} =800μA, V _{CC} =4.25V		2,3			0.4	
LOWLINE Output Voltage High	LL _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	02,04,06	3.5		V
LOWLINE Output Voltage Low	LL _{VOL}	I _{SINK} =1.6mA, V _{CC} =4.25V		1	02,04,06		0.4	V
		I _{SINK} =800μA, V _{CC} =4.25V		2,3			0.4	
WDO Output Voltage High	WDO _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
WDO Output Voltage Low	WDO _{VOL}	I _{SINK} =1.6mA, V _{CC} =4.25V		1	02,04,06		0.4	V
		I _{SINK} =800μA, V _{CC} =4.25V		2,3			0.4	
Reset Output Voltage High	R _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	02,04,06	3.5		V
Reset Output Voltage Low	R _{VOL}	I _{SINK} =1.6mA		1	02,04,06		0.4	V
		I _{SINK} =800μA		2,3			0.4	
Output Short-Circuit Current	I _{OS}	RESET=0V		1,2,3	All	1	25	μA
		RESET, RESET, WDO, LL			02,04,06	1	25	
WDI Input Threshold Logic Low	WDI _{VIL}	V _{CC} =5V NOTE 3		1 2,3	All		0.8 0.4	V
WDI Input Threshold Logic High	WDI _{VIH}	V _{CC} =5V NOTE 3		1 2,3	All	3.5 4.0		V
WDI Input Current	WDI _{IN}	WDI=V _{OUT}		1 2,3	All		50 80	μA
		WDI=0V		1 2,3		-50 -80		

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125 °C 2/ Unless otherwise specified						
POWER-FAIL DETECTOR								
PFI Input Threshold	PFI _{VTH}	V _{CC} =5V		1,2,3	All	1.2	1.4	V
PFI Input Current	PFI _{IN}			1,2,3	All	-25	25	nA
PFO Output Voltage High	PFO _{VOH}	I _{SOURCE} =1μA, V _{CC} =5V		1,2,3	All	3.5		V
PFO Output Voltage Low	PFO _{VOL}	I _{SINK} =3.2mA		1	All		0.4	V
		I _{SINK} =1.6mA		2,3		0.4		
PFO Short-Circuit Source Current	PFO _{IOS}	PFI=V _{IH} , PFO=0V		1,2,3	All	1.0	25	μA
CHIP-ENABLE GATING								
CE IN Thresholds Logic Low	CE _{VIL}			1	02,04,06		0.8	V
				2,3		0.4		
CE IN Thresholds Logic High	CE _{VIH}			1	02,04,06	3.0		V
				2,3		4.0		
CE IN Pull-Up Current	CE _{INPI}			1,2,3	02,04,06	1.0	25	μA
CE OUT Output Voltage High	CE _{VOH}	I _{SOURCE} =3.0mA, V _{CC} =4.75V		1,2,3	02,04,06	V _{OUT} -1.5		V
		I _{SOURCE} =1μA, V _{CC} =0V				V _{OUT} -0.05		
CE Output Voltage Low	CE _{VOL}	I _{SINK} =3.2mA		1	02,04,06		0.4	V
		I _{SINK} =1.6mA		2,3		0.4		
CE Propagation Delay	t _{PDCE}	V _{CC} =5V		9	02,04,06		200	ns
				10,11		300		
OSCILLATOR								
OSC IN Input Current Pull-Up	OSCI _{IN}			1,2,3	02,04,06		25	μA
OSC SEL Input Pull-Up Current	OSC _{SELIN}			1,2,3	02,04,06	1	25	μA
OSC IN Frequency Range	OSC _{INfrq}	OSC SEL=0V		9,10,11	02,04,06	0	250	kHz
OSC IN Frequency with External Capacitor	OSC _{IN}	OSC SEL=0V, COSC=47pF NOTE 4		9	02,04,06	4		kHz

NOTE 2: V_{CC}=full operating range, V_{BATT}=+2.8V.

NOTE 3: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125kΩ

NOTE 4: Typical for design purposes only but not tested. Guaranteed for SMD 5962-90711 and 5962-90712.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	8 pin CERDIP	MAX690MJA/883B	5962-9071201MPA
01	10 pin Flatpack	MAX690MFB/883B	5962-9071201MXC
01	20 pin LCC	MAX690MLP/883B	5962-9071201M2C
02	8 pin CERDIP	MAX691MJA/883B	5962-9071101MPA
02	20 pin LCC	MAX691MLP/883B	5962-9071101M2C
03	8 pin CERDIP	MAX692MJA/883B	5962-9071202MPA
03	10 pin Flatpack	MAX692MFB/883B	5962-9071202MXC
03	20 pin LCC	MAX692MLP/883B	5962-9071202M2C
04	8 pin CERDIP	MAX693MJA/883B	5962-9071102MPA
04	20 pin LCC	MAX693MLP/883B	5962-9071102M2C
05	8 pin CERDIP	MAX694MJA/883B	5962-9071203MPA
05	10 pin Flatpack	MAX694MFB/883B	5962-9071203MXC
05	20 pin LCC	MAX694MLP/883B	5962-9071203M2C
06	8 pin CERDIP	MAX695MJA/883B	5962-9071103MPA

TERMINAL CONNECTIONS:

	MAX690/692/694	MAX690/692/694	MAX690/692/694	MAX691/693/695	MAX691/693
	J8	F10	L20	J16	L20
1	V _{OUT}	V _{OUT}	NC	V _{BATT}	NC
2	V _{CC}	V _{CC}	V _{BATT}	V _{OUT}	V _{BATT}
3	GND	GND	V _{OUT}	V _{CC}	V _{OUT}
4	PFI	NC	V _{CC}	GND	V _{CC}
5	_____	PFI	GND	BATT ON	GND
	PFO				
6	WDI	_____	NC	_____	NC
		PFO		LOWLINE	
7	_____	WDI	NC	OSC IN	BATT ON
	RESET				
8	V _{BATT}	NC	NC	OSC SEL	_____
					LOWLINE
9		_____	NC	PFI	OSC IN
		RESET			OSC SEL
10		V _{BATT}	NC	_____	
				PFO	
11			NC	WDI	NC
12			PFI	_____	PFI
				CE OUT	
13			_____	_____	_____
			PFO	CE IN	PFO
14			WDI	_____	WDI
				WDO	
15			NC	_____	_____
				RESET	CE OUT
16			NC	RESET	NC
17			NC		_____
					CE IN
18			NC		_____
					WDO
19			_____		_____
			RESET		RESET
20			NC		RESET

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.