

***μ*IPM™-DIP**

6.0Ω, 500V

Integrated Power Module for Small Appliance Motor Drive Applications

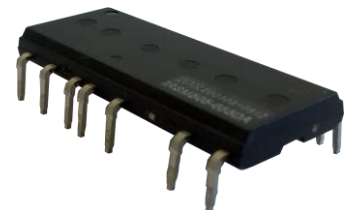
Description

IRSM505-015 and IRSM515-015 are 3-phase Integrated Power Modules (IPM) designed for advanced appliance motor drive applications such as energy efficient fans and pumps. These advanced IPMs offers a combination of low $R_{DS(on)}$ Trench FREDFET technology and the industry benchmark half-bridge high voltage, rugged driver in a familiar package. The modules are optimized for low EMI characteristics.

IRSM505-015 includes temperature feedback while IRSM515-015 does not.

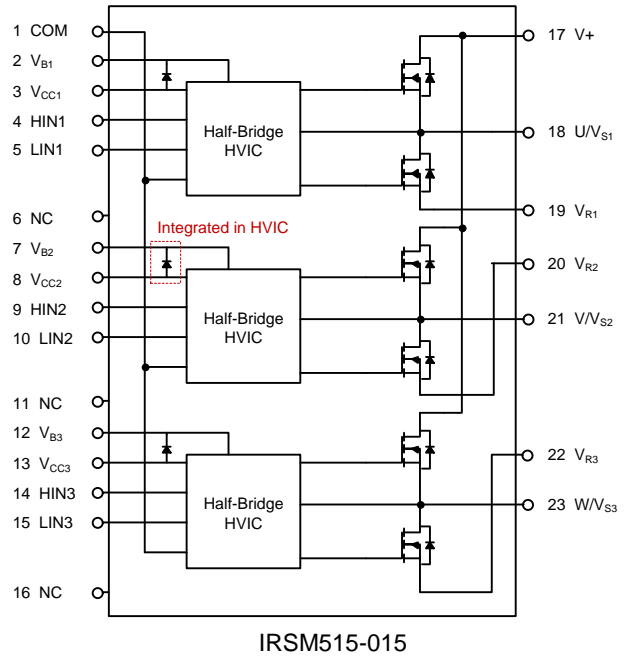
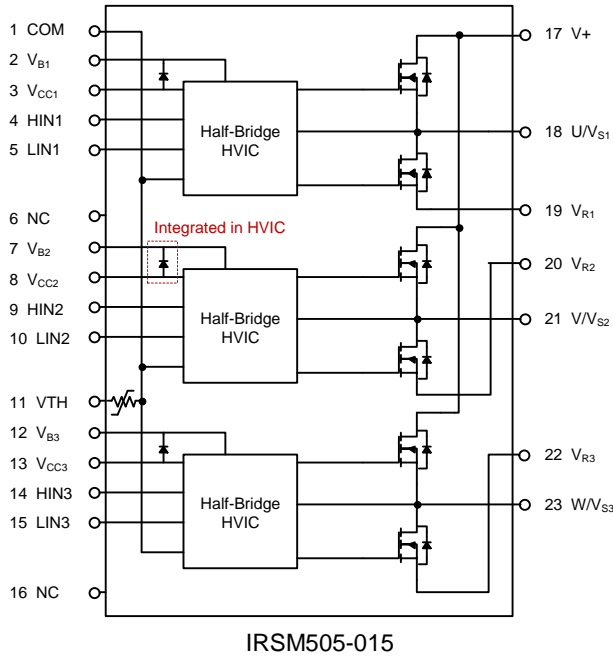
Features

- 500V 3-phase inverter including high voltage gate drivers
- Integrated bootstrap functionality
- Low 6.0Ω (max, 25°C) $R_{DS(on)}$ Trench FREDFET
- Under-voltage lockout for all channels
- Matched propagation delay for all channels
- Temperature feedback via NTC (IRSM505-015 only)
- Optimized dV/dt for loss and EMI trade offs
- Open-source for single and leg-shunt current sensing
- 3.3V logic compatible with advanced input filter
- Driver tolerant to negative transient voltage (-Vs)
- Isolation 1900V_{RMS}, 1min
- RoHS Compliant
- Certified by UL - File Number E252584



| Base Part Number | NTC | Package Type | Standard Pack | | Orderable Part Number |
|------------------|-----|--------------|---------------|----------|-----------------------|
| | | | Form | Quantity | |
| IRSM505-015 | Yes | SOP23 | Tube | 240 | IRSM505-015PA |
| | | DIP23 | Tube | 240 | IRSM505-015DA |
| | | DIP23A | Tube | 240 | IRSM505-015DA2 |
| IRSM515-015 | No | SOP23 | Tube | 240 | IRSM515-015PA |
| | | DIP23 | Tube | 240 | IRSM515-015DA |
| | | DIP23A | Tube | 240 | IRSM515-015DA2 |

Internal Electrical Schematic



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table.

| Symbol | Description | Min | Max | Unit |
|---------------------------|---|-------------------|--------------------|------------|
| BV_{DSS} | MOSFET Blocking Voltage | --- | 500 | V |
| $I_o @ T_C=25^\circ C$ | DC Output Current per MOSFET | --- | 1.2 | A |
| $I_{OP} @ T_C=25^\circ C$ | Pulsed Output Current per MOSFET (Note 1) | --- | 9 | |
| $P_d @ T_C=25^\circ C$ | Maximum Power Dissipation per MOSFET | --- | 18 | W |
| V_{ISO} | Isolation Voltage (1min) | --- | 1900 | V_{RMS} |
| T_J | Operating Junction Temperature | -40 | 150 | $^\circ C$ |
| T_C | Operating Case Temperature | -40 | 150 | $^\circ C$ |
| T_S | Storage Temperature | -40 | 150 | $^\circ C$ |
| $V_{S1,2,3}$ | High Side Floating Supply Offset Voltage | $V_{B1,2,3} - 20$ | $V_{B1,2,3} + 0.3$ | V |
| $V_{B1,2,3}$ | High Side Floating Supply Voltage | -0.3 | 525 | V |
| V_{CC} | Low Side and Logic Supply voltage | -0.3 | 25 | V |
| V_{IN} | Input Voltage of LIN, HIN | COM -0.3 | $V_{CC} + 0.3$ | V |

Note 1: Pulse Width = 100 μ s, Single Pulse

Recommended Operating Conditions

| Symbol | Description | Min | Max | Unit |
|---------------------|--|--------------------|--------------------|------|
| V+ | Positive DC Bus Input Voltage | --- | 400 | V |
| V _{S1,2,3} | High Side Floating Supply Offset Voltage | (Note 2) | 400 | V |
| V _{B1,2,3} | High Side Floating Supply Voltage | V _S +12 | V _S +20 | V |
| V _{CC} | Low Side and Logic Supply Voltage | 13.5 | 16.5 | V |
| V _{IN} | Input Voltage of LIN, HIN, I _{TRIP} , EN, FLT | 0 | 5 | V |
| F _p | PWM Carrier Frequency | --- | 20 | kHz |

Note 2: Logic operational for V_s from COM-8V to COM+500V. Logic state held for V_s from COM-8V to COM-V_{BS}.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_C = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to all six channels. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

| Symbol | Description | Min | Typ | Max | Units | Conditions |
|--|--|-----|------|-----|-------|--|
| BV _{DSS} | Drain-to-Source Breakdown Voltage | 500 | --- | --- | V | T _J =25°C, I _{LK} =250μA |
| I _{LKH} | Leakage Current of High Side FET | | 12 | | μA | T _J =25°C, V _{DS} =500V |
| I _{LKL} | Leakage Current of Low Side FET Plus Gate Drive IC | | 14 | | μA | T _J =25°C, V _{DS} =500V |
| R _{DS(on)} | Drain to Source ON Resistance | --- | 5.0 | 6.0 | Ω | T _J =25°C, V _{CC} =15V, I _d =0.5A |
| | | --- | 12.3 | --- | Ω | T _J =150°C, V _{CC} =15V, I _d =0.5A (Note 3) |
| V _{SD} | Mosfet Body Diode Forward Voltage | --- | 0.8 | --- | V | T _J =25°C, V _{CC} =15V, I _D =0.5A |
| V _{IN,th+} | Positive Going Input Threshold | 2.2 | --- | --- | V | |
| V _{IN,th-} | Negative Going Input Threshold | --- | --- | 0.8 | V | |
| V _{CCUV+} , V _{BSUV+} | V _{CC} and V _{BS} Supply Under-Voltage, Positive Going Threshold | 8 | 8.9 | 9.8 | V | |
| V _{CCUV-} , V _{BSUV-} | V _{CC} and V _{BS} supply Under-Voltage, Negative Going Threshold | 6.9 | 7.7 | 8.5 | V | |
| V _{CCUVH} , V _{BSUVH} | V _{CC} and V _{BS} Supply Under-Voltage Lock-Out Hysteresis | --- | 1.2 | --- | V | |
| I _{QBS} | Quiescent V _{BS} Supply Current V _{IN} =0V | --- | 42 | 60 | μA | |
| I _{QBS, ON} | Quiescent V _{BS} Supply Current V _{IN} =4V | --- | 42 | 60 | μA | |
| I _{QCC} | Quiescent V _{CC} Supply Current V _{IN} =0V | --- | 1.7 | 4 | mA | |
| I _{QCC, ON} | Quiescent V _{CC} Supply Current V _{IN} =4V | --- | 1.8 | 4 | mA | |
| I _{IN+} | Input Bias Current V _{IN} =4V | --- | 5.9 | 18 | μA | V _{IN} =3.3V |
| I _{IN-} | Input Bias Current V _{IN} =0V | --- | --- | 2 | μA | V _{IN} =0V |
| R _{BR} | Internal Bootstrap Equivalent Resistor Value | --- | 250 | --- | Ω | T _J =25°C |

Note 3: Characterized, not tested at manufacturing

Dynamic Electrical Characteristics

$(V_{CC-COM}) = (V_B - V_S) = 15\text{ V}$. $T_C = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Description | Min | Typ | Max | Units | Conditions |
|---------------|---|-----|-----|-----|---------------|---|
| T_{ON} | Input to Output Propagation Turn-On Delay Time | --- | 0.7 | 1.5 | μs | $I_D=120\text{mA}$, $V_+=30\text{V}$ See Fig.1 |
| T_{OFF} | Input to Output Propagation Turn-Off Delay Time | --- | 0.9 | 1.5 | μs | |
| $T_{FIL,IN}$ | Input Filter Time (HIN, LIN) | 200 | 300 | --- | ns | $V_{IN}=0$ & $V_{IN}=3.3\text{V}$ |
| DT | Deadtime Inserted | --- | 400 | --- | ns | $V_{IN}=0$ & $V_{IN}=3.3\text{V}$ without external deadtime |
| E_{ON} | Turn-on switching energy loss | --- | 17 | --- | μJ | $V_i=320\text{V}$, $I_D=0.3\text{A}$, $L=40\text{mH}$, $T_C=25^\circ\text{C}$ (Note 4) |
| E_{OFF} | Turn-off switching energy loss | --- | 3 | --- | μJ | |
| E_{REC} | Recovery energy loss | --- | 4 | --- | μJ | |
| $E_{ON,150}$ | Turn-on switching energy loss | --- | 30 | --- | μJ | $V_i=320\text{V}$, $I_D=0.3\text{A}$, $L=40\text{mH}$, $T_C=150^\circ\text{C}$ (Note 4) |
| $E_{OFF,150}$ | Turn-off switching energy loss | --- | 4 | --- | μJ | |
| $E_{REC,150}$ | Recovery energy loss | --- | 9 | --- | μJ | |

Note 4: Characterized, not tested at manufacturing

Thermal and Mechanical Characteristics

| Symbol | Description | Min | Typ | Max | Units | Conditions |
|---------------|-------------------------------------|-----|-----|-----|--------------------|-----------------------------------|
| $R_{th(J-C)}$ | Junction to Case Thermal Resistance | --- | 7.4 | --- | $^\circ\text{C/W}$ | High Side V-Phase Mosfet (Note 5) |

Note 5: Characterized, not tested at manufacturing. Case temperature (T_C) point shown in Figure 2.

Internal NTC – Thermistor Characteristics (IRSM505-015 Only)

| Symbol | Description | Min | Typ | Max | Units | Conditions |
|-------------------|--------------------------------------|-----|------|-----|------------------|--|
| R_{25} | Resistance | --- | 47 | --- | $\text{k}\Omega$ | $T_C=25^\circ\text{C}$, $\pm 5\%$ tolerance |
| R_{125} | Resistance | --- | 1.41 | --- | $\text{k}\Omega$ | $T_C=125^\circ\text{C}$ |
| B | B-constant (25-50 $^\circ\text{C}$) | --- | 4050 | --- | K | $\pm 2\%$ tolerance (Note 6) |
| Temperature Range | | -40 | --- | 125 | $^\circ\text{C}$ | |

Note 6: See application notes for usage

Qualification Information†

| | | |
|-----------------------------------|-------------------------|---------------------------|
| Qualification Level | | Industrial ^{††} |
| Moisture Sensitivity Level | | MSL3 ^{†††} |
| RoHS Compliant | | Yes |
| UL Certified | | Yes – File Number E252584 |
| ESD | Machine Model | Class B |
| | Human Body Model | Class 2 |

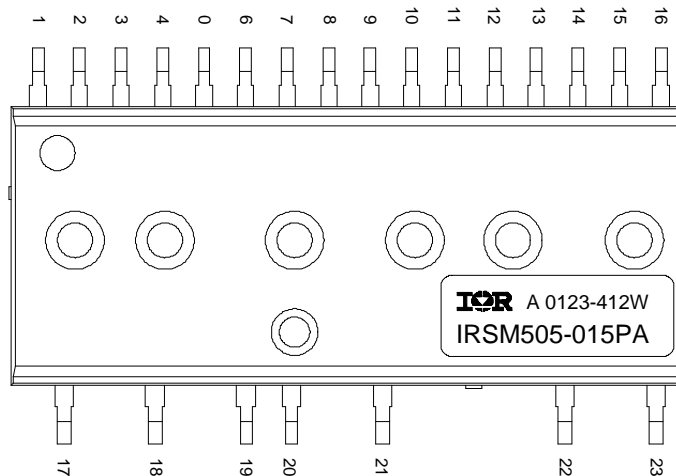
† Qualification standards can be found at International Rectifier’s web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† SOP23 package only. Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Module Pin-Out Description

| Pin | Name | Description |
|-----|-------------------|--|
| 1 | COM | Logic Ground |
| 2 | V _{B1} | High Side Floating Supply Voltage 1 |
| 3 | V _{CC1} | 15V Supply 1 |
| 4 | HIN1 | Logic Input for High Side Gate Driver - Phase 1 |
| 5 | LIN1 | Logic Input for Low Side Gate Driver - Phase 1 |
| 6 | NC | Not Connected |
| 7 | V _{B2} | High Side Floating Supply Voltage 2 |
| 8 | V _{CC2} | 15V Supply 2 |
| 9 | HIN2 | Logic Input for High Side Gate Driver - Phase 2 |
| 10 | LIN2 | Logic Input for Low Side Gate Driver - Phase 2 |
| 11 | V _{TH} | Thermistor Output (IRSM505-015DA) |
| | NC | Not Connected (IRSM515-015DA) |
| 12 | V _{B3} | High Side Floating Supply Voltage 3 |
| 13 | V _{CC3} | 15V Supply 3 |
| 14 | HIN3 | Logic Input for High Side Gate Driver - Phase 3 |
| 15 | LIN3 | Logic Input for Low Side Gate Driver - Phase 3 |
| 16 | NC | Not Connected |
| 17 | V+ | DC Bus Voltage Positive |
| 18 | U/V _{S1} | Output - Phase 1, High Side Floating Supply Offset 1 |
| 19 | V _{R1} | Phase 1 Low Side Source |
| 20 | V _{R2} | Phase 2 Low Side Source |
| 21 | V/V _{S2} | Output - Phase 2, High Side Floating Supply Offset 2 |
| 22 | V _{R3} | Phase 3 Low Side Source |
| 23 | W/V _{S3} | Output - Phase 3, High Side Floating Supply Offset 2 |



Referenced Figures



Figure 1a: Input to Output propagation turn-on delay time.



Figure 1b: Input to Output propagation turn-off delay time.

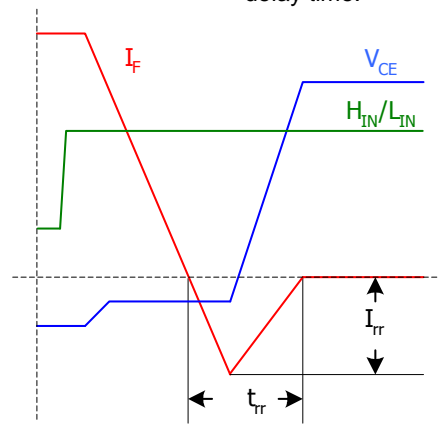
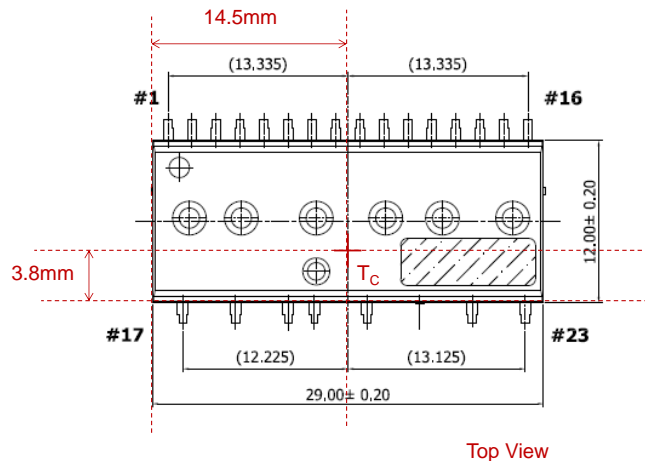


Figure 1c: Diode Reverse Recovery.

Figure 1: Switching Parameter Definitions



Top View

Figure 2: T_C measurement point for $R_{th(j-c)}$

Application Notes

A basic application schematic is shown below.

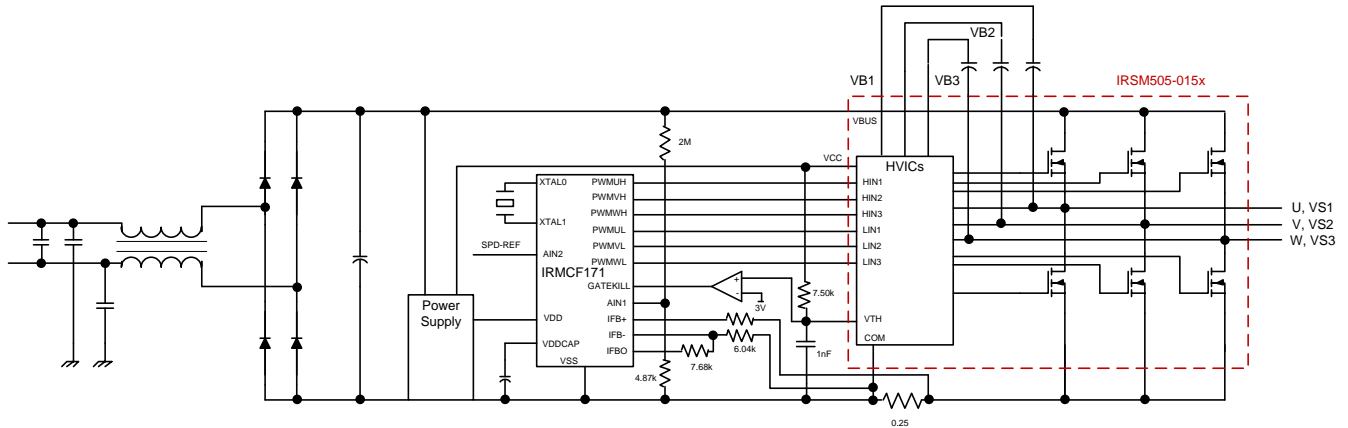


Figure 3: Basic sensor-less motor drive circuit connection. Motor is connected to U, V, W

A complete reference design board for running any permanent magnet motor via sensorless sinusoidal control is available. The board – photo below – features the μ IPM™-DIP module and the iMotion™ digital control IC. Reference design kits are available on the [International Rectifier website](http://www.irf.com) (irf.com > Design Resources > Reference Designs > Intelligent Power Modules)



Figure 4: Reference design board featuring the μ IPM™-DIP module and the iMotion™ IRMCF171 digital control IC

Figures 5-7 show the typical current capability for this module at specified conditions. In all tests, the application board – the IRMCS1071-1-D reference board – was placed in a box to prevent cooling from ambient airflow. Figure 5 is derived from using a heat sink that maintains T_C at 125°C. Figures 6-7 represent current capability for the module as used without any heat sink. ΔT_{JA} represents the difference in temperature between the junction of the high-side V-phase Mosfet and the ambient, measured 10cm above and 6cm away from the board. Ambient temperature kept within 28-29°C.

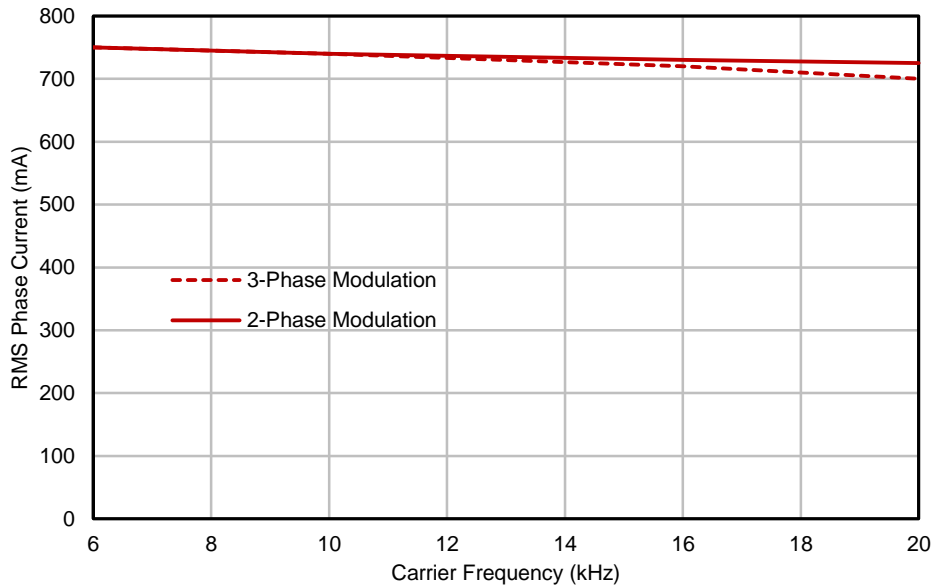


Figure 5: Maximum sinusoidal phase current vs PWM switching frequency with a heat sink. Space Vector Modulation, $V_+ = 320V$, $T_A = 28^\circ C$, $T_J = 150^\circ C$, $T_C = 125^\circ C$

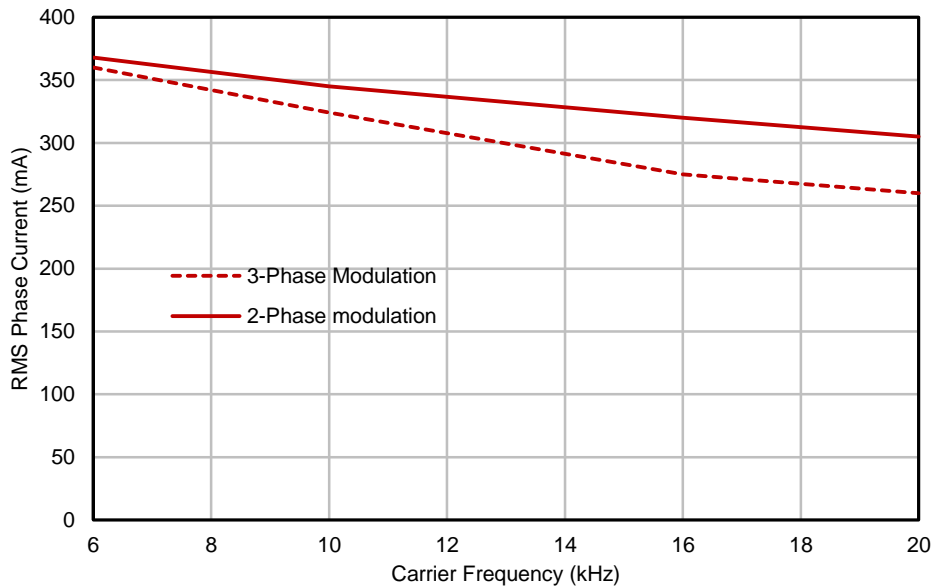


Figure 6: Maximum sinusoidal phase current vs PWM switching frequency, no heat sink. Space Vector Modulation, $V_+ = 320V$, $T_A = 28^\circ C$, $T_J = 128^\circ C$

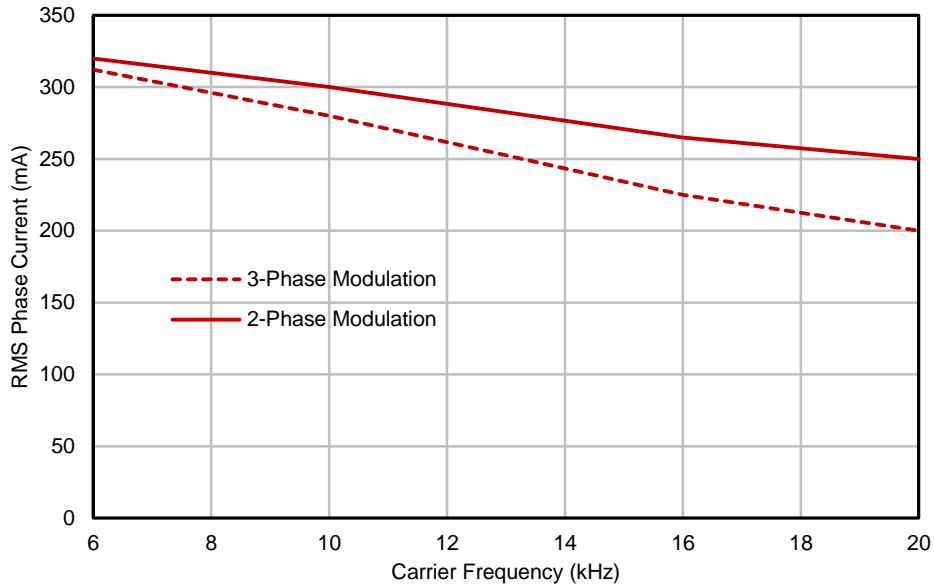


Figure 7: Maximum sinusoidal phase current vs PWM switching frequency, no heat sink. Space Vector Modulation, $V_+ = 320V$, $T_A = 28^\circ C$, $T_J = 98^\circ C$

The module contains an NTC – connected between COM and the V_{TH} pin – which can be used to monitor the temperature of the module. The NTC is effectively a resistor whose value decreases as the temperature rises. The NTC resistance can be calculated at any temperature as follows:

$$R_{TH} = R_{25} e^{B \left(\frac{1}{T_{TH}} - \frac{1}{T_{25}} \right)}, \text{ where } R_{25} \text{ is } 47k\Omega \text{ and } B \text{ is } 4050K$$

An external resistor network is connected to the NTC, the simplest of which is one resistor pulled up to V_{CC} as shown in Figure 3. The V_{TH} vs NTC temperature, T_{TH} curve for this configuration is shown in Figure 8 below. The min, typical and max curves result from the NTC having a $\pm 5\%$ tolerance on its resistance and $\pm 2\%$ tolerance on the B-parameter.

Figure 9 shows the thermistor temperature, T_{TH} plotted against the high-side V-phase junction temperature, T_J for a module without a heat sink. It is thus advisable to shut down the module when T_{TH} reaches $125^\circ C$.



Figure 8: V_{TH} vs T_{TH} with V_{TH} pin pulled up to V_{CC} with a 7.50kΩ (1%, 100ppm) resistor. A 15V, 1% variation in V_{CC} is assumed.

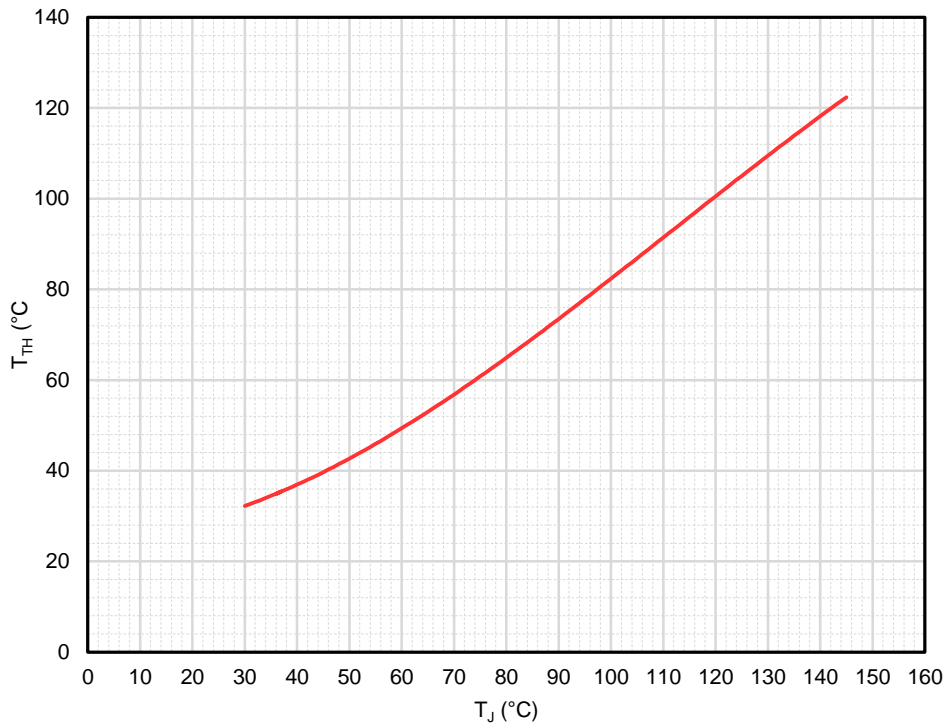


Figure 9: T_{TH} vs T_J for a module without a heat sink. V_{CC}=15.4V, R=7.50kΩ

SOP23 Package Outline



Dimensions in mm

DIP23A Package Outline



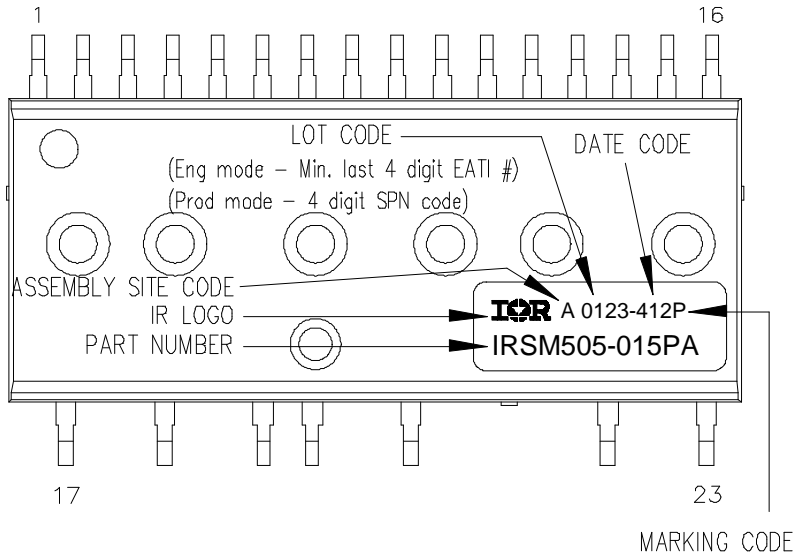
Dimensions in mm

DIP23 Package Outline



Dimensions in mm

Top Marking



Marking Code P = Pb Free; Y = Engineering Samples

Date Code YWW format, where Y = least significant digit of the production year , WW = two digits representing the week of the production year

Revision History

Nov 2014 Corrected logic in Figure 1. Added UL certification note